Triple Outputs Switching Converter With I²C for AMOLED Display

FEATURES

- Input voltage: 2.5V ~ 4.8V
- Excellent line and load transient response
- Programmable output voltage from 4.6V to 5V in 100mV steps (Default: 4.6V)
- Programmable output voltage from -6.6V to -0.5V in 100mV steps (Default: -4V)
- Programmable output voltage from 6.5V to 8.0V in 50mV steps (Default: 7.6V)
- Max Output current for ELVDD and ELVSS
- **1000mA @ V_{IN}=2.5V, ELVDD=4.6V, ELVSS= -4V**
- **1000mA @ V_{IN}=2.7V, ELVDD=4.6V, ELVSS= -5.5V**
- 150mA Max Output current for AVDD
- Short Circuit Protection (SCP)
- WLCSP 2.017×2.017-25B

APPLICATIONS

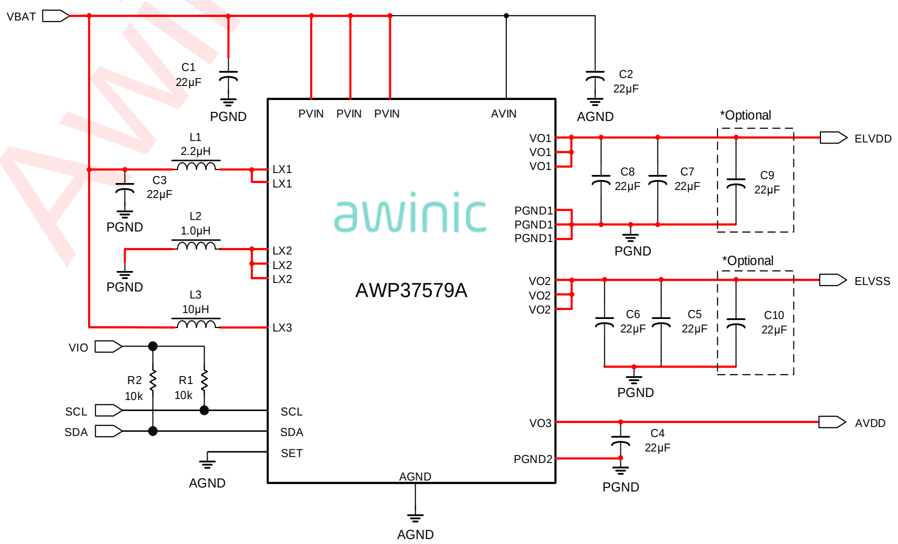
Active Matrix OLED

GENERAL DESCRIPTION

The AWP37579ACSR is specially designed for AMOLED (Active Matrix organic LED) Display panels. It integrates two high performance boost converters, VO1 (positive voltage ELVDD) and VO3 (AVDD), one inverting buck-boost converter for VO2 (negative voltage ELVSS). These converters have excellent line and load transient response.

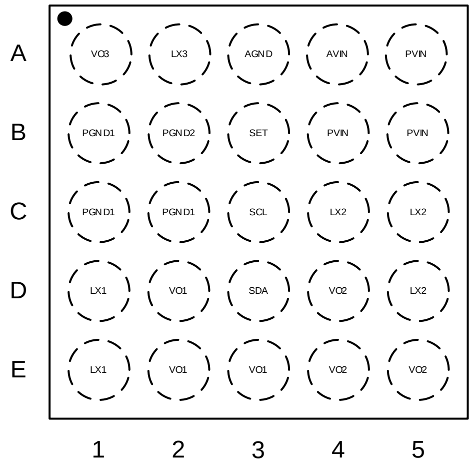
The output voltage can be programmed by I²C protocols, which conveniently enables the ELVSS output voltage transition in fine steps. I²C address is 0x03H.

TYPICAL APPLICATION CIRCUIT

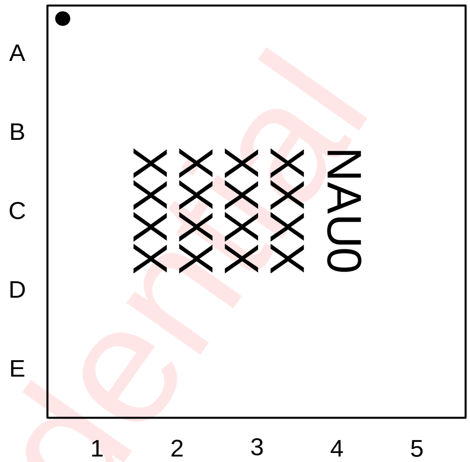


PIN CONFIGURATION AND TOP MARK

AWP37579ACSR
(Top View)



AWP37579ACSR Marking
(Top View)

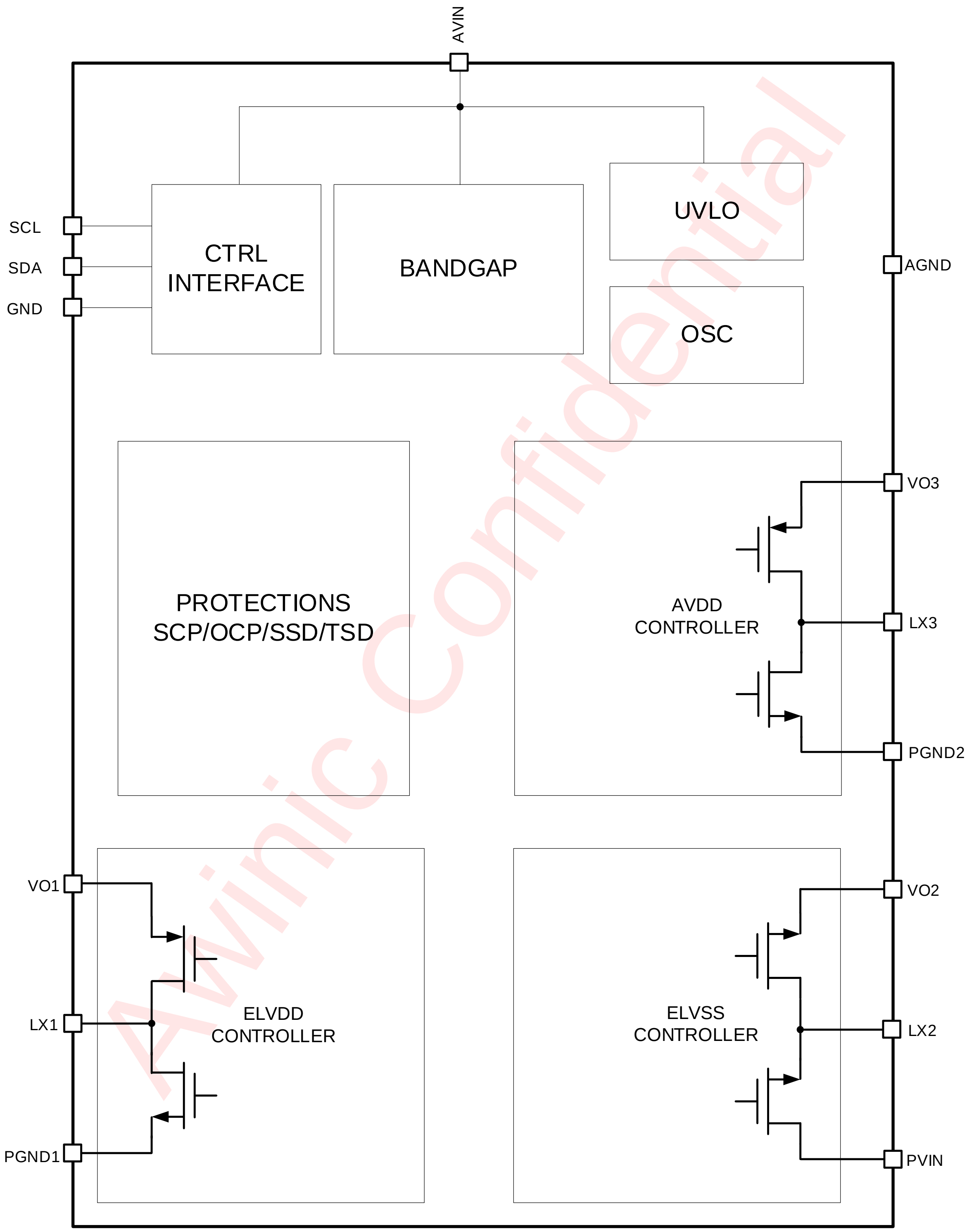


NAU0 - AWP37579ACSR
XXXX/XXXX/XXXX/XXXX - Production Tracing Code

PIN DEFINITION

Ball No.	Symbol	I/O	Description
D1, E1	LX1	Output	Switching node of ELVDD Boost converter
D2, E2, E3	VO1	Output	Output voltage of ELVDD Boost converter
B1, C1, C2	PGND1	GND	Power ground for ELVDD Boost converter
C4, C5, D5	LX2	Output	Switching node of ELVSS inverting Buck-boost converter
D4, E4, E5	VO2	Output	Output voltage of ELVSS inverting Buck-boost converter
A5, B4, B5	PVIN	Input	Input supply voltage for Power
A2	LX3	Output	Switching node of AVDD Boost converter
A1	VO3	Output	Output voltage of AVDD Boost converter
B2	PGND2	GND	Power ground for AVDD Boost converter
A4	AVIN	Input	Input supply voltage for analog
A3	AGND	GND	Analog ground
D3	SDA	Input	I^2C Serial Data Bidirectional
C3	SCL	Input	I^2C Serial Clock Input
B3	SET	Input	Floating Pin. It is recommended that the SET pin be grounded.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37579ACSR	-40°C ~ 85°C	WLCSP 2.017×2.017-25B	NAU0	MSL1	RoHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range AVIN, PVIN		-0.3V to 6V
Input voltage range	SCL, SDA, SET	-0.3V to 6V
Output voltage range	VO1	-0.3V to 6V
	LX1	-0.3V to 7V
	VO3	-0.3V to 10V
	LX3	-0.3V to VO3+0.3V
	VO2	-8V to 0.3V
	LX2	-8V to PVIN+0.3V
Junction-to-ambient thermal resistance θ_{JA}		58°C/W
Operating free-air temperature range T_A		-40°C to 85°C
Operating junction temperature range T_J		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-65°C to 160°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including HBM CDM)(NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test standard: JESD78F		+IT：+200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023(HBM). ESDA/JEDEC JS-002-2022(CDM).

Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IN}	Input voltage		2.5	3.7	4.8	V
C_{IN}	Input capacitance		40	66		μF
C_{OUT}(NOTE 3)	Output capacitance	C_{OUT} of VO1	44			μF
		C_{OUT} of VO2	44			μF
		C_{OUT} of VO3	22			μF
L_1(NOTE 4)	Inductance for VO1			2.2		μH
				4.7		μH
L_2(NOTE 4)	Inductance for VO2			1.0		μH
				2.2		μH
L_3(NOTE 4)	Inductance for VO3			4.7		μH
				10		μH
T_A	Operating free-air temperature range		-40	25	85	°C

NOTE3: The minimum value of the required capacitor for 1000mA load at V_{VO1}= 4.6V or V_{VO2} = -4.0V is 13.2μF and for 150mA load at V_{VO3} = 7.6V is 3.9μF. In order to improve the stability at lower input voltage and heavy loads, it is recommended that another 22μF capacitor be added to the VO1 and VO2 outputs.

NOTE4: In addition to typical application, AWP37579ACSR can supports L1 = 4.7μH, L2 = 2.2μH and L3 = 4.7μH.

ELECTRICAL CHARACTERISTICS

AVIN = PVIN = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4V, V_{VO3} = 7.6V, typical values are at T_A = T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT AND THERMAL PROTECTION						
AVIN, PVIN	Input voltage range		2.5	3.7	4.8	V
I_{SD}	Shutdown current	SDA = SCL = GND, total current flowing into AVIN and PVIN			1.5	μA
I_Q	Quiescent current	IOUT = 0mA			6	mA
V_{UVLO}	Under-voltage lockout threshold	AVIN Falling	1.75	2.05	2.15	V
		AVIN Rising	1.85	2.15	2.25	V
T_{SD}	Thermal shutdown temperature	Temperature Rising		165		°C
ELVDD BOOST CONVERTER(VO1)						
V_{VO1}	Output voltage		4.6	4.6	5	V
	Output voltage accuracy	No load	-0.5		0.5	%
		No load, T_A = -40°C to +85°C	-0.8		0.8	%
I_{O1MAX} (NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V, V_{VO2}= -4V	1000			mA
		AVIN = PVIN = 2.7V ~ 4.8V, V_{VO2}= -5.5V	1000			mA
R_{DSONS}	Switch on-resistance	I_{DS} = 200 mA		80		mΩ
R_{DSONR}	Rectifier on-resistance			60		mΩ
f_{SW1}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT1}	Switch current limit	Inductor peak current	2.8	3.5		A
V_{SCP1}	Short-circuit threshold in operation	Voltage decrease from nominal V_{VO1}		0.9x V_{VO1}		V
t_{SCP1}	Short-circuit detection time in operation			1		ms
R_{DCHG1}	Discharge resistance	FD = ON, I_{O1} = 1mA	30	50	70	Ω
Line Regulation	$V_{VO1\_LINEREG}$	I_{O1} = 100mA, V_{IN} = 2.5V to 4.8V		10		mV
Load Regulation	$V_{VO1\_LOADREG}$	I_{O1} = 1mA ~ 1000mA		25		mV
ELVSS INVERTING BUCK-BOOST CONVERTER (VO2)						
V_{VO2}	Output voltage range		-6.6	-4.0	-0.5	V
	Output voltage accuracy	No load	-25		25	mV
		No load, T_A = -40°C to +85°C	-40		40	mV
I_{O2MAX} (NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 5.0V, V_{VO2}= -4V			-1000	mA
		AVIN = PVIN = 2.7V ~ 5.0V, V_{VO2}= -5.5V			-1000	mA
R_{DSONS}	Switch on-resistance	I_{DS} = 200 mA		45		mΩ
R_{DSONR}	Rectifier on-resistance			45		mΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW2}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT2}	Switch current limit	AVIN = PVIN = 2.5 V	4.8	5.8		A
R_{DCHG2}	Discharge resistance	FD = ON, I_{O2} = 1 mA	30	50	70	Ω
V_{SCP2}	Short circuit threshold in operation	Voltage increase from nominal V_{VO2}		0.8x V_{VO2}		V
t_{SCP2}	Short circuit detection time in operation			1		ms
V_{SSD}	Start-up short detection threshold			200		mV
Line Regulation	$V_{VO2\_LINEREG}$	I_{O2} = 100mA, V_{IN} = 2.5V to 4.8V		10		mV
Load Regulation	$V_{VO2\_LINEREG}$	I_{O2} = 1mA ~ 1000mA		25		mV
AVDD BOOST CONVERTER (VO3)						
V_{VO3}	Output voltage		6.5	7.6	8.0	V
	Output voltage accuracy	No load	-0.8		0.8	%
		No load, T_A= -40°C to +85°C	-1.0		1.0	%
I_{O3MAX}	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V	150			mA
R_{DSONS}	Switch on-resistance	I_{DS} = 30 mA		300		mΩ
R_{DSONR}	Rectifier on-resistance			500		mΩ
f_{SW3}	Switching frequency			1.45		MHz
			-10		10	%
I_{LIMIT3}	Switch current limit	Inductor peak current	0.8	1.0		A
R_{DCHG3}	Discharge resistance	FD = ON, I_{O3} = 1 mA	40	70	100	Ω
V_{SCP3}	Short-circuit threshold in operation	Voltage decrease from nominal V_{VO3}		0.8x V_{VO3}		V
t_{SCP3}	Short-circuit detection time in operation			1		ms
Line Regulation	$V_{VO3\_LINEREG}$	I_{O3} = 50mA, V_{IN} = 2.5V to 4.8V		5		mV
Load Regulation	$V_{VO3\_LINEREG}$	I_{O3} = 1mA ~ 150mA		10		mV
CTRL INTERFACE(SCL, SDA)						
V_{IH}	High level input voltage	AVIN = PVIN = 2.5V ~ 4.8V	0.84			V
V_{IL}	Low level input voltage	AVIN = PVIN = 2.5V ~ 4.8V			0.36	V
POWER SEQUENCE						
t_{SS1} (NOTE 6)	VO1 soft-start time			3		ms
t_{SS2} (NOTE 6)	VO2 soft-start time			3		ms
t_{SS3} (NOTE 6)	VO3 soft-start time			3		ms

NOTE5: The specific parameters of the peripheral inductors are as follows:

L1: DFE252012F-2R2M=P2 3.3A, 82mΩ, 252012 L2: SKFB252010-1R0M 4.4A, 38mΩ, 252010

L3: DFE252012F-100M=P2 1.4A, 480mΩ, 252012

Test Condition: Ambient temperature is 60°C, the load current is only between the VO1 and VO2, VO3 is no load, AWP37579ACSR works stably in laboratory test environment.

NOTE6: Guaranteed by design characterization and correlation with process controls. Not fully test in production.

I²C INTERFACE TIMING

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock Frequency				400	kHz
$t_{DEGLITCH}$	Deglitch Time	SCL		83		ns
		SDA		115		ns
$t_{HD:STA}$	(Repeat-Start) Start Condition Hold Time		0.6			μs
t_{LOW}	Low Level Width of SCL		1.3			μs
t_{HIGH}	High Level Width of SCL		0.6			μs
$t_{SU:STA}$	(Repeat-Start) Start Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		0			μs
$t_{SU:DAT}$	Data Setup Time		0.1			μs
t_R	Rising Time of SDA and SCL				0.3	μs
t_F	Falling Time of SDA and SCL				0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{BUF}	Time Between Start and Stop Condition		1.3			μs

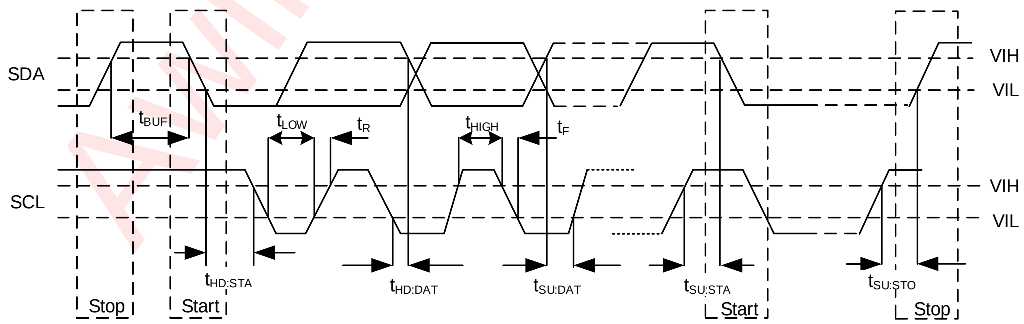


Figure 1 I²C Interface Timing

TYPICAL CHARACTERISTICS

AVIN = PVIN = VIN = 3.7V, V_{VO1}= 4.6V, V_{VO2}= -4V, V_{VO3}= 7.6V, L1= 2.2μH, L2= 1.0μH, L3= 4.7μH. Typical values are at T_A = T_J = 25°C (unless otherwise noted)

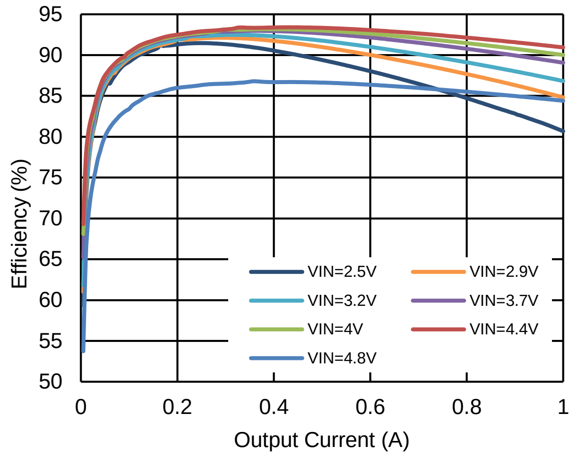


Figure 2 VO1 and VO2 Combined Efficiency

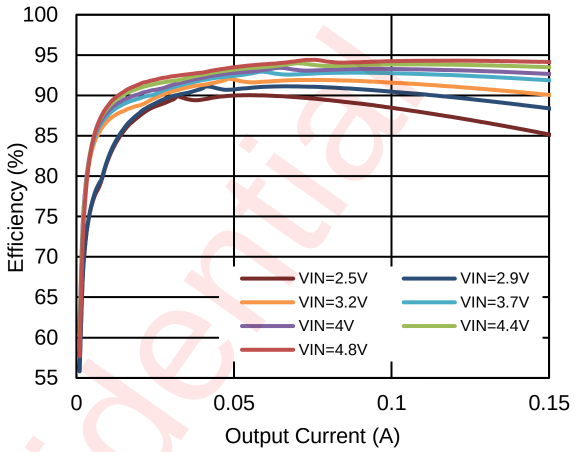


Figure 3 VO3 Efficiency

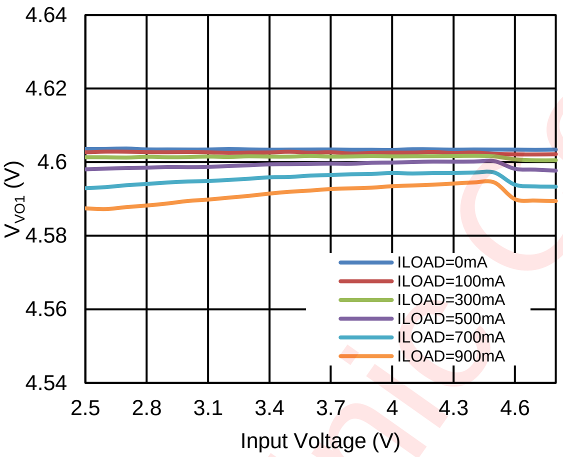


Figure 4 VO1 Line Regulation

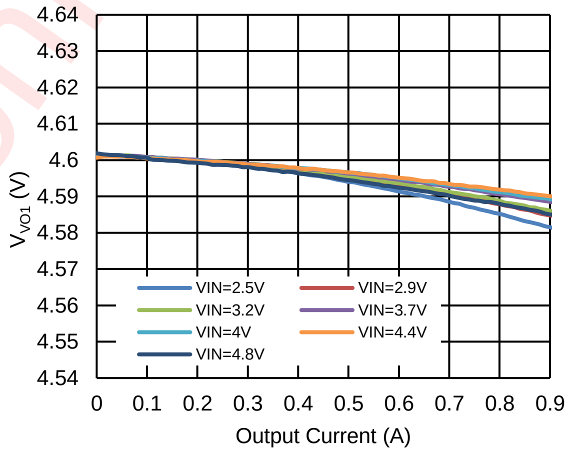


Figure 5 VO1 Load Regulation

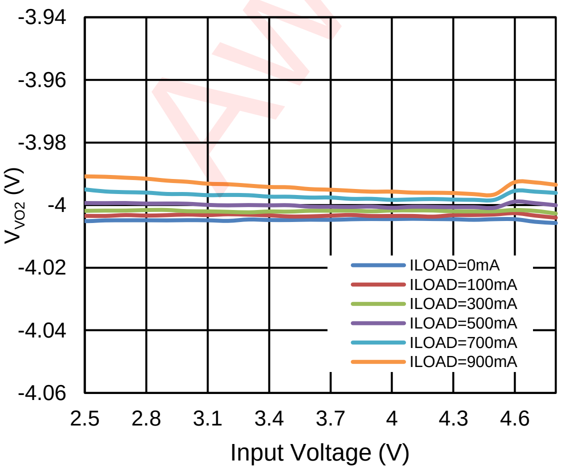


Figure 6 VO2 Line Regulation

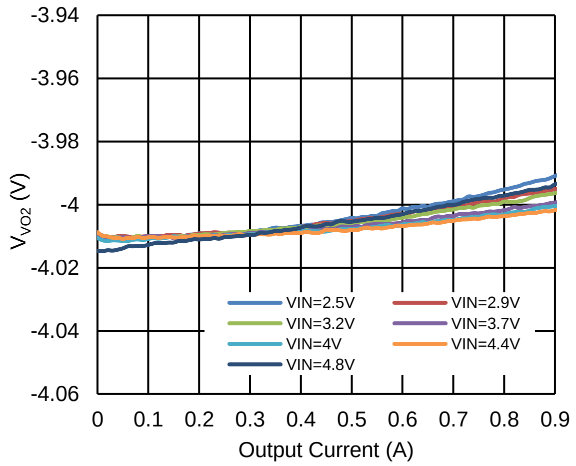


Figure 7 VO2 Load Regulation

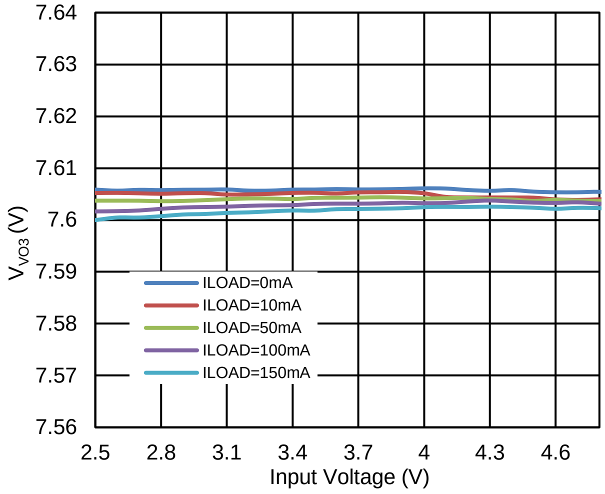


Figure 8 VO3 Line Regulation

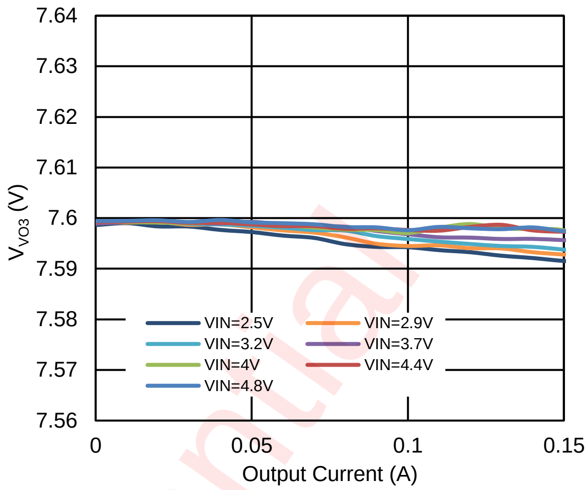


Figure 9 VO3 Load Regulation

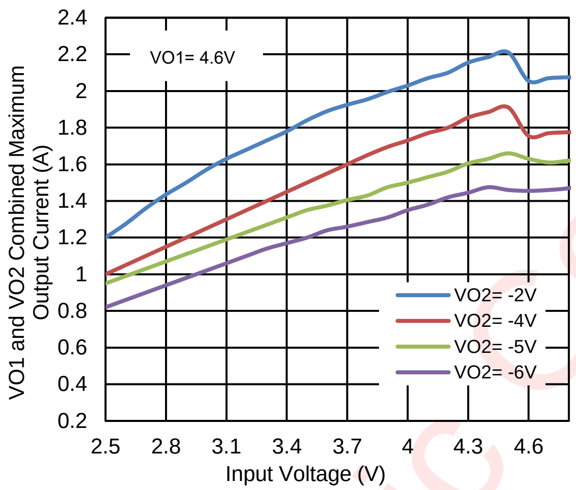


Figure 10 VO1 and VO2 Combined Maximum Output Current (NOTE 5)

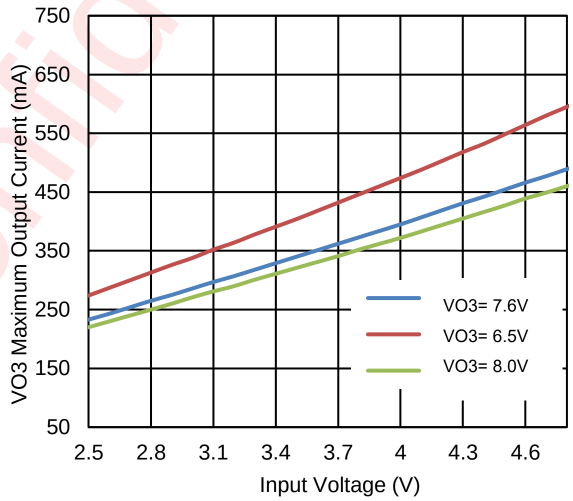


Figure 11 VO3 Maximum Output Current (NOTE 5)

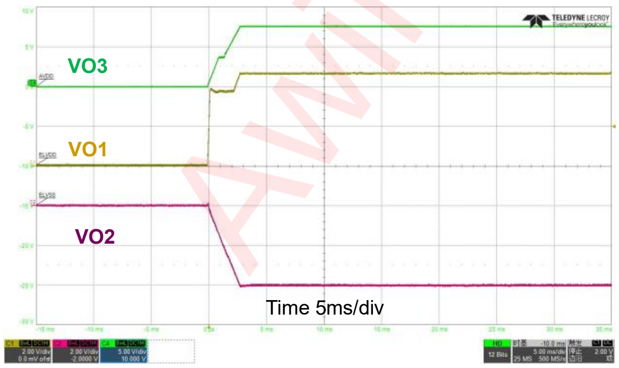


Figure 12 Start up Sequence

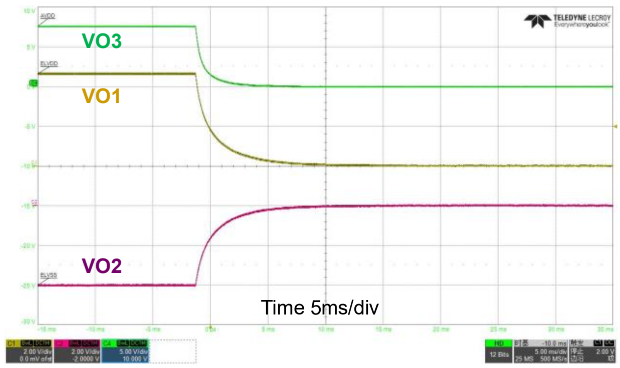


Figure 13 Shut down Sequence with FD ON

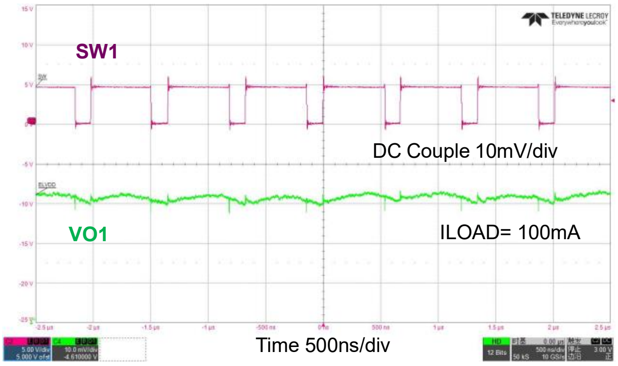


Figure 14 VO1 Switching and Output Waveforms at light load

Figure 15 VO1 Switching and Output Waveforms at heavy load

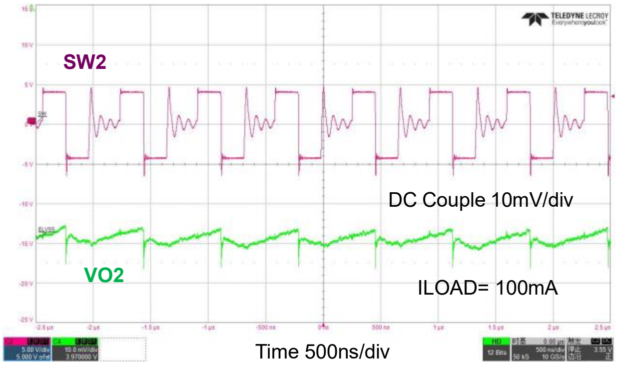


Figure 16 VO2 Switching and Output Waveforms at light load

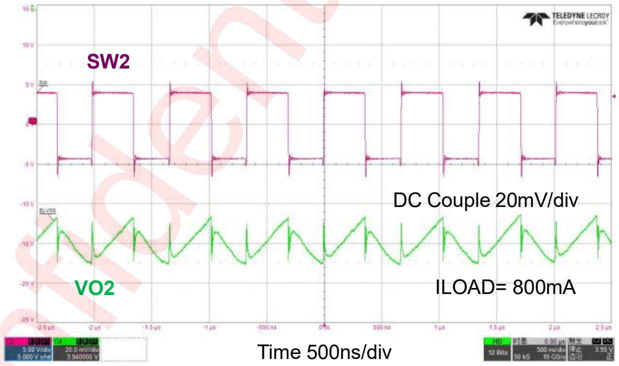


Figure 17 VO2 Switching and Output Waveforms at heavy load

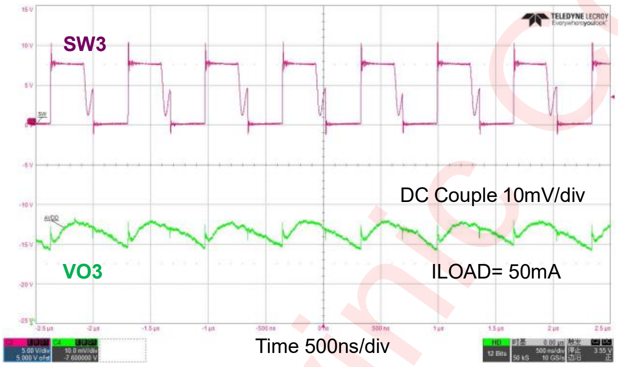


Figure 18 VO3 Switching and Output Waveforms at light load

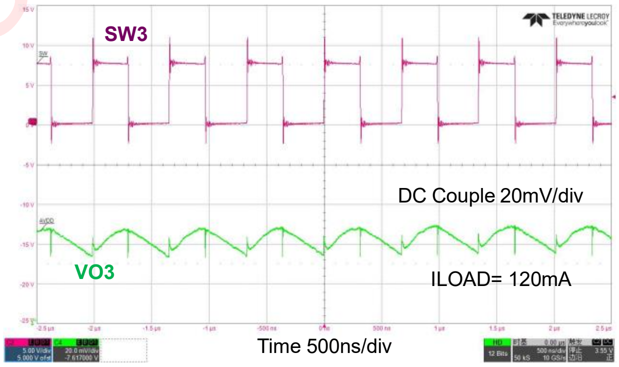


Figure 19 VO3 Switching and Output Waveforms at heavy load

Figure 20 Line transient at No load

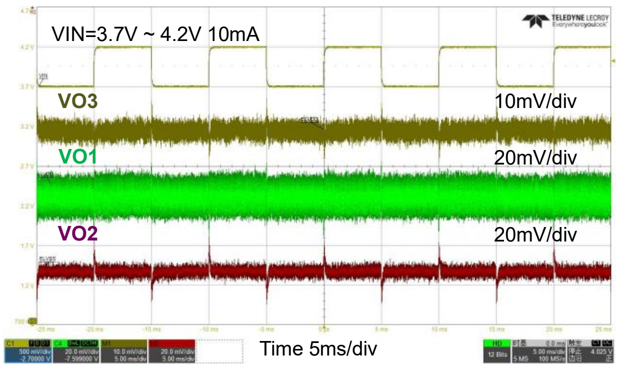


Figure 21 Line transient at light load (10mA)

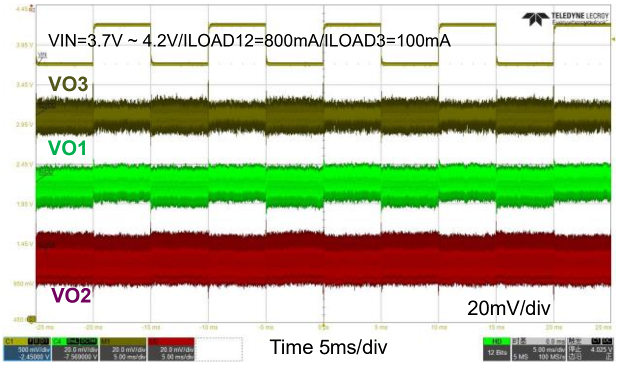


Figure 22 Line transient at heavy load

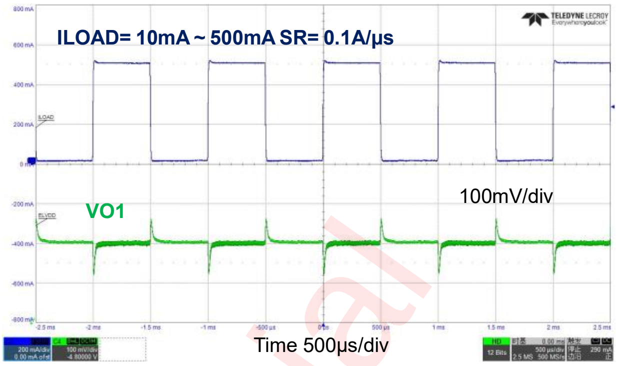


Figure 23 VO1 load transient (10~500mA/SR=0.1A/μs)

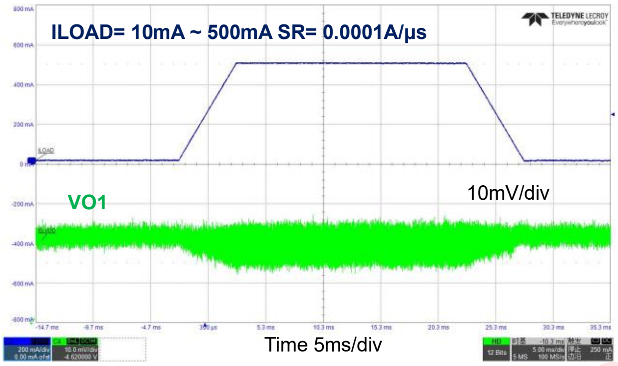


Figure 24 VO1 load transient (10~500mA/SR=0.0001A/μs)

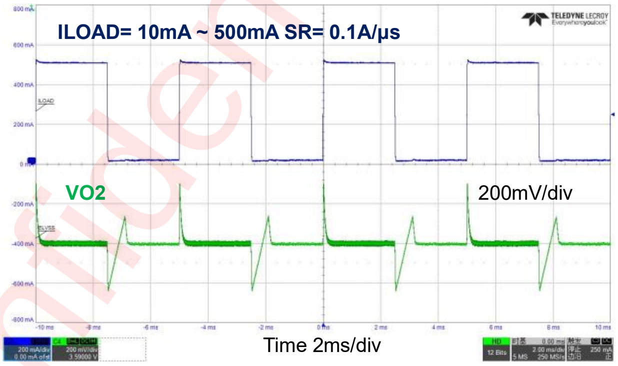


Figure 25 VO2 load transient (10~500mA/SR=0.1A/μs)

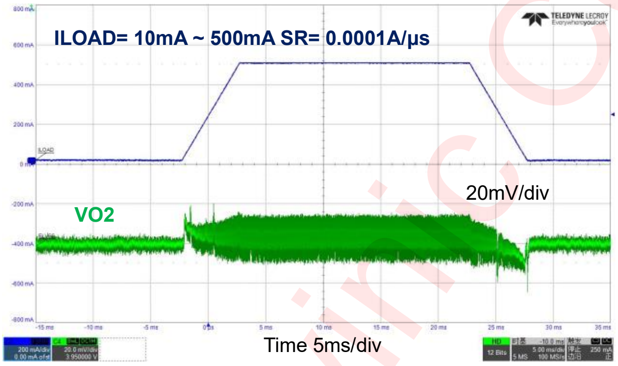


Figure 26 VO2 load transient (10~500mA/SR=0.0001A/μs)

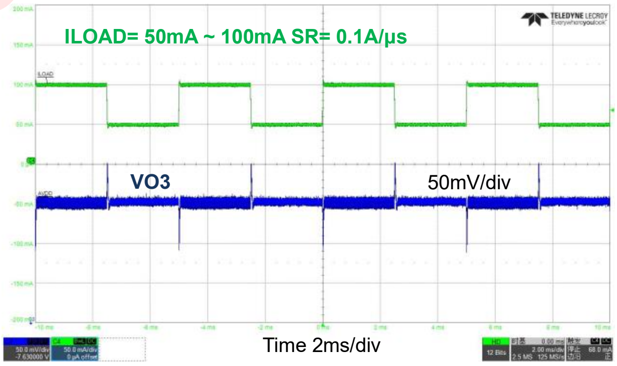


Figure 27 VO3 load transient (50~100mA/SR=0.1A/μs)

DETAILED FUNCTIONAL DESCRIPTION

Sequence

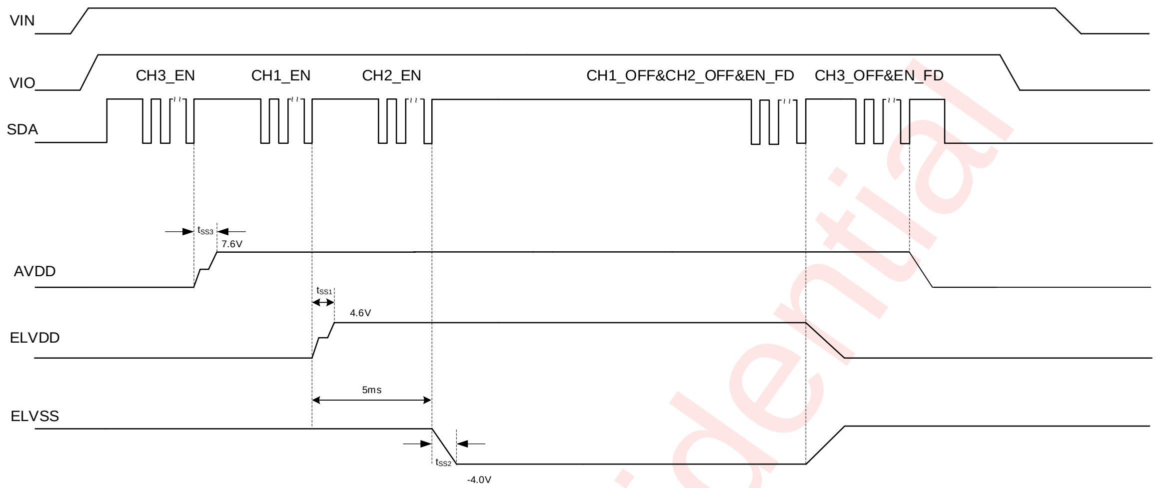


Figure 28 Power-up Sequence Timing diagram with I2C

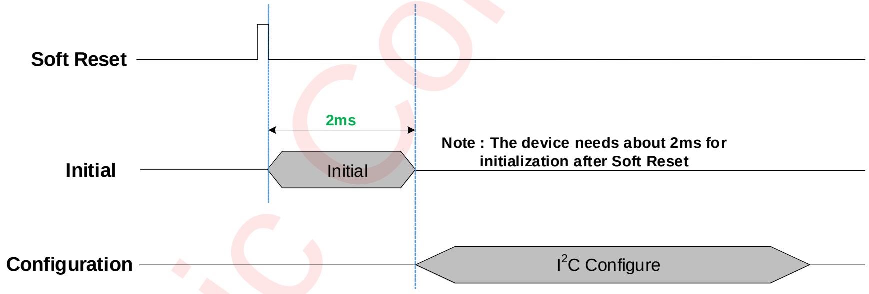


Figure 29 Software Reset Timing diagram

The power-up sequence with I²C is shown as Figure 28. To limit inrush current, it is recommend that configuring CH3_EN firstly so that the AVDD boost convert begins soft-start, the soft-start lasts for 3ms typically.

Secondly, it is suggested that a t_{DELAY} (generally: 5ms) time between CH1_EN and CH2_EN. The soft-start time for the ELVDD boost convert and the ELVSS inverting buck-boost convert is 3ms typically.

The software reset timing diagram is shown as Figure 29. By writing SFRST=1 via I²C interface will reset the AWP37579ACSR internal circuits and all configuration registers, after the soft reset command is input through I²C, it needs to wait at least **2ms** before any other I²C command can be accepted.

ELVSS Transition

AWP37579ACSR also has the slew rate control during the transition of the ELVSS output voltage, which aims to accomplish smooth voltage changes. The default ramp time is 100μs typically, step is 100mV, the wider the transition range of the ELVSS output voltage, the longer the transition time. The ramp time can configured by RAMP_MD.

AWP37579ACSR supports fine steps in the transition of ELVSS, which is configured by CH2_VOCTL<2:1>, the minimum step is 25mV. CH2_VOCTL<2:1> is written to take effect and needs to be written CH2_VOSEL <5:0>again. Additionally, it should be noted that if voltage adjustment is required based on CH2_VOSEL <5:0>, CH2_VOCTL<2:1> must be rewritten to 00.

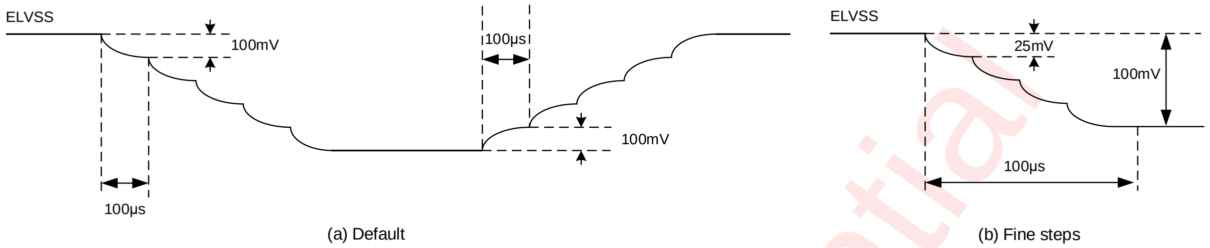


Figure 30 ELVSS Transition

Maximum Output Current Capacity

AWP37579ACSR operates with an input voltage range of 2.5V to 4.8V. However, due to different input and output voltage, the maximum output current capacity is quite different, and also affected by peripheral inductors and capacitors, additional input capacitors are recommended for lower input supply voltage.

The maximum output current in T_A= 60°C for different V_{IN} and V_{O2} voltages is shown in Table 1.

Table 1. The maximum output current

V_{IN} (V)	The maximum output current (A)				
	V_{VO2}= -2V	V_{VO2}= -4V	V_{VO2}= -5V	V_{VO2}= -5.5V	V_{VO2}= -6V
2.5	1.2	1	0.95	0.9	0.82
2.6	1.275	1.05	0.99	0.95	0.86
2.7	1.36	1.1	1.03	1	0.9
2.8	1.435	1.15	1.07	1.04	0.94
2.9	1.5	1.2	1.11	1.08	0.98
3	1.57	1.25	1.15	1.12	1.02
3.1	1.63	1.3	1.19	1.16	1.06
3.2	1.68	1.35	1.23	1.2	1.1
3.3	1.73	1.4	1.27	1.24	1.14
3.4	1.78	1.45	1.31	1.28	1.17

Under Voltage Lock-out

Under Voltage Lock-out (UVLO) is implemented to detect the input voltage AVIN. Once AVIN drops below UVLO falling threshold, all of the three converters (AVDD, ELVDD and ELVSS) stop switching; If AVIN increases above UVLO rising threshold, the three converters restart switching and resume to their previous settings.

Start-up Short Detection (SSD)

The start-up short detection block detects the ELVSS output voltage to monitor whether ELVSS and ELVDD are short connected. When SSD function is enabled, if the ELVSS output voltage is pulled up to 0.2V (Default) after CH1_EN, SSD function is triggered and the ELVDD and ELVSS converters shut down immediately. SSD function is disabled by default, and the trigger threshold is configured by CH2_SSD_SEL.

Short Circuit Protection (SCP)

The short circuit protection block monitors the output voltages of the AVDD, ELVDD and ELVSS converters to protect the device of short connections to ground or overload. When a SCP or overload event occurs, all the three converters shut down.

An SCP or overload event occurs in the following cases:

(1) After the output voltages of all the three converters are properly established, ELVDD output voltage falls below 90% of the target voltage and lasts for 1ms; ELVSS and AVDD output voltage falls below 80% of the target voltage and lasts for 1ms;

(2) In soft-start process, V_{ELVDD}, V_{ELVSS} and V_{AVDD} are not in regulation 4ms when ELVDD and ELVSS output voltages begin to establish.

Thermal Shut-Down (TSD)

The Thermal Shut-Down (TSD) function protects the device when overheating occurs. If the IC's junction temperature exceeds 165°C, three converters stop operation. It can not exit this state automatically.

General I²C Operation

The device supports the I²C serial bus and data transmission protocol. It operates as a slave on the I²C bus. The maximum clock frequency specified by the I²C standard is 400kHz. Connect to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ when I²C frequency is 400kHz. Different high level from 1.2V to 5V of this I²C interface is supported.

Device Address

AWP37579ACSR 7-bit slave address (A7~A1) is 0000011 binary (0x03H). After the START condition, the I²C master sends the 7-bit chip address followed by an eighth (A0) read or write bit (R/W). R/W= 0 indicates a WRITE function and R/W = 1 indicates a READ function.

Table 2. Device Address

A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	1	R/W

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

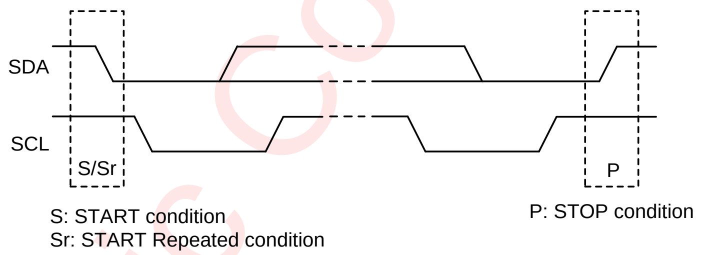


Figure 31 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

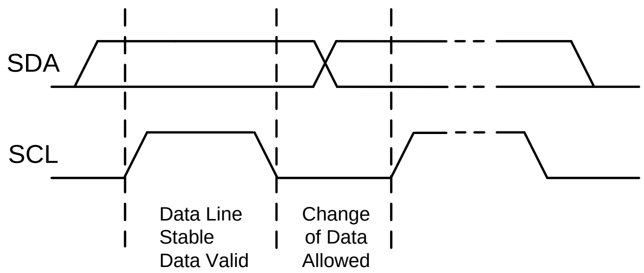


Figure 32 Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

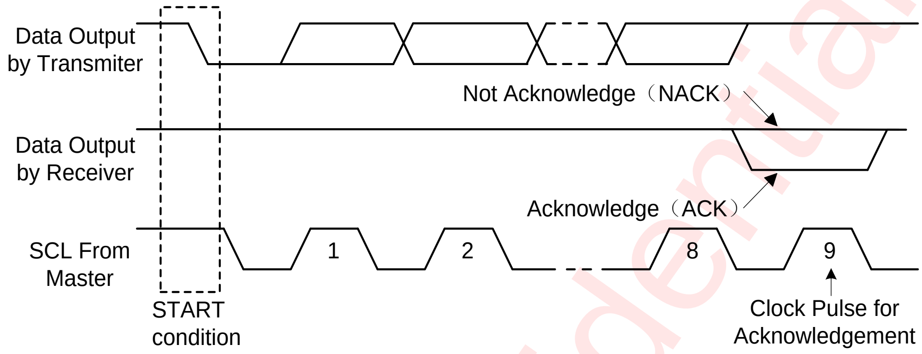


Figure 33 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal
h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)
i) Master generates STOP condition to indicate write cycle end

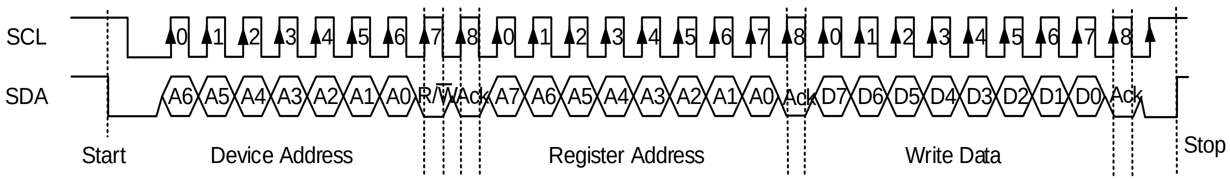


Figure 34 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master generates STOP condition followed with START condition or REPEAT START condition
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle is ended.

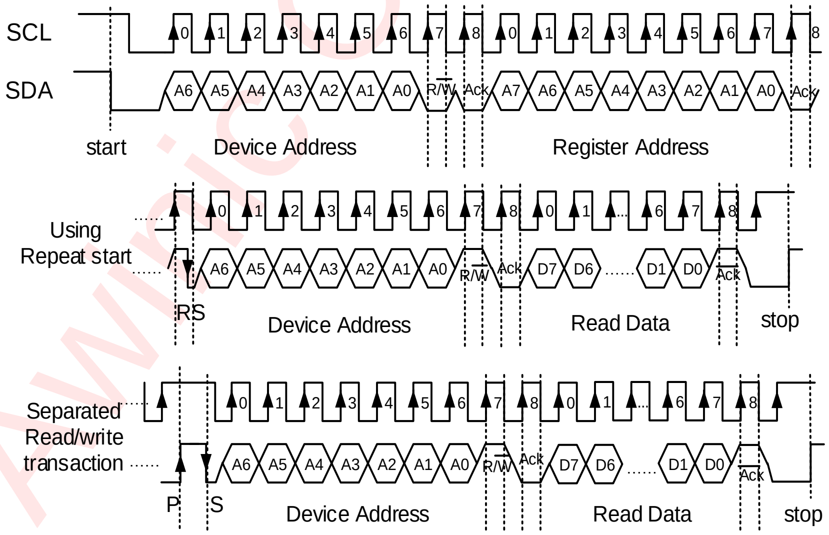


Figure 35 I²C Read Byte Cycle

REGISTER CONFIGURATION

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**ID**	RO	DEVICE_ID								0x03
0x01	**SFRST**	WO	RSVD							SFRST	0x00
0x02	**EN**	R/W	PR_OSC_ADJ <2:0>			EN_LF	EN_FD	CH3_EN	CH1_EN	CH2_EN	0x80
0x03	**CTR1**	R/W	RSVD		LF_SEL <1:0>		CH1_VOSEL <3:0>				0x00
0x04	**CTR2**	R/W	CH2_VOSEL <5:0>						CH2_VOCTL <2:1>		0x68
0x05	**CTR3**	R/W	RSVD		CH3_VOSEL <5:0>						0x08
0x06	**CTR4**	R/W	RSVD		CH2_SSD_SEL		RAMP_MD		**PMIC_EN <1:0>**		0x50
0x07	**FLTDIS**	R/W	RSVD	DIS_UVLO	DIS_OLP	DIS_SSD	DIS_ASCP	DIS_ELDSCP	DIS_ELSSCP	DIS_OTP	0x00
0x08	**FLAG**	RO	RSVD	OLP_FLAG	UVLO_FLAG	OTP_FLAG	SSD_FLAG	AVDDSCP_FLAG	ELVDDSCP_FLAG	ELVSSSCP_FLAG	0x00

NOTES: The output voltage must be configured after setting the PMIC_EN <1:0> = 11B.

Register Detailed Description

DEVICE_ID (Address 00H)

Bit	Symbol	R/W	Description	Default
7:0	DEVICE_ID	RO	Device ID 0x03	0x03

SFRST: Software reset (Address 01H)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	WO	Not used	0x00
0	SFRST	WO	Soft reset **0: Disable** 1: Enable	

EN: Output Voltage Enable (Address 02H)

Bit	Symbol	R/W	Description	Default
7:5	PR_OSC_ADJ<2:0>	R/W	Switching Frequency Adjustment. **It is not configured effectly until CH3_EN =1.** 000: 1.1MHz 001: 1.2MHz 010: 1.3MHz 011: 1.4MHz **100: 1.45MHz**	0x80
4	EN_LF	R/W	Low Frequency enable **0: Disable** 1: Enable	
3	EN_FD	R/W	Fast Diacharge enable **0: Disable** 1: Enable	
2	CH3_EN	R/W	AVDD Boost enable **0: Disable** 1: Enable	
1	CH1_EN	R/W	ELVDD Boost enable **0: Disable** 1: Enable	
0	CH2_EN	R/W	ELVSS Inverting Buck-Boost enable **0: Disable** 1: Enable	

CTR1 (Address 03H)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R/W	Not used	0x00
5:4	LF_SEL<1:0>	R/W	Low Frequency Select **00: ELVSS:1/3 ELVDD/AVDD: 1/3** 01: ELVSS:1/2 ELVDD/AVDD: 1/4 10: ELVSS:1/3 ELVDD/AVDD: 1/6 11: ELVSS:1/4 ELVDD/AVDD: 1/8	
3:0	CH1_VOSEL<3:0>	R/W	Boost Voltage setting of ELVDD **0000: 4.6V** 0010: 4.7V 0100: 4.8V 0110: 4.9V 1000: 5.0V (100mV/step)	

CTR2 (Address 04H)

Bit	Symbol	R/W	Description	Default
7:2	CH2_VOSEL<5:0>	R/W	Inverting Buck-Boost (IBB) Voltage setting of ELVSS 000000: -6.6V ~ 111101: -0.5V (100mV/step) **Default:** **011010: -4V**	0x68
1:0	CH2_VOCTL<2:1>	R/W	Fine ELVSS transition steps. Final CH2 Voltage=CH2_VOSEL<5:0>+CH2_VOCTL<2:1> **00: 0mV (Default)** 01: 25mV plus 10: 50mV plus 11: 75mV plus	

CTR3 (Address 05H)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	R/W	Not used	0x08
5:0	CH3_VOSEL<5:0>	R/W	Boost Voltage setting of AVDD 000000: 8.00V 000001: 7.95V 000010: 7.90V 000011: 7.85V 000100: 7.80V 000101: 7.75V 000110: 7.70V 000111: 7.65V **001000: 7.60V** 001001: 7.55V 001010: 7.50V 001011: 7.45V 001100: 7.40V 001101: 7.35V 001110: 7.30V 001111: 7.25V 010000: 7.20V 010001: 7.15V 010010: 7.10V 010011: 7.05V 010100: 7.00V 010101: 6.95V 010110: 6.90V 010111: 6.85V 011000: 6.80V	

			011001: 6.75V 011010: 6.70V 011011: 6.65V 011100: 6.60V 011101: 6.55V 011110: 6.50V (50mV/step)	

CTR4 (Address 06H)

Bit	Symbol	R/W	Description	Default
7	Reserved	R/W	Not used	0x50
6	Reserved	R/W	Prohibit modification. This bit is set to 1 by default.	
5:4	CH2_SSD_SEL	R/W	Select SSD Threshold Voltage 00: 100mV **01: 200mV** 10: 300mV 11: 400mV	
3:2	RAMP_MD	R/W	ELVSS Ramp Mode Select **00: 100μs/step** 01: 150μs/step 10: 300μs/step	
1:0	PMIC_EN <1:0>	R/W	PMIC Enable bits. **The IC can only operate normally when PMIC_EN <1:0> = 11B.** **00: Disable** 11: Enable	

FLTDIS (Address 07H)

Bit	Symbol	R/W	Description	Default
7	Reserved	R/W	Not used	0x00
6	DIS_UVLO	R/W	Disable UVLO Function **0: Normal enable** 1: Disable	
5	DIS_OLP	R/W	Disable OLP Function **0: Normal enable** 1: Disable	
4	DIS_SSD	R/W	Disable SSD Function **0: Disable SSD** 1: Normal enable	
3	DIS_ASCP	R/W	Disable AVDD SCP Function **0: AVDD SCP** 1: Disable AVDD SCP	
2	DIS_ELDSCP	R/W	Disable ELVDD SCP Function **0: ELVDD SCP** 1: Disable ELVDD SCP	

1	DIS_ELSSCP	R/W	Disable ELVSS SCP Function **0: ELVSS SCP** 1: Disable ELVSS SCP	
0	DIS_OTP	R/W	Disable OTP Function **0: OTP** 1: Disable OTP	

FLAG (Address 08H)

Bit	Symbol	R/W	Description	Default
7	Reserved	RO	Not used	0x00
6	OLP_FLAG	RO	OLP Fault Flag **0: Normal** 1: OLP Fault	
5	UVLO_FLAG	RO	UVLO Fault Flag **0: Normal** 1: UVLO Fault	
4	OTP_FLAG	RO	OTP Fault Flag **0: Normal** 1: OTP Fault	
3	SSD_FLAG	RO	SSD Fault Flag **0: Normal** 1: SSD Fault	
2	AVDDSCP_FLAG	RO	AVDD SCP Fault Flag **0: Normal** 1: AVDD SCP Fault	
1	ELVDDSCP_FLAG	RO	ELVDD SCP Fault Flag **0: Normal** 1: ELVDD SCP Fault	
0	ELVSSSCP_FLAG	RO	ELVSS SCP Fault Flag **0: Normal** 1: ELVSS SCP Fault	

PCB LAYOUT CONSIDERATION

It is recommended to follow the below PCB layout guidelines:

1) A common ground plane between AGND and PGND to minimize ground shifts is recommended.

2) Put inductors as close as possible to the device, creating forbidden area under inductors for each PCB layer. Traces of switching nodes (LX1, LX2 and LX3) should be short and wide.

3) Place input capacitors on PVIN and output capacitors on outputs as close as possible to the device.

4) If vias are used for power paths, multiple vias are necessary to obtain lower equivalent resistance on power paths and facilitate heat dissipation.

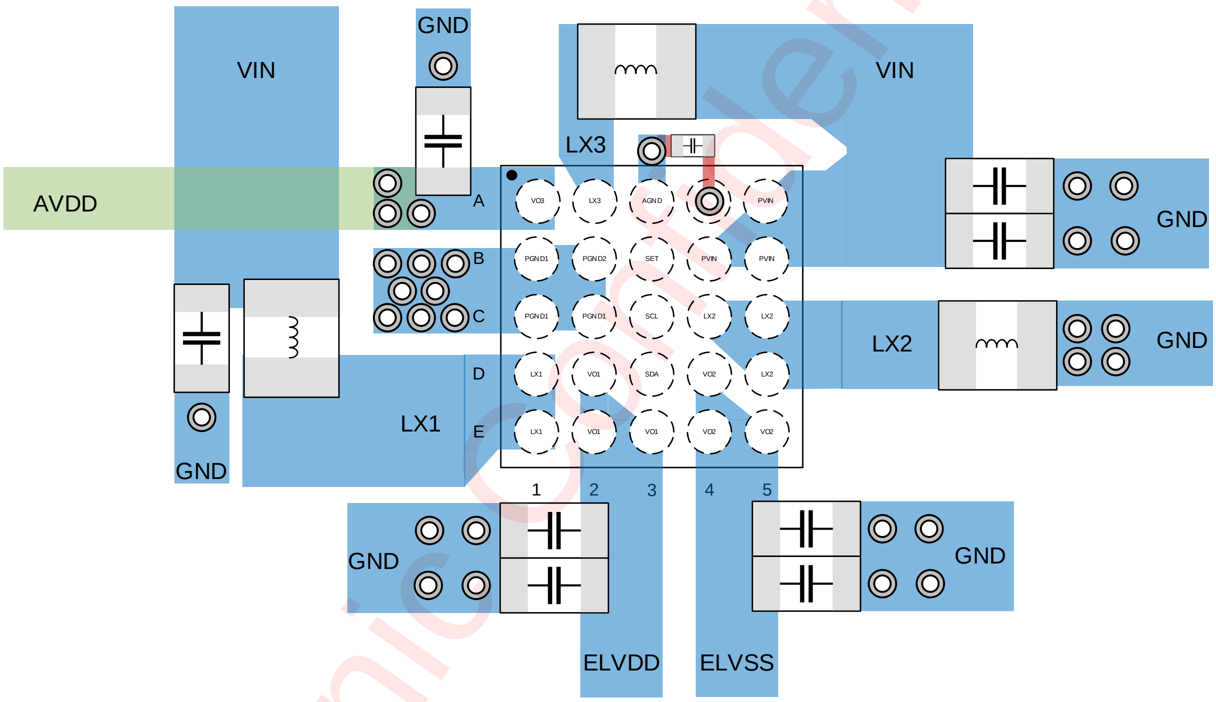
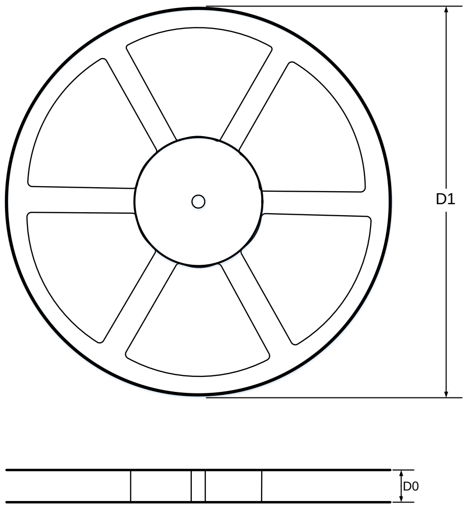


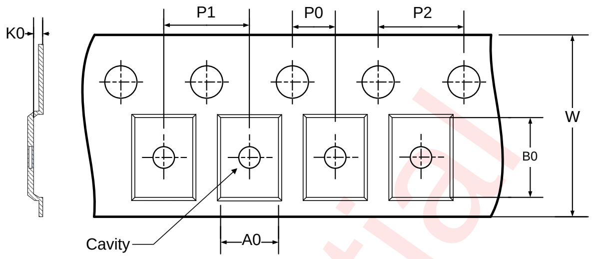
Figure 36 AWP37579A PCB Layout example

TAPE AND REEL INFORMATION

REEL DIMENSIONS

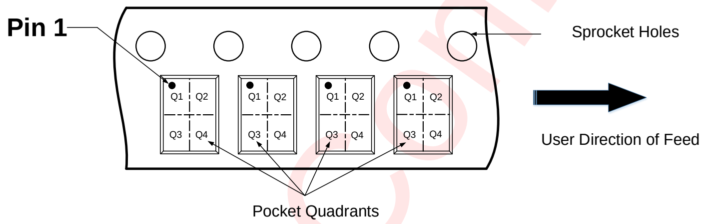


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



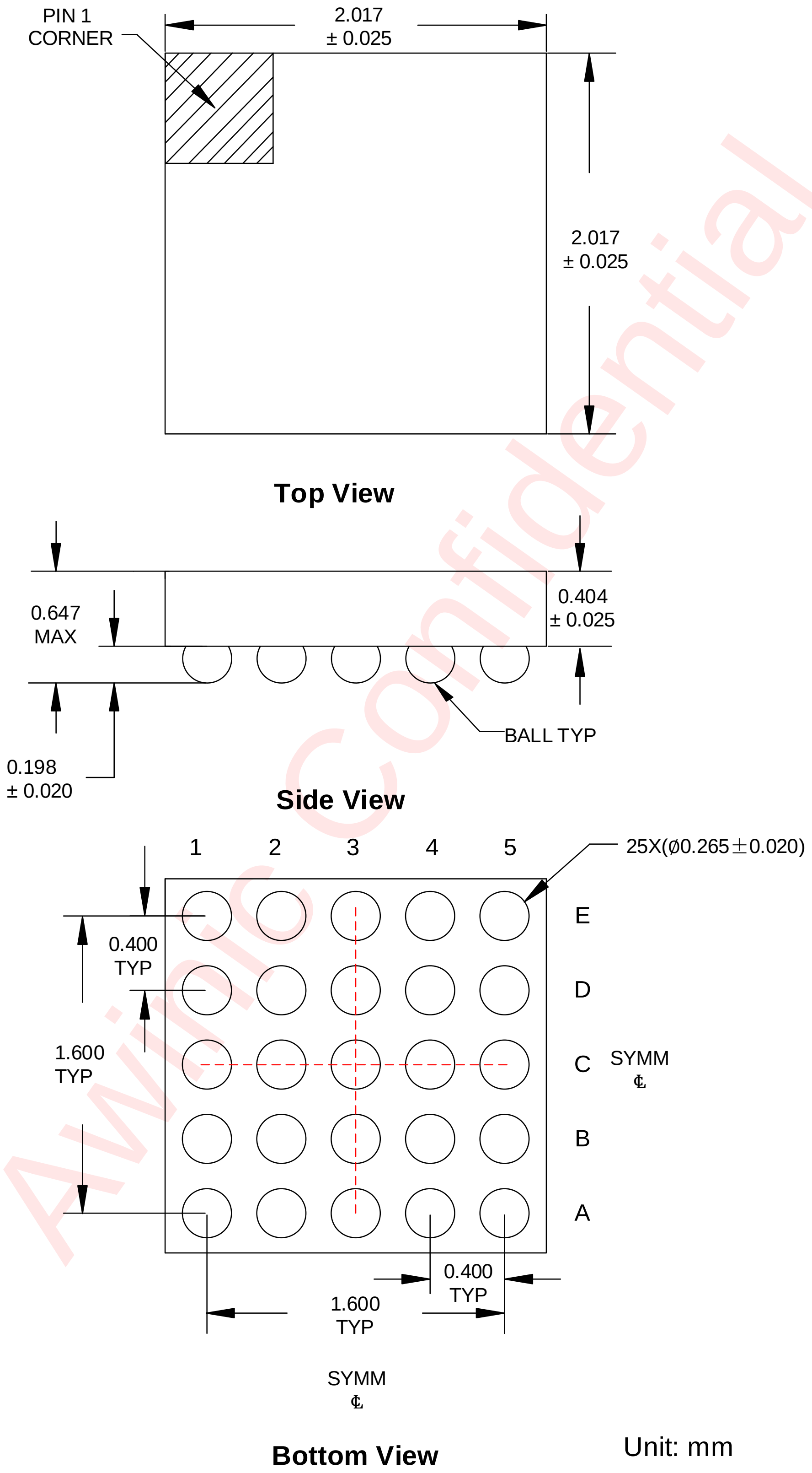
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

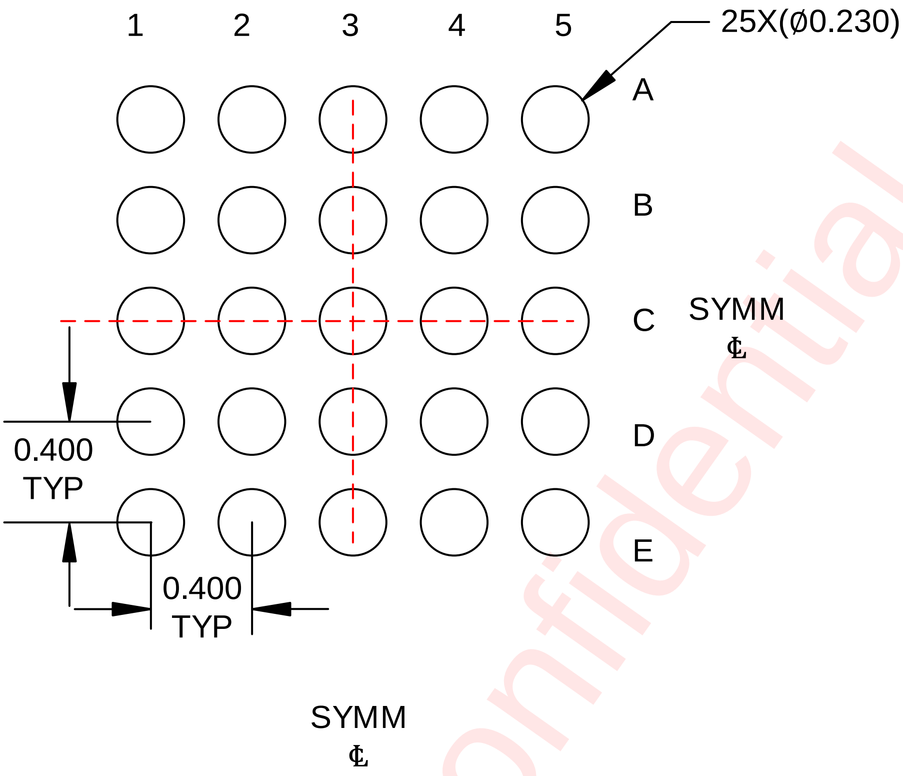
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	2.25	2.25	0.70	2.00	4.00	4.00	8.00	Q1

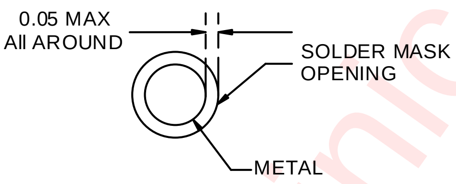
All dimensions are nominal

PACKAGE DESCRIPTION

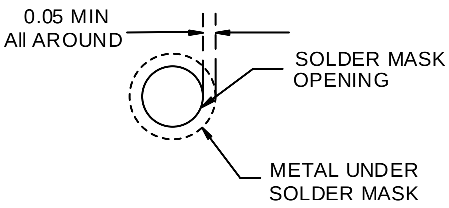


LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Jan. 2026	Officially released

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