

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	BSC057N08NS3G
▶ Overseas	Part Number	BSC057N08NS3G
▶ Equivalent	Part Number	BSC057N08NS3G

EV is the abbreviation of name EVVO

N-SGT Enhancement Mode MOSFET

General Description

The BSC057N08NS3G use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable.

General Features

$V_{DS} = 85V$ $I_D = 100A$

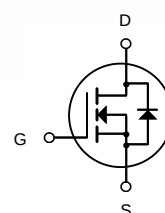
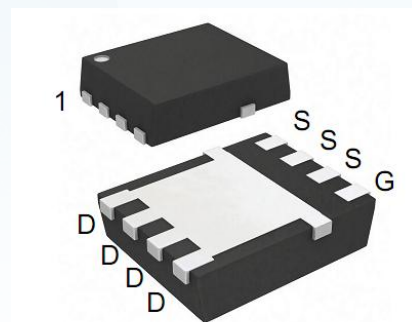
$R_{DS(ON)} < 5.6m\Omega @ V_{GS}=10V$

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



N-Channel MOSFET

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	85	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	63.3	A
I_{DM}	Pulsed Drain Current ²	400	A
EAS	Single Pulse Avalanche Energy ³	273.8	mJ
$P_D @ T_C=25^\circ C$	Total Power Dissipation ⁴	107.8	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance from Junction-to-Ambient ³	1.16	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	60	$^\circ C/W$

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	85	-	-	V
Gate-body Leakage current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = 85V, V _{GS} = 0V	-	-	1	μA
	T _J =100°C			-	-	100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
Drain-Source on-Resistance ⁴		R _{DS(on)}	V _{GS} = 10V, I _D = 20A	-	4.3	5.6	mΩ
Forward Transconductance ⁴		g _{fs}	V _{DS} = 5V, I _D =20A	-	57.8	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = 40V, V _{GS} =0V, f =1MHz	-	4645	-	pF
Output Capacitance		C _{oss}		-	673	-	
Reverse Transfer Capacitance		C _{rss}		-	41	-	
Gate Resistance		R _g	f=1MHz	-	2.0	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = 10V, V _{DS} = 40V, I _D = 20A	-	61.3	-	nC
Gate-Source Charge		Q _{gs}		-	21	-	
Gate-Drain Charge		Q _{gd}		-	11	-	
Turn-on Delay Time		t _{d(on)}	V _{GS} =10V, V _{DD} = 40V, R _G = 3Ω, I _D = 20A	-	16.5	-	ns
Rise Time		t _r		-	51.8	-	
Turn-off Delay Time		t _{d(off)}		-	37.1	-	
Fall Time		t _f		-	8.2	-	
Body Diode Reverse Recovery Time		t _{rr}	I _F =20A, di/dt = 100A/μS	-	69	-	ns
Body Diode Reverse Recovery Charge		Q _{rr}		-	141	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = 20A, V _{GS} = 0V	-	-	1.2	V
Continuous Source Current	T _C =25°C	I _S	-	-	-	100	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature T_J(MAX)=150°C
2. The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=37A
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

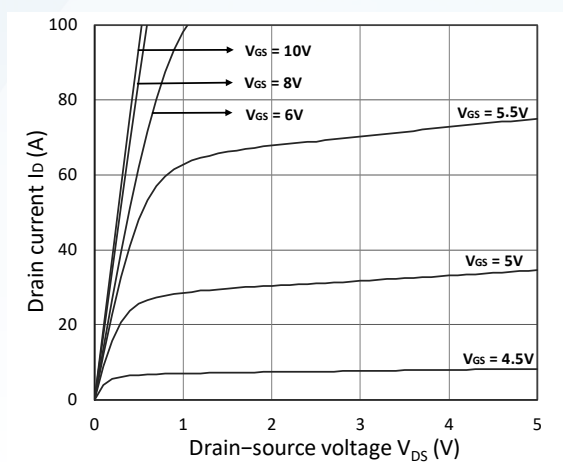


Figure 1. Output Characteristics

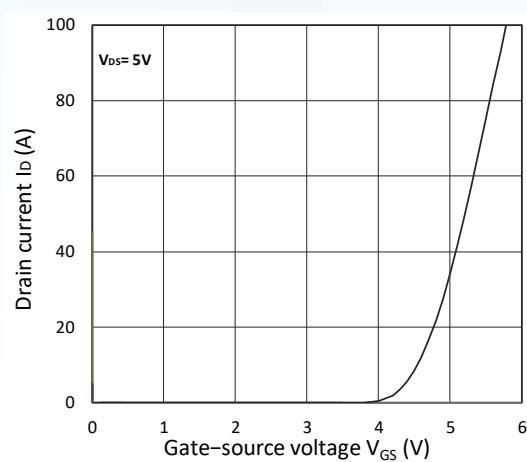


Figure 2. Transfer Characteristics

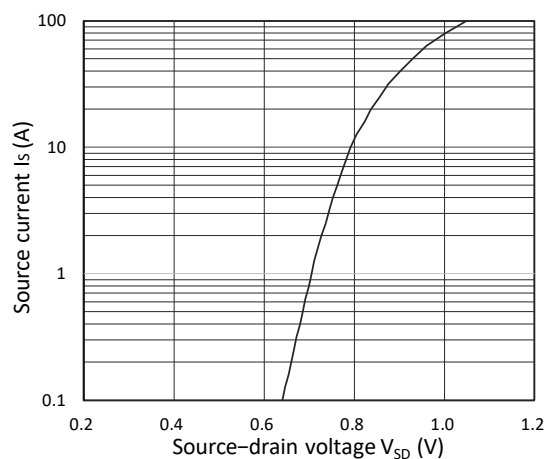
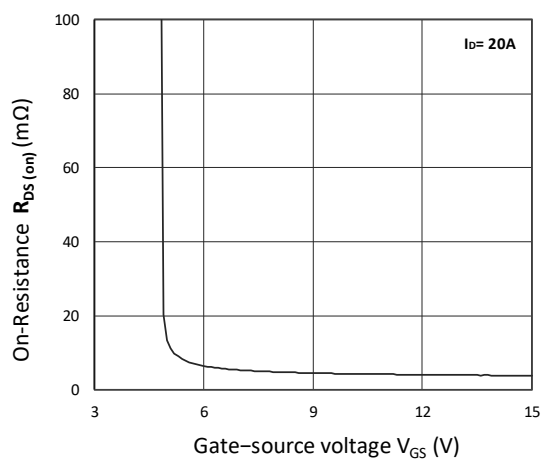
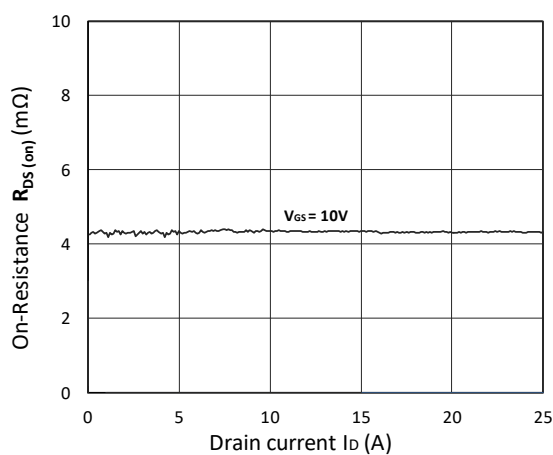
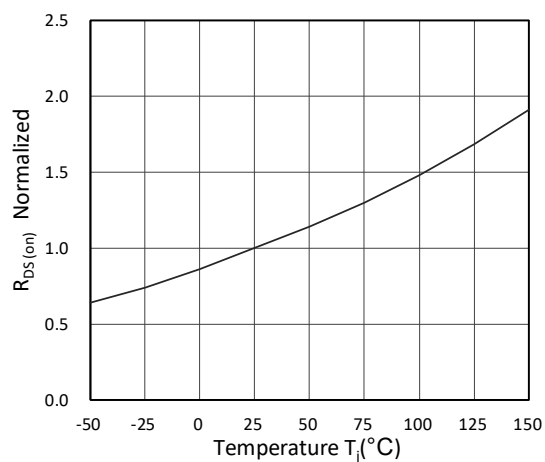


Figure 3. Forward Characteristics of Reverse

Figure 4. $R_{DS(on)}$ vs. V_{GS} Figure 5. $R_{DS(on)}$ vs. I_D Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

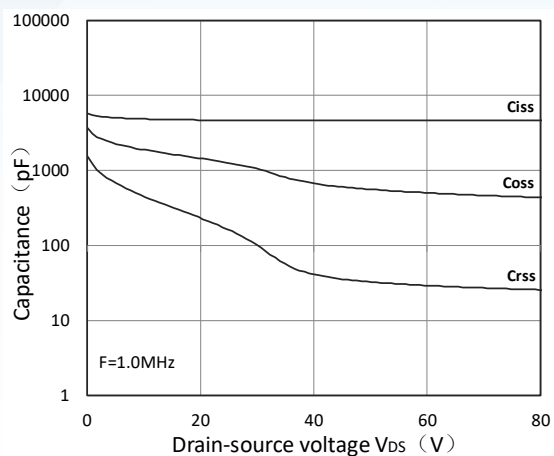


Figure 7. Capacitance Characteristics

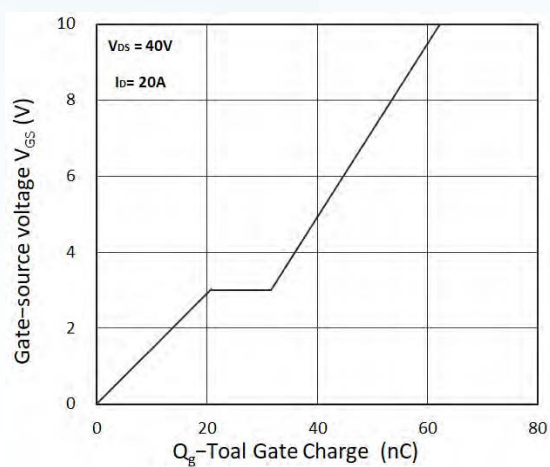


Figure 8. Gate Charge Characteristics

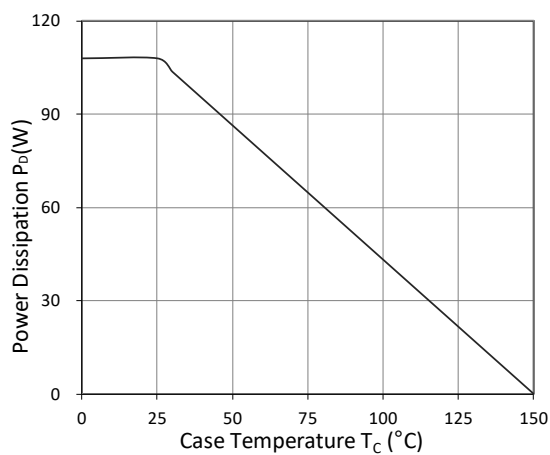


Figure 9. Power Dissipation

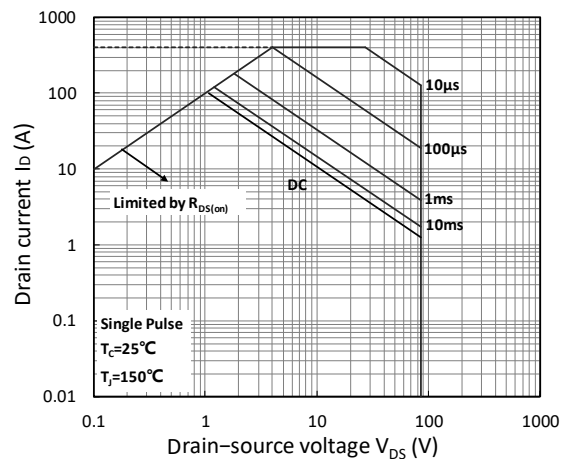


Figure 10. Safe Operating Area

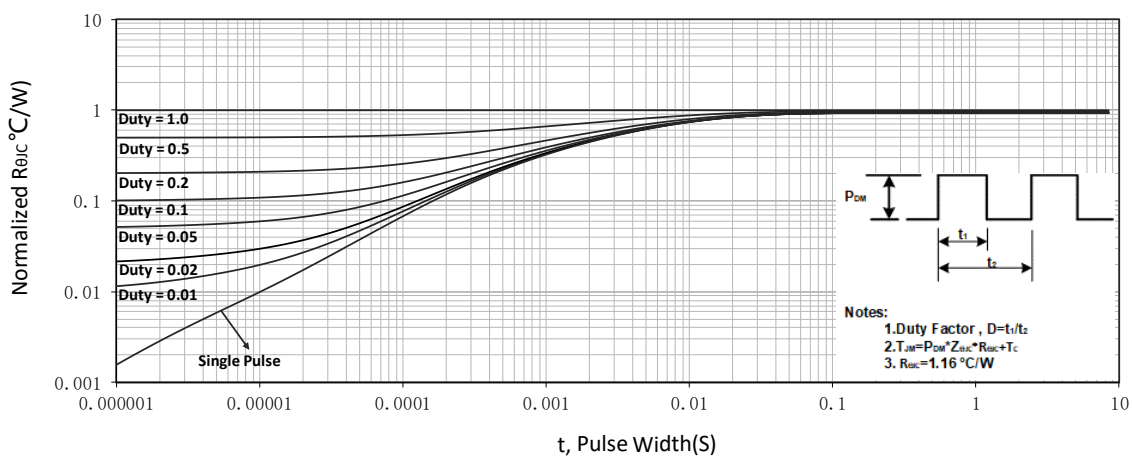
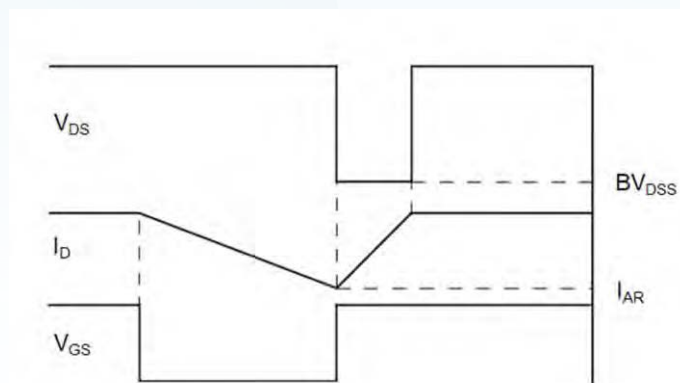
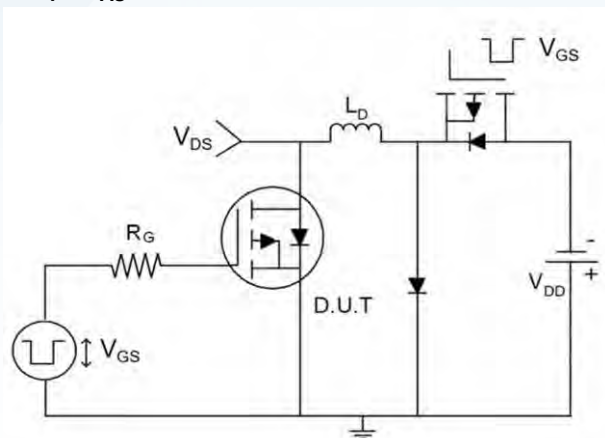
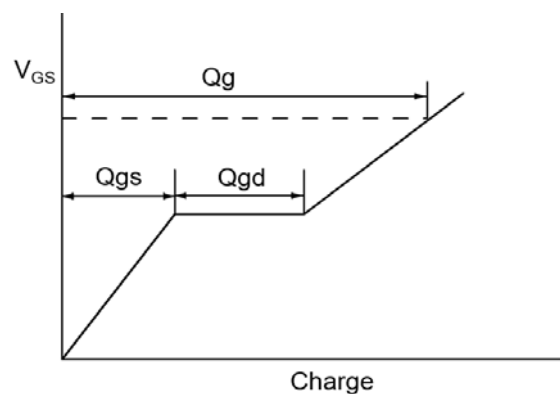
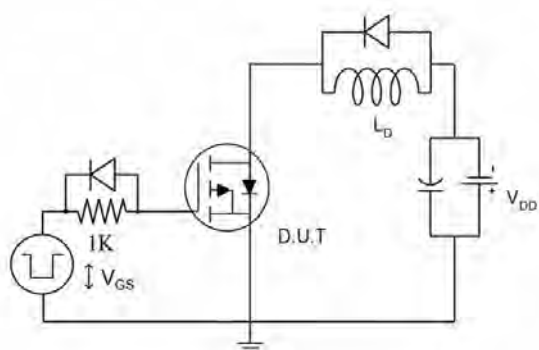


Figure 11. Normalized Maximum Transient Thermal Impedance

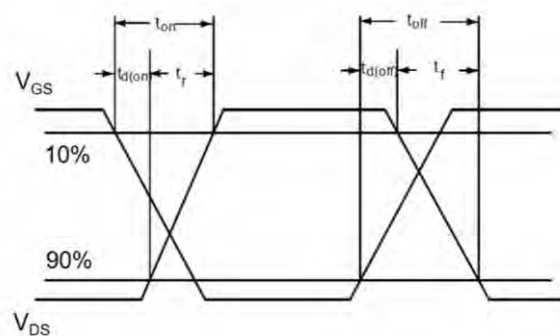
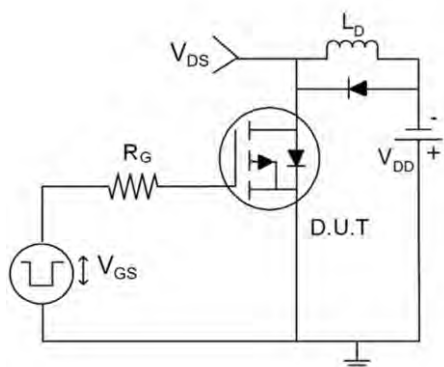
1) E_{AS} Test Circuits

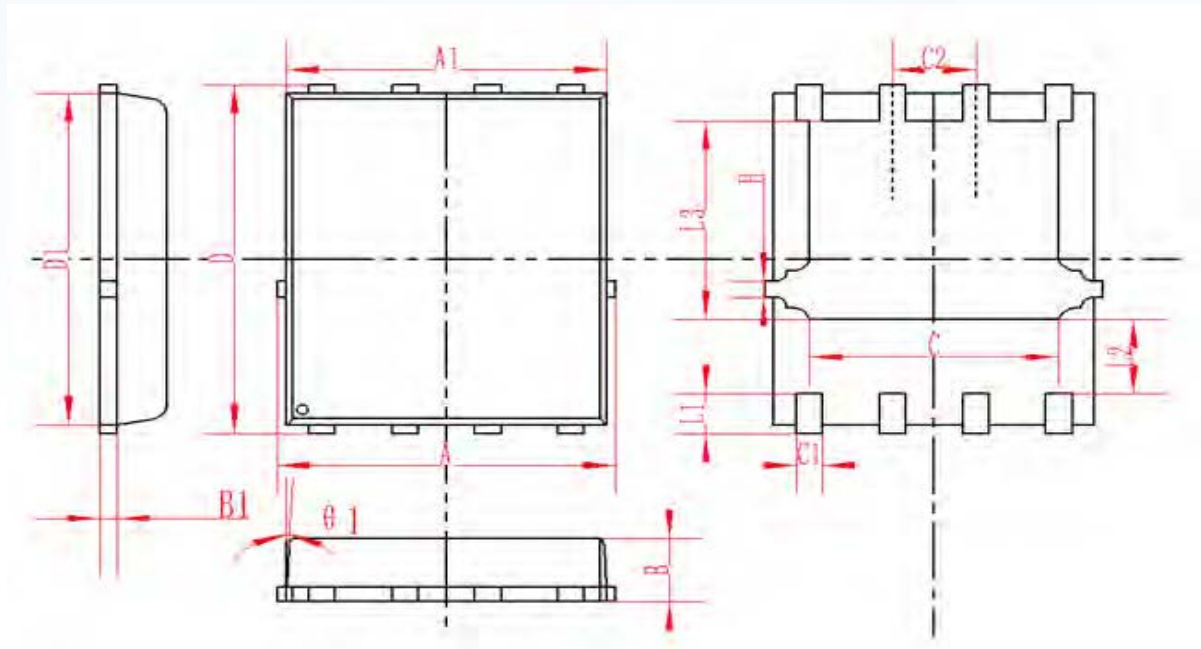


2) Gate Charge Test Circuit



3) Switch Time Test Circuit



DFN5X6-8L Package Information


SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010

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