钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TPS70933

具有使能功能的 TPS709 150mA、30V、1μA I_Q 稳压器

网址 www.sztdbdt.com

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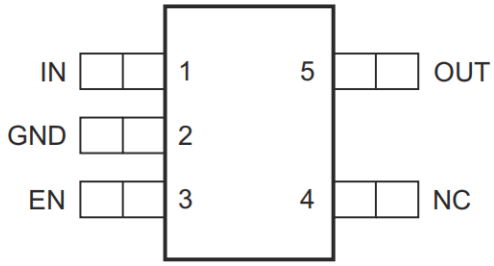
semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Ultra-low IQ: 1 μ A
- Reverse current protection
- Low I shutdown: 150nA
- Input voltage: 2.7 V to 30 V
- Supports 200mA peak output
- Accuracy within operating temperature range is 2%
- Fixed output available:
1.2 V to 6.5 V
- Thermal shutdown protection and overcurrent protection
- Package: SOT-23-5, WSON-6



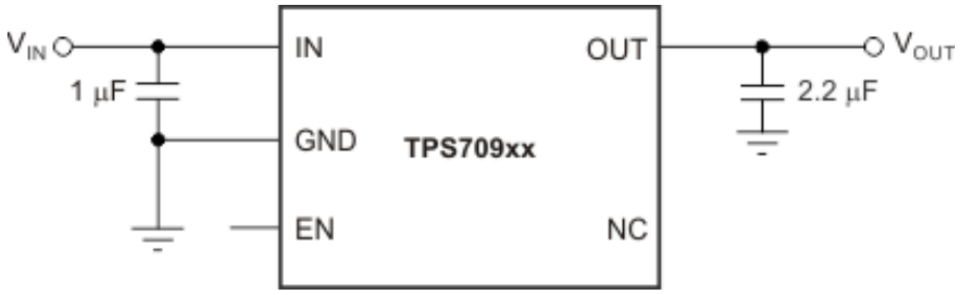
DBV Package, 5-Pin SOT-23,
Top View

Applications

- Smoke and heat detectors
- Thermostats
- Motion detectors (PIR, uWave, etc.)
- Cordless power tools
- battery packs
- Electricity meters
- Water meters

Description

The TPS709 series linear regulators are ultra-low quiescent current devices designed for power-sensitive applications. A precision bandgap and error provide 2% accuracy over the temperature range. With a quiescent current of only 1μA, this device is an ideal solution for battery-powered, always-on systems very low idle power dissipation. For added safety, these devices also feature thermal shutdown, current limiting, and reverse current protection.Shutdown mode is enabled by pulling the EN pin low The shutdown current in this mode is as low as 150nA (typical).



典型应用电路

表 **5-1. Pin Functions**

PIN					I/O	DESCRIPTION
NAME	DRV TPS709	DBV TPS709	DBV TPS709A	DBV TPS709B		
EN	4	3	5	5	I	Enable pin. Drive this pin high to enable the device. Drive this pin low to put the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	2	1	—	Ground
IN	6	1	3	2	I	Unregulated input to the device
NC	2, 5	4	4	4	—	No internal connection
OUT	1	5	1	3	O	Regulated output voltage. Connect a small 2.2-µF or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad		—	—	—	—	The thermal pad is electrically connected to the GND node. Connect this pad to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

specified at T_J = – 40°C to 125°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	– 0.3	32	V
	V_{EN}	– 0.3	7	
	V_{OUT}	– 0.3	7	
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Operating junction temperature, T_J		– 55	150	°C
Storage temperature, T_{stg}		– 55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
V_{EN}	Enable voltage	0		6.5	V
T_J	Operating junction temperature	– 40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS709		UNIT
		DBV	DRV	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.1	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.5	97.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.86	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.7	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at ambient temperature (T_A) = –40°C to +85°C, V_{IN} = $V_{OUT(typ)}$ + 1 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-μF ceramic (unless otherwise noted); typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	V_{OUT} < 3.3 V	–2%		2%	
		V_{OUT} ≥ 3.3 V	–1%		1%	
ΔV_{OUT}	Line regulation	($V_{OUT(nom)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = $V_{OUT(typ)}$ + 1.5 V or 3 V (whichever is greater), 100 μA ≤ I_{OUT} ≤ 150 mA		20	50	
V_{DO}	Dropout voltage(1) (3)	TPS70933, I_{OUT} = 50 mA		295	650	mV
		TPS70933, I_{OUT} = 150 mA		960	1400	
		TPS70950, I_{OUT} = 50 mA		245	500	
		TPS70950, I_{OUT} = 150 mA		690	1200	
		TPS70965, I_{OUT} = 50 mA		180	500	
		TPS70965, I_{OUT} = 150 mA		460	1000	
$I_{(CL)}$	Output current limit(4)	V_{OUT} = 0.9 × $V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.05	μA
		I_{OUT} = 0 mA, V_{OUT} > 3.3 V		1.4	2.25	
		I_{OUT} = 150 mA		350		
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		
		f = 1 kHz		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		μV_{RMS}
t_{STR}	Start-up time(2)	$V_{OUT(nom)}$ ≤ 3.3 V		200	600	μs
		$V_{OUT(nom)}$ > 3.3 V		500	1500	
$V_{EN(HI)}$	Enable pin high-level input voltage	Device enabled	0.9			V
$V_{EN(LOW)}$	Enable pin low-level input voltage	Device disabled	0		0.4	V
I_{EN}	EN pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
$I_{(REV)}$	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		
t_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		

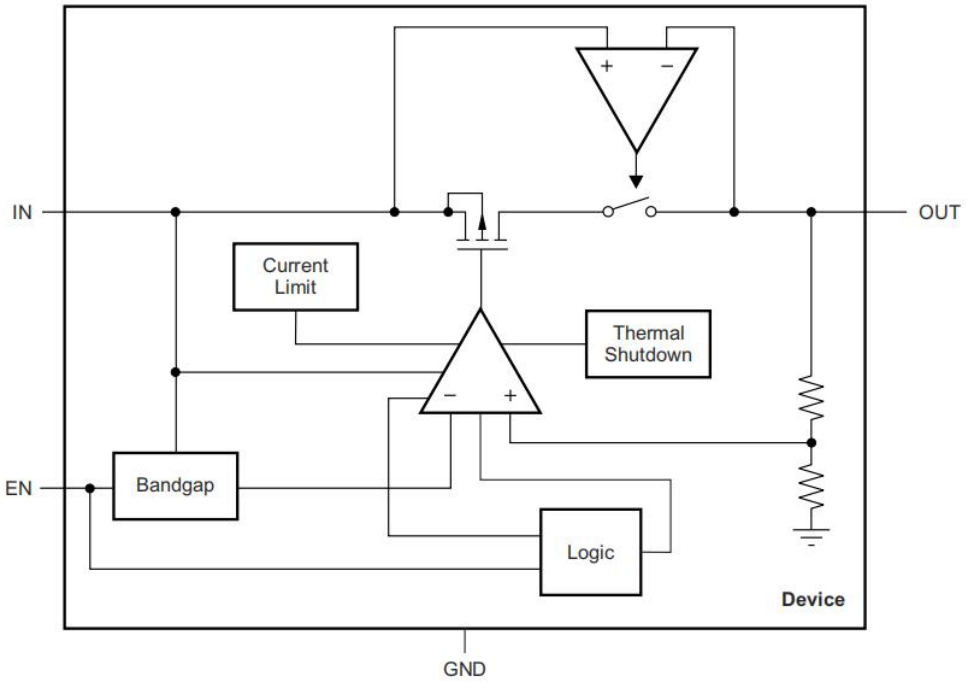
(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(nom)}$.
(2) Start-up time = time from EN assertion to 0.95 × $V_{OUT(nom)}$ and load = 47 Ω.
(3) Dropout is only valid when V_{OUT} ≥ 2.8 V because of the minimum input voltage limits.
(4) Measured with V_{IN} = V_{OUT} + 3 V for V_{OUT} ≤ 2.5 V. Measured with V_{IN} = V_{OUT} + 2.5 V for V_{OUT} > 2.5 V.

7 Detailed Description

7.1 Overview

The TPS709 series of devices are ultra-low quiescent current, low-dropout (LDO) linear regulators. The TPS709 offers reverse current protection to block any discharge current from the output into the input. The TPS709 also features current limit and thermal shutdown for reliable operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS709 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as (V_{OUT} = I_{LIMIT} × R_{LOAD}). The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Protection* section for more details.

The TPS709 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current. The TPS709 continues to operate for output currents between 150 mA and 200 mA but some data sheet parameters may not be met.

7.3.2 Dropout Voltage

The TPS709 use a PMOS pass transistor to achieve low dropout voltage. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

7.3.3 Undervoltage Lockout (UVLO)

The TPS709 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

7.3.4 Reverse-Current Protection

The TPS709 has integrated reverse-current protection. Reverse-current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse-current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 5.0-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

7.4 Device Functional Modes

The TPS709 has the following functional modes:

1. **Enabled:** When the enable pin (EN) goes above 0.9 V, the device is enabled. EN is pulled high by a 300-nA current source; therefore, EN can be left floating to enable the device. Do not connect EN to VIN. The EN pin is clamped by a 6.5-V Zener diode. Do not exceed the 7-V absolute maximum rating on the enable pin or excessive current flowing into the Zener clamp will destroy the device.
2. **Disabled:** When EN goes below 0.4 V, the device is disabled. During this time, OUT is high impedance and the current into IN ($I_{(SHUTDOWN)}$) is typically 150 nA.

8.1 Application Information

The TPS709 is a series of devices that consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, makes this device ideal for RF portable applications, current limit, and thermal protection. The TPS709 is specified from –40°C to +125°C.

8.1.1 Input and Output Capacitor

The TPS709 devices are stable with output capacitors with an effective capacitance of 2.0 μF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 μF. The maximum capacitance for stability is 47 μF. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 2.2-μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is necessary if line transients greater than 10 V in magnitude are anticipated.

8.1.2 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

8.2 Typical Application

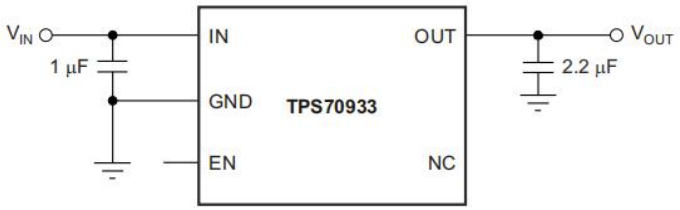


图 8-1. Wide Input, 3.3-V, Low-I_Q Rail

8.2.1 Design Requirements

表 8-1 summarizes the design requirements for 图 8-1.

表 8-1. Design Requirements for a Wide Input, 3.3-V, Low-I_Q Rail Application

PARAMETER	DESIGN SPECIFICATION
V_{IN}	5 V to 20 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 μA
I_{OUT} (max)	150 mA

8.2.2 Detailed Design Procedure

Select a 2.2-µF, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

Select a 1.0-µF, 25-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

8.2.3 Application Curves

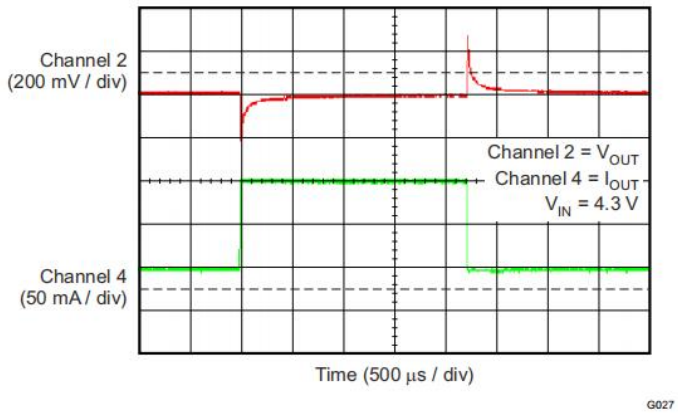


图 8-2. TPS70933 Load Transient (50 mA to 150 mA)

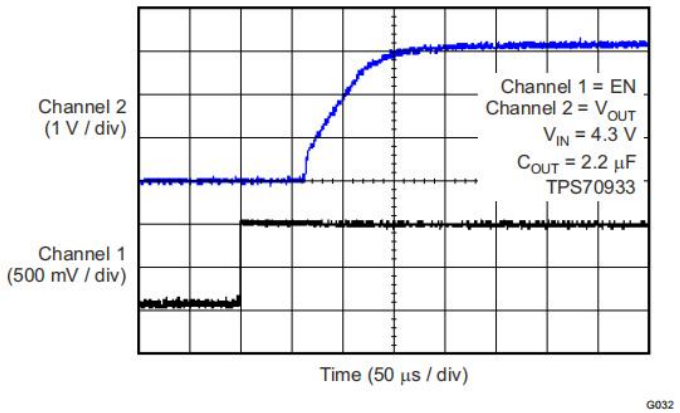


图 8-3. Power-Up With Enable

9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_{DISS}) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 方程式 1:

$$P_{DISS} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

10 Layout

10.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the device GND pin.

10.1.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS709 into thermal shutdown degrades device reliability.

10.2 Layout Example

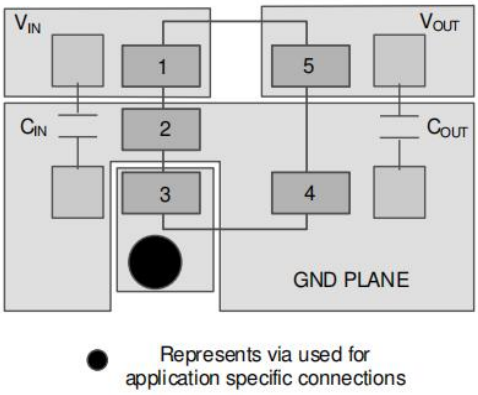
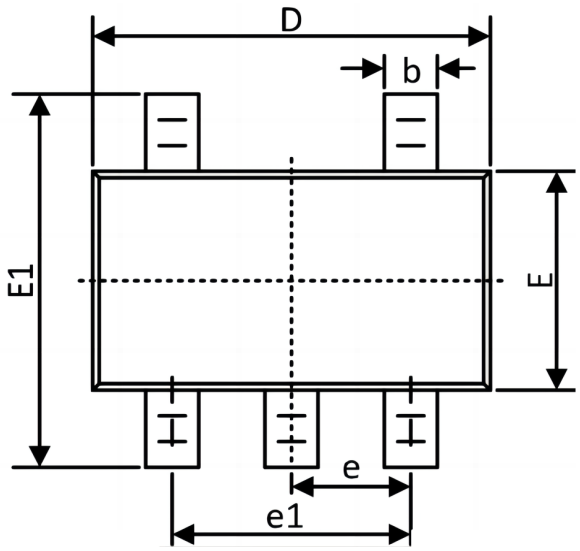


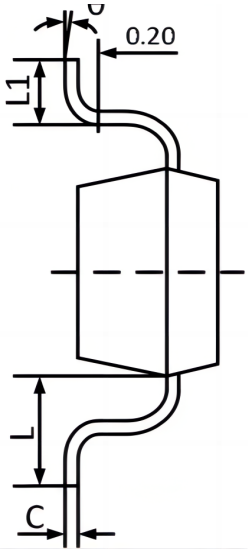
图 10-1. Layout Example for DBV Package

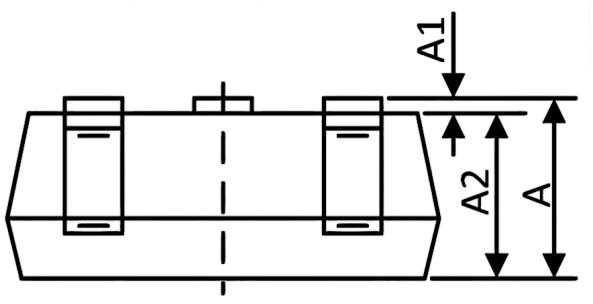
Order information

Order Number	Package	Package Quantity	Marking On The park
TPS70933DBVR-TUDI	SOT23	Tape,Reel,3000	TPS70933DBVR
TPS70933DBVT-TUDI	SOT23	Tape,Reel,3000	TPS70933DBVT

Package SOT23-5







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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