16 Multi-Function LED Driver and GPIO Controller with I²C Interface

Features

- 16 multi-function I/O, each for LED drive (current-source dimming) or GPIO mode
- P0_0~P0_1/P1_0~P1_3 support 2 intelligent breathing mode: BLINK and SMART-FADE, breathing time is adjustable
- 256 steps linear dimming in LED drive mode
- Any GPIO can be configured as an input or an output independently
- Support interrupt, 8μs deglitch, low-level active
- Standard I²C interface, AD1/AD0 select I²C device address
- SDA, SCL, RSTN, and all GPIO can accept in 1.8V logic input
- Supply shutdown function, low-level active
- 2.5V~5.5V power supply
- QFN 3×3-24L package

Applications

Cell Phone
PDA
MP3/MP4
CD
Mini display

General Description

AW9527 is a 16 multi-function LED driver and GPIO controller. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

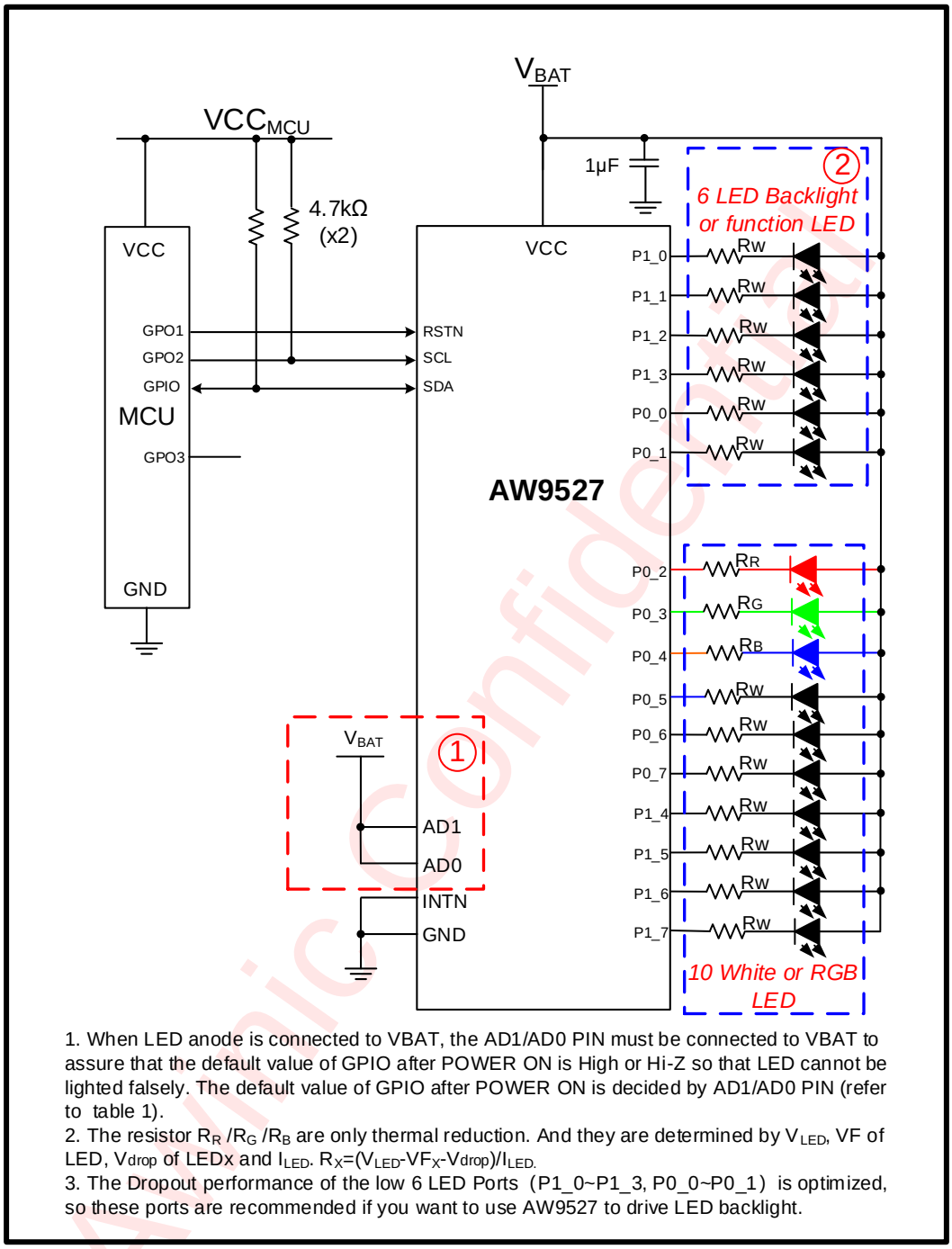
After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I²C device address selection inputs, AD0 and AD1. All I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9527 reads GPIO state through the I²C interface, the interrupt is cleared. Interrupt has 8μs deglitch.

When the I/O ports are configured as LED drive mode, AW9527 can set the current of LED drive between 0~IMAX by I²C interface, which is divided by 256 steps linear dimming. The default maximum current (IMAX) is 37mA, and IMAX can be changed in GCR register.

AW9527 supports two intelligent breathing modes: BLINK mode and SMART-FADE mode. BLINK mode allows LED automatic to flash periodically according the setting time parameter. P0_0~P0_1/ P1_0~P1_3 support intelligent breathing mode.

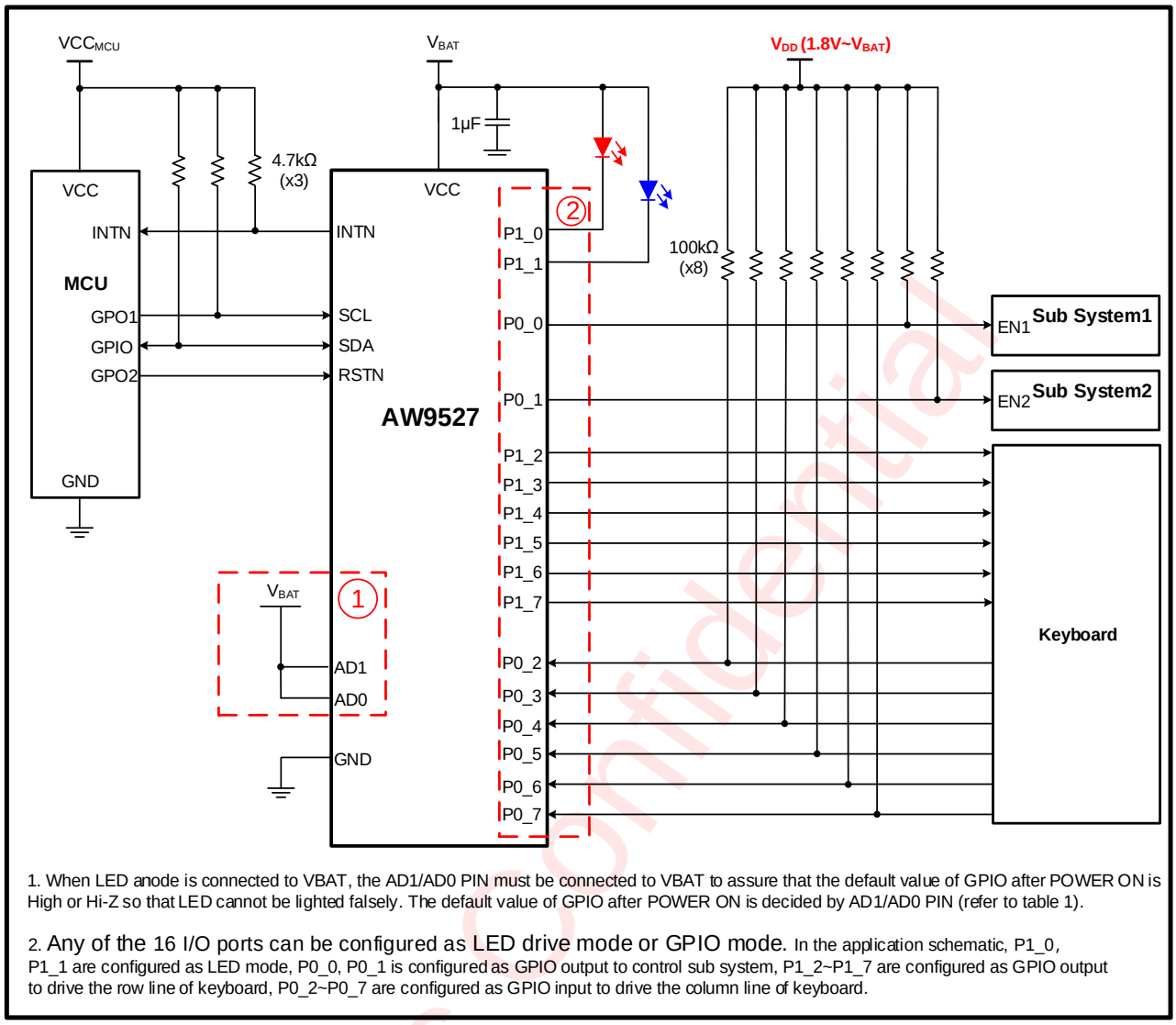
AW9527 is available in QFN 3×3-24L package, and 2.5V~5.5V power supply.

Typical Application Circuits



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).
2. The resistor R_R /R_G /R_B are only thermal reduction. And they are determined by V_{LED}, VF of LED, V_{drop} of LEDx and I_{LED}. $R_X=(V_{LED}-VF_X-V_{drop})/I_{LED}$.
3. The Dropout performance of the low 6 LED Ports（P1_0~P1_3, P0_0~P0_1）is optimized, so these ports are recommended if you want to use AW9527 to drive LED backlight.

Figure 1 Drive 16 function LED, including 6 ports feasible for LED backlight



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

2. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. In the application schematic, P1_0, P1_1 are configured as LED mode, P0_0, P0_1 is configured as GPIO output to control sub system, P1_2~P1_7 are configured as GPIO output to drive the row line of keyboard, P0_2~P0_7 are configured as GPIO input to drive the column line of keyboard.

Figure 2 Function LED + keyboard/IO Extended

Pin Configuration And Top Mark

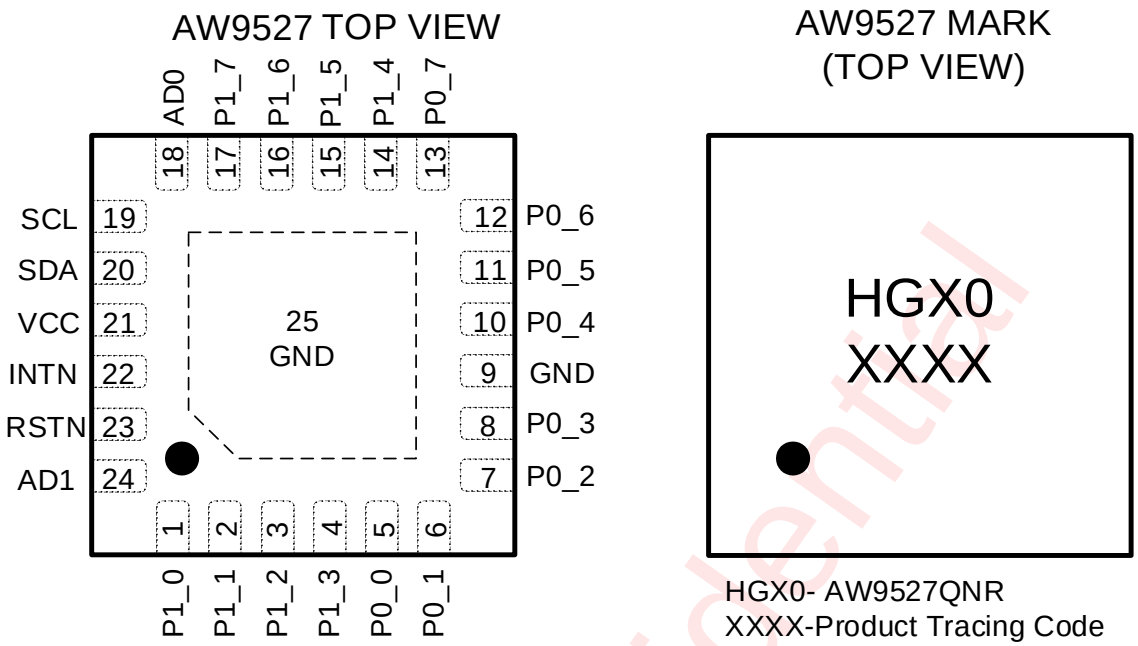


Figure 3 AW9527 PIN CONFIGURATION AND MARKING

Pin Definition

Pin No.	Name	Description
1	P1_0	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
2	P1_1	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
3	P1_2	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
4	P1_3	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
5	P0_0	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
6	P0_1	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode, support intelligence breathing mode. The default state after power on is related to AD1/AD0 PIN.
7	P0_2	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
8	P0_3	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.

Pin No.	Name	Description
9	GND	Ground supply
10	P0_4	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
11	P0_5	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
12	P0_6	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
13	P0_7	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
14	P1_4	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
15	P1_5	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
16	P1_6	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
17	P1_7	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
18	AD0	I^2C interface device address, connect to VBAT or GND, and control the default state of output pin (refer to table 1).
19	SCL	I^2C interface clock bus
20	SDA	I^2C interface data bus
21	VCC	Power supply
22	INTN	Interrupt output pin, open-drain mode, need external pull-up resistor; interrupt low active.
23	RSTN	Active LOW reset input. Connect to GND through a pull-down resistor if no active connection is used.
24	AD1	I^2C interface device address, connect to VBAT or GND, and control the default state of output pin (refer to table 1).
25	GND	Ground supply

Functional Block Diagram

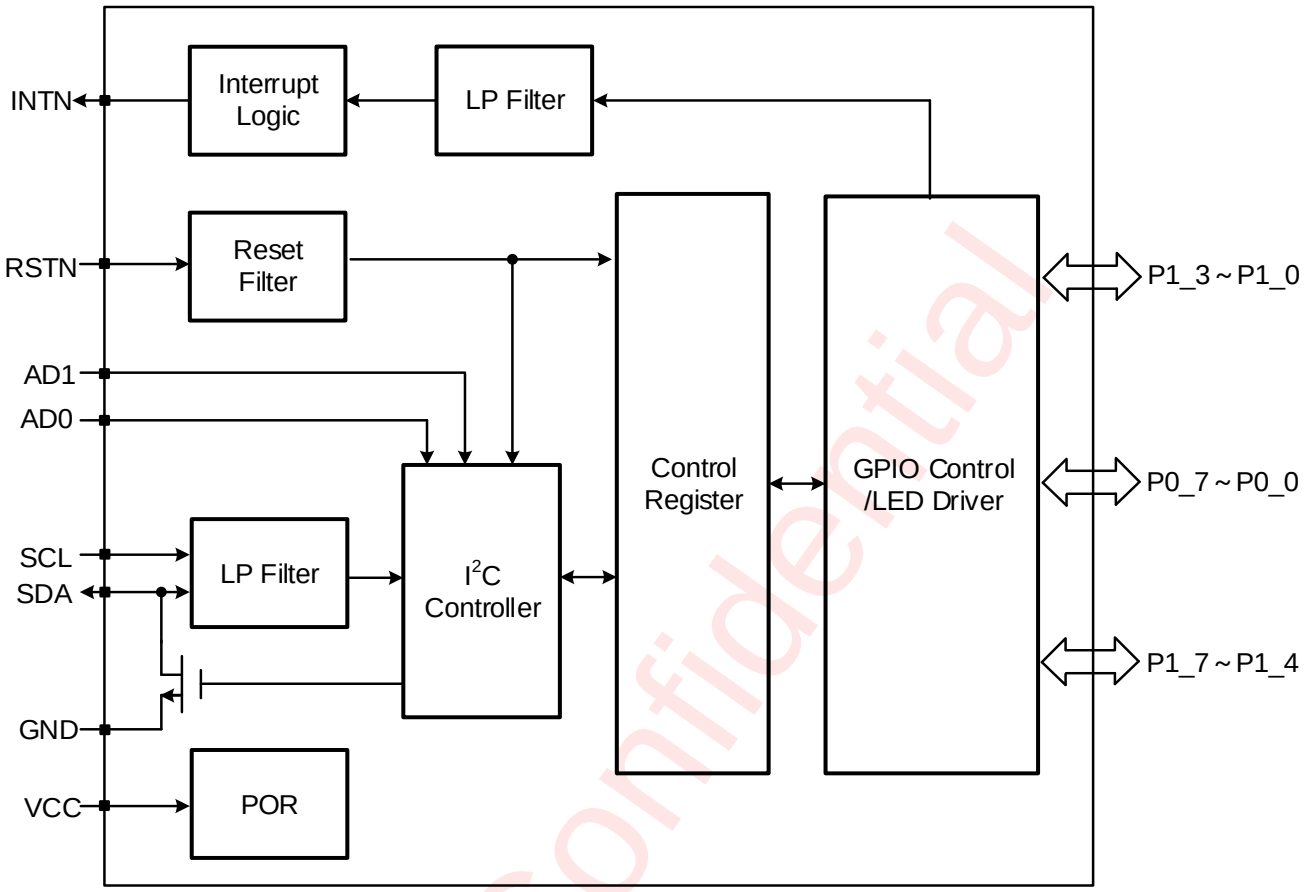


Figure 4 AW9527 Functional Block

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9527QNR	-40°C ~ 85°C	QFN 3mm×3mm -24L	HGX0	MSL3	RoHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Parameters	Range
Supply voltage, VCC	-0.3V to 6 V
SCL, SDA, AD0, AD1, INTN, RSTN, P0_0~P0_7, P1_0~P1_7	-0.3V to VCC
Max power(P_{Dmax}, package@ T_A=25°C)	1.2 W
Package thermal impedance, θ_{JA}	42°C /W
Max junction temperature, T_{Jmax}	150°C
Storage Temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE 2)	
HBM	±2000V
CDM	±1500V
Latch-Up	
Test Condition: JESD78F	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2023(HBM), ANSI/ESDA/JEDEC JS -002-2022(CDM).

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Input voltage	2.5	3.6	5.5	V
C_{IN}	Input capacitance	0.1	1	100	μF
T_A	Operating free-air temperature range	-40	25	85	°C

Electrical Characteristics

V_{CC}=3.8V, T_A=25°C for typical values (unless otherwise noted).

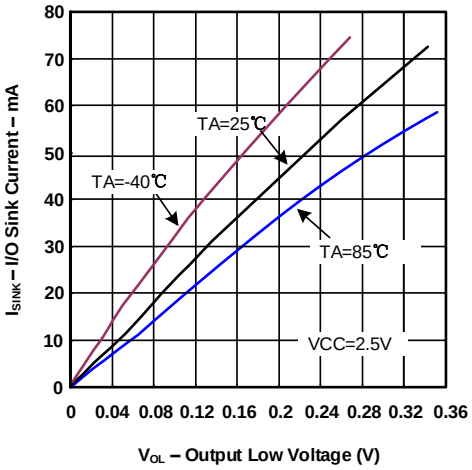
Parameter		Test Condition		Min.	Typ.	Max.	Unit
Supply voltage and current							
VCC	Supply voltage			2.5		5.5	V
$I_{shutdown}$	Shutdown current	RSTN=GND			0.1	5	μA
I_{CC}	Standby mode	RSTN=1.8V; V_I = GND or VCC; AD0=AD1=GND; I_O=0mA; F_{SCL}=0kHz	VCC=5.5V		30	60	μA
			VCC=3.6V		10	20	μA
			VCC=2.7V		2	5	μA
		RSTN=1.8V V_I = GND or VCC; AD0=AD1=GND; I_O=0mA; F_{SCL}=400kHz	VCC=5.5V		50	80	μA
			VCC=3.6V		12	24	μA
			VCC=2.7V		6	10	μA
LED Driver							
I_{MAX}	Max current of LED drive	Configure DIMx Reg. as FFH		31.9	37	43.1	mA
V_{drop1}	Dropout voltage on low 6 ports(P1-0~P1_3, P0_0~P0_1)	I_{OUT}=20mA			60		mV
V_{drop2}	Dropout voltage on high 10 ports(P0-2~P0_7, P1_4~P1_7)	I_{OUT}=20mA			80		mV
Digital pin output							
V_{OH}	High-level output voltage(P0_7~P0_0, P1_7~P1_0)	VCC=2.5V, I_{SOURCE}=10mA			VCC-170		mV
		VCC=3.6V, I_{SOURCE}=20mA			VCC-250		mV
		VCC=5V, I_{SOURCE}=20mA			VCC-200		mV
V_{OL}	Low-level output voltage(P0_7~P0_0, P1_7~P1_0)	VCC=2.5V, I_{SINK}=20mA			90		mV
		VCC=3.6V, I_{SINK}=20mA			70		mV
		VCC=5V, I_{SINK}=20mA			60		mV
V_{OL}	Low-level output voltage(SDA, INTN)	VCC=2.5V, I_{SINK}=6mA			150		mV
		VCC=3.6V, I_{SINK}=6mA			100		mV
		VCC=5V, I_{SINK}=6mA			75		mV
Digital pin input							
V_{IH}	High-level input voltage (SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)			1.4			V
V_{IL}	Low-level input voltage					0.4	V

Parameter		Test Condition	Min.	Typ.	Max.	Unit
	(SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)					
I_{IH}, I_{IL}	Input current(SCL, SDA, AD0, AD1, P0_7~P0_0, P1_7~P1_0)	V_I=VCC or GND	-0.2		+0.2	μA
$R_{\_RSTN}$	internal pull-low resistor in RSTN PIN			100k		Ω
C_I	Input capacitance(SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0)	V_I=VCC or GND		3		pF
t_{SP_RSTN}	Pulse width that RSTN PIN can filter	RSTN=VCC		10		μs

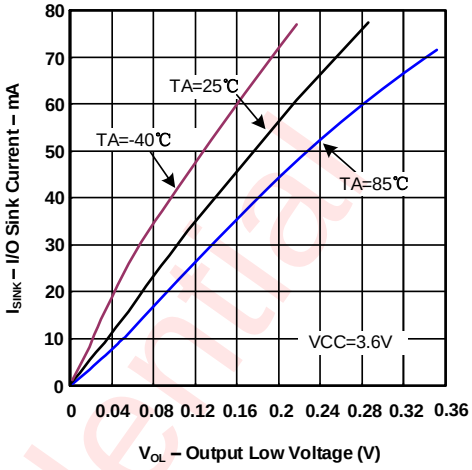
Typical Characteristics

Ambient temperature is 25°C, input voltage is 3.6V, unless otherwise noted .

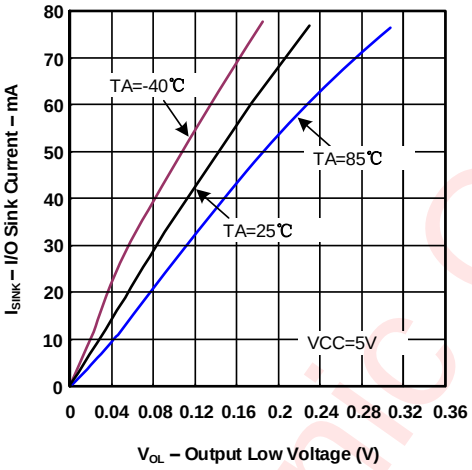
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



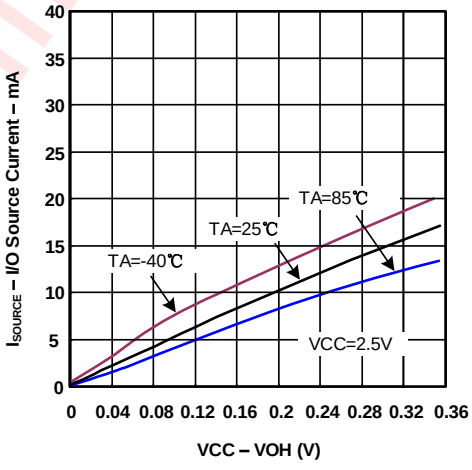
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



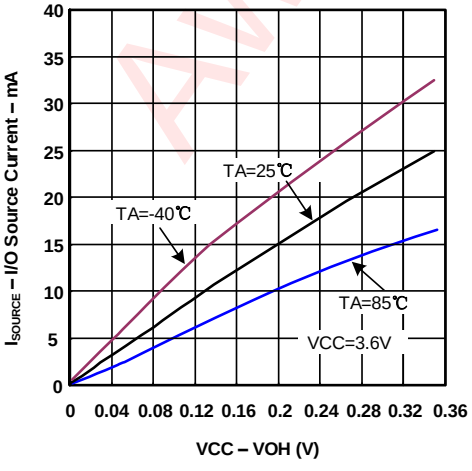
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



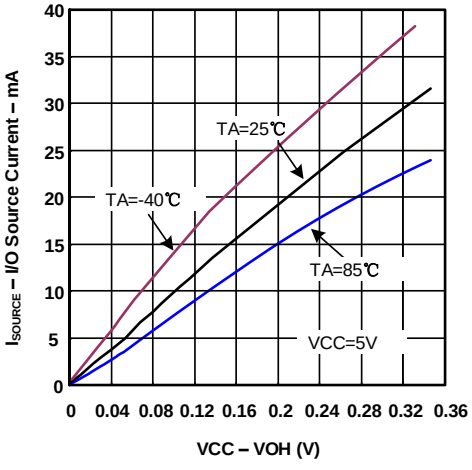
GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



I²C Interface Timing Requirements

Parameter		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

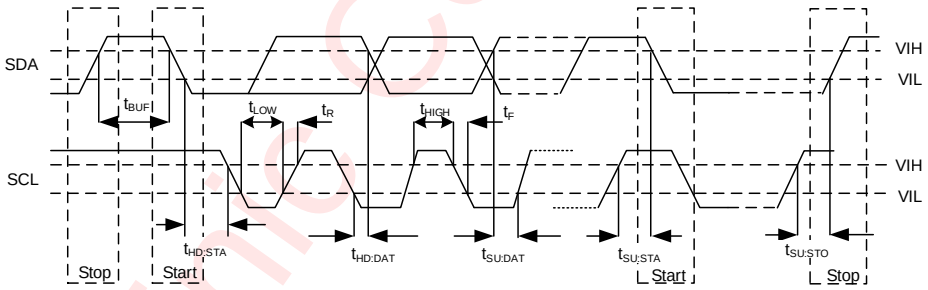


Figure 5 I²C Interface Timing

Detailed Functional Description

AW9527 is a 16 multi-function IO controller, which is applied for LED drive or GPIO. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

When configured as GPIO mode, all I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9527 read GPIO state through the I²C interface, the interrupt is cleared.

When configured as LED drive, drive current range is 0~IMAX, which has 256 steps. Default IMAX is 37mA, and it can be changed in GCR register.

AW9527 supports two types of intelligent breathing modes: BLINK and SMART-FADE. In BLINK mode, AW9527 completes "fade-on" and "fade-off" breathing periodically. In SMART-FADE mode, AW9527 runs "fade-on" and "fade-off" independently with register Output_Port0/ Output_Port1 configuration.

Power On

After power-up, about 100μs delay is required before RSTN set to high, otherwise, the device may work incorrectly. The minimal wait time for I²C communication is 5ms, during this period, some internal modules (such as LDO) start to work and reach a stable state.

Below is the recommended operation timing：

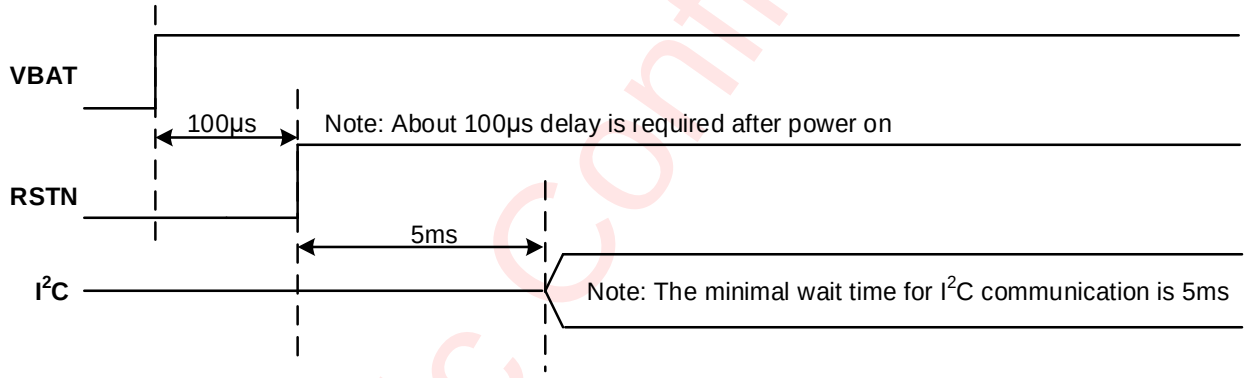


Figure 6 AW9527 Power On

GPIO Output

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I²C slave address selection inputs, AD0 and AD1, refer to table 1 for detail. The P1 port is Push-Pull mode; P0 port is Open-Drain mode (default) and can be configured as Push-Pull mode. When P0 port is Open-Drain mode, it need pull-up resistor.

Table 1. Default state of IO ports , AD1/AD0 and P0_x/P1_x

AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

GPIO Input/Output Direction Select

The register Config_Port0 and Config_Port1 can configure a port as input or output. Each bit of the register is corresponding to each port, the bit set '1' as input, '0' as output. The default value is '0' as output.

GPIO Input

User can get the current state of GPIO through reading the register Input_Port0 and Input_Port1 by I²C Interface. AW9527 GPIO support 1.8V logic input.

Interrupt

AW9527 can monitor IO state to generate interrupt when configure port as GPI and GPIO interrupt enabled. External MCU is required acknowledge by INTN pin. INTN is open-drain output, low-level active, and need external pull-up resistor.

When AW9527 detect port change, any input state from high-level to low-level or from low-level to high-level will generate interrupt after 8us internal deglitch. External MCU read Input_Port0/Input_Port1 register to clear interrupt. P1 port state change must clear interrupt by read Input_Port1 register; P0 port state change must clear interrupt by read Input_Port0 register.

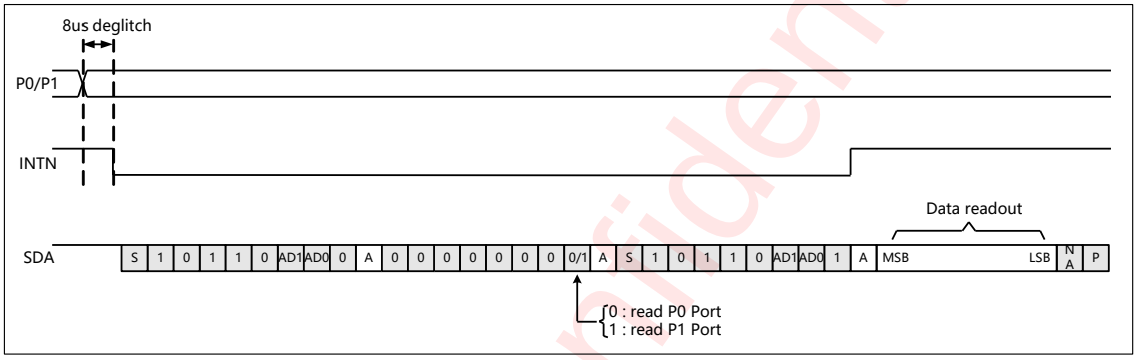


Figure 7 Interrupt generation and clear

LED Drive

AW9527 is co-anode current source LED drive. LED drive IMAX is configured by GCR (ISEL) register, to select 4 grades. The default IMAX is 37mA.

In LED drive mode, LED dim step can be manually controlled by external MCU. Drive current is from 0~IMAX divided by 256 steps.

Table 2. 256 steps dimming

DIMx bit								D
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	1/255×I_{MAX}
0	0	0	0	0	0	1	0	2/255×I_{MAX}
……								……
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

Blink Breathing Mode

P0_0~P0_1, P1_0~P1_3 of AW9527 supports BLINK breathing mode. In this mode, AW9527 will complete periodic blink effect automatically until exit the BLINK mode or close breathing function.

1. Configure P0_0~P0_1,P1_0~P1_3 to LED driver mode. According to application situation, set register PATEN to enable breathing mode. Set Config_Port0/ Config_Port1 (Table 8, 9 pay attention to the switch of GPIO and breathing function) to open BLINK function.
2. Configure the timing parameter for BLINK breathing effects:
   - Fade-on process——FDTMR.TFDON(Table 16). The time of fade-on effect has 6 kinds of choice (0ms~5040ms). The fade-on has 64 step dimming level and LED turns on gradually from dark.
   - Full on process——FUTMR.TFLON (Table 17). Full on state has 6 kinds of choice(0ms~5040ms). The LED driving current of this period is decided by GCR[1:0].
   - Fade-off process——FDTMR.TFDOFF(Table 16). The time of fade-off effect has 6 kinds of choice (0ms~5040ms). The fade-off has 64 step dimming level and LED turns off gradually from bright.
   - Full off process——FUTMR.TFLOFF (Table 17). Full off state has 6 kinds of choice(0ms~5040ms). The LED driving current is 0 in this period.
3. After setting blinking parameter, enable GO control bit and the LED in BLINK mode starts blink periodically and automatically. It is allowed to enable GO control bit only once. Before re-enabling GO control bit, it demands soft reset or hard reset, which means a reconfiguration of registers.

All ports share the same fade-on/ fade-off/ full-on/ full-off parameter. **None of these parameters can be set to zero. They can not be modified during blinking.**

AW9527 exits BLINK mode by disable Config_Port0/Config_Port1 corresponding bit or disable PATEN setting. The difference is AW9527 will exit BLINK immediately by disable PATEN, but we must wait it complete breathing period by another one. During BLINK mode, it is invalid to write dimming code. If the process of BLINK mode is interrupted, dimming code will maintain inner programmed code. So dimming code should be written after the end of an entire BLINK mode.

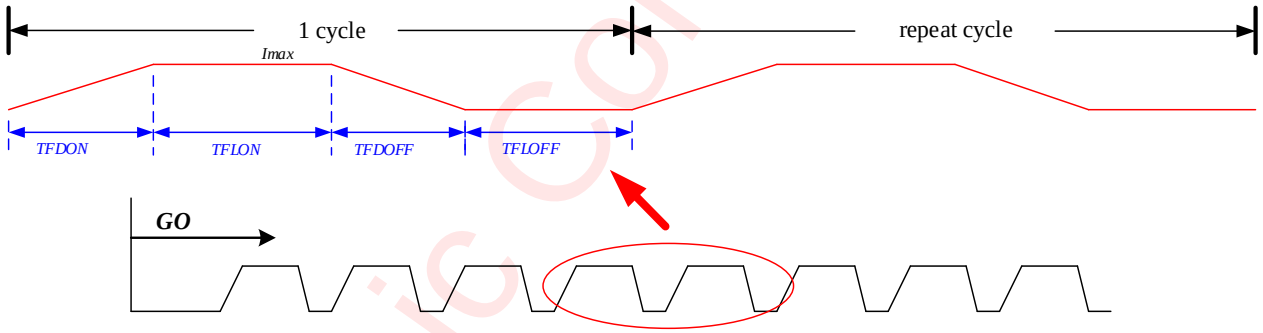


Figure 8 Blink Breathing Mode

Smart-Fade Mode

The SMART-FADE mode of AW9527 is semi-automatic breathing, which will simplify 64 steps fade-on and fade-off interface operation into 1bit writing operation: Writing '1' means current of LED fade-on to Imax; Writing '0' means current of LED fade-off to zero.

Configure SMART-FADE mode:

1. Set PATEN register and open breathing mode according to the application;
2. Set Config_Port0/ Config_Port1 (View Table 8, 9 pay attention to the switch of GPIO and breathing function), SMART-FADE mode is default;
3. Set Output_Port0/ Output_Port1 bit to complete fade-on or fade-off (View Table 6, 7 pay attention to the switch of GPIO and breathing function).

It is recommended that writing a "0" to corresponding bit in the Output_Port0/Output_Port1 register to avoid unexpected fade-on before enabling SMART-FADE mode. All ports share the same fade-on/ fade-off parameter. **These parameters must not be all zero and not be modified during fading on or off.**

During fading, it is not allowed to switch fade mode. For example, writing "0" to corresponding Output_Port0/ Output_Port1 is not allowed when fading on. Until reaching the maximum brightness, it is allowed to writing "0"

to corresponding Output_Port0/ Output_Port1.

AW9527 exits SMART-FADE mode by disable PATEN. During SMART-FADE mode, it is invalid to write dimming code. If the process of SMART-FADE mode is interrupted, dimming code will maintain inner programmed code. So dimming code should be written after the end of an entire SMART-FADE mode.

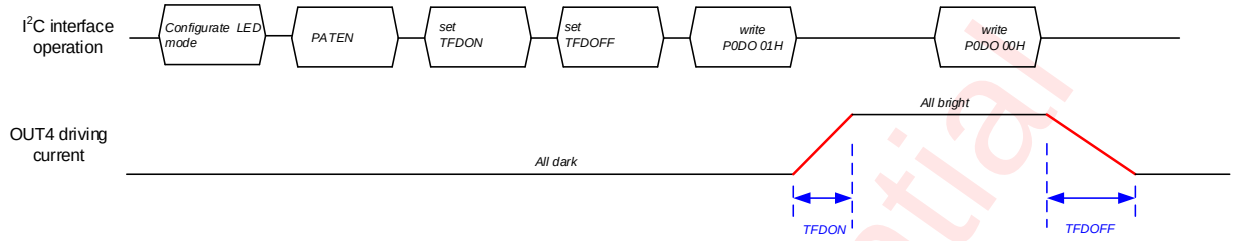


Figure 9 Smart-Fade Mode

I²C Interface

AW9527 support I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (AD1/AD0) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

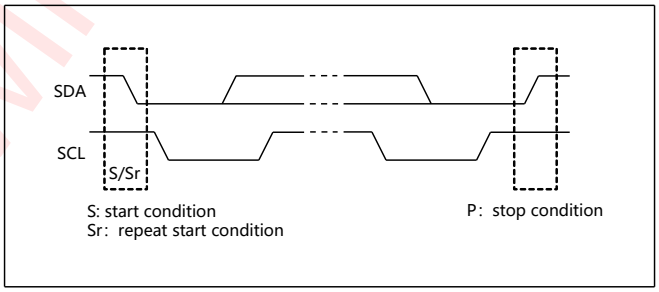


Figure 10 Start and stop condition

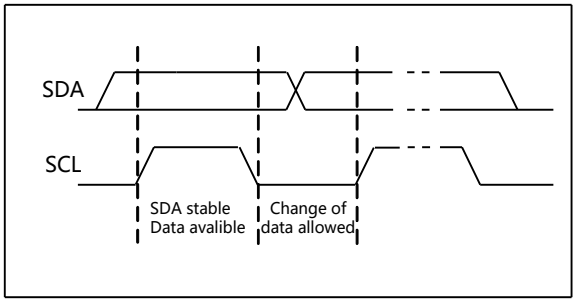


Figure 11 Bit Transfer

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

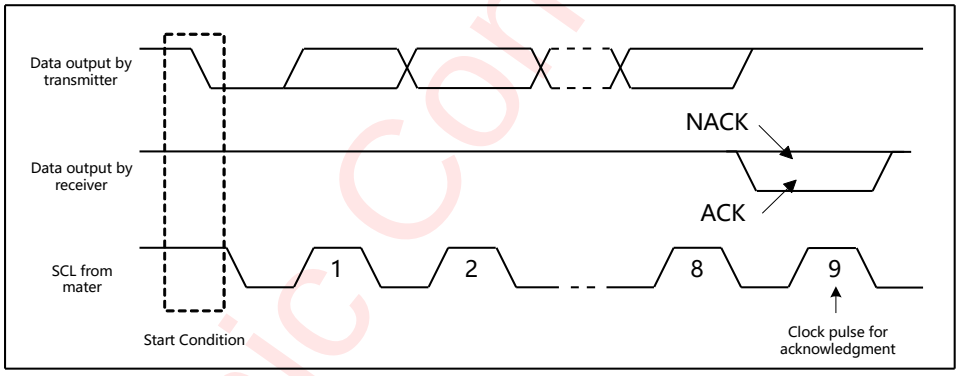


Figure 12 Acknowledgment On I²C Bus

Device Address

Below is the device address of AW9527. AD1/AD0 bit in device address match with AD1/AD0 pin respectively.

1	0	1	1	0	AD1	AD0	R/$\overline{W}$

AD1/AD0 value match with AW9527 pin AD1/AD0 respectively

Figure 13 AW9527 Device Address

Write

Data is transmitted to the AW9527 by sending the device address and setting the least-significant bit to a logic 0. The register address byte is sent after the device address and determines which register receives the data that follows the command byte.

After sending data to one register, the next data byte is sent to the other register. There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated

independently of the other registers.

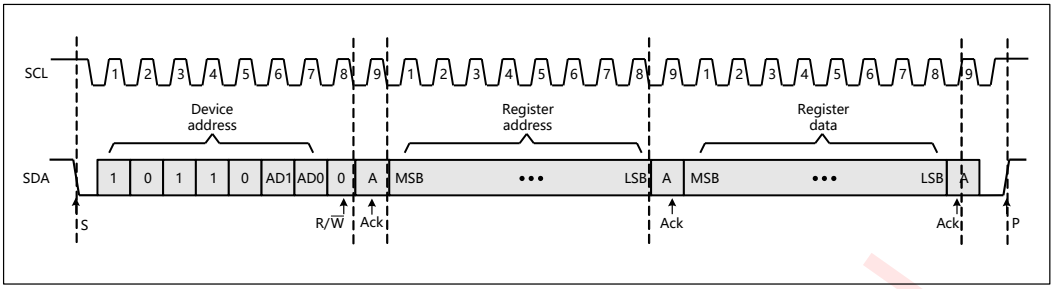


Figure 14 AW9527 Write Operation

Read

The bus master first must send the AW9527 address with the least-significant bit set to a logic 0. The register address byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the register address byte then is sent by the AW9527.

After a restart, the value of the register defined by the register address byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

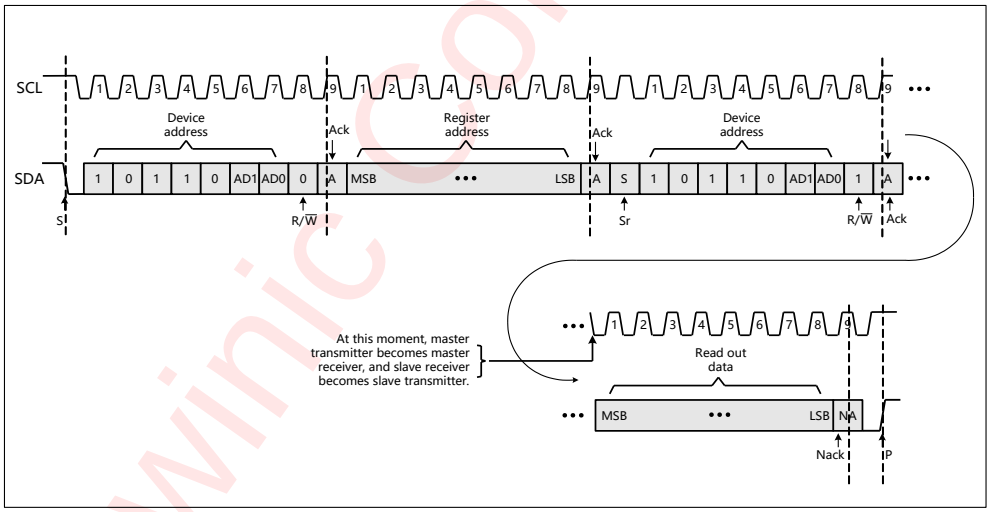


Figure 15 AW9527 Read Operation

Reset Function

AW9527 support 3 reset mode: power on reset, hardware reset, software reset. Each reset mode can reset registers to default value.

Hardware Reset

Hardware reset timing is as the following figure.

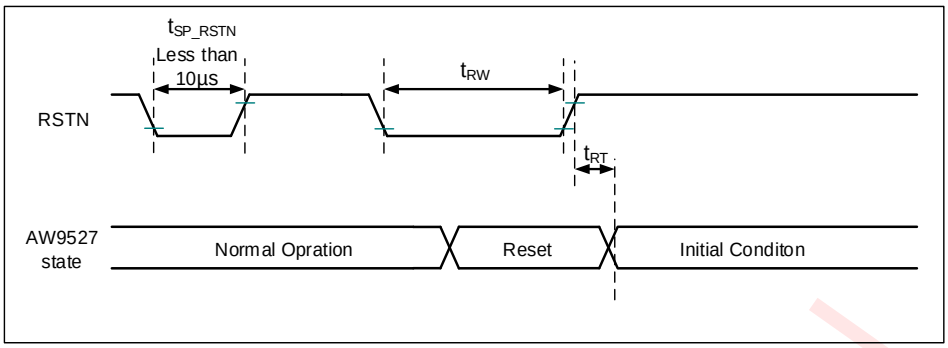


Figure 16 Hardware Reset Timing

Table 3. Hardware Reset Parameter

Parameter		Condition	min	typ	max	unit
t_{RW}	Reset pulse low level width	VSS=0V, VCC=2.5V~5.5V, T=-40℃~125℃	20			μs
t_{RT}	Reset recovery time		1			μs

Note:

1. The hardware reset PIN(RSTN)has a built-in deglitch block。Spike due to an electrostatic discharge on RSTN line does not cause irregular system reset according to the table below：

Reset pulse(RSTN)	AW9527 action
Shorter than 10μs(typical)	Reset Rejected
Longer than 20μs	Reset

2. After reset, AW9527 is in default state. All GPIO are configured as output, which value is decided by 2 device address (AD1/AD0) (refer to table 1). The interrupt (INTN) is cleared and pulled up by external pull-up resistor.
3. Spike Rejection also applies during a valid reset pulse as shown below:

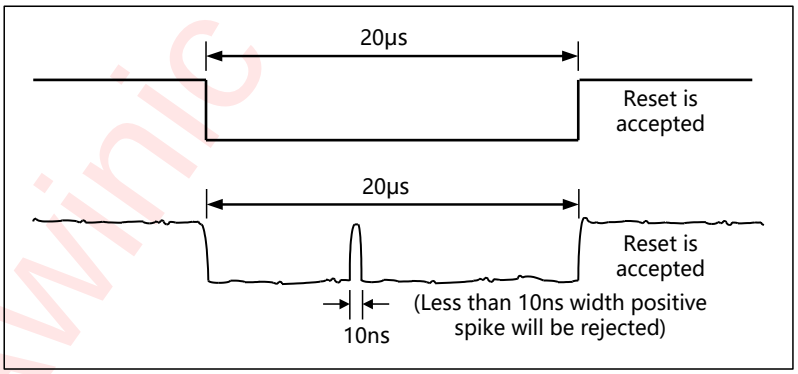


Figure 17 Operation When RSTN SLOW

Software Reset

AW9527 support software reset mode. Writing 00H to the software register(7FH) will generate a reset pulse. After software reset, AW9527 is in default state, which is the same as hardware reset. The software reset timing is as below. After the software reset command is send through the I^2C interface, it takes at least 1ms for chip to acknowledge the new I^2C command.

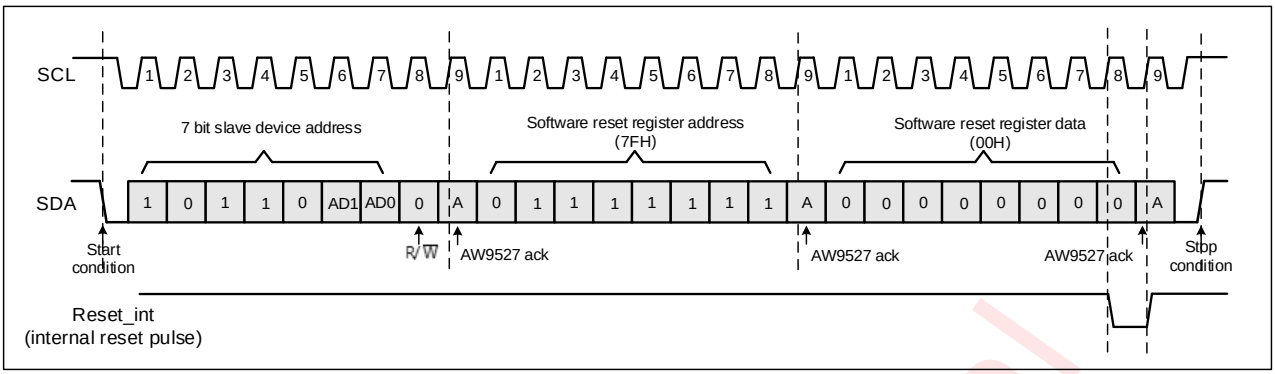


Figure 18 Software Reset Timing

Registers

Table 4. AW9527 register list

Address	W/R	Default Value	Function	Description
00H	R	Equal to P0	Input_Port0	P0 port input state
01H	R	Equal to P1	Input_Port1	P1 port input state
02H	W/R	Refer to table 1	Output_Port0	P0 port output state In SMART-FADE mode, P0_0~P0_1 can be used for “fade-on” and “fade-off” dimming control.
03H	W/R	Refer to table 1	Output_Port1	P1 port output state In SMART-FADE mode, P1_0~P1_3 can be used for “fade-on” and “fade-off” dimming control.
04H	W/R	00H	Config_Port0	P0 port direction configure In breathing mode, control P0_0~P0_1 to enter into BLINK mode or SMART-FADE mode.
05H	W/R	00H	Config_Port1	P1 port direction configure In breathing mode, control P1_0～P1_3 to enter into BLINK mode or SMART-FADE mode.
06H	W/R	00H	Int_Port0	P0 port interrupt enable
07H	W/R	00H	Int_Port1	P1 port interrupt enable
10H	R	23H	ID	ID register (read only)
11H	W/R	00H	GCR	Global control register
12H	W/R	FFH	P0WKMD	P0 port mode configure
13H	W/R	FFH	P1WKMD	P1 port mode configure
14H	W/R	00H	PATEN	Enable LED breathing mode
15H	W/R	00H	FDTMR	In BLINK or SMART-FADE mode, LED “fade-on” or “fade-off” time parameter
16H	W/R	00H	FLTMR	In BLINK mode, LED light all on or all off time parameter
20H	W	00H	DIM0	P1_0 LED current control
21H	W	00H	DIM1	P1_1 LED current control
22H	W	00H	DIM2	P1_2 LED current control
23H	W	00H	DIM3	P1_3 LED current control
24H	W	00H	DIM4	P0_0 LED current control
25H	W	00H	DIM5	P0_1 LED current control
26H	W	00H	DIM6	P0_2 LED current control
27H	W	00H	DIM7	P0_3 LED current control
28H	W	00H	DIM8	P0_4 LED current control
29H	W	00H	DIM9	P0_5 LED current control
2AH	W	00H	DIM10	P0_6 LED current control
2BH	W	00H	DIM11	P0_7 LED current control

Address	W/R	Default Value	Function	Description
2CH	W	00H	DIM12	P1_4 LED current control
2DH	W	00H	DIM13	P1_5 LED current control
2EH	W	00H	DIM14	P1_6 LED current control
2FH	W	00H	DIM15	P1_7 LED current control
7FH	W	00H	SW_RSTN	Soft reset
Other	-	-	-	Reserved

Register Detail Description

Table 5. Input state register(00H, 01H)

Address	Name	Description	Default
00H	Input_Port0	P0 port current logic state, 0-low level；1-high level	X
01H	Input_Port1	P1 port current logic state, 0-low level；1-high level	X

The Input state registers (00H,01H) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port registers will be accessed next.

Table 6. Port0 output state register (02H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Name	Description	Default
D7	Output_Port0[7]	P0_7 pin state 0：Low level 1：High level	Refer to table11
D6	Output_Port0[6]	P0_6 pin state 0：Low level 1：High level	
D5	Output_Port0[5]	P0_5 pin state 0：Low level 1：High level	
D4	Output_Port0[4]	P0_4 pin state 0：Low level 1：High level	
D3	Output_Port0[3]	P0_3 pin state 0：Low level 1：High level	
D2	Output_Port0[2]	P0_2 pin state 0：Low level 1：High level	
D1	Output_Port0[1]	P0WKMD[1]=1,as driving P0_1 pin state 0：Low level	

Bit	Name	Description	Default
		1：High level P0WKMD[0]=0 & PATEN[5]=1, P0_1 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D0	Output_Port0[0]	P0WKMD[0]=1,as driving P0_0 pin state 0：Low level 1：High level P0WKMD[0]=0 & PATEN[4]=1, P0_0 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Table 7. Port1 output state register (03H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D7	Output_Port1[7]	P1_7 pin state 0：Low level 1：High level	Refer to table1
D6	Output_Port1[6]	P1_6 pin state 0：Low level 1：High level	
D5	Output_Port1[5]	P1_5 pin state 0：Low level 1：High level	
D4	Output_Port1[4]	P1_4 pin state 0：Low level 1：High level	
D3	Output_Port1[3]	P1WKMD[3]=1,as driving P1_3 pin state 0：Low level 1：High level P1WKMD[3]=0 &PATEN[3]=1,P1_3 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D2	Output_Port1[2]	P1WKMD[2]=1,as driving P1_2 pin state 0：Low level 1：High level P1WKMD[2]=0 &PATEN[2]=1,P1_2 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D1	Output_Port1[1]	P1WKMD[1]=1,as driving P1_1 pin state 0：Low level 1：High level P1WKMD[1]=0 &PATEN[1]=1,P1_1 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Bit	Symbol	Description	Default
D0	Output_Port1[0]	P1WKMD[0]=1,as driving P1_0 pin state 0：Low level 1：High level P1WKMD[0]=0 &PATEN[0]=1,P1_0 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

The Output state register(02H, 03H)show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

P0_0~P0_1 and P1_0~P1_3 also support 2 intelligent breathing mode. When P0_0~P0_1 and P1_0~P1_3 configure as LED mode and corresponding PATEN is active, Output_Port0[0]~Output_Port0[1] and Output_Port1[0]~Output_Port1[3] is used to select fade-on or fade-off in Smart-Fade Mode respectively.

Table 8. Port0 configuration register (04H),GPIO input or output select register or as BLINK,SMART-FADE Mode select

Bit	Name	Description	Default
D7	Config_Port0[7]	P0_7 input or output choice 0：output 1：input	0
D6	Config_Port0[6]	P0_6 input or output choice 0：output 1：input	0
D5	Config_Port0[5]	P0_5 input or output choice 0：output 1：input	0
D4	Config_Port0[4]	P0_4 input or output choice 0：output 1：input	0
D3	Config_Port0[3]	P_3 input or output choice 0：output 1：input	0
D2	Config_Port0[2]	P0_2 input or output choice 0：output 1：input	0
D1	Config_Port0[1]	P0WKMD[1]=1, P0_1 input or output choice 0：output 1：input P0WKMD[1] =0 & PATEN[5]=1, P0_1 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	Config_Port0[0]	P0WKMD[0] =1, P0_0 input or output choice 0：output 1：input	0

Bit	Name	Description	Default
		P0WKMD[0] =0 & PATEN[4]=1, P0_0 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	

Table 9. Port1 configuration register (05H),GPIO input or output select register or as BLINK,SMART-FADE Mode select

Bit	Symbol	Description	Default
D7	Config_Port1[7]	P1_7 input or output choice 0：output 1：input	0
D6	Config_Port1[6]	P1_6 input or output choice 0：output 1：input	0
D5	Config_Port1[5]	P1_5 input or output choice 0：output 1：input	0
D4	Config_Port1[4]	P1_4 input or output choice 0：output 1：input	0
D3	Config_Port1[3]	P0WKMD[3] =1 , P1_3 input or output choice 0：output 1：input P0WKMD[3]=0 & PATEN[3]=1, P1_3 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D2	Config_Port1[2]	P0WKMD[2] =1 , P1_2 input or output choice 0：output 1：input P0WKMD[2]=0 & PATEN[2]=1, P1_2 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D1	Config_Port1[1]	P0WKMD[1] =1 , P1_1 input or output choice 0：output 1：input P0WKMD[1]=0 & PATEN[1]=1, P1_1 BLINK or SMART-FADE mode choice	0

Bit	Symbol	Description	Default
		0：SMART-FADE mode 1：BLINK mode	
D0	Config_Port1[0]	P0WKMD[0] =1 , P1_0 input or output choice 0：output 1：input P0WKMD[0]=0 & PATEN[0]=1, P1_0 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

The Configuration registers (04H, 05H) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

P0_0~P0_1 and P1_0~P1_3 also support 2 intelligent breathing mode. When P0_0~P0_1 and P1_0~P1_3 configure as LED mode and corresponding PATEN is active, Config_Port0[0]~Config_Port0[1] and Config_Port1[0]~Config_Port1[3] is used to select SMART-FADE mode or BLINK respectively.

Table 10. Interrupt enable register(06H, 07H)

Address	Name	Description	Default
06H	Int_Port0	P0 port interrupt enable. 0-enable; 1-disable	00H
07H	Int_Port1	P1 port interrupt enable. 0-enable; 1-disable	00H

The Interrupt enable register (06H, 07H) are used to configure the interrupt enable or disable of GPIO. If a bit in this register is set to 1, the interrupt function of the corresponding port pin is disabled. If a bit in this register is cleared to 0, the interrupt function of corresponding port pin is enabled. \

Table 11. ID register(10H)

Address	Name	Description	Default
10H	ID	ID register, read only, the readout value is 23H	23H

ID register(10H)is a read only register which stores the device ID. The ID read value of AW9527 is 23H.

Table 12. GCR ,Global control register(11H)

Address	Name	Description	Default
D[7]	GO	Writing 1 to enable breathing in BLINK mode.	0
D[6:5]	reserved	-	-
D[4]	GPOMD	Set P0 port GPIO output drive mode。if D[4]=0, P0 port is Open-Drain mode; if D[4]=1, P0 port is Push-Pull mode.	0
D[3:2]	reserved	-	-
D[1:0]	ISEL	256 step dimming range select 00：0~I_{MAX} 01：0~(I_{MAX}×3/4) 10：0~(I_{MAX}×2/4) 11：0~(I_{MAX}×1/4)	00

D[4] is used to configure P0 port output drive as Open-Drain or Push-Pull mode。When P0 port use as output

with Open-Drain mode, it needs pull-up resistor. If in Push-pull mode, it needs no pull-up resistor.

D[1:0] is used to configure the max drive current of LED。AW9527 set max current I_{MAX} to 37mA(typical) default, and through register ISEL[1:0] can set to I_{MAX}×1/4,I_{MAX}×2/4, I_{MAX}×3/4,I_{MAX},so the 256 step dimming range changes.

Except D4, D[1:0], other bits (D[7:5]\D[3:2]) are used for test purpose and the default value is 0. If user needs to configure register 11H, then the bits D[7:5]\D[3:2] must configure to 0, or system function error may occur.

Table 13. P0WKMD(12H), P0 Port GPIO control switch to LED driver register

Address	Name	Description	Default
12H	P0WKMD	Configure P0_7~P0_0 as LED or GPIO mode。 1：GPIO mode 0：LED mode	FFH

P0 Port GPIO control switch to LED driver register(12H)can configure P0 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 12H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 14. P1WKMD(13H), P1 Port GPIO control switch to LED driver register

Address	Name	Description	Default
13H	P1WKMD	Configure P1_7~P1_0 as LED or GPIO mode。 1：GPIO mode 0：LED mode	FFH

P1 Port GPIO control switch to LED driver register(13H)can configure P1 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 13H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 15. PATEN(14H), Enable Breathing REGISTER

Address	Name	Description	Default
D[7:6]	reserved	-	-
D[5]	PATEN[5]	P0_1 enable breath mode	0
D[4]	PATEN[4]	P0_0 enable breath mode	0
D[3]	PATEN[3]	P1_3 enable breath mode	0
D[2]	PATEN[2]	P1_2 enable breath mode	0
D[1]	PATEN[1]	P1_1 enable breath mode	0
D[0]	PATEN[0]	P1_0 enable breath mode	0

Table 16. FDTMR(15H),Fade-on or fade-off time setting register in BLINK or SMART-FADE

Address	Name	Description	Default
D[7:6]	reserved	-	-
D[5:3]	TFDOFF	Fade-off time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms	000

Address	Name	Description	Default
		others：Must not be configured	
D[2:0]	TFDON	Fade-on time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000

Table 17. FULL_TMR(16H),All-on or all-off time setting register in BLINK mode

Address	Name	Description	Default
D[7:6]	reserved	-	-
D[5:3]	TFLOFF	All-off time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000
D[2:0]	TFLON	All-on time setting 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms others：Must not be configured	000

Table 18. 256 step dimming control register (20H~2FH)

Address	Name	Description	Default
20H	DIM0	P1_0 port LED current control	00H
21H	DIM1	P1_1 port LED current control	00H
22H	DIM2	P1_2 port LED current control	00H
23H	DIM3	P1_3 port LED current control	00H
24H	DIM4	P0_0 port LED current control	00H
25H	DIM5	P0_1 port LED current control	00H
26H	DIM6	P0_2 port LED current control	00H
27H	DIM7	P0_3 port LED current control	00H
28H	DIM8	P0_4 port LED current control	00H
29H	DIM9	P0_5 port LED current control	00H
2AH	DIM10	P0_6 port LED current control	00H
2BH	DIM11	P0_7 port LED current control	00H
2CH	DIM12	P1_4 port LED current control	00H

2DH	DIM13	P1_5 port LED current control	00H
2EH	DIM14	P1_6 port LED current control	00H
2FH	DIM15	P1_7 port LED current control	00H

The dimming control register (20H~2FH) are used to configure P0 port and P1 port LED current. Each port supports 256 step dimming. For the detailed configuration, refer to table 2.

Table 19.Soft reset register(7FH)

Address	Name	Description	Default
7FH	Software Reset	Write 00H to generate a reset pulse	X

The soft reset register (7FH) support software reset function, which brings convenience to software engineer. Every time write 00H to this register, it generate a reset pulse. The software reset timing, please refer to figure 18.

Table 20. Reserve register

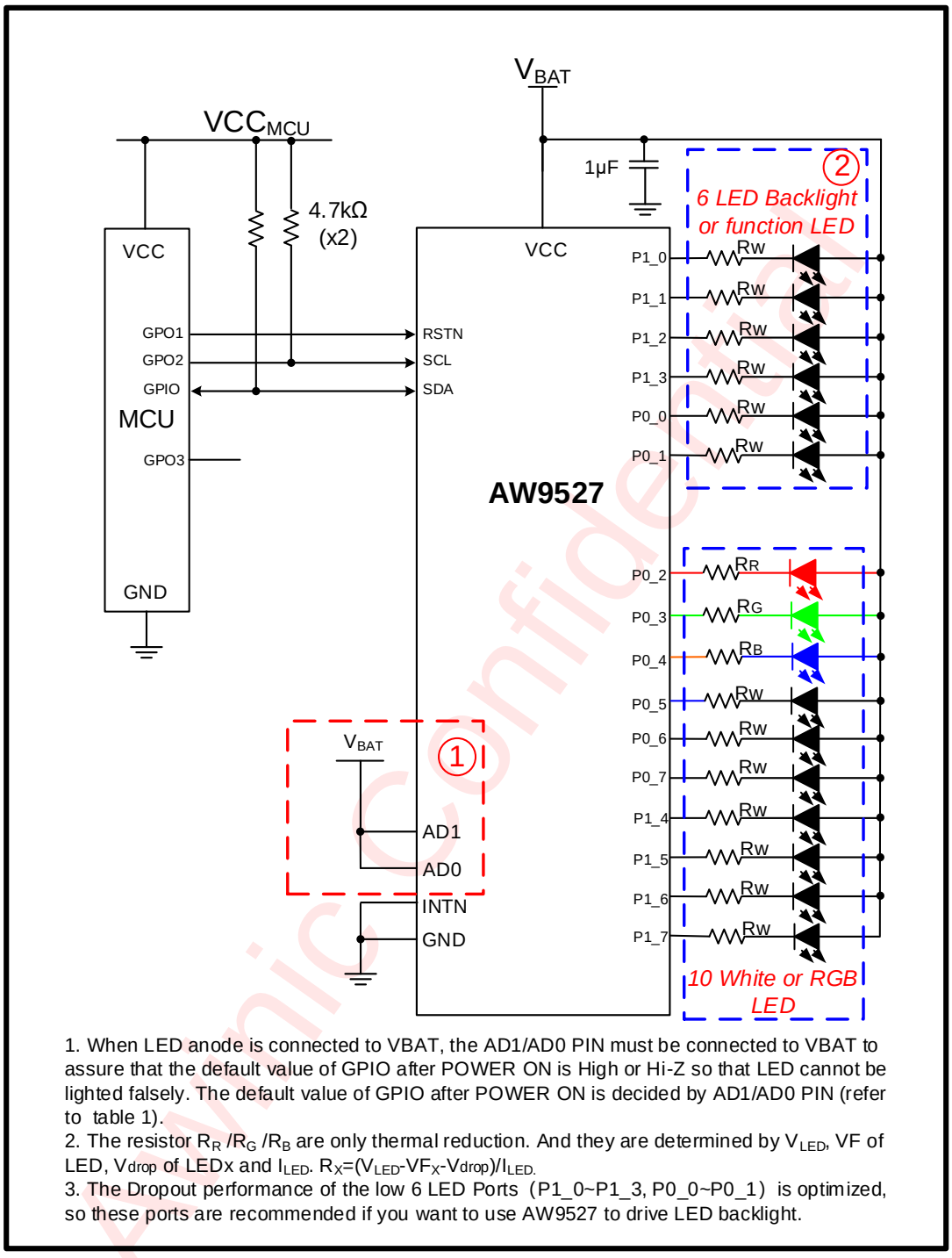
Address	Name	Description
08H~0FH 14H~1FH 30H~7EH 80H~FFH	Reserve register, for test purpose or not defined.	X

Reserve register(08H~10H, 14H~1FH, 30H~7EH, 80H~FFH)are for test purpose or not defined, user should not write these registers, or may cause function error.

Application Information

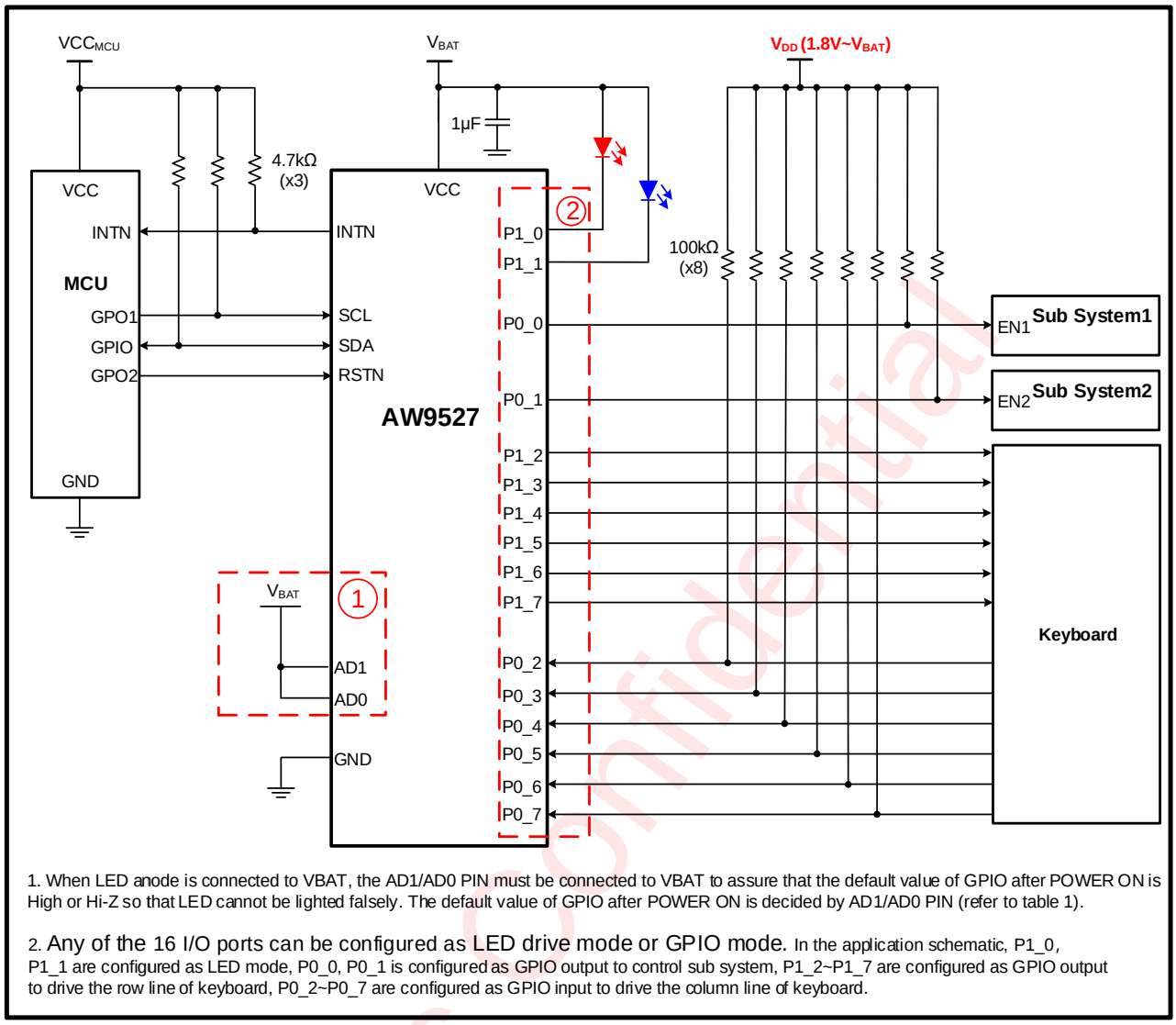
AW9527 is a 16 multi-function LED driver and GPIO controller. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently. After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I^{2}C device address selection inputs, AD0 and AD1. All I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9527 reads GPIO state through the I^{2}C interface, the interrupt is cleared. Interrupt has 8μs deglitch. When the I/O ports are configured as LED drive mode, AW9527 can set the current of LED drive between 0~IMAX by I^{2}C interface, which is divided by 256 steps linear dimming. The default maximum current (IMAX) is 37mA, and IMAX can be changed in GCR register. AW9527 supports two intelligent breathing modes: BLINK mode and SMART-FADE mode. BLINK mode allows LED automatic to flash periodically according the setting time parameter. P0_0~P0_1/P1_0~P1_3 support intelligent breathing mode.

Typical Application



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).
2. The resistor R_R /R_G /R_B are only thermal reduction. And they are determined by V_{LED}, VF of LED, V_{drop} of LEDx and I_{LED}. R_X=(V_{LED}-VF_X-V_{drop})/I_{LED}.
3. The Dropout performance of the low 6 LED Ports（P1_0~P1_3, P0_0~P0_1）is optimized, so these ports are recommended if you want to use AW9527 to drive LED backlight.

Figure 19 Drive 16 function LED, including 6 ports feasible for LED backlight



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

2. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. In the application schematic, P1_0, P1_1 are configured as LED mode, P0_0, P0_1 is configured as GPIO output to control sub system, P1_2~P1_7 are configured as GPIO output to drive the row line of keyboard, P0_2~P0_7 are configured as GPIO input to drive the column line of keyboard.

Figure 20 Function LED + keyboard/IO Extended

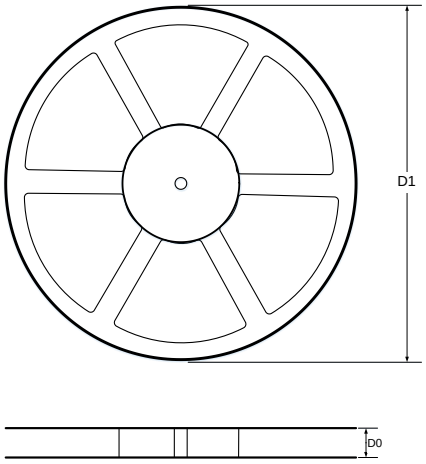
PCB Layout Consideration

To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

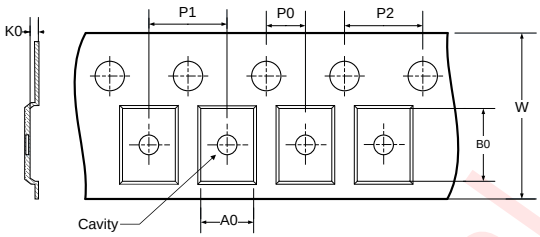
1. The C1 should be placed as close to the chip as possible.
2. The GND pad must be well connected to the ground of the PCB, and add as many thermal vias as possible near the GND on the PCB for the heat conductivity of the device and PCB.

Tape And Reel Information

REEL DIMENSIONS

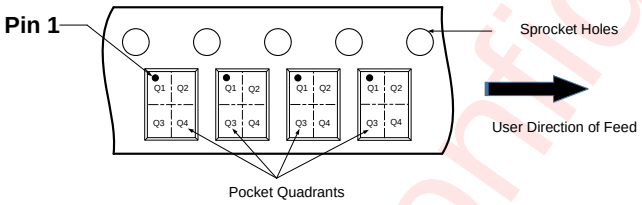


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



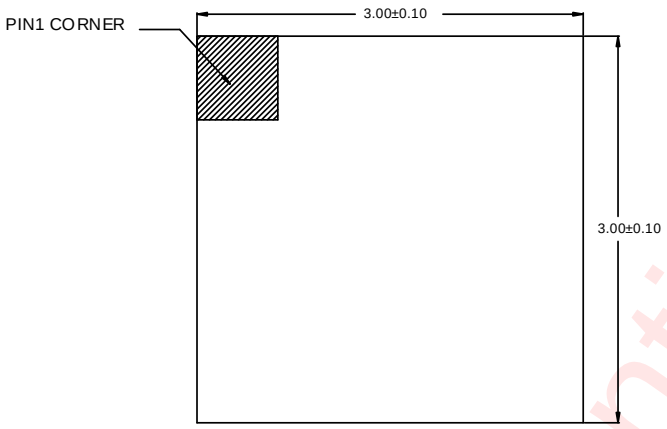
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

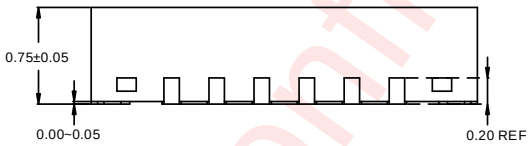
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

All dimensions are nominal

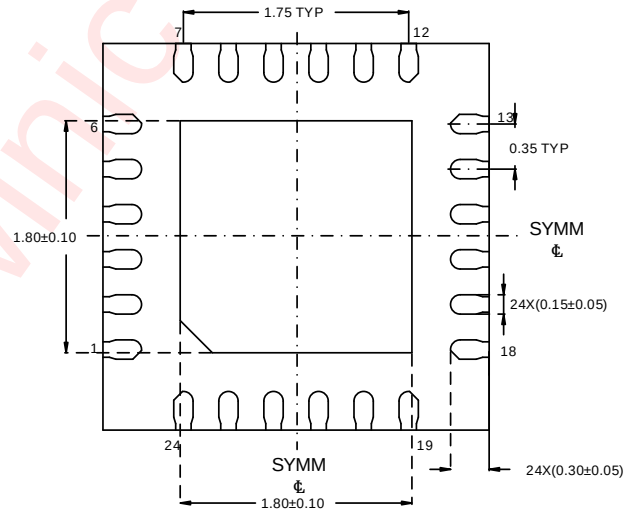
Package Description



Top View



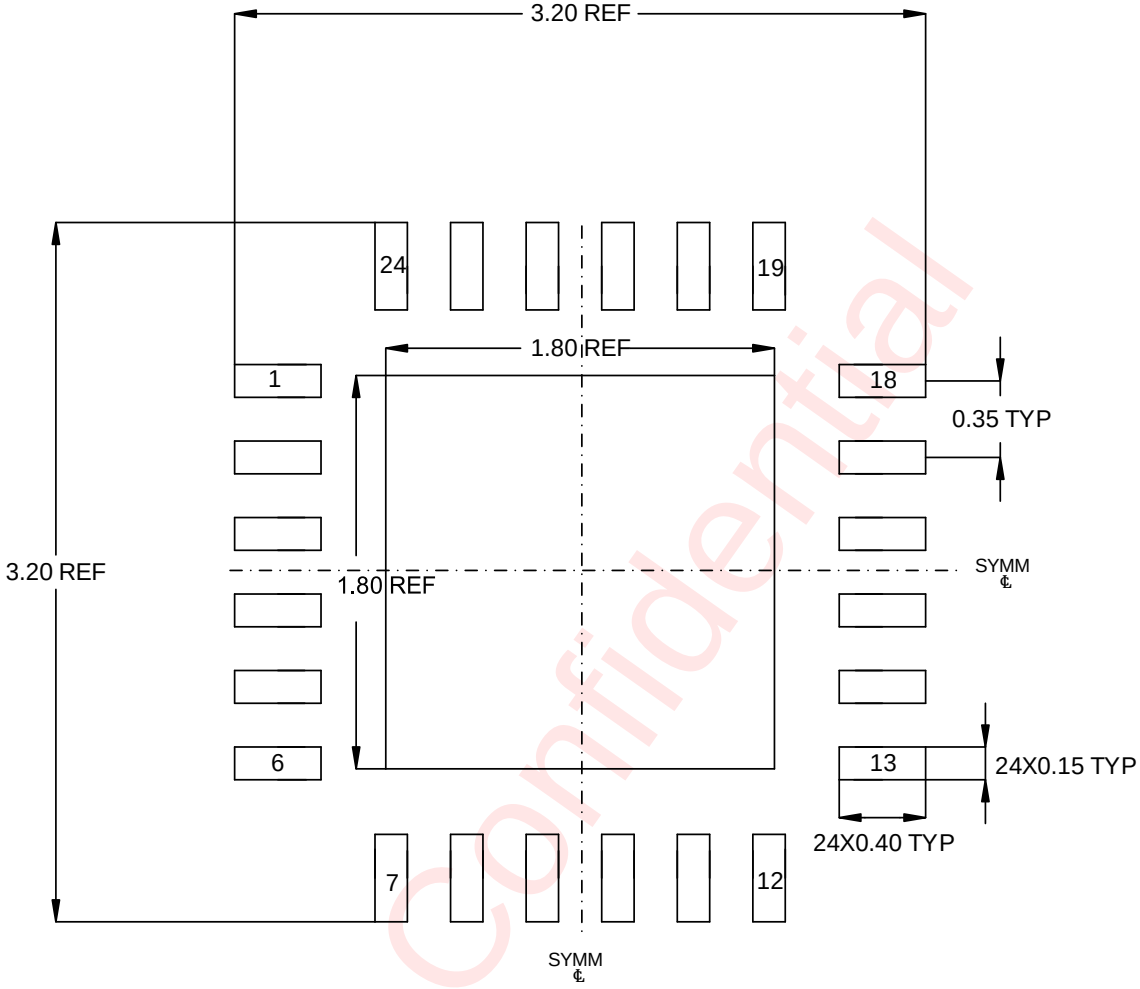
Side View

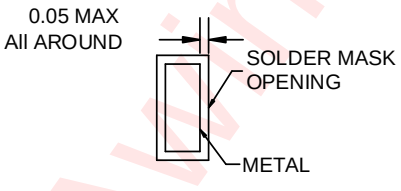


Bottom View

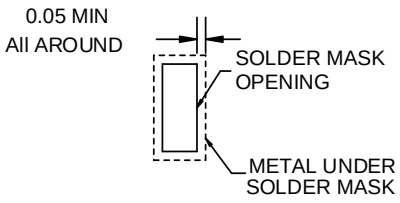
Unit: mm

Land Pattern Example





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Aug. 2024	Officially Released

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