

4xSPST MIPI Antenna Tuning Switch

Features

- High Voltage Handling
- Very Low On-Resistance, 1.1Ω
- Low Off- Capacitance, 160fF
- High linear performance
- MIPI RFFE V2.1 interface
- Small FCQFN 1.5mm x 1.1mm x 0.37mm - 10L package
- Single VIO supply, no VDD
- Broadband frequency range: 0.4 to 3.8GHz

Applications

- Antenna Tuning Switch
- Band Switching
- Impedance Tuning

General Description

The AW17145 is four single-pole-single-throw (4xSPST) antenna tuning switch, using CMOS silicon-on-insulator (SOI) process. The high voltage handling, high linear performance and very low R_{on} and C_{off} make the switch very suitable for high performance antenna tuning application.

The AW17145 is perfectly compatible with MIPI RFFE V2.1 control interface. It is provided very small FCQFN 1.5mm x 1.1mm x 0.37mm – 10L package.

Typical Application Circuit

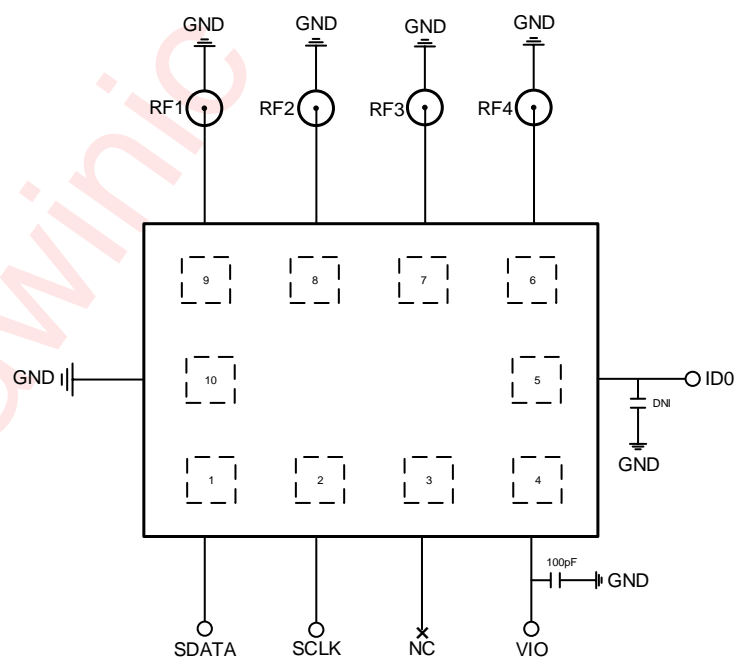


Figure 1 Typical Application Circuit of AW17145

Pin Configuration And Top Mark

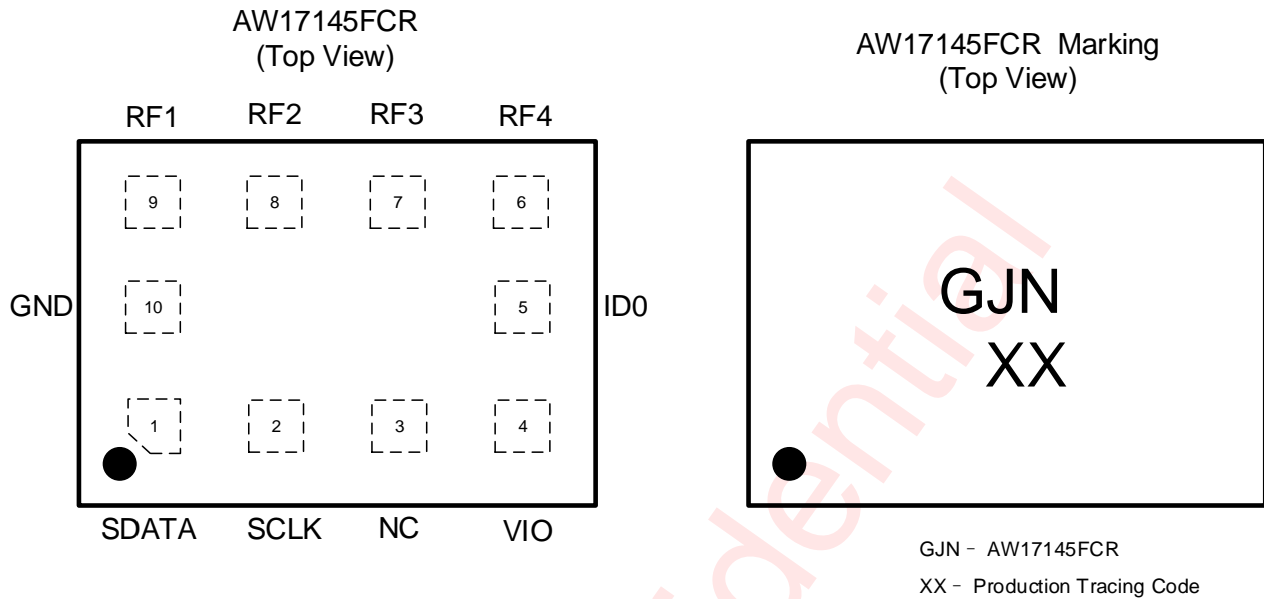


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	SDATA	RFFE SDATA line
2	SCLK	RFFE SCLK line
3	NC	Not connect
4	VIO	VIO supply
5	ID0	ID0 pin
6	RF4	RF4 port
7	RF3	RF3 port
8	RF2	RF2 port
9	RF1	RF1 port
10	GND	Ground

Functional Block Diagram

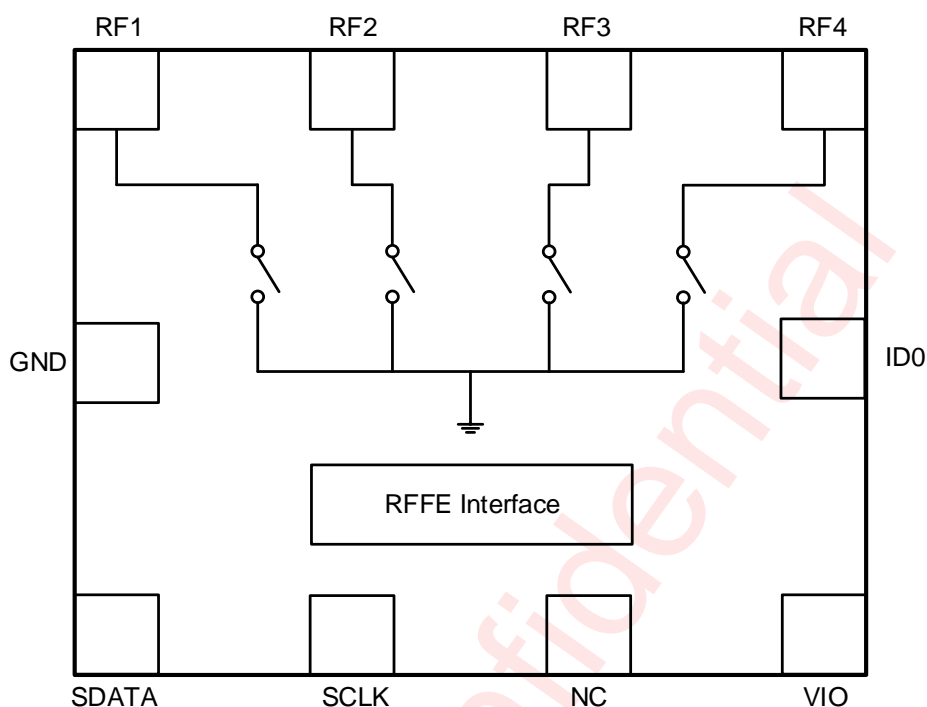


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW17145FCR	-40°C~85°C	FCQFN 1.5mm x 1.1mm x 0.37mm -10L	GJN	MSL1	ROHS+HF	3000 units/Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Interface Supply Voltage Range V_{IO}	-0.3V to 2.8V
Interface Control Voltage Range SDATA, SCLK, ID0	-0.3V to 2.8V
Peak RF Operating Voltage $V_{IO}=1.8V$, $V_{SWR}=1:1$, $Temp=25^{\circ}C$, 25% duty cycle RF power (RF1/2/3/4 to GND)	53V
Operating Free-air Temperature Range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C

ESD	
HBM(Human Body Model) ^(NOTE 2)	±1000V
CDM (Charged Device Model) ^(NOTE 3)	±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Electrical Characteristics

V_{IO}=1.8V, V_{CTL_H}=1.8V, V_{CTL_L}=0V, PIN=0dBm, VSWR=1:1, Temp=25°C. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V _{IO}	Interface Supply Voltage		1.65	1.8	1.95	V
I _{VIO}	V _{IO} Supply Current	Active Mode		45	85	μA
		Low Power Mode		4	20	μA
V _{CTL_H}	ID0,SDATA,SCLK Control Voltage High	Must not exceed V _{IO} voltage	0.8* V _{IO}	V _{IO}	1.95	V
V _{CTL_L}	ID0,SDATA,SCLK Control Voltage Low	Must not exceed V _{IO} voltage	0	0	0.3*V _{IO}	V
T _{ON}	Switching Time -ON	From end of RFFE Sequence to 90% of final RF amplitude		6	10	μs
T _{OFF}	Switching Time -OFF	From end of RFFE Sequence to 10% of final RF amplitude		4	10	μs
RF Specifications						
ISO	Adjacent Port Isolation (One Port On, Another Port Off)	617-960MHz	40	44		dB
		960-2170MHz	28	32		dB
		2170-2700MHz	23	27		dB
		3300-3800MHz	18	21		dB
ISO	Adjacent Port Isolation (All Ports Off)	617-960MHz	30	34		dB
		960-2170MHz	24	28		dB
		2170-2700MHz	22	26		dB
		3300-3800MHz	18	22		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ISO	Non- Adjacent Port Isolation (One Port On, Another Port Off)	617-960MHz	45	52		dB
		960-2170MHz	35	40		dB
		2170-2700MHz	30	34		dB
		3300-3800MHz	24	28		dB
ISO	Non- Adjacent Port Isolation (All Ports Off)	617-960MHz	55	59		dB
		960-2170MHz	51	56		dB
		2170-2700MHz	48	52		dB
		3300-3800MHz	41	46		dB
R _{on}	On Resistance	Switch Path On @ DC		1.1	1.5	Ω
C _{OFF}	Off Capacitance	Switch Path Off @ 900MHz		160	220	fF
2f ₀	Second Harmonics (RFx Port Off Harmonics)	GSM850/900, PIN=+35dBm,CW		-81	-71	dBm
3f ₀	Third Harmonics (RFx Port Off Harmonics)	GSM850/900, PIN=+35dBm,CW		-80	-70	dBm
2f ₀	Second Harmonics (RFx Port Off Harmonics)	GSM1800/1900, PIN=+33dBm,CW		-85	-75	dBm
3f ₀	Third Harmonics (RFx Port Off Harmonics)	GSM1800/1900, PIN=+33dBm,CW		-82	-72	dBm
V _{RF}	RFx Port Off V _{peak} (25% duty cycle RF power)	GSM850/900 Tx Band	45	50		V
		GSM1800/1900 Tx Band	45	50		V

Timing Requirements

- Once V_{IO} is powered down to 0V, wait at least 10 μs to reapply power to V_{IO}.

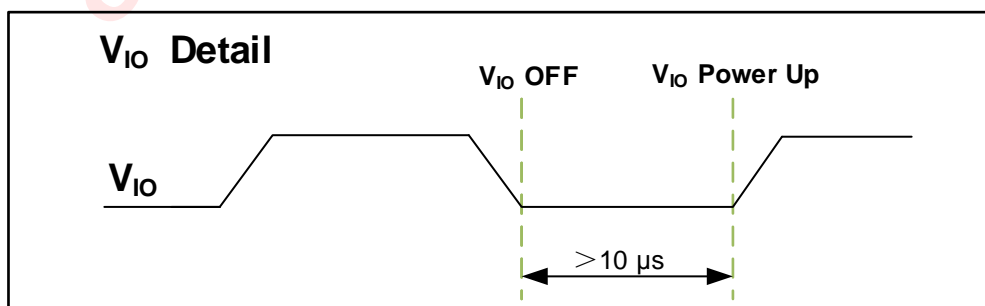


Figure 4 Digital Supply Detail

2. Before applying RF power, V_{IO} must be turned on for at least 20 μs .

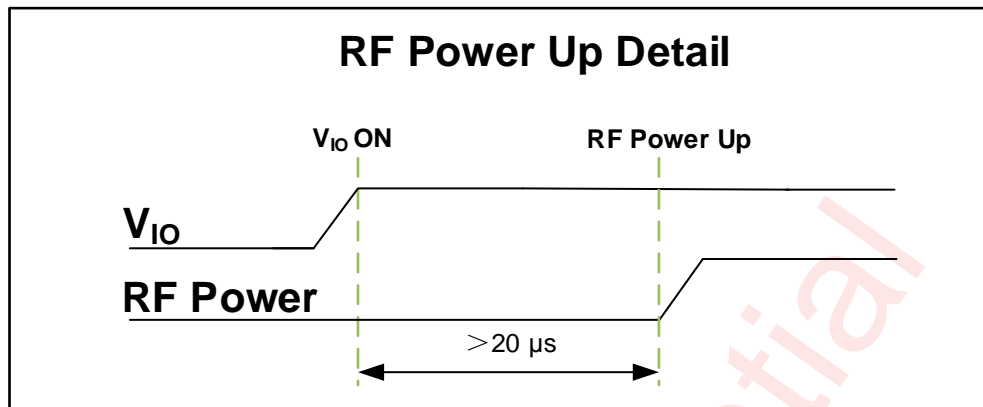


Figure 5 RF Power-Up Detail

3. Before sending SDATA/SCLK, V_{IO} must be applied for at least 800 ns to ensure correct data transmission. And after the RFFE bus is idle, wait at least 20 μs to apply the RF signal.

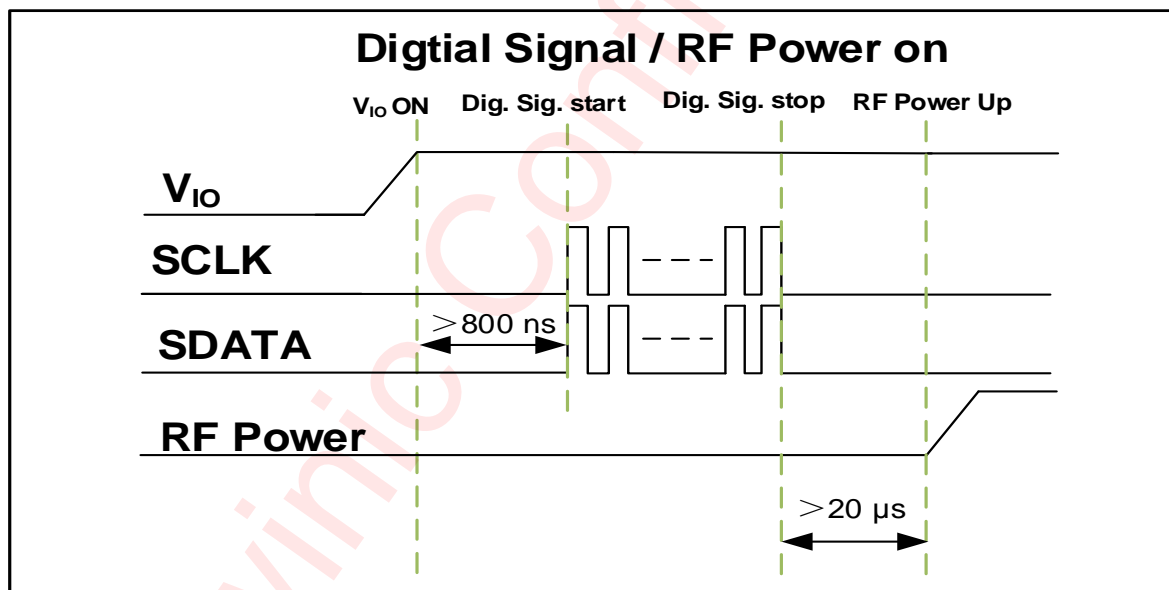


Figure 6 Digital Signal / RF Power-On Detail

4. There shall be no RFFE bus operations during RF Signal active to prevent the device. So RF input signal shall be applied T_{UP} after RFFE bus operations being finished and be removed T_{DOWN} before RFFE bus operations being started.

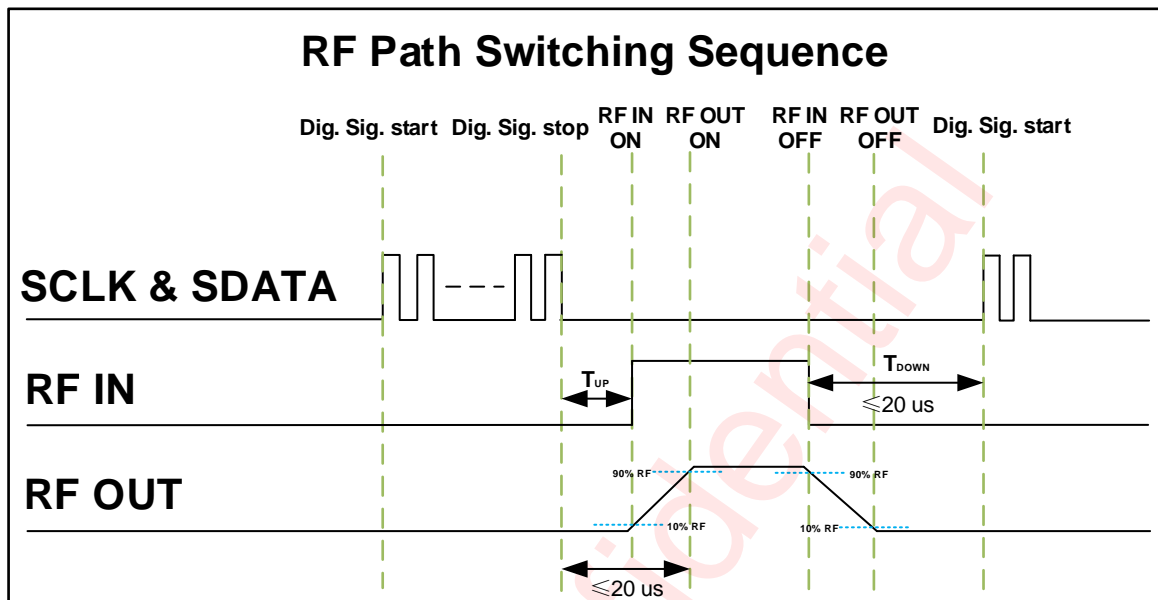


Figure 7 RF Path Switching Sequence

5. If "Lower Power Mode" is used, there must be a 10 μs delay before exiting "Lower Power Mode".

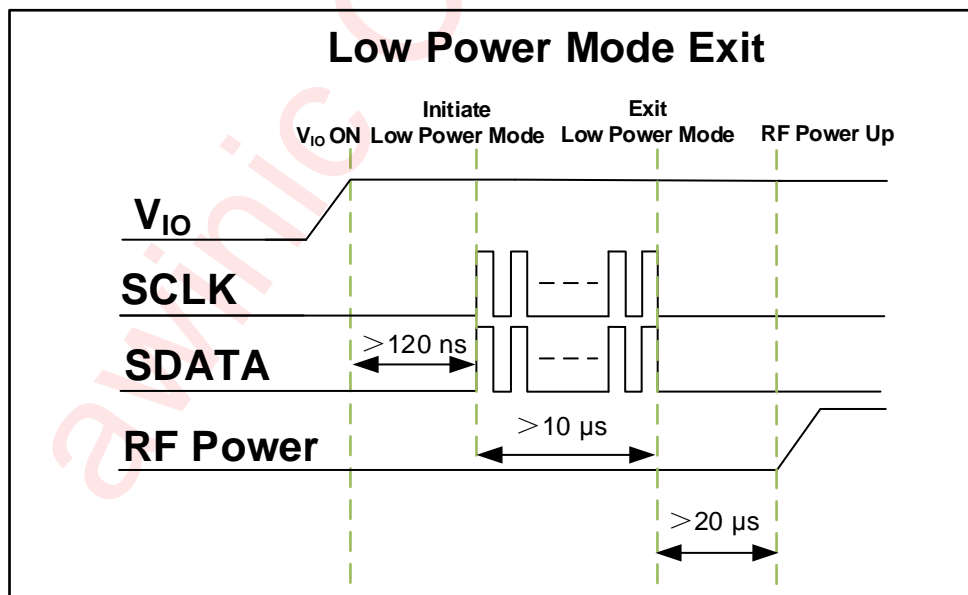


Figure 8 Lower Power Mode Exit Timing

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: ID0 = 0→0x06 ID0 = 1→0x07

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Normal operation	Normal operation mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 write:

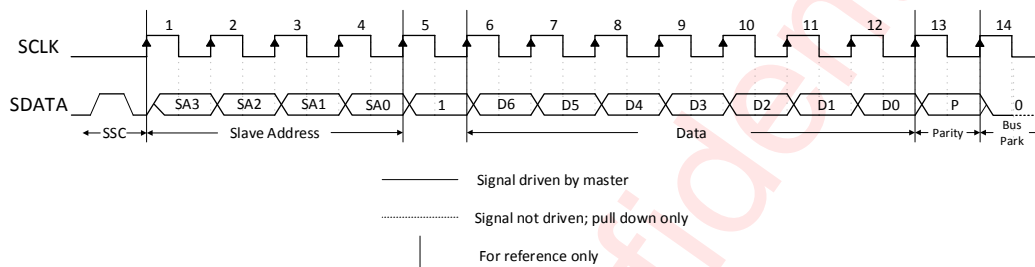


Figure 9 Register 0 Write Command Sequence

Register write:

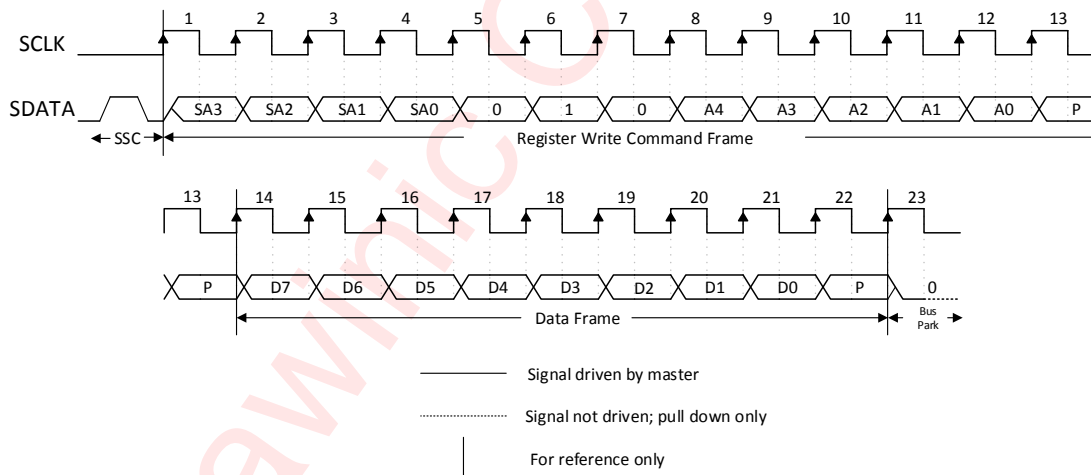


Figure 10 Register Write Command Sequence

Register read:

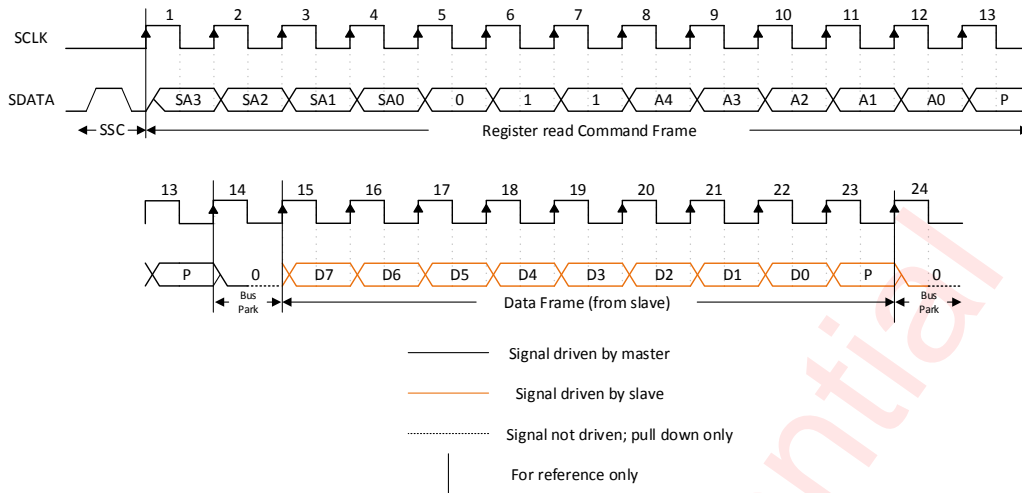


Figure 11 Register Read Command Sequence

Extended Register write:

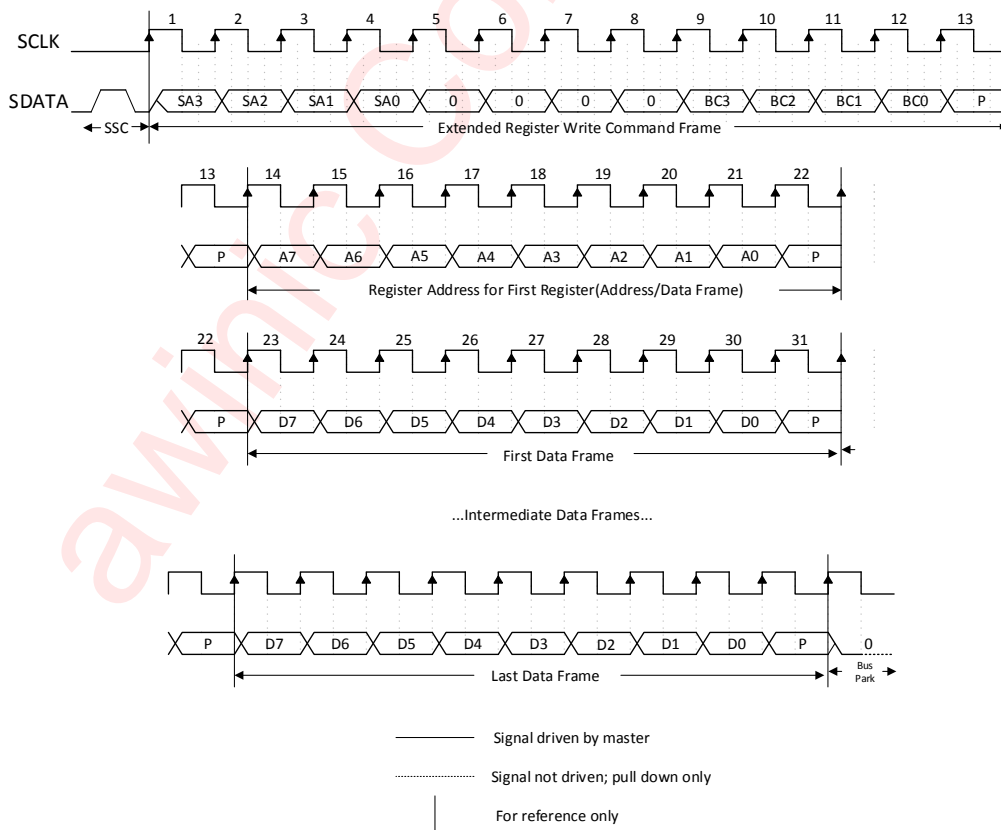


Figure 12 Extended Register write command sequence

Extended Register read:

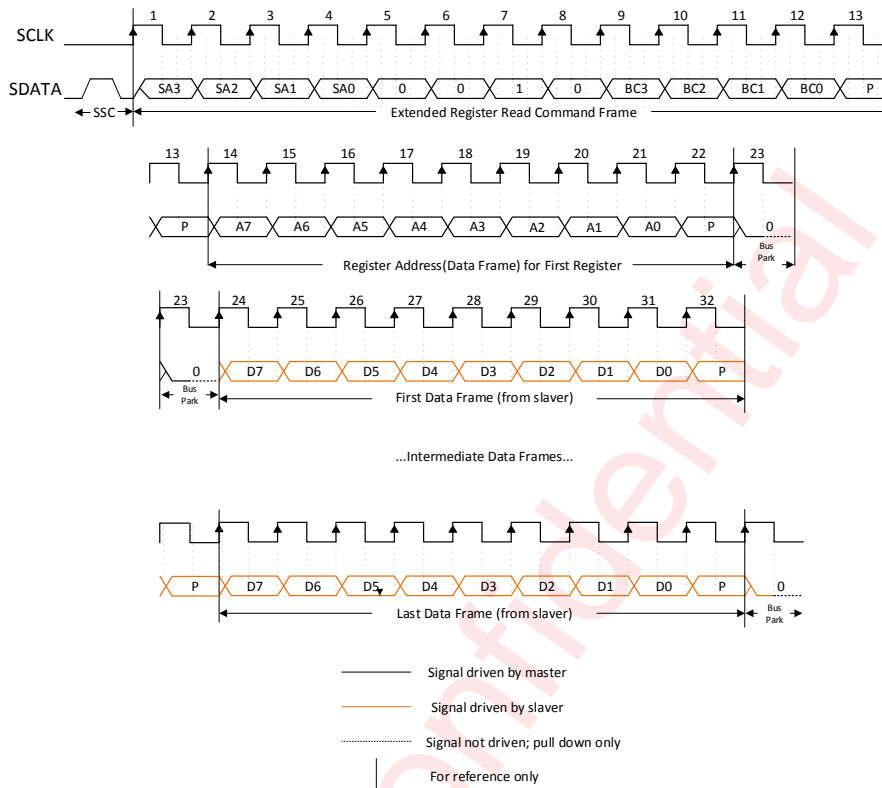


Figure 13 Extended Register read command sequence

Masked write:

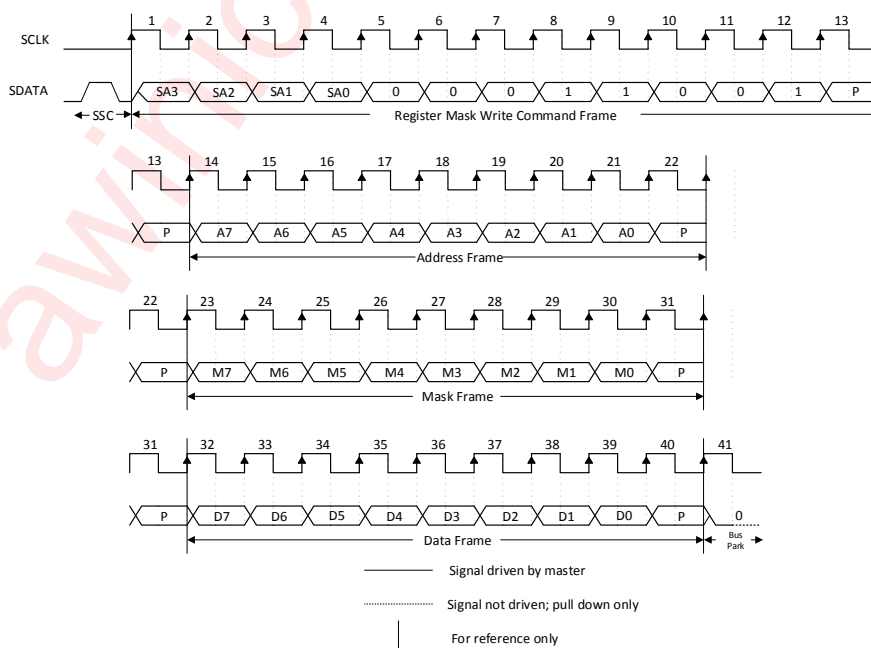


Figure 14 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER_0 : Model control Register(Address 0000h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	SPARE	Reserved for future use	RW	No	0-10	0000
3:0	MODE_CTRL	0000: ALL off 0001: RF1 on 0010: RF2 on 0011: RF1/2 on 0100: RF3 on 0101: RF1 /3 on 0110: RF2/3 on 0111: RF1/2/3 on 1000: RF4 on 1001: RF1/4 on 1010: RF2/4 on 1011: RF1/2/4 on 1100: RF3/4 on 1101: RF1/3/4 on 1110: RF2/3/4 on 1111: RF1/2/3/4 on	RW MW	No	Yes 0-10	0000

RFFE_STATUS : RFFE Status Register(Address 001Ah)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset	W	No	No	0
6	CMD_FR_P_ERR	Command Frame received with a parity error	RW	No	No	0
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	RW	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	RW	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	RW	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	RW	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	RW	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	RW	No	No	0

GSID0_1 : Group ID 0-1 Register(Address 001Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID0	Group Slave ID0	RW	No	No	0000
3:0	GSID1	Group Slave ID1	RW	No	No	0000

PM_TRIG : Pwr_mode and Trig Register(Address 001Ch)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	PWR_MODE[1]	0: normal operation 1: low power	RW MW	Yes	No	0
6	PWR_MODE[0]	0: active 1: start up – Reset all register to default	RW MW	Yes	No	0
5:3	TRIGGER_MASK	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	No	No	000
2:0	TRIGGER	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	Yes	No	000

PRODUCT_ID : Product ID Register(Address 001Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Lower eight bits of Product ID	R	No	No	0x02

MANUFACTURER_ID : Manufacture ID Register(Address 001Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	MFG_ID	Lower eight bits of Manufacturer ID	R	No	No	0x49

MAN_USID : User ID Register(Address 001Fh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	MFG_ID	Upper four bits of Manufacturer ID	R	No	No	0100
3:0	USID	Programmable Unique Slave ID The default value at reset is selected via pin ID0 ID0 = 0: 0x6 ID0 = 1: 0x7	RW	No	No	0110

EXT_PRODUCT_ID : Extend Product ID Register(Address 0020h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Upper eight bits of Product ID	R	No	No	0x00

REVISION_ID : Revision ID Register(Address 0021h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	REV_ID	Revision ID	R	No	No	0x00

GSID2_3 : Group ID 2-3 Register(Address 0022h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID2	Group Slave ID2	R/W	No	No	0000
3:0	GSID3	Group Slave ID3	R/W	No	No	0000

UDR_RST : UDR Reset Register(Address 0023h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal 1: software reset	R/W	Yes	No	0
6:0	RESERVED	Reserved	R/W	No	No	0x00

ERR_SUM : Error Command Status Register(Address 0024h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	SPARE	Reserved for future use	R/W	No	No	0
6	COM_FR_P_ERR	Command Frame received with a parity error	R/W	No	No	0
5	COM_LEN_ERR	Command Sequence received with an incorrect length	R/W	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	R/W	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	R/W	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	R/W	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	R/W	No	No	0

0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	R/W	No	No	0
---	-------------	--	-----	----	----	---

BUS_LD : SDATA Driver Strength Register(Address 002Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:1	reserved	reserved	R/W	No	No	0x00
0	BUS_LD	SDATA drive strength 0: 50pf 1: 80pf	R/W	No	No	0

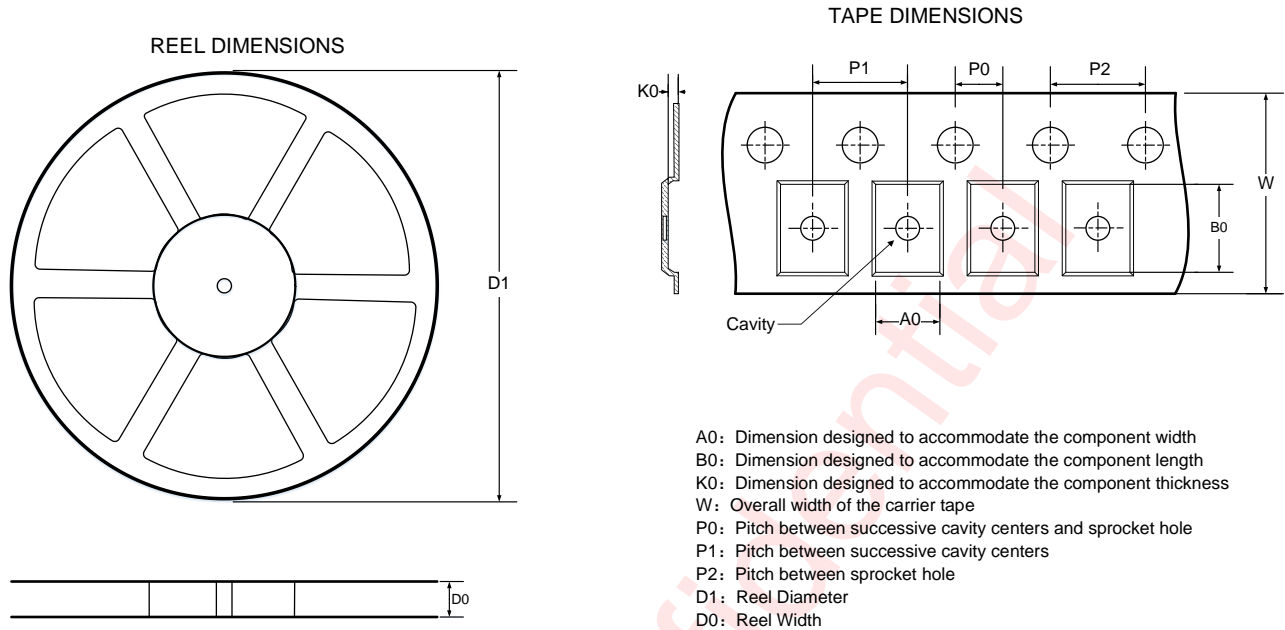
EXT_TRIG_MASK : Extend Trig Mask Register(Address 002Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG_MASK	Setting bit EXT_TRIG_MASK[n] disables EXT_TRIG[n]	RW MW	No	No	0x00

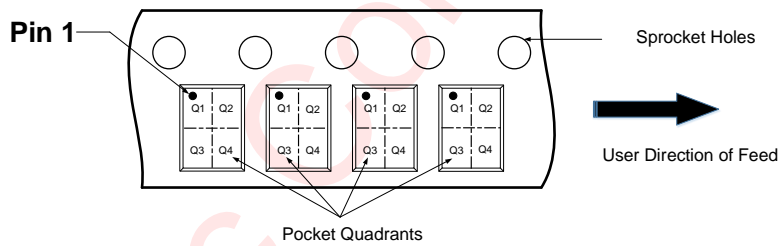
EXT_TRIG : Extend Trig Register(Address 002Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG	Setting bit EXT_TRIG[n] loads EXT_TRIG[n]'s associated register	R/W MW	Yes	No	0x00

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



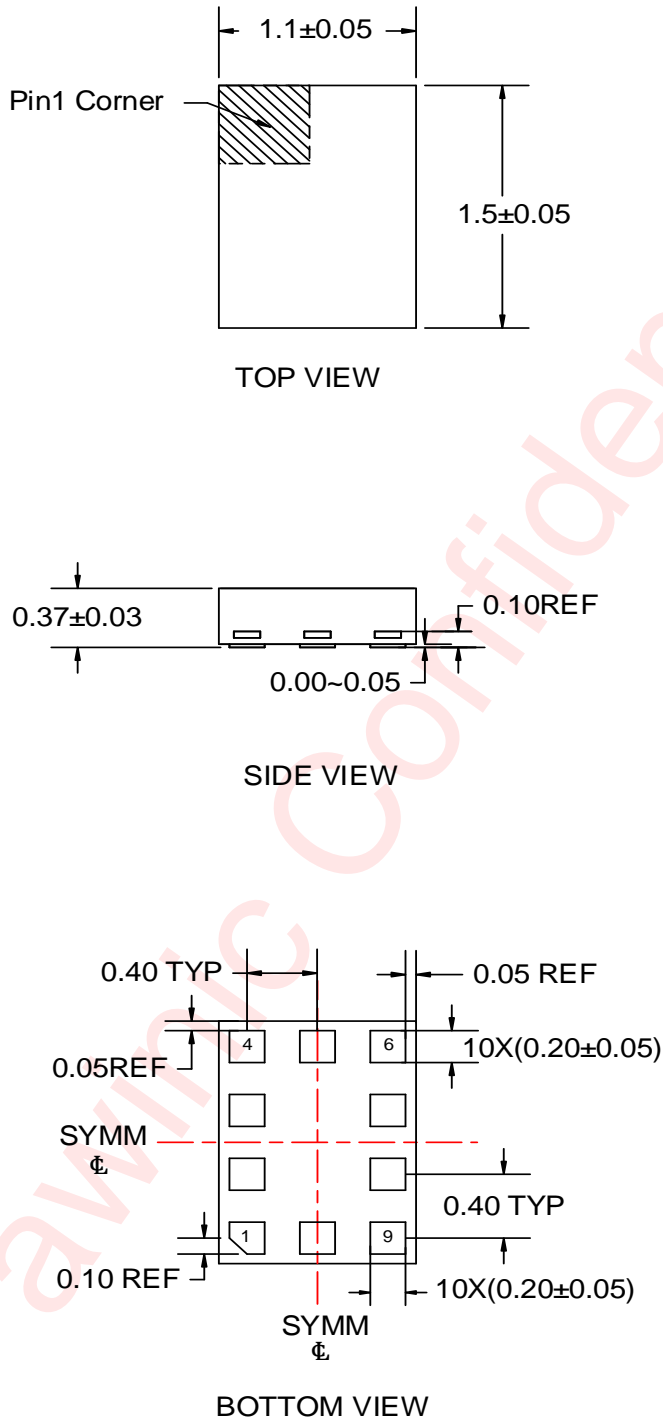
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.27	1.67	0.48	2	4	4	8	Q1

All dimensions are nominal

Figure 15 Tape and Reel

Package Description



Unit: mm

Figure 16 Package Outline

Land Pattern Data

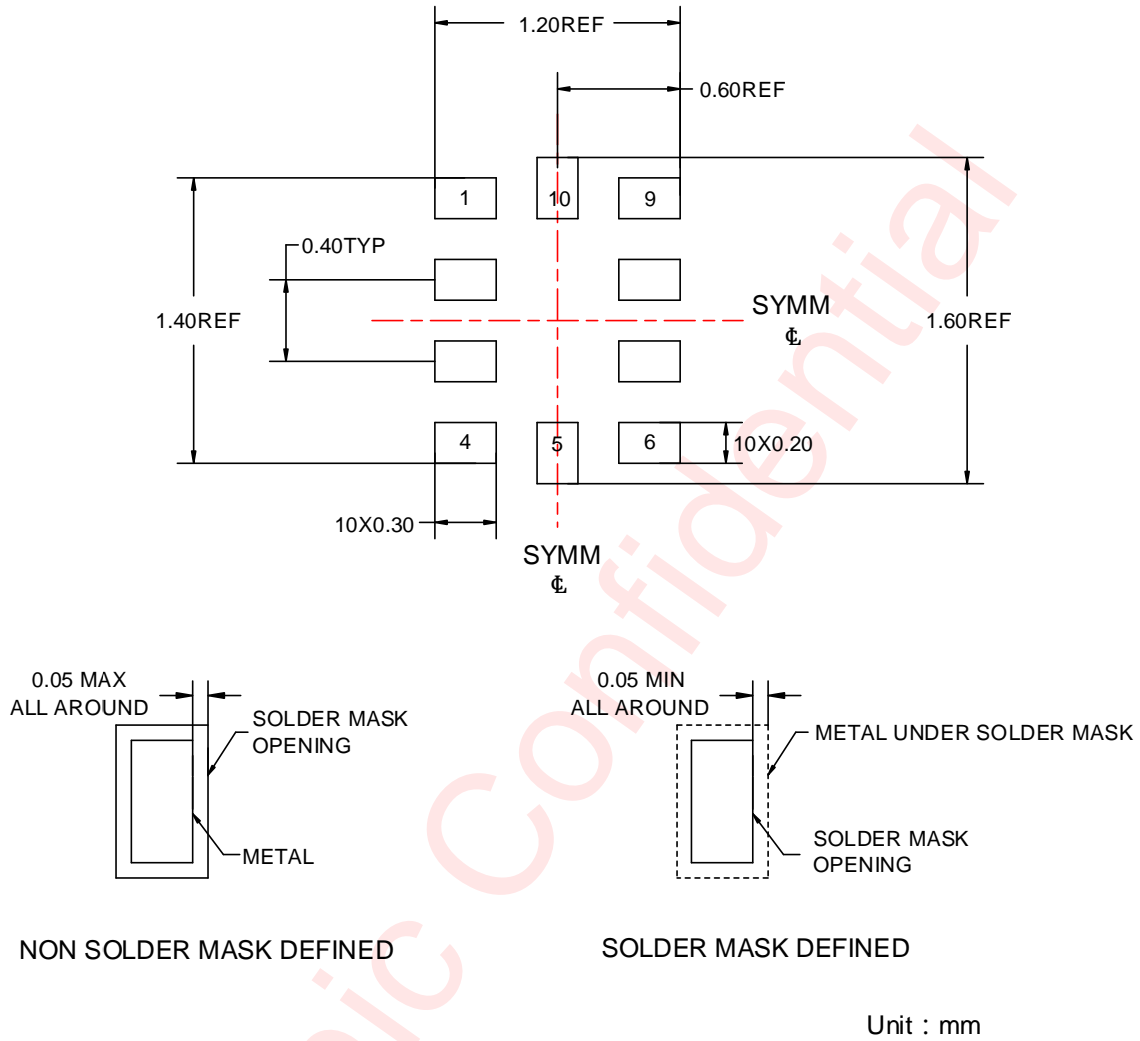


Figure 17 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Nov. 2020	Officially Released

awinic Confidential

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.