EM74HC165; EM74HCT165

8-bit parallel-in/serial out shift register

Draft datasheet, Rev0.1 May 10, 2024

1.General Description

The EM74HC165 and EM74HCT165 are 8-bit serial or parallel-in/serial-out shift register. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input ($\overline{PL}$) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When $\overline{PL}$ is HIGH data enters the register serially at DS. When the clock enable input ($\overline{CE}$) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on $\overline{CE}$ will disable the CP input. Inputs include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide operating voltage 2.0 V to 6.0 V
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For EM74HC165: CMOS level
  - For EM74HCT165: TTL level
- Complies with JEDEC standard:
  - JESD8C(2.7 V to 3.6 V)
  - JESD7A(2.0 V to 6.0 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
EM74HC165D	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	3000
EM74HCT165D			
EM74HC165PW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	3000
EM74HCT165PW			

4.Function Diagram

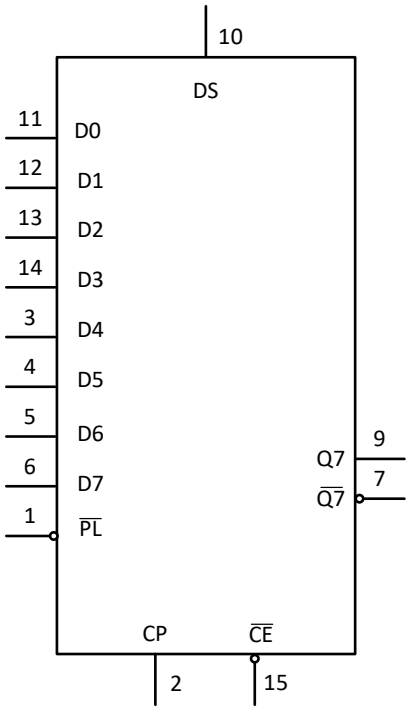


Fig 1.Logic symbol

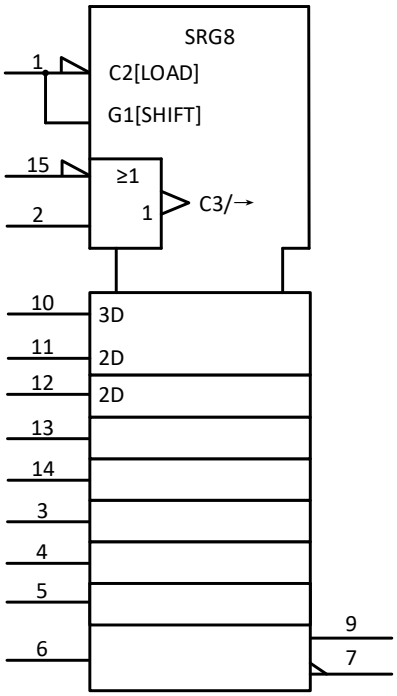


Fig 2.IEC logic symbol

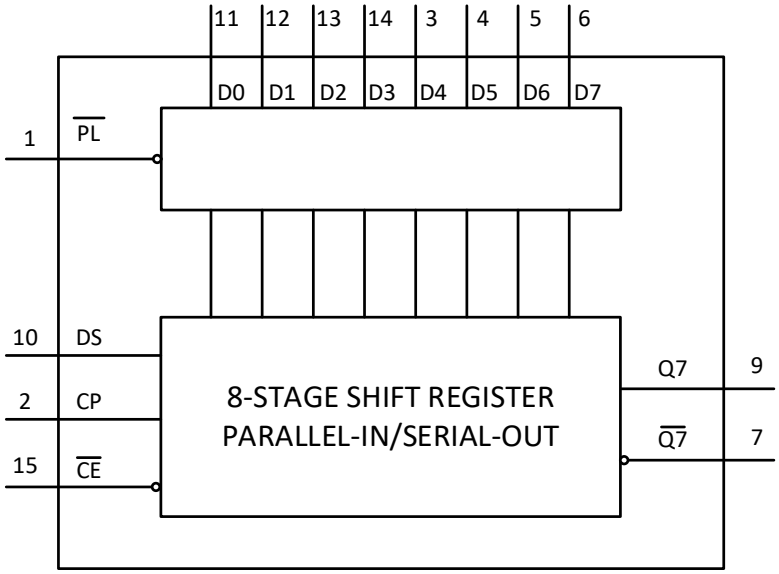


Fig 3.Logic diagram

5.Pinning Information

5.1. Pin map

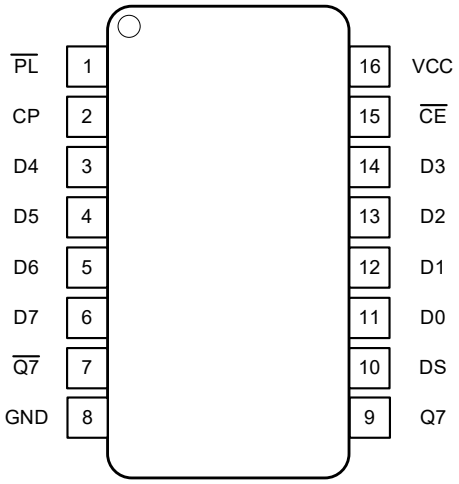


Fig 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{PL}$	1	asynchronous parallel load input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	complementary output from the last stage
GND	8	ground(0V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs (also referred to as Dn)
$\overline{CE}$	15	clock enable input (active LOW)
V_{CC}	16	supply voltage

6.Functional Description

Table 3. Function table

Operating modes	Inputs					Qn registers		Outputs	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	I	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	I	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
Hold"do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

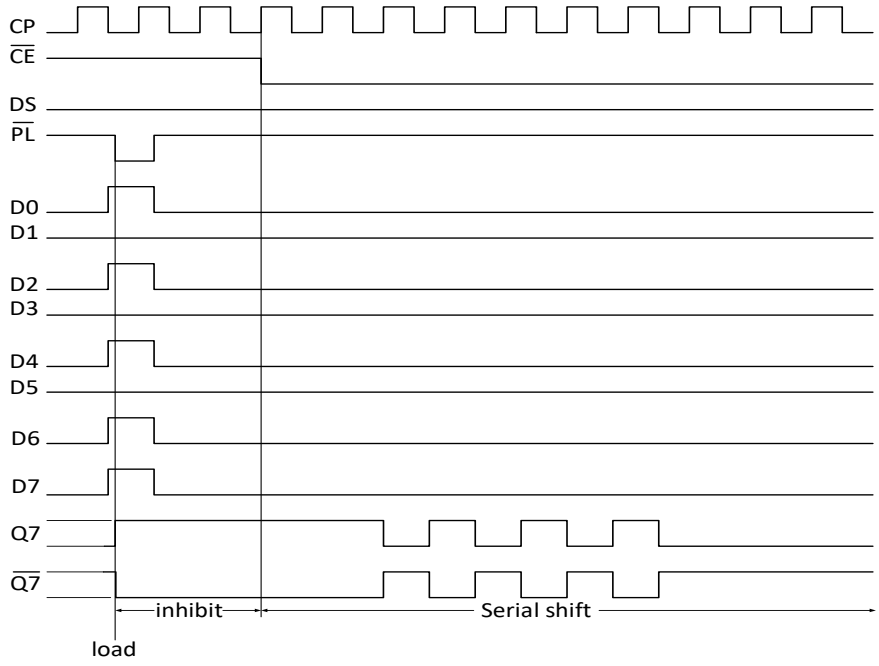


Fig 5. Timing diagram

7.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V [1]		±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]		±20	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	EM74HC165			EM74HCT165			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
EM74HC165								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2		1.5		V
		V_{CC} = 4.5 V	3.15	2.4		3.15		V
		V_{CC} = 6.0 V	4.2	3.2		4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V		0.8	0.5		0.5	V
		V_{CC} = 4.5 V		2.1	1.35		1.35	V
		V_{CC} = 6.0 V		2.8	1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20μA; V_{CC} = 2.0 V	1.9	2.0		1.9		V
		I_O = -20μA; V_{CC} = 4.5 V	4.4	4.5		4.4		V
		I_O = -20μA; V_{CC} = 6.0 V	5.9	6.0		5.9		V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	4.32		3.7		V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	5.81		5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20μA; V_{CC} = 2.0 V		0	0.1		0.1	V
		I_O = 20μA; V_{CC} = 4.5 V		0	0.1		0.1	V
		I_O = 20μA; V_{CC} = 6.0 V		0	0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V		0.15	0.33		0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V		0.16	0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	μA

I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 6.0 V			80		160	μA
C_I	input capacitance			3.5				pF
EM74HCT165								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6		2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V		1.2	0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20μA	4.4	4.5		4.4		V
		I_O = -4.0 mA	3.84	4.32		3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL};						
		I_O = 20μA; V_{CC} = 4.5 V		0	0.1		0.1	V
		I_O = 5.2 mA; V_{CC} = 6 V		0.15	0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6 V			±1		±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 5.5 V			80		160	μA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND;V_{CC} = 4.5 V to 5.5 V						
		Dn and DS inputs		35	157.5		171.5	μA
		CP $\overline{CE}$, and $\overline{PL}$ inputs		65	292.5		318.5	μA
C_I	input capacitance			3.5				pF

[1]All typical values are measured at T_{amb} = 25℃.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

GND = 0 V; tr = tf = 6 ns; CL = 50 pF; Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
EM74HC165								
t_{pd}	propagation delay	CP or $\overline{CE}$ to Q7, $\overline{Q7}$; see Fig. 6 [2]						
		V_{CC} = 2.0 V		52	205		250	ns
		V_{CC} = 4.5 V		19	41		50	ns
		V_{CC} = 5.0 V; C_L = 15 pF		16				ns
		V_{CC} = 6.0 V		14	35		43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Fig.7						
		V_{CC} = 2.0 V		50	205		250	ns
		V_{CC} = 4.5 V		18	41		50	ns
		V_{CC} = 5.0 V; C_L = 15 pF		15				ns
		V_{CC} = 6.0 V		14	35		43	ns
		D7 to Q7, $\overline{Q7}$; see Fig.8						
		V_{CC} = 2.0 V		36	150		180	ns
		V_{CC} = 4.5 V		13	30		36	ns
		V_{CC} = 5.0 V; C_L = 15 pF		11				ns
		V_{CC} = 6.0 V		10	26		31	ns
t_t	transition time	Q7,$\overline{Q7}$ output;see Fig.6 [3]						
		V_{CC} = 2.0 V		19	95		110	ns
		V_{CC} = 4.5 V		7	19		22	ns
		V_{CC} = 6.0 V		6	16		19	ns

t_W	pulse width	CP HIGH or LOW; see Fig. 6						
		V_{CC} = 2.0 V	100	17		120		ns
		V_{CC} = 4.5 V	20	6		24		ns
		V_{CC} = 6.0 V	17	5		20		ns
		$\overline{PL}$ LOW; see Fig.7						
		V_{CC} = 2.0 V	100	14		120		ns
		V_{CC} = 4.5 V	20	5		24		ns
		V_{CC} = 6.0 V	17	4		20		ns
t_{rec}	recovery time	$\overline{PL}$ to CP, $\overline{CE}$; see Fig.7						
		V_{CC} = 2.0 V	125	22		150		ns
		V_{CC} = 4.5 V	25	8		30		ns
		V_{CC} = 6.0 V	21	6		26		ns
t_{SU}	set up time	DS to CP, $\overline{CE}$; see Fig.9						
		V_{CC} = 2.0 V	100	11		120		ns
		V_{CC} = 4.5 V	20	4		24		ns
		V_{CC} = 6.0 V	17	3		20		ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Fig.9						
		V_{CC} = 2.0 V	100	17		120		ns
		V_{CC} = 4.5 V	20	6		24		ns
		V_{CC} = 6.0 V	17	5		20		ns
		Dn to $\overline{PL}$; see Fig.10						
		V_{CC} = 2.0 V	100	22		120		ns
		V_{CC} = 4.5 V	20	8		24		ns
		V_{CC} = 6.0 V	17	6		20		ns
t_h	hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Fig.9						

		V_{CC} = 2.0 V	5	6		5		ns
		V_{CC} = 4.5 V	5	2		5		ns
		V_{CC} = 6.0 V	5	2		5		ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Fig.9						
		V_{CC} = 2.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns
f_{max}	maximum frequency	for CP; see Fig.6						
		V_{CC} = 2.0 V	5	17		4		MHz
		V_{CC} = 4.5 V	24	51		20		MHz
		V_{CC} = 5.0 V; C_L = 15 pF		56				MHz
		V_{CC} = 6.0 V	28	61		24		MHz
C_{PD}	power dissipation capacitance	per package ; V_I = GND to V_{CC} ; [4]		35				pF
EM74HCT165								
t_{pd}	propagation delay	$\overline{CE}$, CP to Q7, $\overline{Q7}$; see Fig. 6 [2]						
		V_{CC} = 4.5 V		17	43		51	ns
		V_{CC} = 5.0 V; C_L = 15 pF		14				ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Fig. 7						
		V_{CC} = 4.5 V		20	50		60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		17				ns
		D7 to Q7, $\overline{Q7}$; see Fig. 8						
		V_{CC} = 4.5 V		14	35		42	ns
		V_{CC} = 5.0 V; C_L = 15 pF		11				ns
t_t	transition time	Q7, $\overline{Q7}$ output; see Fig.6 [3]						
		V_{CC} = 4.5 V		7	19		22	ns

t_W	pulse width	CP input; see Fig. 6						
		V_{CC} = 4.5 V	20	6		24		ns
		$\overline{PL}$ input; see Fig.7						
		V_{CC} = 4.5 V	25	9		30		ns
t_{rec}	recovery time	$\overline{PL}$ to CP, $\overline{CE}$; see Fig.7						
		V_{CC} = 4.5 V	25	8		30		ns
t_{su}	set up time	DS to CP, $\overline{CE}$; see Fig. 9						
		V_{CC} = 4.5 V	25	2		30		ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Fig. 9						
		V_{CC} = 4.5 V	25	7		30		ns
		Dn to $\overline{PL}$; see Fig. 10						
		V_{CC} = 4.5 V	25	10-		30		ns
t_h	hold time	DS to CP, CE and Dn to $\overline{PL}$; see Fig. 9						
		V_{CC} = 4.5 V	9			11		ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Fig. 9						
		V_{CC} = 4.5 V	0			0		ns
f_{max}	maximum frequency	CP input; see Fig.6						
		V_{CC} = 4.5 V	21	44		17		MHz
		V_{CC} = 5.0 V; C_L = 15 pF		48				MHz
C_{PD}	power dissipation capacitance	per package V_I = GND to V_{CC} - 1.5 V; [4]		35				pF

[1] All typical values are measured at VCC = 5.0 V and Tamb = 25℃.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_t is the same as t_{THL} and t_{TLH}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

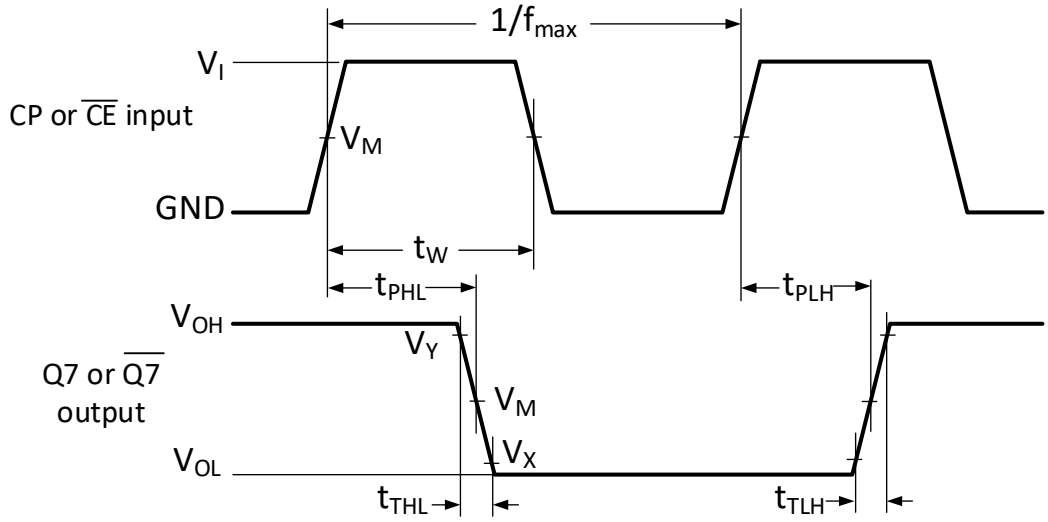
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

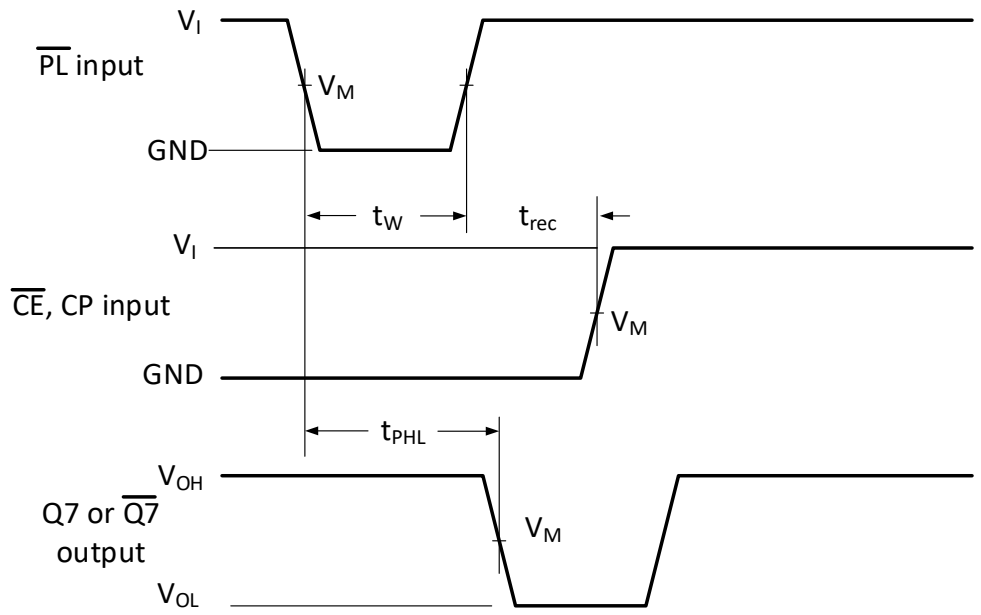
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

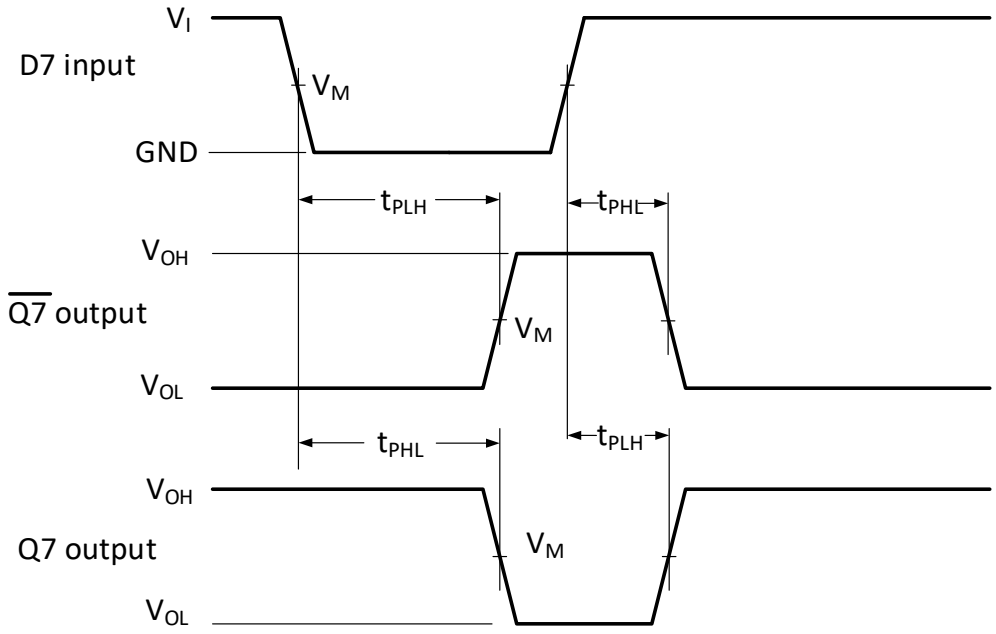
Fig 6. The clock (CP) or clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

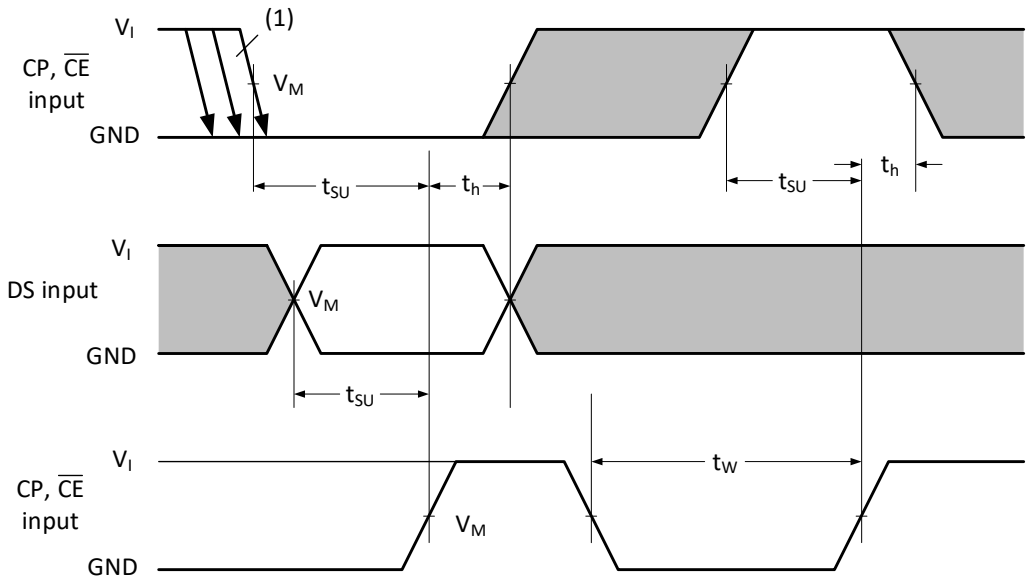
Fig 7. The parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW



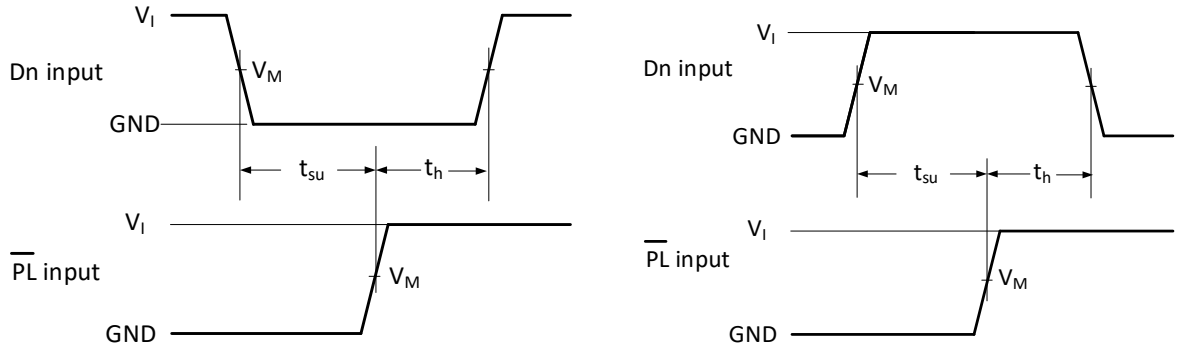
The shaded areas indicate when the input is permitted to change for predictable output performance

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW, see Section 1.

Fig 9. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$)



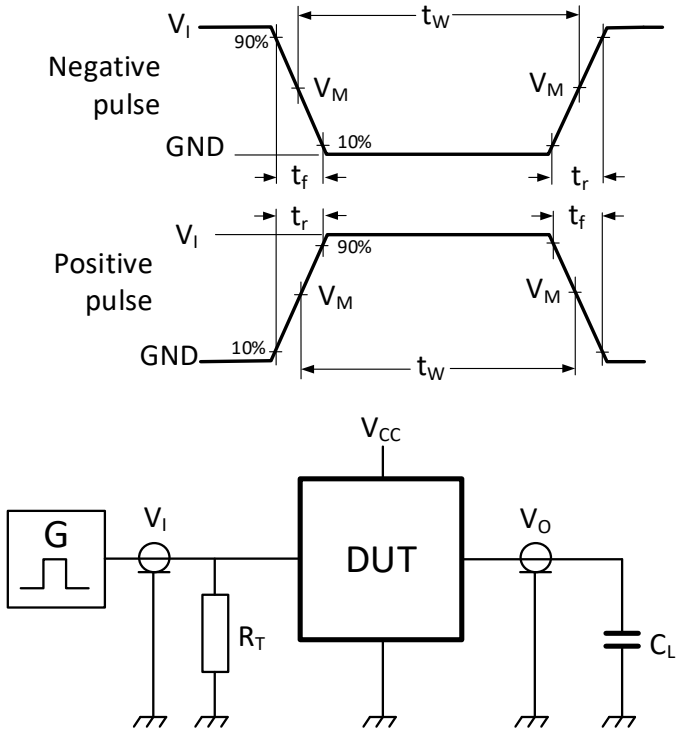
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. The set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
EM74HC165	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
EM74HCT165	1.3V	1.3V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
C_L = Load capacitance including jig and probe capacitance.

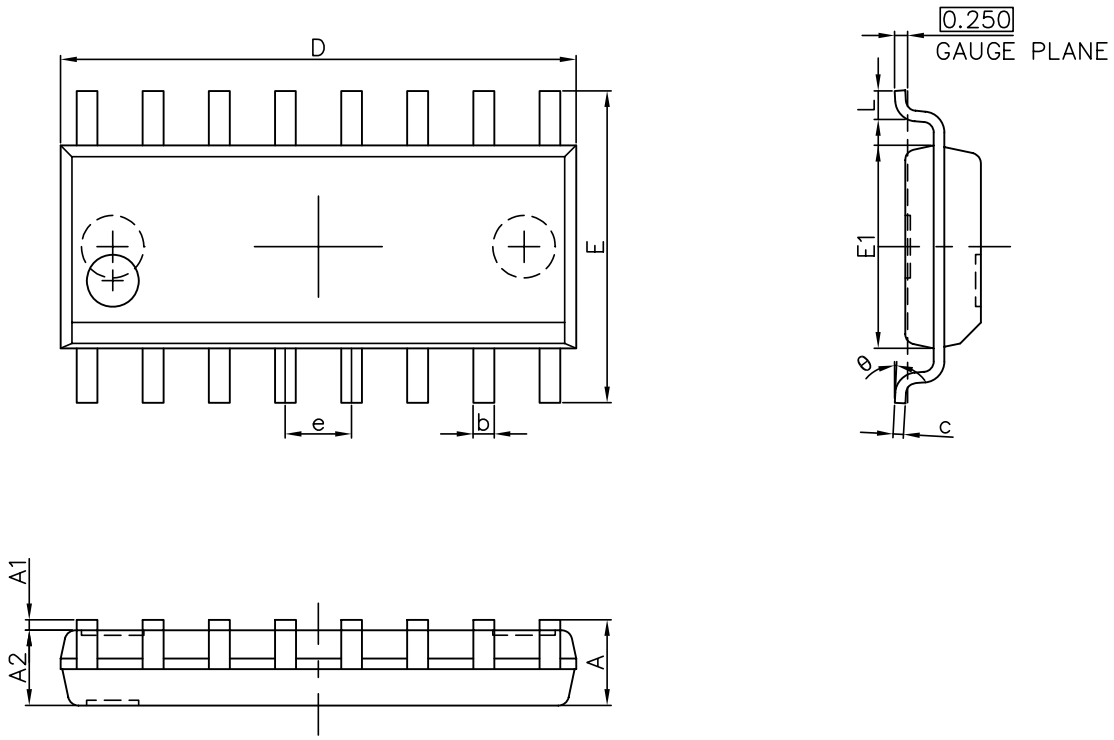
Fig 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	$t_r = t_f$	C_L	
EM74HC165	V_{CC}	6.0 ns	50 pF	t_{PHL}, t_{PLH}
EM74HCT165	3.0V	6.0 ns	50 pF	t_{PHL}, t_{PLH}

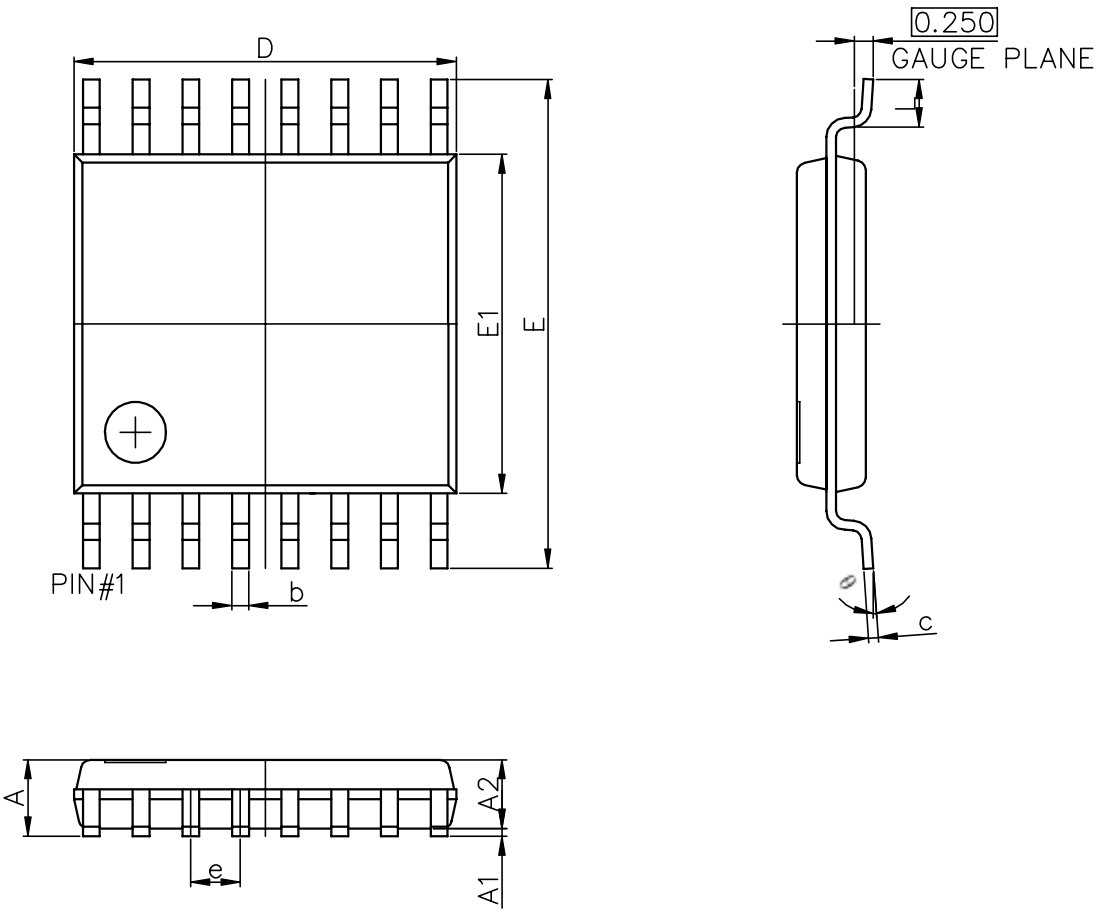
11. Package Outline

SOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.750	——	0.069
A1	0.150	0.250	0.006	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
e	1.270(BSC)		0.050(BSC)	
E	5.900	6.100	0.232	0.240
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-16L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.200	——	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
e	0.650(BSC)		0.026(BSC)	
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74HC165; EM74HCT165 Rev0.1	May 10, 2024	Draft datasheet		