钍地半导体
Tudi Semiconductor

Product Specification

TUDI-CAT9555

O Port with Interrupt

网址 www.sztdbdt.com

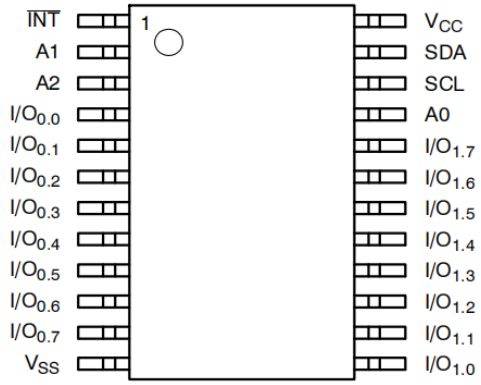
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- 400 kHz I2C Bus Compatible
- 2.3 V to 5.5 V Operation
- Low Stand-by Current
- 5 V Tolerant I/Os
- 16 I/O Pins that Default to Inputs at Power-up
- High Drive Capability
- Individual I/O Configuration
- Polarity Inversion Register
- Active Low Interrupt Output
- Internal Power-on Reset
- No Glitch on Power-up
- Noise Filter on SDA/SCL Inputs
- Cascadable up to 8 Devices
- Industrial Temperature Range
- 24-lead SOIC and TSSOP, and 24-pad TQFN (4 x 4 mm) Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



CAT9555

Applications

- White Goods (dishwashers, washing machines)
- Handheld Devices (cell phones, PDAs, digital cameras)
- Data Communications (routers, hubs and servers)

Description

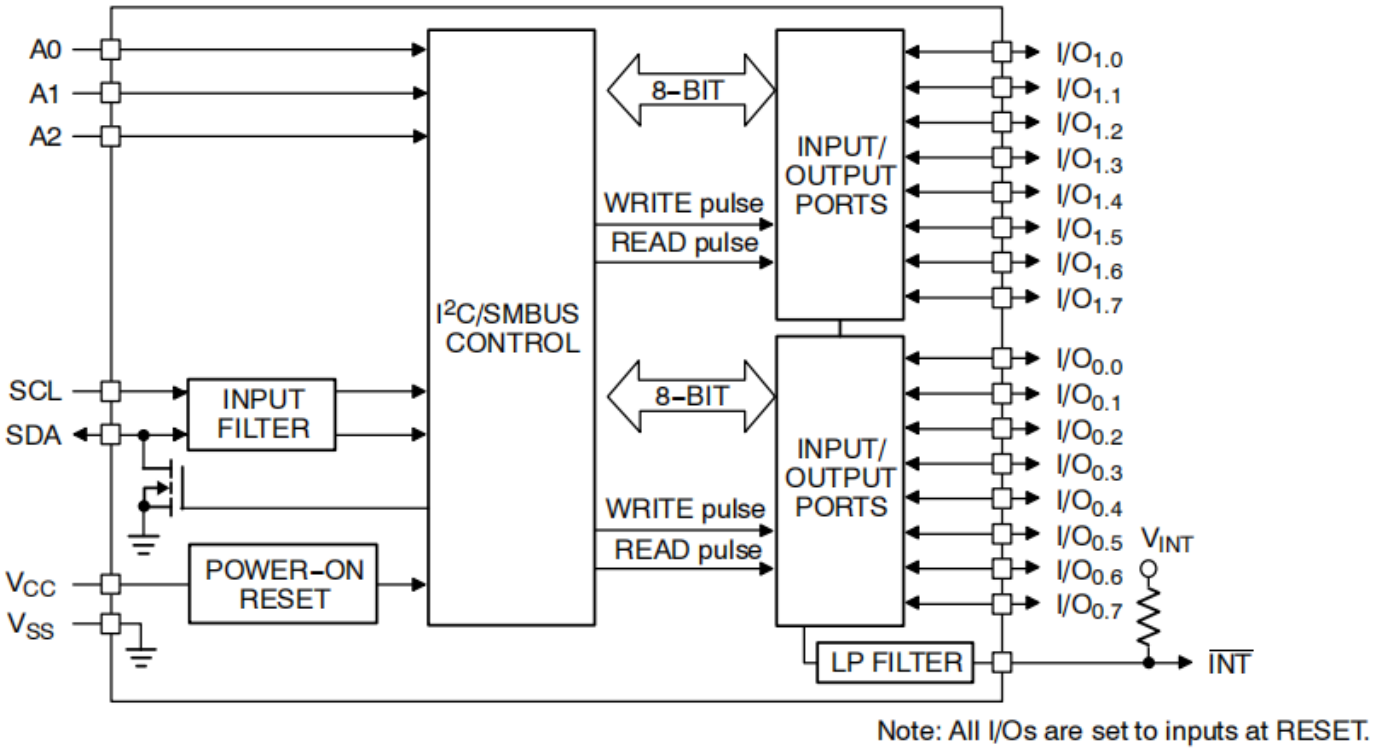
The CAT9555 is a CMOS device that provides 16-bit parallel input/output port expansion for I^2C and SMBus compatible applications. These I/O expanders provide a simple solution in applications where additional I/Os are needed: sensors, power switches, LEDs, pushbuttons, and fans.

The CAT9555 consists of two 8-bit Configuration ports (input or output), Input, Output and Polarity inversion registers, and an I^2C/SMBus/compatible serial interface.

Any of the sixteen I/Os can be configured as an input or output by writing to the configuration register.

The system master can invert the CAT9555 input data by writing to the active-high polarity inversion register. The CAT9555 features an active low interrupt output which indicates to the system master that an input state has changed.

The three address input pins provide the device ' s extended addressing capability and allow up to eight devices to share the same bus. The fixed part of the I^2C slave address is the same as the CAT9554, allowing up to eight of these devices in any combination to be connected on the same bus.



Note: All I/Os are set to inputs at RESET.

Figure 2. Block Diagram

Table 1. PIN DESCRIPTION

SOIC / TSSOP	TQFN	Pin Name	Function
1	22	$\overline{INT}$	Interrupt Output (open drain)
2	23	A1	Address Input 1
3	24	A2	Address Input 2
4–11	1–8	$I/O_{0.0}$ – $I/O_{0.7}$	I/O Port 0.0 to I/O Port 0.7
12	9	V_{SS}	Ground
13–20	10–17	$I/O_{1.0}$ – $I/O_{1.7}$	I/O Port 1.0 to I/O Port 1.7
21	18	A0	Address Input 0
22	19	SCL	Serial Clock
23	20	SDA	Serial Data
24	21	V_{CC}	Power Supply

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	–0.5 to +6.5	V
Voltage on Any Pin with Respect to Ground	–0.5 to +5.5	V
DC Current on $I/O_{1.0}$ to $I/O_{1.7}$, $I/O_{0.0}$ to $I/O_{0.7}$	±50	mA
DC Input Current	±20	mA
V_{CC} Supply Current	160	mA
V_{SS} Supply Current	200	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	–65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
V_{ZAP} (Note 1)	ESD Susceptibility	JEDEC Standard JESD 22	2000	V
I_{LTH} (Note 1)	Latch–up	JEDEC JESD78A	100	mA

1. This parameter is tested initially and after a design or process change that affects the parameter.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply voltage		2.3	–	5.5	V
I_{CC}	Supply current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	–	135	200	μA
I_{stbl}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs	–	1.1	1.5	mA
I_{stbh}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{CC}; f_{SCL} = 0 kHz; I/O = inputs	–	0.75	1	μA
V_{POR}	Power−on reset voltage	No load; V_I = V_{CC} or V_{SS}	–	1.5	1.65	V
SCL, SDA, $\overline{INT}$						
V_{IL} (Note 2)	Low level input voltage		−0.5	–	0.3 x V_{CC}	V
V_{IH} (Note 2)	High level input voltage		0.7 x V_{CC}	–	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	Leakage current	V_I = V_{CC} = V_{SS}	−1	–	+1	μA
C_I (Note 3)	Input capacitance	V_I = V_{SS}	–	–	6	pF
C_O (Note 3)	Output capacitance	V_O = V_{SS}	–	–	8	pF
A0, A1, A2						
V_{IL} (Note 2)	Low level input voltage		−0.5	–	0.3 x V_{CC}	V
V_{IH} (Note 2)	High level input voltage		0.7 x V_{CC}	–	5.5	V
I_{LI}	Input leakage current		−1	–	1	μA
I/Os						
V_{IL}	Low level input voltage		−0.5	–	0.3 x V_{CC}	V
V_{IH}	High level input voltage		0.7 x V_{CC}	–	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.5 V; V_{CC} = 2.3 V to 5.5 V (Note 4)	8	8 to 20	–	mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V to 5.5 V (Note 4)	10	10 to 24	–	
V_{OH}	High level output voltage	I_{OH} = −8 mA; V_{CC} = 2.3 V (Note 5)	1.8	–	–	V
		I_{OH} = −10 mA; V_{CC} = 2.3 V (Note 5)	1.7	–	–	
		I_{OH} = −8 mA; V_{CC} = 3.0 V (Note 5)	2.6	–	–	
		I_{OH} = −10 mA; V_{CC} = 3.0 V (Note 5)	2.5	–	–	
		I_{OH} = −8 mA; V_{CC} = 4.75 V (Note 5)	4.1	–	–	
		I_{OH} = −10 mA; V_{CC} = 4.75 V (Note 5)	4.0	–	–	
I_{IH}	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC}	–	–	1	μA
I_{IL}	Input leakage current	V_{CC} = 5.5 V; V_I = V_{SS}	–	–	−100	μA
C_I (Note 3)	Input capacitance		–	–	5	pF
C_O (Note 3)	Output capacitance		–	–	8	pF

2. V_{IL} min and V_{IH} max are reference values only and are not tested.
3. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
4. Each I/Os must be externally limited to a maximum of 25 mA and each octal ($I/O_{0.0}$ to $I/O_{0.7}$ and $I/O_{1.0}$ to $I/O_{1.7}$) must be limited to a maximum current of 100 mA for a device total of 200 mA.
5. The total current sourced by all I/Os must be limited to 160 mA.

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified) (Note 6)

Symbol	Parameter	Standard I²C		Fast I²C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 7)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 7)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
PORT TIMING						
t_{PV}	Output Data Valid				200	ns
t_{PS}	Input Data Setup Time			100		ns
t_{PH}	Input Data Hold Time			1		μs
INTERRUPT TIMING						
t_{IV}	Interrupt Valid				4	μs
t_{IR}	Interrupt Reset				4	μs

6. Test conditions according to “AC Test Conditions” table.
7. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

Table 6. A.C. TEST CONDITIONS

Input Rise and Fall time	≤ 10 ns
CMOS Input Voltages	0.2 V_{CC} to 0.8 V_{CC}
CMOS Input Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}
Output Reference Voltages	0.5 V_{CC}
Output Load: SDA, $\overline{INT}$	Current Source: I_{OL} = 3 mA; C_L = 100 pF
Output Load: I/Os	Current Source: I_{OL}/I_{OH} = 10 mA; C_L = 50 pF

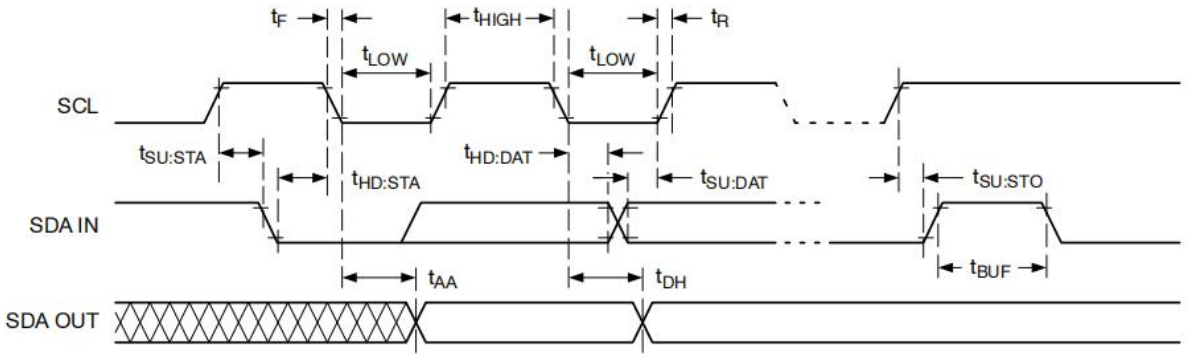


Figure 3. I²C Serial Interface Timing

$\overline{\text{INT}}$: Interrupt Output

The open−drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Since there are two 8−bit ports that are read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1, or vice versa.

Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

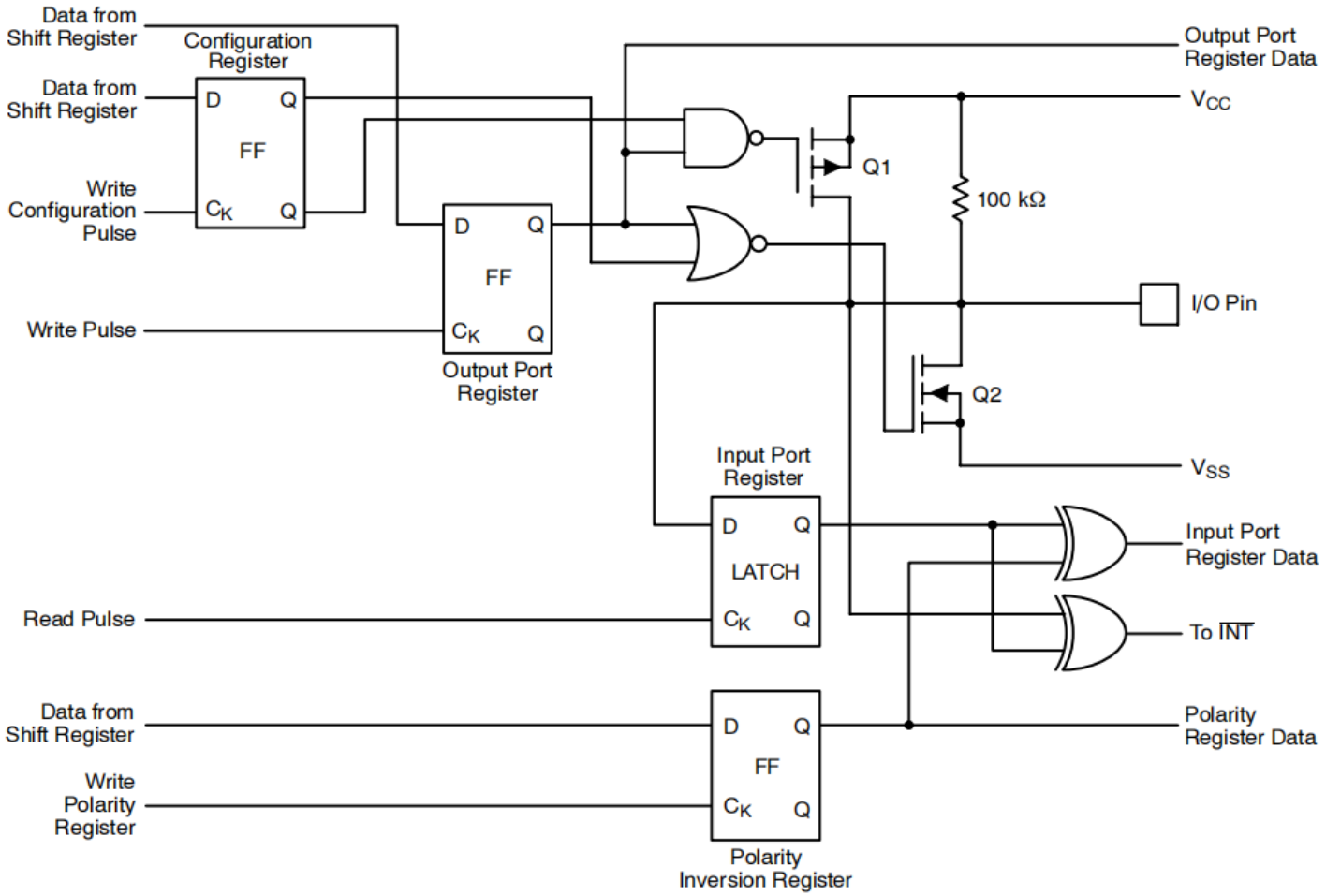


Figure 6. Simplified Schematic of I/Os

FUNCTIONAL DESCRIPTION

The CAT9555 general purpose input/output (GPIO) peripheral provides up to sixteen I/O ports, controlled through an I^2C compatible serial interface.

The CAT9555 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9555 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 7).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9555 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9555 for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 (Figure 8). The CAT9555 uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7−bit slave address is the R/$\overline{W}$ bit that specifies whether a read or write operation is to be performed. When this bit is set to "1", a read operation is initiated, and when set to "0", a write operation is selected.

Following the START condition and the slave address byte, the CAT9555 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9555 then performs a read or a write operation depending on the state of the R/$\overline{W}$ bit.

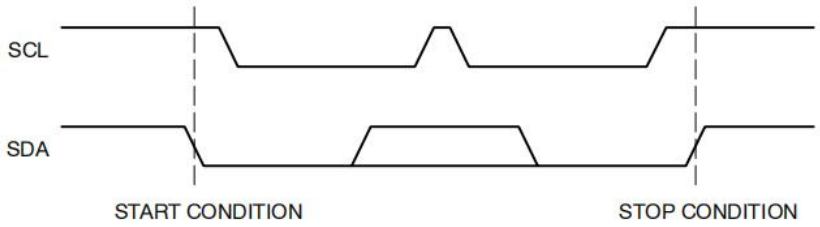


Figure 7. START/STOP Condition

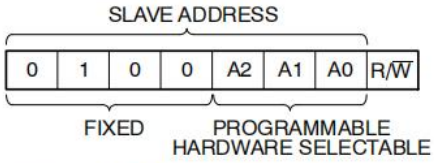


Figure 8. CAT9555 Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 9).

The CAT9555 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each data byte.

When the CAT9555 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9555 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT9555 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

The CAT9555 internal registers and their address and function are shown in Table 7.

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 7. REGISTER COMMAND BYTE

Command (hex)	Register
0h	Input Port 0
1h	Input Port 1
2h	Output Port 0
3h	Output Port 1
4h	Polarity Inversion Port 0
5h	Polarity Inversion Port 1
6h	Configuration Port 0
7h	Configuration Port 1

Table 8. REGISTERS 0 AND 1 – INPUT PORT REGISTERS

bit	$I_{0.7}$	$I_{0.6}$	$I_{0.5}$	$I_{0.4}$	$I_{0.3}$	$I_{0.2}$	$I_{0.1}$	$I_{0.0}$
default	X	X	X	X	X	X	X	X
bit	$I_{1.7}$	$I_{1.6}$	$I_{1.5}$	$I_{1.4}$	$I_{1.3}$	$I_{1.2}$	$I_{1.1}$	$I_{1.0}$
default	X	X	X	X	X	X	X	X

Table 9. REGISTERS 2 AND 3 – OUTPUT PORT REGISTERS

bit	$O_{0.7}$	$O_{0.6}$	$O_{0.5}$	$O_{0.4}$	$O_{0.3}$	$O_{0.2}$	$O_{0.1}$	$O_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$O_{1.7}$	$O_{1.6}$	$O_{1.5}$	$O_{1.4}$	$O_{1.3}$	$O_{1.2}$	$O_{1.1}$	$O_{1.0}$
default	1	1	1	1	1	1	1	1

Table 10. REGISTERS 4 AND 5 – POLARITY INVERSION REGISTERS

bit	$N_{0.7}$	$N_{0.6}$	$N_{0.5}$	$N_{0.4}$	$N_{0.3}$	$N_{0.2}$	$N_{0.1}$	$N_{0.0}$
default	0	0	0	0	0	0	0	0
bit	$N_{1.7}$	$N_{1.6}$	$N_{1.5}$	$N_{1.4}$	$N_{1.3}$	$N_{1.2}$	$N_{1.1}$	$N_{1.0}$
default	0	0	0	0	0	0	0	0

Table 11. REGISTERS 6 AND 7 – CONFIGURATION REGISTERS

bit	$C_{0.7}$	$C_{0.6}$	$C_{0.5}$	$C_{0.4}$	$C_{0.3}$	$C_{0.2}$	$C_{0.1}$	$C_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$C_{1.7}$	$C_{1.6}$	$C_{1.5}$	$C_{1.4}$	$C_{1.3}$	$C_{1.2}$	$C_{1.1}$	$C_{1.0}$
default	1	1	1	1	1	1	1	1

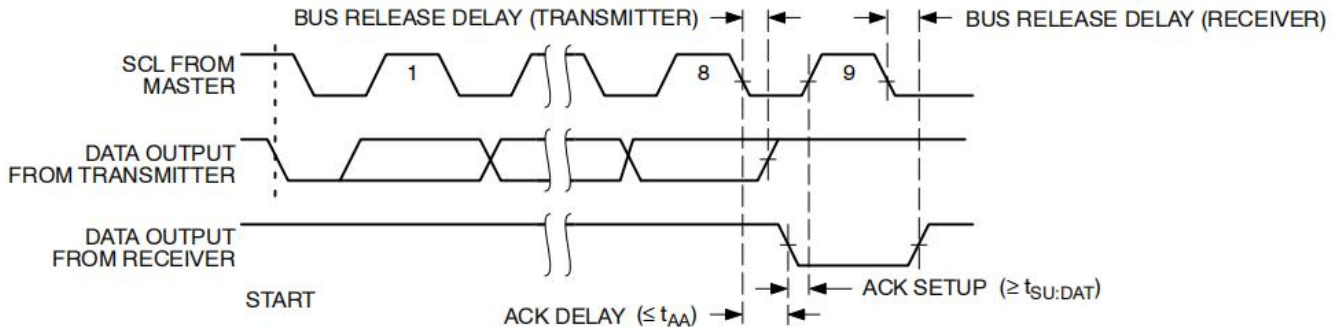


Figure 9. Acknowledge Timing

Registers and Bus Transactions

The CAT9555 internal registers and their address and function are shown in Table 7.

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0h	Input Port 0
1h	Input Port 1
2h	Output Port 0
3h	Output Port 1
4h	Polarity Inversion Port 0
5h	Polarity Inversion Port 1
6h	Configuration Port 0
7h	Configuration Port 1

Table 8. REGISTERS 0 AND 1 – INPUT PORT REGISTERS

bit	$I_{0.7}$	$I_{0.6}$	$I_{0.5}$	$I_{0.4}$	$I_{0.3}$	$I_{0.2}$	$I_{0.1}$	$I_{0.0}$
default	X	X	X	X	X	X	X	X
bit	$I_{1.7}$	$I_{1.6}$	$I_{1.5}$	$I_{1.4}$	$I_{1.3}$	$I_{1.2}$	$I_{1.1}$	$I_{1.0}$
default	X	X	X	X	X	X	X	X

Table 9. REGISTERS 2 AND 3 – OUTPUT PORT REGISTERS

bit	$O_{0.7}$	$O_{0.6}$	$O_{0.5}$	$O_{0.4}$	$O_{0.3}$	$O_{0.2}$	$O_{0.1}$	$O_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$O_{1.7}$	$O_{1.6}$	$O_{1.5}$	$O_{1.4}$	$O_{1.3}$	$O_{1.2}$	$O_{1.1}$	$O_{1.0}$
default	1	1	1	1	1	1	1	1

Table 10. REGISTERS 4 AND 5 – POLARITY INVERSION REGISTERS

bit	$N_{0.7}$	$N_{0.6}$	$N_{0.5}$	$N_{0.4}$	$N_{0.3}$	$N_{0.2}$	$N_{0.1}$	$N_{0.0}$
default	0	0	0	0	0	0	0	0
bit	$N_{1.7}$	$N_{1.6}$	$N_{1.5}$	$N_{1.4}$	$N_{1.3}$	$N_{1.2}$	$N_{1.1}$	$N_{1.0}$
default	0	0	0	0	0	0	0	0

Table 11. REGISTERS 6 AND 7 – CONFIGURATION REGISTERS

bit	$C_{0.7}$	$C_{0.6}$	$C_{0.5}$	$C_{0.4}$	$C_{0.3}$	$C_{0.2}$	$C_{0.1}$	$C_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$C_{1.7}$	$C_{1.6}$	$C_{1.5}$	$C_{1.4}$	$C_{1.3}$	$C_{1.2}$	$C_{1.1}$	$C_{1.0}$
default	1	1	1	1	1	1	1	1

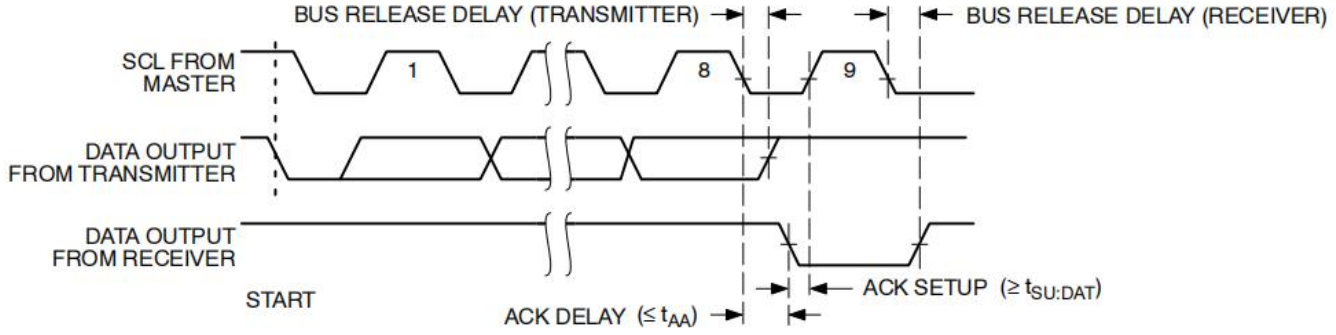


Figure 9. Acknowledge Timing

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip-flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set ("1") the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared ("0"), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power-up, the I/Os are configured as inputs with a weak pull-up resistor to V_{CC}.

Writing to the Port Registers

Data is transmitted to the CAT9555 registers using the write mode shown in Figure 10 and Figure 11.

The CAT9555 registers are configured to operate at four register pairs: Input Ports, Output Ports, Polarity Inversion Ports and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte of data is sent to the Configuration Port 1 (register 7), the next byte will be stored in the Configuration Port 0 (register 6). Each 8-bit register may be updated independently of the other registers.

Reading the Port Registers

The CAT9555 registers are read according to the timing diagrams shown in Figure 12 and Figure 13. Data from the register, defined by the command byte, will be sent serially on the SDA line. Data is clocked into the register on the failing edge of the acknowledge clock pulse. After the first byte is read, additional data bytes may be read, but the second read will reflect the data from the other register in the pair. For example, if the first read is data from Input Port 0, the next read data will be from Input Port 1. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

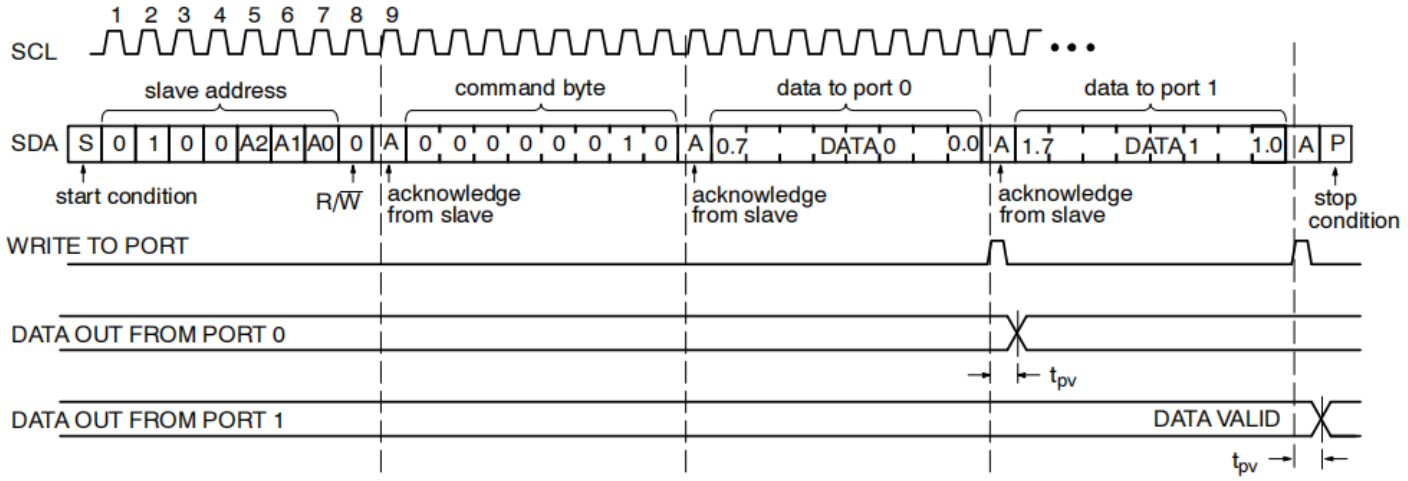


Figure 10. Write to Output Port Register

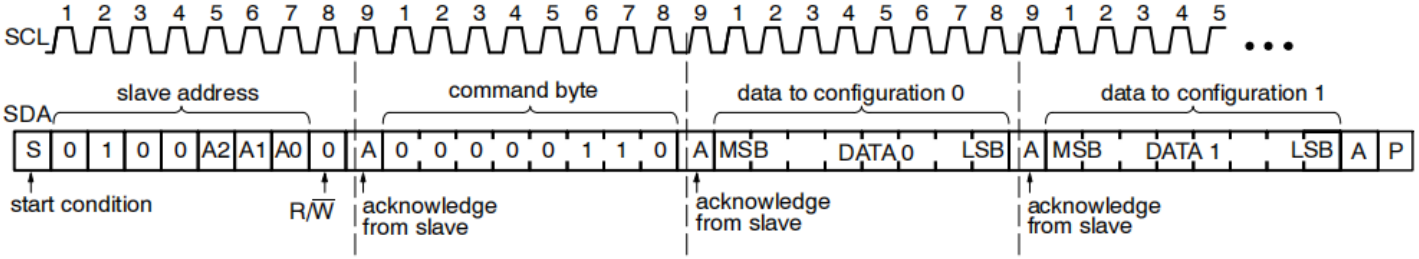
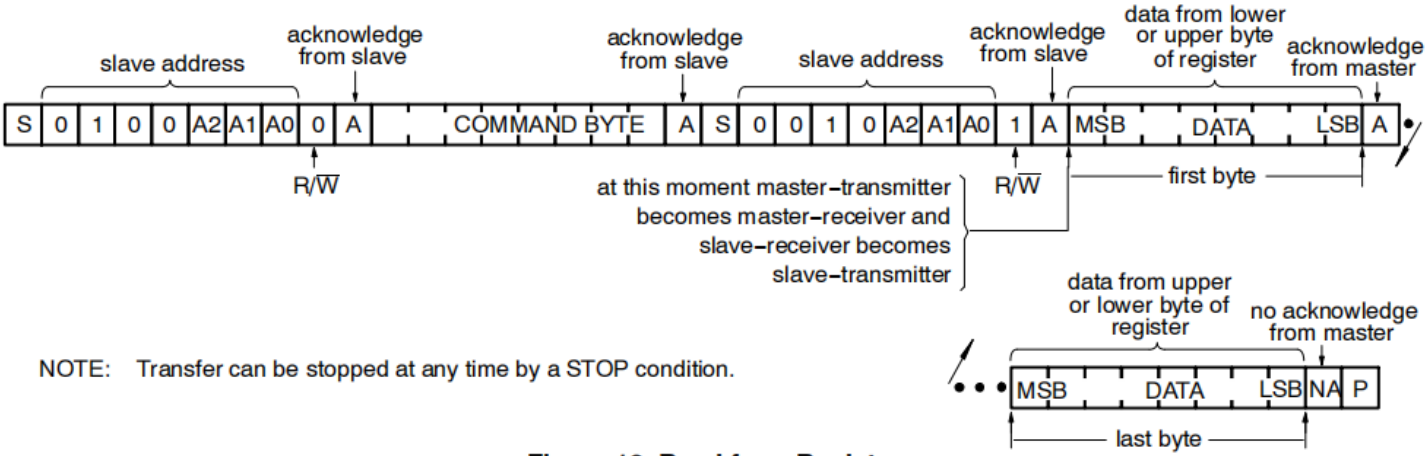


Figure 11. Write to Configuration Register

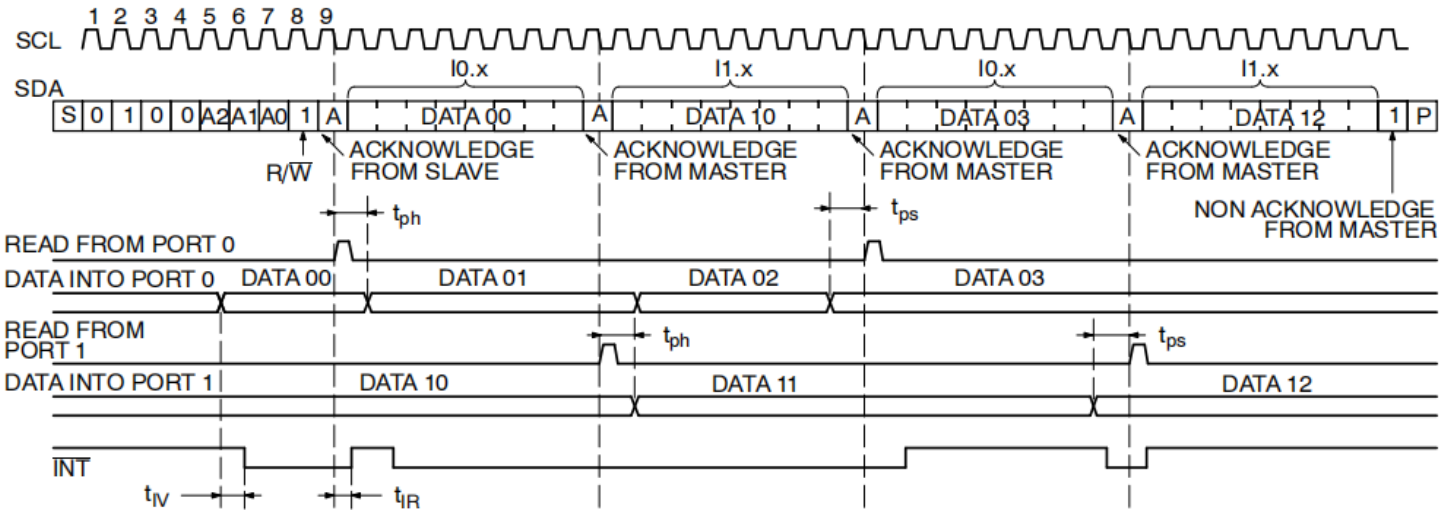
Power-On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power-on reset pulse holds the CAT9555 in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset condition is released and the internal state machine and the CAT9555 registers are initialized to their default state.



NOTE: Transfer can be stopped at any time by a STOP condition.

Figure 12. Read from Register



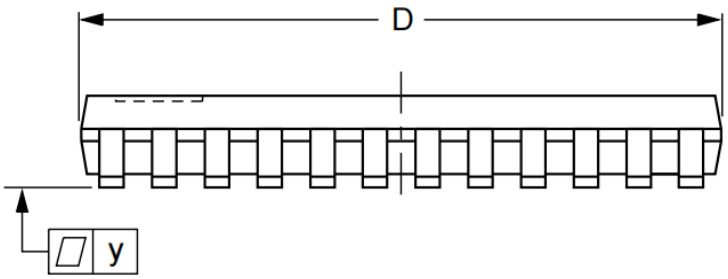
NOTE: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port register).

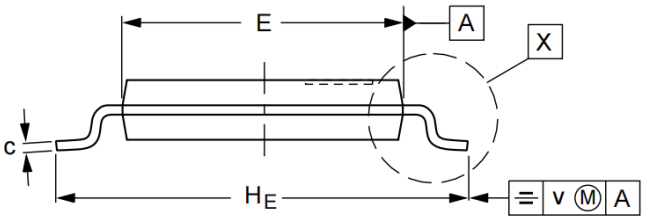
Figure 13. Read Input Port Register

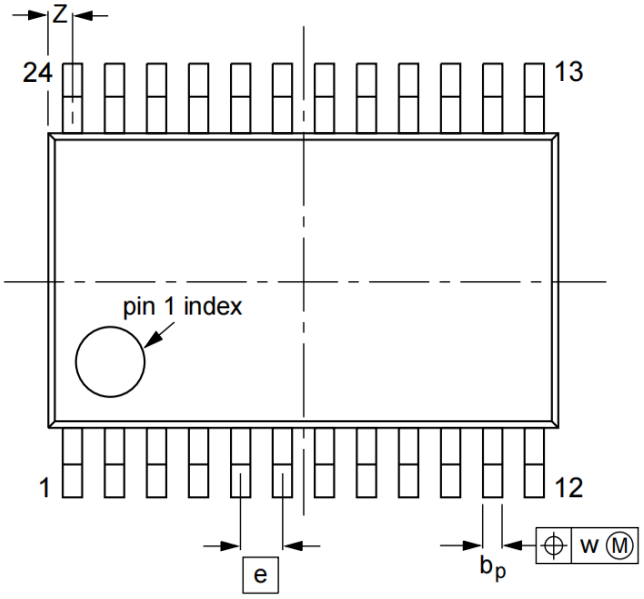
Order information

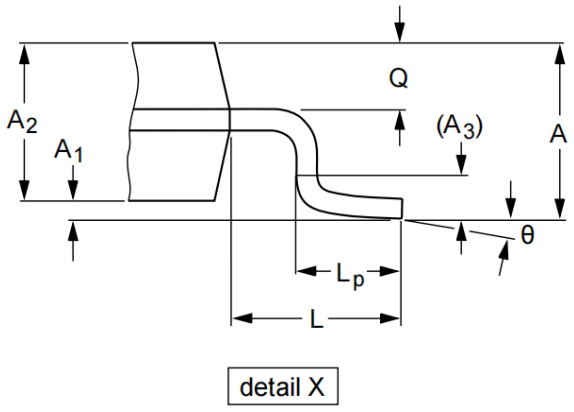
Order Number	Package	Package Quantity	Marking On The park
CAT9555YI-T2-TUDI	TSSOP24	Tape,Reel,2500	CAT9555YI-T2

Package TSSOP24









UNIT	A max	A_1	A_2	A_3	bp	c	D(1)	E(2)	e	He	L	Lp	Q	V	w	y	z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

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