

Overvoltage Protection Load Switch with Bidirectional Blocking and Surge Protection

Features

- Integrated ultra-low Ron switch: typical 20mΩ
- Bidirectional blocking between IN and OUT
- Pin-selectable overvoltage protection threshold $V_{OVP}=13V/17V/Rset$
- Fast overvoltage protection turn-off response: typical 80ns
- Surge protection compliant with IEC61000-4-5 up to ±100V
- Wide input voltage range from 3.1V to 28V
- 5A continuous current
- Autonomous mode and slave mode operation
- WLCSP 2.19mm X1.75mm-20B, 0.4mm pitch package

Applications

- Smartphones and Tablets
- Portable Devices
- Charging Ports

General Description

The AW32102E is a high input voltage, large current and ultra-low Ron load switch with bidirectional blocking.

The AW32102E is turned off very fast once the input voltage exceeds the OVP threshold to prevent damage to the protected downstream devices. The IN and OUT pin is capable of withstanding fault voltages up to 28VDC. The AW32102E provides a selectable OVP threshold of 13V/17V or Rset.

The AW32102E features reverse-blocking of output voltage. When the switch is open, the IN and OUT ports are completely cut off, preventing leakage current from IN to OUT and from OUT to IN.

The AW32102E OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to +/-100V. It also features over-temperature protection that prevents itself from thermal damaging.

Autonomous mode allows manual operation. Slave mode operation allows the device be controlled by a system controller.

◆ Typical Application Circuit

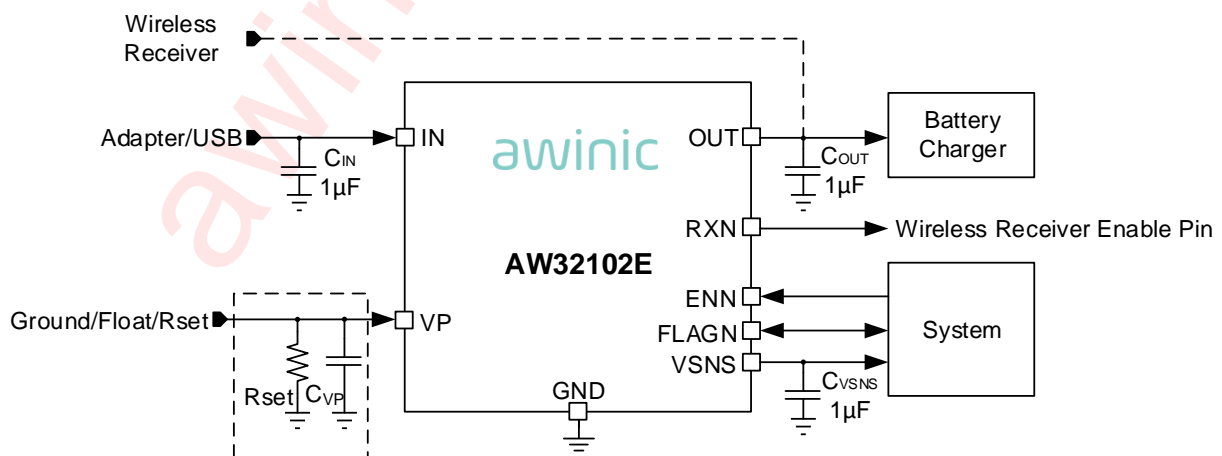


Figure 1 Typical Application Circuit of AW32102E

Pin Configuration And Top Mark

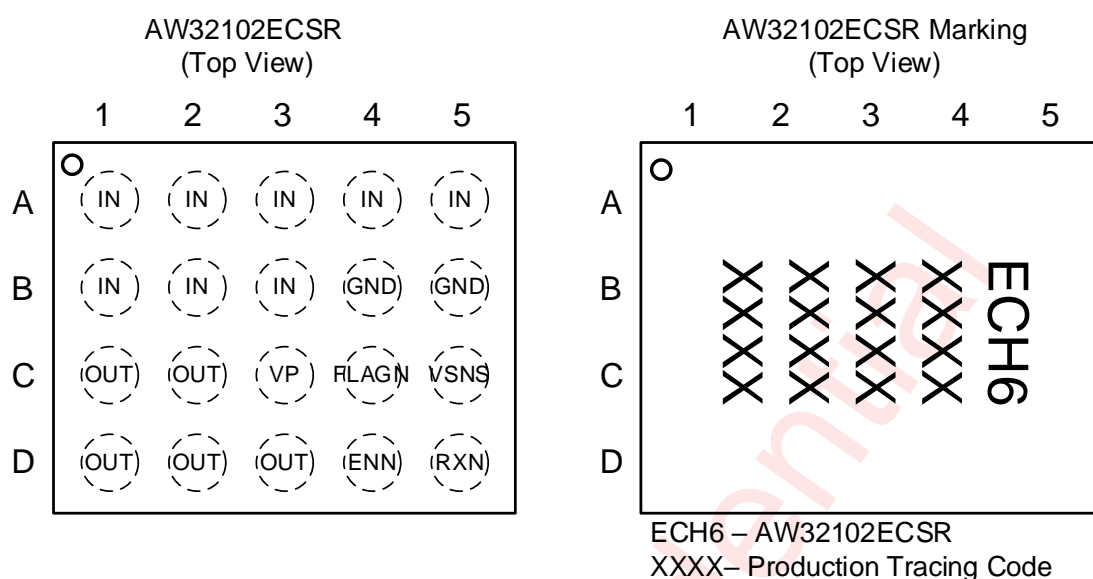


Figure 2 Pin Configuration And Top Mark

Pin Definition

PIN	NAME	DESCRIPTION
A1,A2,A3,A4,A5	IN	Switch input and power supply.
B1,B2,B3		
B4,B5	GND	Device ground.
C1,C2,D1,D2,D3	OUT	Switch output.
C3	VP	Setting overvoltage protection threshold. VP=Low, setting $V_{OVP}=17V$; VP=High or floating, setting $V_{OVP}=13V$. When a resistor from this pin to GND will set the OVP threshold value.
C4	FLAGN	Digital I/O Pin. The FLAGN pin is pulled high to indicate to the system when OTG mode can be triggered in autonomous mode. Slave mode: Pull this pin logic low, or tie to external GND. Autonomous mode: Connect to the System digital I/O pin (or equivalent) that pulls logic low to enter OTG mode when IN is connected to an OTG load and a power source is applied to OUT.
C5	VSNS	Sensing V_{IN} with output clamp capability.
D4	ENN	Active low logic enable pin. Slave mode: Connect this pin to system's enable logic pin. Autonomous mode: Pull this pin logic low or tie to the external GND.
D5	RXN	Wireless receiver active Low logic enable pin. Slave mode: Pull this pin logic low, or tie to an external GND. Autonomous mode: Connect this pin to the wireless receiver active low enable pin if a system output control pin is not available.

Functional Block Diagram

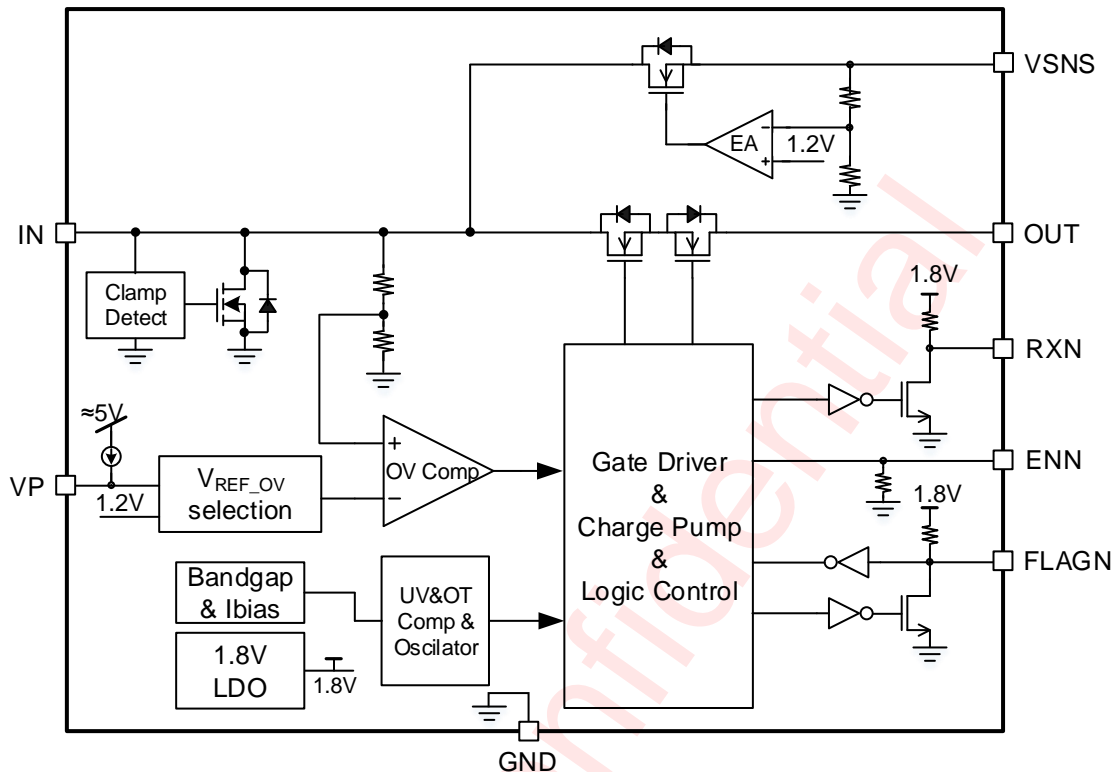


Figure 3 Functional Block Diagram

Typical Application Circuits

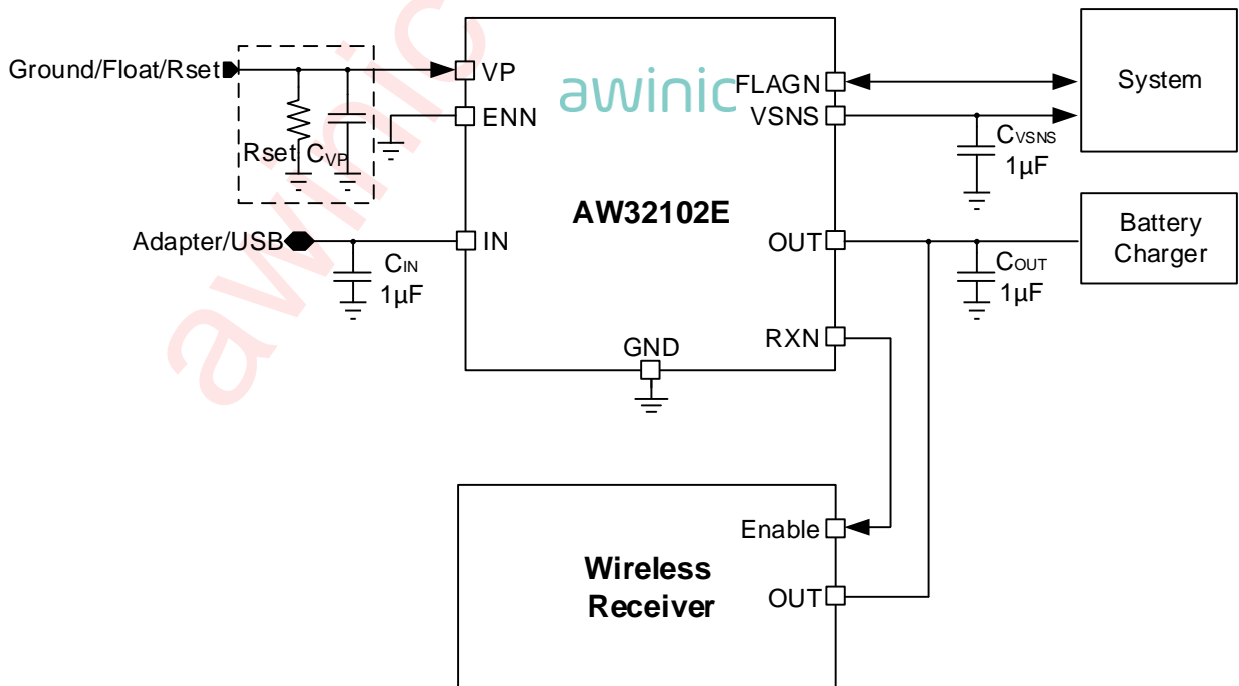


Figure 4 Dual Input Device (Autonomous Mode)

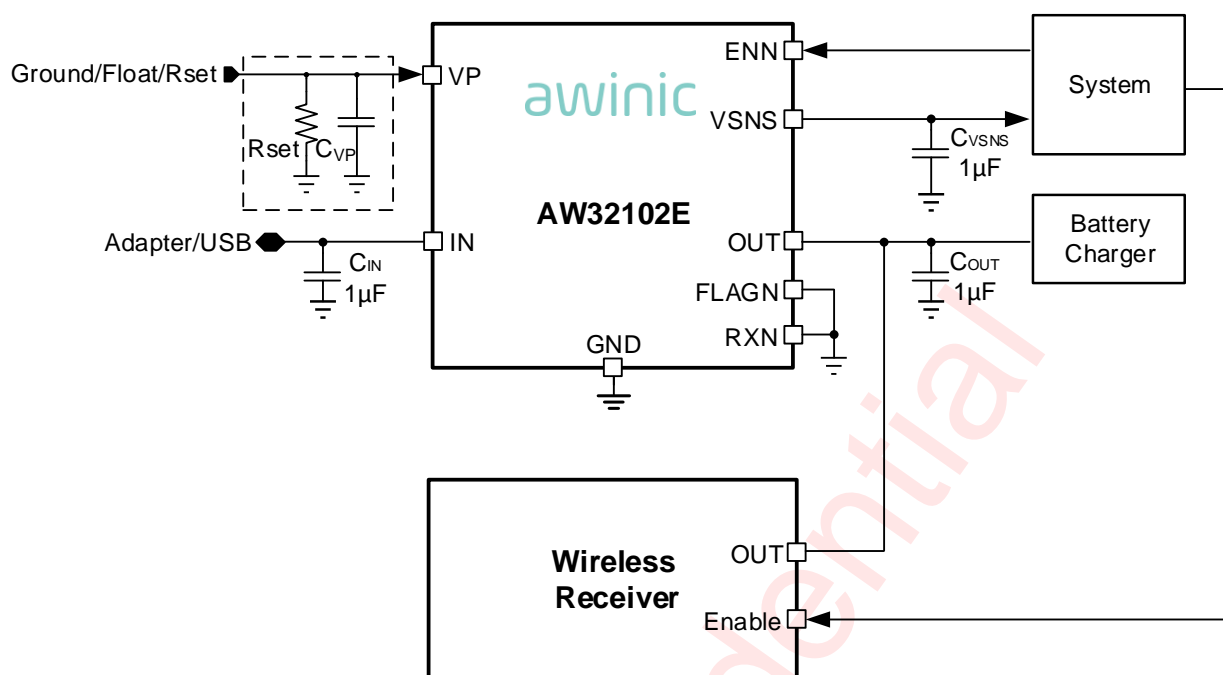


Figure 5 Dual Input Device (Slave mode)

Notice for Typical Application Circuits:

1. Both scheme are just examples, not only apply to Wireless Receiver.
2. The AW32102E has an internal 18µA current source on VP, so it can be left floating and pulled up to internal VDD output voltage.
3. FLAGN and RXN are pulled up to 1.8V via 105kΩ and 55kΩ respectively.
4. The FLAGN and RXN pins connect to GND, the device is set slave mode.
5. V_{IN} is sensed through the VSNS port, which can help the system make decision. C_{VSNS} is not necessary for the device.
6. Cap from VP to GND is needed, when VP connect resistance to GND. A 0.1µF capacitor is recommended for C_{VP} .

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmenta l Information	Delivery Form
AW32102ECSR	-40°C~85°C	WLCSP 2.19mmX1.75mm -20B	ECH6	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Input voltage range V_{IN}		-0.3V to 28V
Output voltage range V_{OUT}		-0.3V to 26V
Output voltage range V_{VSNS}		-0.3V to 28V
Input/Output DC voltage(ENN, VP, RXN, FLAGN)		-0.3V to 6V
Continuous current of switch IN-OUT(NOTE2)		5A
Peak switch current on IN and OUT pin(10ms) (NOTE2)		8A
Continuous current of switch OUT-IN(NOTE2)		5A
Junction-to-ambient thermal resistance θ_{JA}		55°C/W
Maximum operating junction temperature T_{JMAX}		150°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
Human Body Model (All pins, per ESDA/JEDEC JS-001-2017)		±2kV
Charged Device Model (All pins, per ESDA/JEDEC-JS-002-2018)		±1kV
Latch-Up		
Test condition: JESD78E		±200mA
Surge		
Test condition: IEC61000-4-5 test with 2Ω equivalent series resistance.	VIN initial 5V	±100V
	VIN initial 20V	±85V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}/V_{OUT}	Input/Output operating supply voltage	3.1		24	V
C_{IN}	Input capacitance		1	10	μF
C_{VSNS}	VSNS output capacitance		1		μF
C_{OTG}	OTG hot swap capacitance		1	100	μF
C_{OUT}	Output capacitance		1		μF

Electrical Characteristics

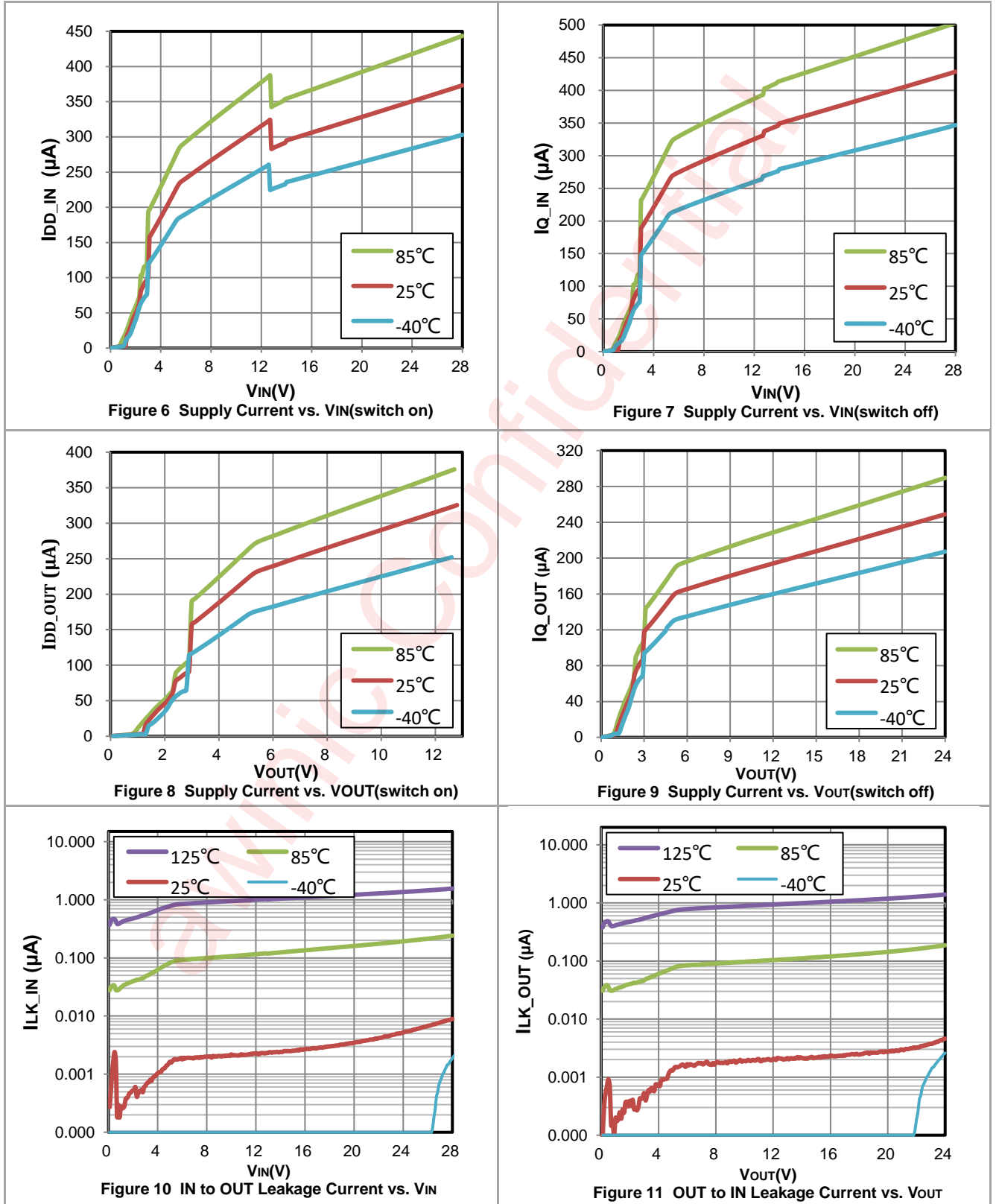
$V_{IN}=5V$, $C_{IN}=1\mu F$, $C_{OUT}=1\mu F$, $C_{VSNS}=1\mu F$, $T_A=25^\circ C$ for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CLAMP_IN}	IN input clamp voltage	$I_{IN}=10mA$, $T_A=+25^\circ C$	30			V
V_{LK_IN}	OUT float voltage	ENN=High, $V_{IN}=4.5V$ to 28V, OUT no load			0.4	V
V_{LK_OUT}	IN float voltage	ENN=High, $V_{OUT}=4.5V$ to 28V, IN no load			0.4	V
I_{Q_IN}	Input quiescent current, standby state	ENN=High, VP and FLAGN float, $V_{IN}=5.0V$		260		μA
I_{DD_IN}	Input operating current	ENN=Low, VP and FLAGN float, $V_{IN}=5.0V$, OUT no load		230		μA
I_{Q_OUT}	Input quiescent current, standby state	ENN=High, VP and FLAGN float, $V_{OUT}=5.0V$		160		μA
I_{DD_OUT}	Input operating current	ENN=Low, VP float, $V_{OUT}=5.0V$, FLAGN=Low, IN no load		230		μA
$R_{ON(IN-OUT)}$	Switch ON resistance from IN to OUT	$T_A=25^\circ C$, ENN=Low, $I_{OUT}=0.5A$		20	31	m Ω
I_{OUT}, I_{OTG}	Continuous output current				5	A
Protection						
V_{UVLO_IN}	IN UVLO trip level	V_{IN} rising	2.78	2.93	3.08	V
		Hysteresis		0.15		V
V_{UVLO_OUT}	OUT UVLO trip level	V_{OUT} rising	2.78	2.93	3.08	V
		Hysteresis		0.15		V
V_{OVP}	V_{IN} OVP threshold	VP to ground, V_{IN} rising	16	17	18	V
		VP to ground, Hysteresis		0.45		V
		VP left floating, V_{IN} rising	12	13	14	V
		VP left floating, Hysteresis		0.25		V
		VP connect a resistor to GND. $R_{set}=110k\Omega$	12.3	13.7	15.1	V
		VP connect a resistor to GND, Hysteresis. $R_{set}=110k\Omega$		0.15		V
V_{CLAMP_VSNS}	VSNS pin clamping voltage	VP to ground, $I_{VSNS}=0$		18		V
		VP left floating, $I_{VSNS}=0$		14		V
V_{DROP_VSNS}	Sense pin voltage drop when loaded	$I_{VSNS}=40mA$		150		mV

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I _{VSNS_LIM}	VSNS short-circuit current limit	V _{IN} =5V, V _{VSNS} =0V;		80		mA
R _{DIS_IN}	IN discharge resistance	ENN=Low, V _{IN} =V _{OUT} =5V		470		Ω
R _{DIS_OUT}	OUT discharge resistance	ENN=Low, V _{IN} =V _{OUT} =5V		470		Ω
T _{SD}	Thermal shutdown	Enter the shutdown state		150		°C
T _{SD_HYS}	Thermal shutdown hysteresis			20		°C
Digital Characteristics						
V _{IL}	Digital Input low level				0.3	V
V _{IH}	Digital Input high level		0.8			V
V _{OL}	Digital output low level	I _{sink} =2mA			0.2	V
V _{OH}	Digital output high level	Output logic high, no load	1.65	1.8		V
R _{FLAGN}	FLAGN pull-up resistance	FLAGN logic high pull-up	80	105	130	kΩ
R _{RXN}	RXN pull-up resistance	RXN logic high pull-up	40	55	70	kΩ
I _{VP}	VP pull-up current	V _P =2.5V	17.5	18	18.5	μA
I _{LEAK_ENN}	ENN Input leakage current	ENN=5V, V _{IN} =5V		8	12	μA
R _{ENN}	ENN pull-down resistance	ENN=5V, V _{IN} =5V		600		kΩ
T _{DEB_IL}	Input logic debounce time	ENN/FLAGN toggle		40		μs
Timing Characteristics						
T _{DEB_IN}	IN input debounce time	V _{UVLO_IN} <V _{IN} <V _{OVP} , ENN=Low, time delay between V _{IN} rising and RXN rising		50		ms
T _{DEB_OUT}	OUT input debounce time	Debounce time of OUT		40		μs
T _{SSTART}	Switch soft-start time	V _{IN} =5V, V _{OUT} from 10% to 90% of V _{IN}		0.5		ms
		V _{OUT} =5V, V _{IN} from 10% to 90% of V _{OUT}		0.5		ms
T _{DIS}	Supply discharge time	Discharge time of IN and OUT on discharge state		50		ms
T _{INIT}	Power up and initialization time	Upon IN or OUT crossing UVLO		100		μs
T _{SS_VSNS}	Soft startup time of V _{VSNS}	V _{IN} =5V, V _{VSNS} from 0.5V to 4.5V, no load			500	μs
T _{OFF_DLY}	Disable the switch delay time	Time delay from ENN, FLAGN or UVLO trigger to disable the load switch		40		μs
T _{OVP_DLY}	The delay time between V _{IN} over voltage and switch turn- off	C _{OUT} = 1μF, R _L = 100Ω, VP float, V _{IN} > V _{OVP} to V _{OUT} stop rising, V _{IN} initial 5V, 100V surge test, T _A = 25°C		80		ns

Typical Characteristics

Ambient temperature is 25°C, $V_{IN}/V_{OUT}=5V$, $C_{IN} = C_{OUT}= C_{VSNS}=1\mu F$, VP floating($V_{OVP}=13V$), unless otherwise noted.



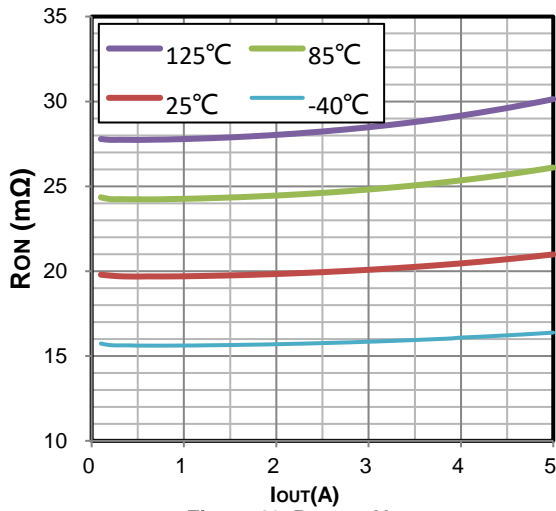


Figure 12 Ron vs. Iout

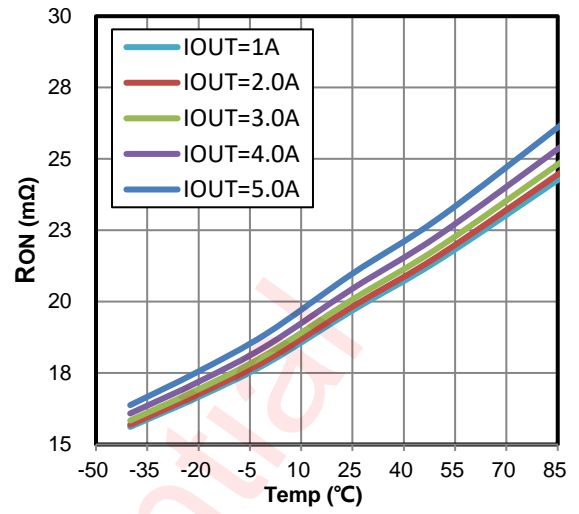


Figure 13 Ron vs. Temperature

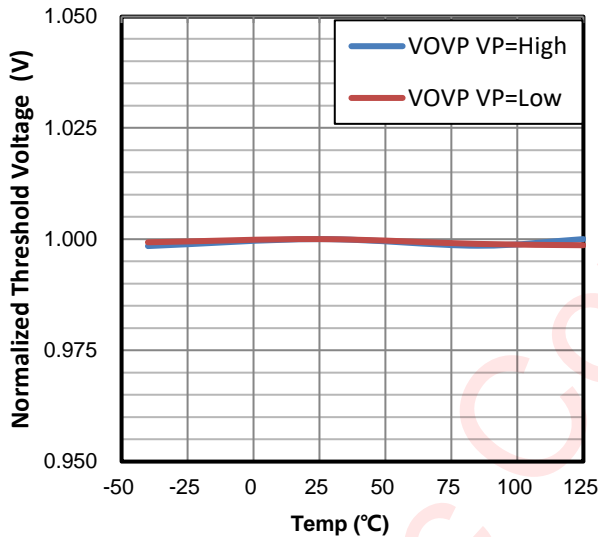


Figure 14 OVP Voltage vs. Temperature

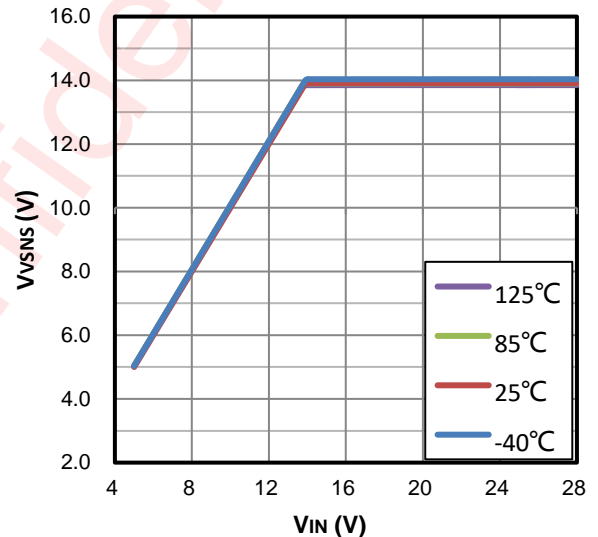


Figure 15 VSNS Clamp Voltage vs. VIN

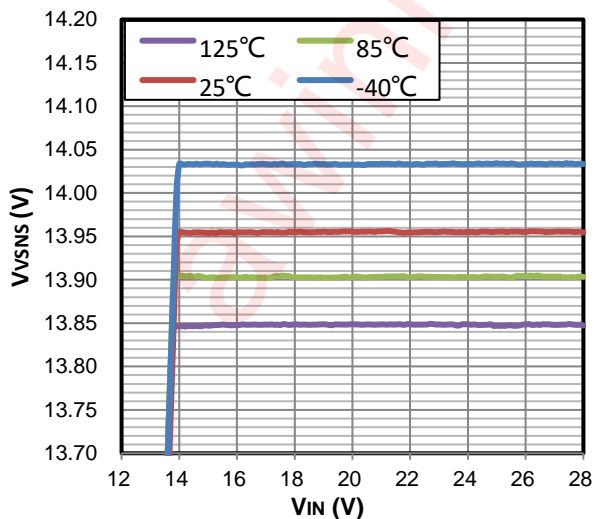


Figure 16 VSNS Clamp Voltage vs. VIN

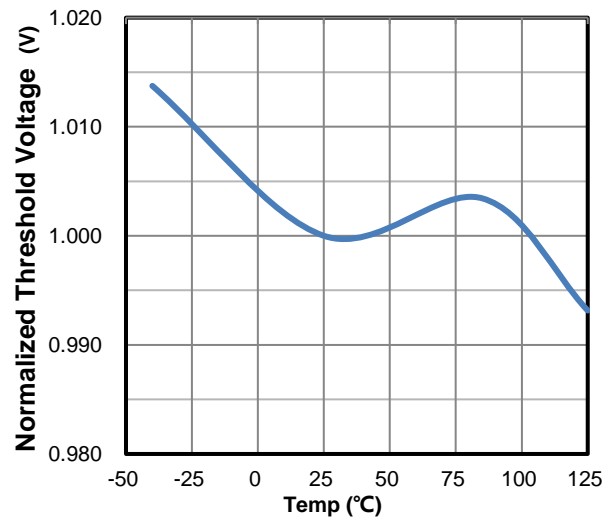


Figure 17 UVLO Voltage vs. Temperature

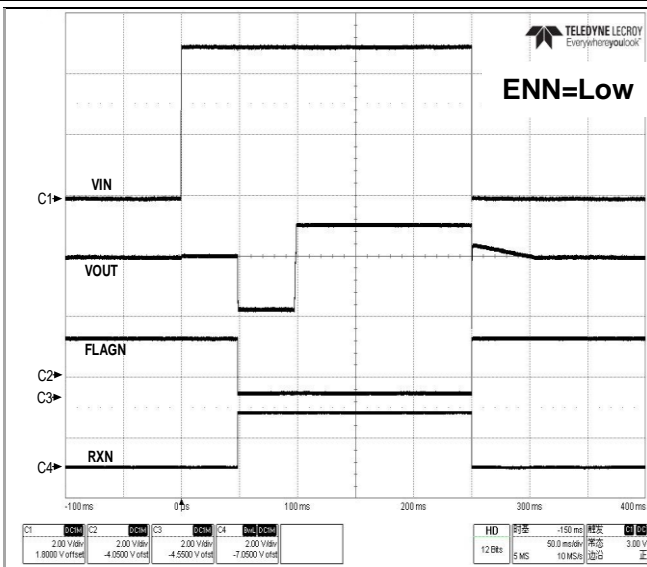


Figure 18 VIN=5V Insert and Remove

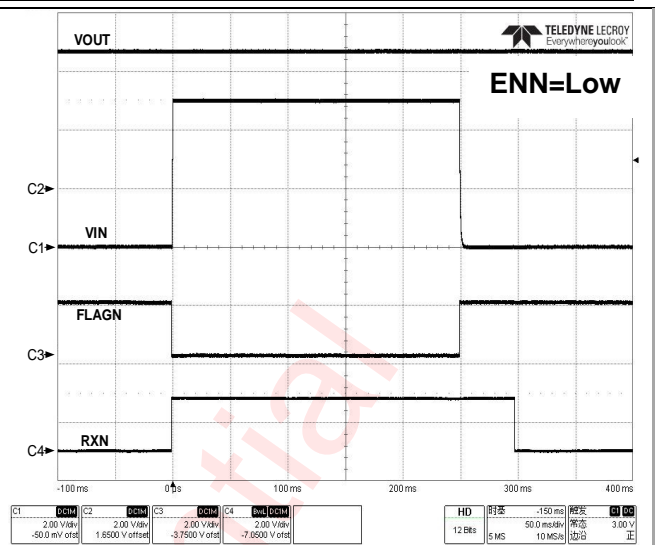


Figure 19 VOUT=5V Switch Turn On-Off by FLAGN

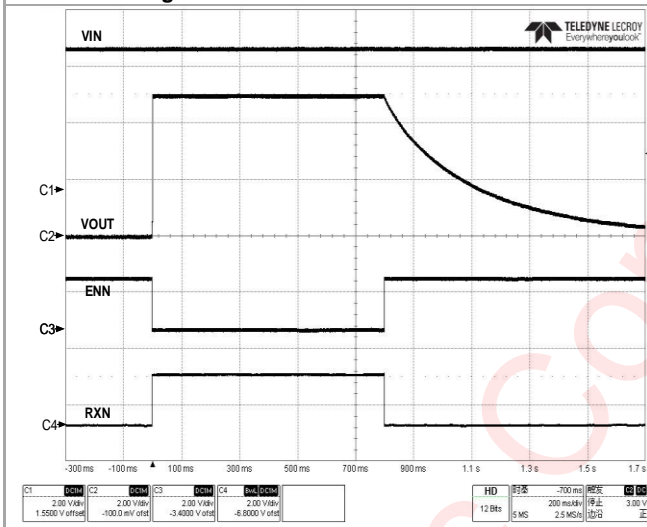


Figure 20 VIN=5V Switch Turn On-Off by ENN

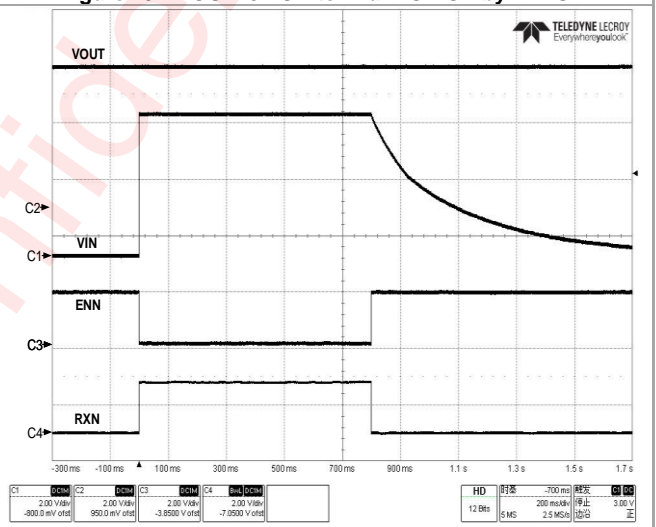


Figure 21 VOUT=5V Switch Turn On-Off by ENN

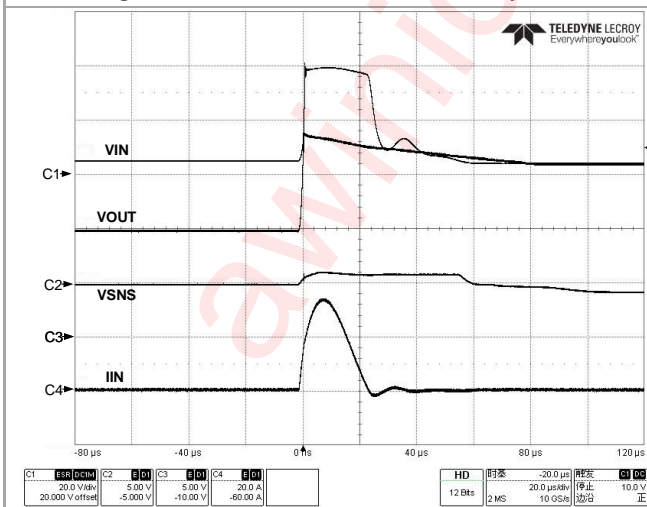


Figure 22 VIN=5V Surge Transient (+100V)

Detailed Functional Description

When a wirelessly charging mobile phone suddenly encounters an USB charging access, dual power sources wired-and will be happened, which may cause permanent damage to the power supply sources. Because of two internal integrated back-to-back switches and the break before make mechanism, AW32102E can achieve effective bidirectional blocking between input and output.

In the dual-source power supply system, the AW32102E is inserted on one of the supply paths, and the aforementioned dual power wired-and problems can be effectively solved under the control logic. The AW32102E switch consists of two back-to-back series MOSFETs with on-resistance as low as 20mΩ, and can transmit up to 5A DC current. Its IN port features overvoltage protection and surge protection to provide effective protection for the rear system. In addition, the system can also detect V_{IN} in real time through VSNS.

Surge Protection

The AW32102E integrates a clamp circuit to suppress input surge voltage. For surge voltages between V_{OVP} and V_{CLAMP_IN} , the switch will be turned off but the clamp circuit will not work. For surge voltages greater than V_{CLAMP_IN} , the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

Over-Voltage Protection

If the IN input voltage exceeds the OVP rising trip level, the switch will be turned off in about 80ns. When the voltage on the input exceeds the selected programmed over-voltage trip point, the device immediately turns off the internal OVP switch, disconnecting the load from the abnormal voltage, preventing damage to any downstream components. The OVP trip point can be selected by the VP pin. Connecting VP to ground, selects the V_{OVP} of typical 17V. With the VP left floating, selects the V_{OVP} of typical 13V. When a resistor from this pin to GND, the OVP threshold value set by Rset resistor is calculated using the Equation 1:

$$V_{OVP}=18 \times 10^{-6} \times R_{set} \times 6.85V \quad (1)$$

Use Equation 1, the resulting OVP threshold minimum is 8.6V, with $R_{set} = 70K\Omega \pm 1\%$, and the threshold accuracy is $\pm 10\%$.

Use Equation 1, the resulting OVP threshold maximum is 25.9V, with $R_{set} = 210K\Omega \pm 1\%$, and the threshold accuracy is $\pm 10\%$.

Bidirectional Blocking

The AW32102E integrates two back-to-back MOSFETs, when the load switch between IN and OUT is open, IN and OUT is bidirectional blocking, thereby blocking any reverse current.

Debounce Period

The valid IN detection occurs after a 50ms input debounce period. If the $V_{OUT} > V_{UVLO_OUT}$ is detected, V_{OUT} is valid and a debounce delay of 40μs begins.

Break Before Make Mechanism

A break before make mechanism will ensure the safety of the dual input sources. In autonomous mode, the IN 50ms debounce period is followed by at least 50ms break-before-make delay that allows time to discharging

OUT until the V_{OUT} invalid. The device keeps the switch open and the wireless receiver disable through pulling RXN high during the break-before-make delay.

A 10mA (or 470 Ω) pull-down at OUT is active during the break-before-make delay. The break-before-make delay is inactive when the IN is removed since UVLO is active and the load-switch is not powered. So the RXN goes low, and the wireless receiver will automatically be enabled again.

Mode Configure

In application, the AW32102ECSR can operate autonomously or be used as a slaver. If the FLAGN and RXN is detected to be low, the device is recognized as working in slave mode, otherwise in autonomous mode. Slave mode allows the charger (system) to act as a master and determine the input priority, while autonomous mode assigns the input priority to the IN power source over the wireless receiver.

Autonomous Mode

In autonomous mode, the device has a higher priority than the wireless receiver to power the output. The device is automatically turned on and off according to the presence of IN input. If V_{IN} is valid ($V_{IN} > V_{UVLO_IN}$), after the debounce time of 50ms, RXN is pulled high by the internal resistor, which disables the wireless charging path. And then, the device discharges to IN and OUT ports until the 50ms full and V_{OUT} invalid on the discharge period. The switch is closed to provide the voltage from IN to OUT; Otherwise the switch is open and the discharge state is continued.

In OTG applications, if V_{OUT} is valid ($V_{OUT} > V_{UVLO_OUT}$), after the debounce time of 40 μ s and the initialization process, FLAGN will be released and pulled up through an internal pull-up resistor. So the system can close the switch by forcing FLAGN low which will provide the voltage from OUT to IN, and output RXN high. The system releases the FLAGN, and the internal pull-up resistor again pulls the FLAGN up and the RXN returns to low after the 50ms discharge time. If the RXN is connected to a wireless receiver, RXN=High can be used to turn off the wireless receiver.

Slave Mode

In slave mode, the switch's state is controlled via the ENN pin. In the case of V_{IN} keep valid in the debounce time of 50ms, the switch can be turned on through pulling low ENN. The turn off process is opposite. In slave mode, the priority of the input power source between dual input devices is assigned by the system.

NOTE: Both the FLAGN and the RXN pins are tied to GND in slave mode.

Concurrent OTG Mode

The wireless receiver can provide a regulated 5V to OUT, not only for supplying the system but also to support OTG operation. This is referred to as concurrent OTG mode.

NOTE: OTG concurrent mode requires slave mode.

FLAGN Logic

The FLAGN pin is a bidirectional input/output pin that controls the transition to and from OTG modes while in autonomous mode. When IN is disconnected (floating) and a valid OUT voltage is detected, the FLAGN pin serves as an output signal and FLAGN is logic high. Subsequently, the load switch can be activated by toggling the FLAGN to low, which triggers OTG mode by transitioning into the ON-state.

Softstart

Both the switch between IN and OUT and the MOSFET between IN and VSNS turn on about 0.5ms soft start time which is designed to limit the peak inrush currents.

VSNS Indication

The voltage at the IN port is to be sensed by the device and outputs to VSNS port, which will have to be clamped to protect the downstream components. The VSNS clamp voltage output are selectable by the V_{OVP+1V} . It can support 40mA to external loads. Once IN exceeds UVLO, it starts to output. It will be turned off when an OTP event was detected.

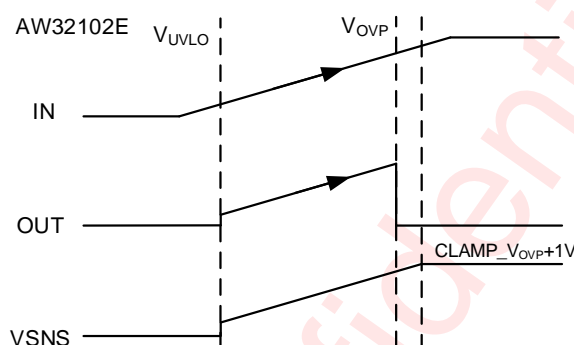


Figure 23 VSNS indication of the AW32102E

VSNS Short Protection

When VSNS is short to ground, the IN to VSNS current is limited to prevent the device burning.

Thermal Shutdown Protection

When the junction temperature rises to approximately 150°C , thermal shutdown(TSD) protection turns off the load switch for cooling the device until the junction temperature falls to approximately 130°C .

Timing Diagrams

Figure 24 through Figure 27 show autonomous mode and slave mode timing diagrams.

In autonomous mode, a 50ms debounce delay, a 50ms break-before-make/discharge period and a soft-start delay are applied when the $V_{IN} > V_{UVLO_IN}$ is detected. The FLAGN pin provides the IN voltage status prior to entering OTG mode. The discharge feature is enabled during the 50ms break-before-make period.

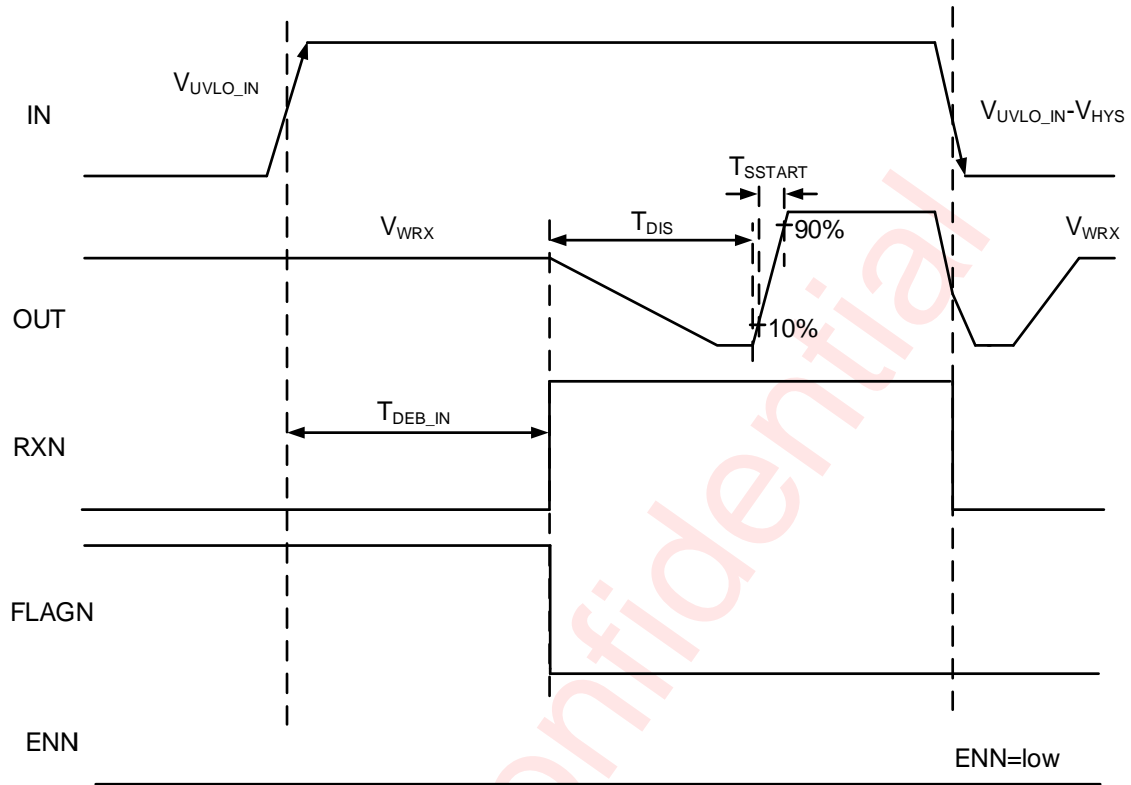


Figure 24 Autonomous Mode Timing: Application of V_{IN} with V_{OUT} Present, Removal of V_{IN}

In slave mode, the on/off-state of the load switch is determined by the ENN logic input pin that is tied to the system logic. A soft-start delay is applied when the ENN pin is toggled low, and the IN 50ms debounce period has expired.

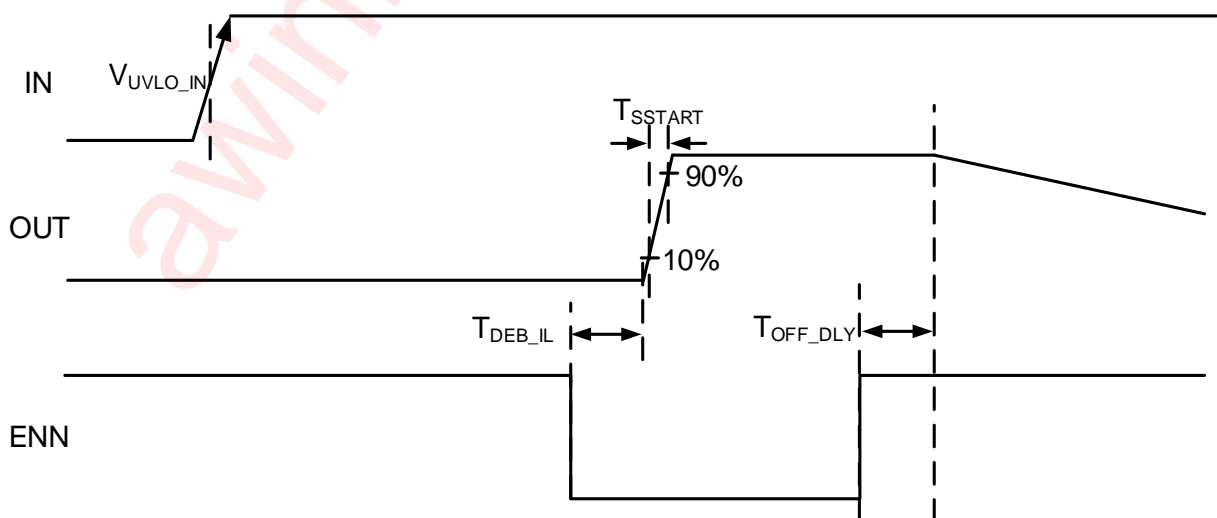


Figure 25 Slave Mode Timing: Application of V_{IN} with System Turned Off, Enabling, Disabling

In OTG modes, a load is applied to the IN and current flows from OUT to IN.

In autonomous mode, the FLAGN is a logic output and toggles high to indicate IN invalid, and OTG can be enabled immediately. The FLAGN pin is bidirectional, and autonomous OTG mode is triggered by pulling the FLAGN input pin low, which triggers a soft-start.

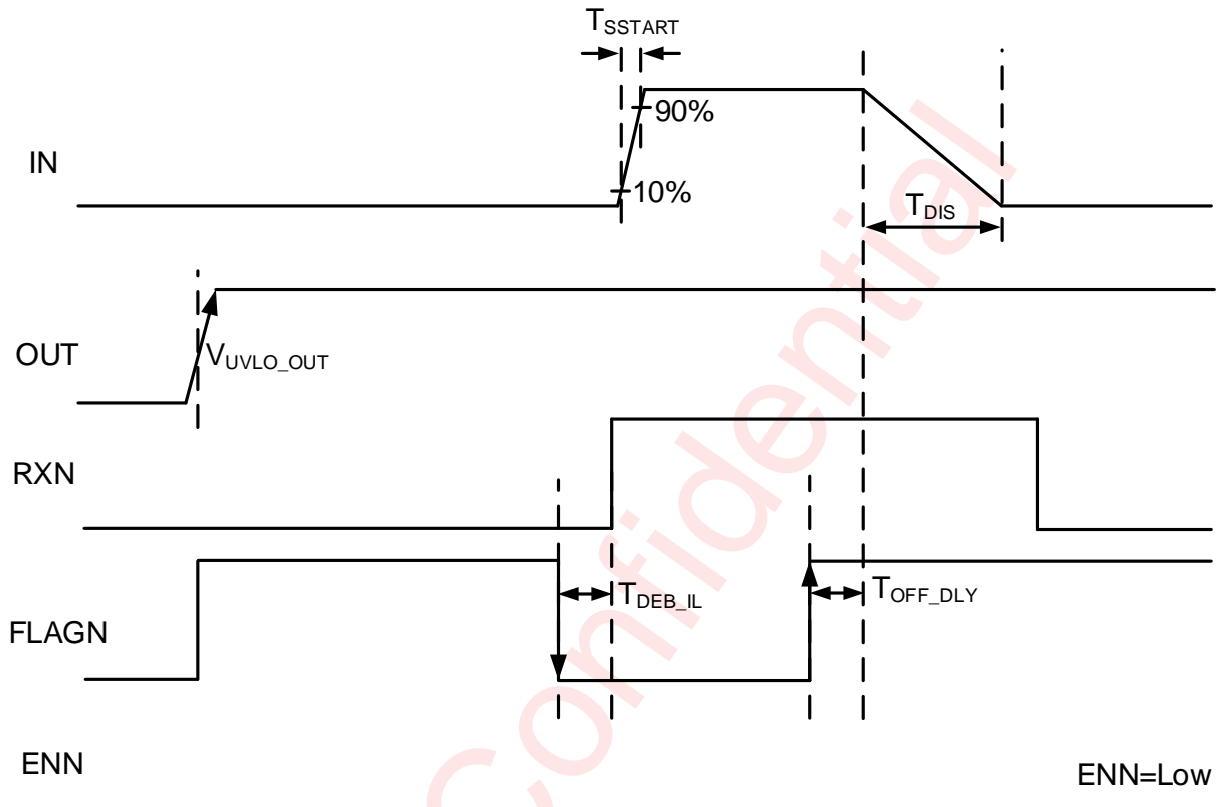


Figure 26 Autonomous Mode Timing: Application of V_{OUT} , Enabling (OTG), Disabling

In slave mode, OTG occurs when a valid OUT voltage is applied, no voltage is detected at the IN

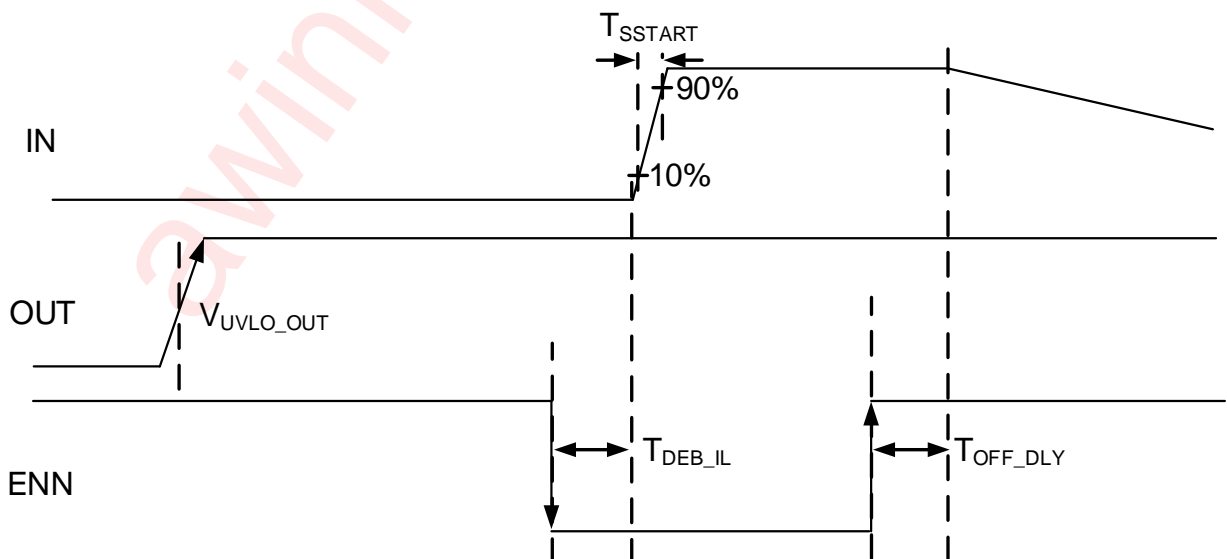


Figure 27 Slave Mode Timing: Application of V_{OUT} , Enabling (OTG), Disabling

PCB Layout Consideration

To obtain the optimal performance of AW32102E, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible, especially C_{IN} , C_{OUT} and C_{VSNs} . For example, Place the input capacitor C_{IN} on the top layer (same layer as the AW32102E) and close to IN pin.
2. The AW32102E integrate an up to 5A rated MOSFET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.
3. Use rounded corners on the power trace from the power supply connector to AW32102E to decrease EMI coupling.

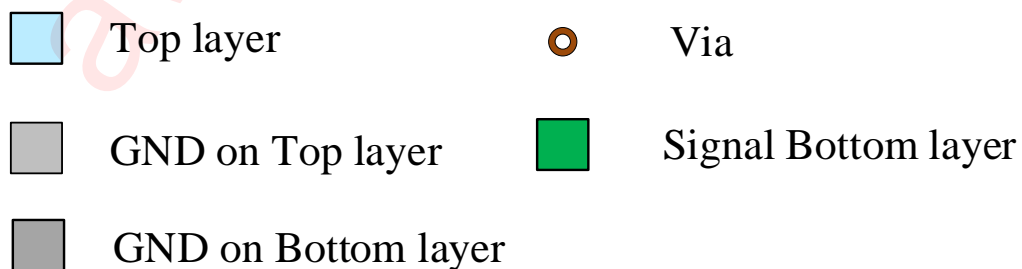
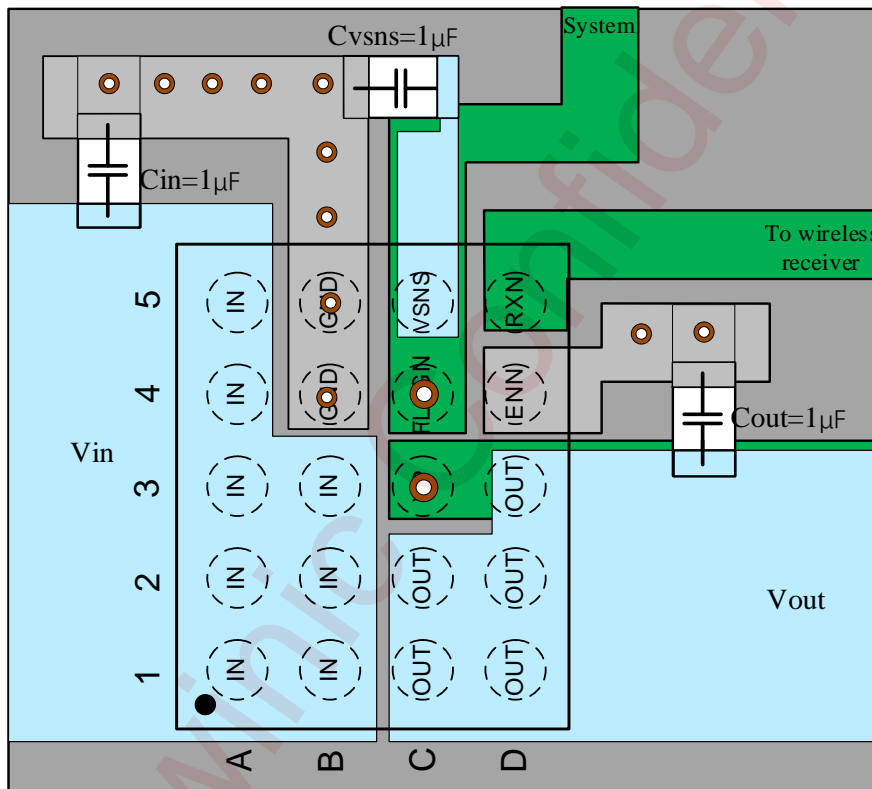
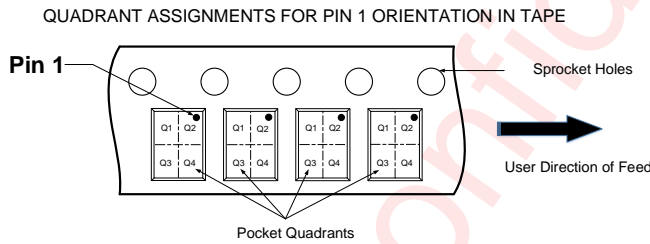
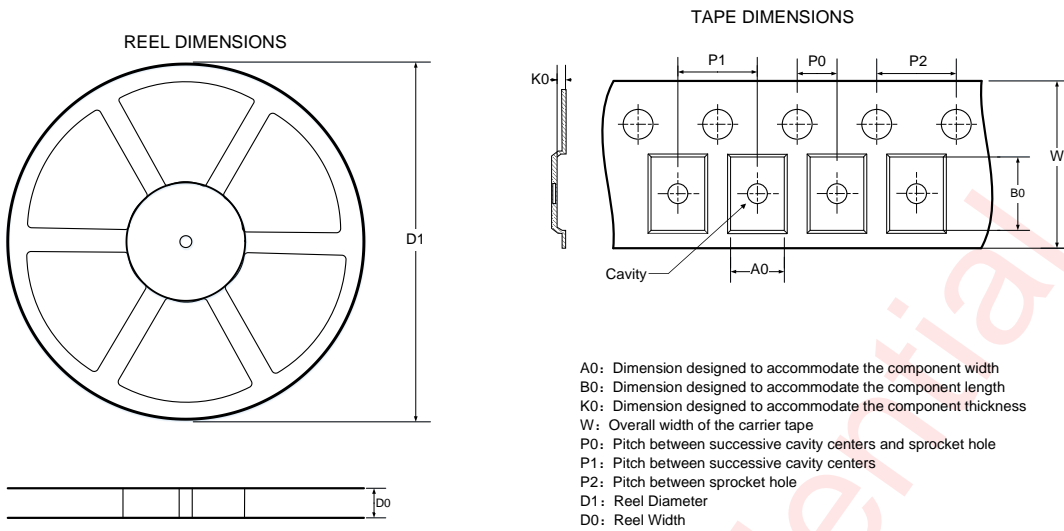


Figure 28 External Components Placements and PCB Layout Example

Tape And Reel Information

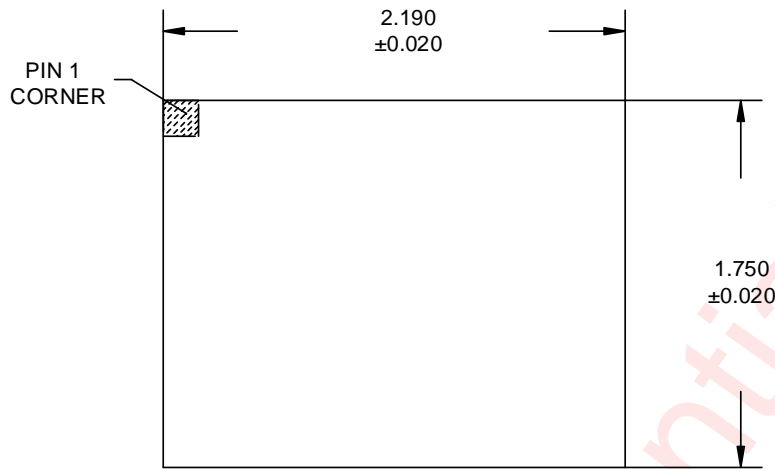


DIMENSIONS AND PIN1 ORIENTATION

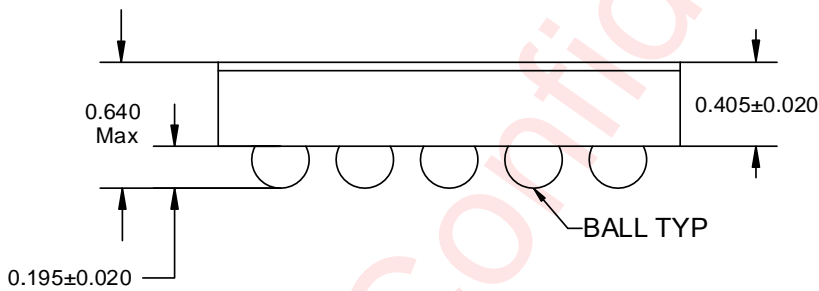
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.87	2.31	0.74	2.00	4.00	4.00	8.00	Q2

All dimensions are nominal

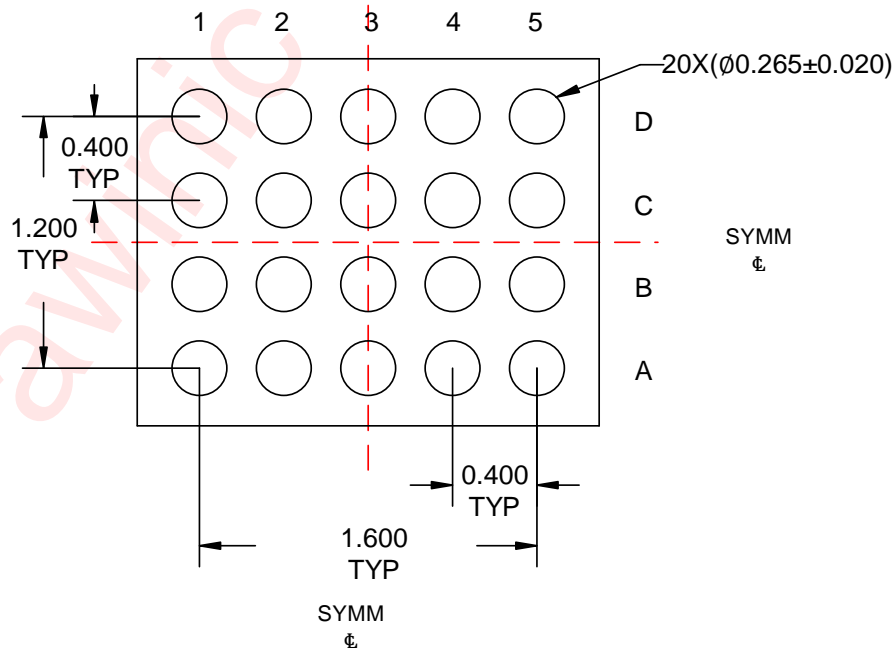
Package Description



Top View



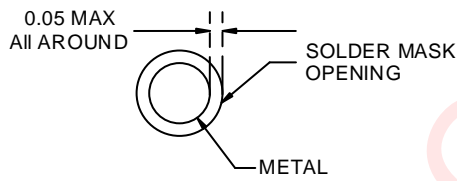
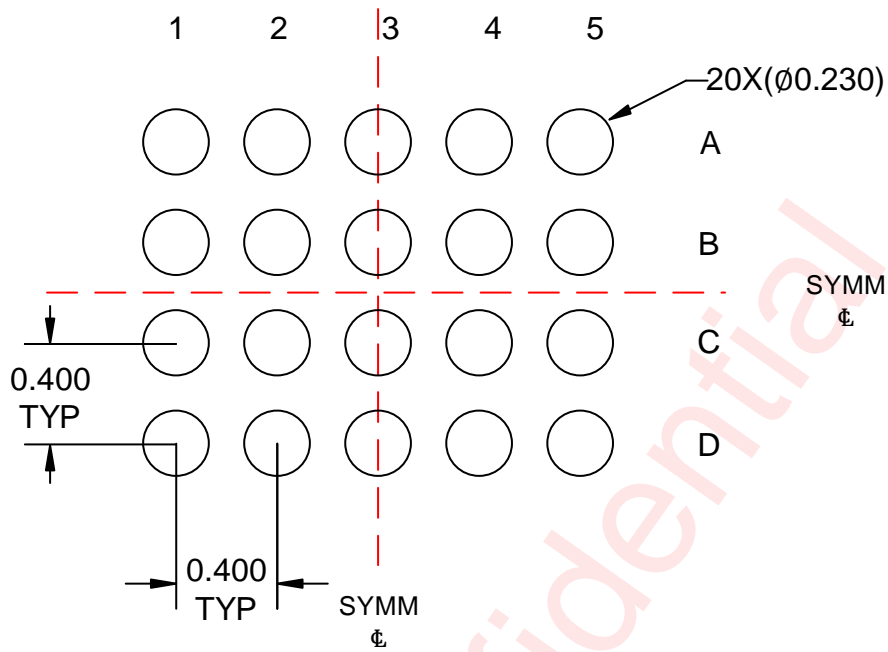
Side View



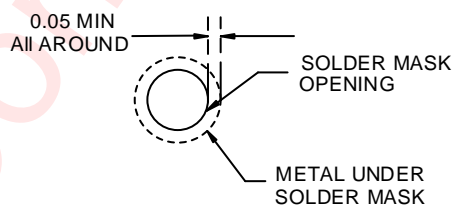
Bottom View

Unit: mm

Land Pattern Data



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov. 2021	Datasheet V1.0 released.
V1.1	Nov. 2022	<ol style="list-style-type: none">1. Updated the Pin 1 mark from a solid circle to a hollow circle in Configuration And Top Mark.2. Updated the T_{SSTART} in the Electrical Characteristics table.3. Updated part of Figure 7, Figure 14 and Figure 17.

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