

8-bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

Features

- No Direction-Control Signal Required
- Maximum Data Rates
 - 70Mbps (Push Pull),
 - 2Mbps (Open Drain)
- Power Supply Range:
 - A Port and VCCA: 1.1V to 3.6 V
 - B Port and VCCB: 1.65 V to 5.5 V
 - $VCCA \leq VCCB$
- Pull Up Resistors are Integrated in A Port and B Port
- No Power-Supply Sequencing Required: Either VCCA or VCCB Can be Ramped First
- Support Ultra-Low Power Consumption Mode with OE Pin is Low Voltage Level
- ESD Protection Exceeds ANSI/ESDA/JEDEC (A Port):
 - $\pm 4\text{kV}$ Human Body Model (JS-001-2023)
 - $\pm 1\text{kV}$ Charged-Device Model (JS-002-2022)
- IEC 61000-4-2 ESD (B port):
 - $\pm 6\text{kV}$ Contact Discharge
 - $\pm 8\text{kV}$ Air-Gap Discharge
- WBTSSOP 6.5mmx4.4mm-20L package

Applications

Mobile phones
Desktop PCs
IoT equipment
Tablet PCs

General Description

AW39128 is a 8-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. It needs two separate power supply rails, with the A ports tracks the VCCA ranging from 1.1V to 3.6V, and the B ports tracks the VCCB ranging from 1.65V to 5.5V. This makes the chip has capabilities of support both lower and higher logic signal levels translation between any of the 1.2V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The OE input circuit is supplied by VCCA. Meanwhile, OE is recommended to be tied to GND through an external pull-down resistor to ensure all I/O to be pulled to the supply voltage. No power supply sequencing requirements means either VCCA or VCCB can be powered up first, and OE should be enabled after both VCCA and VCCB are established.

Typical Application Circuit

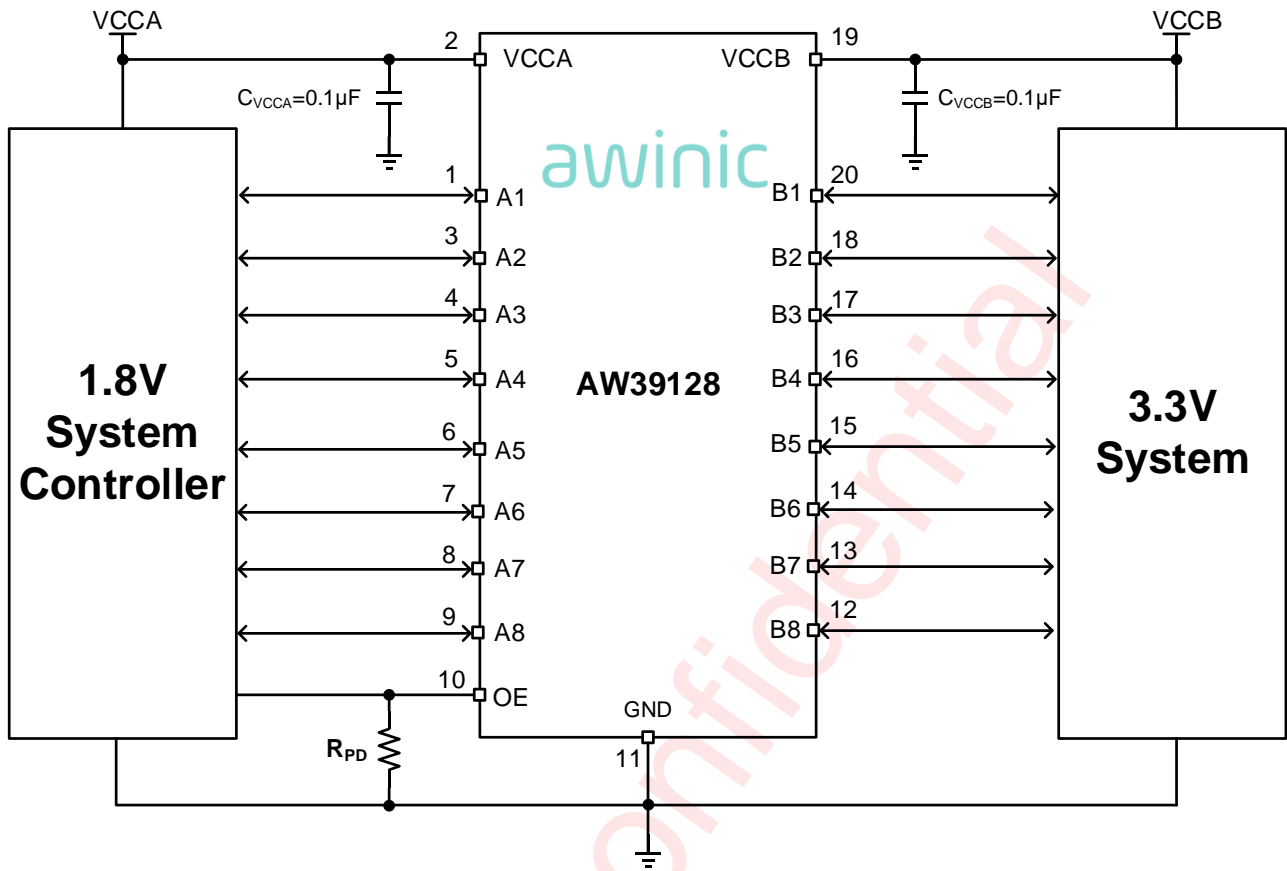
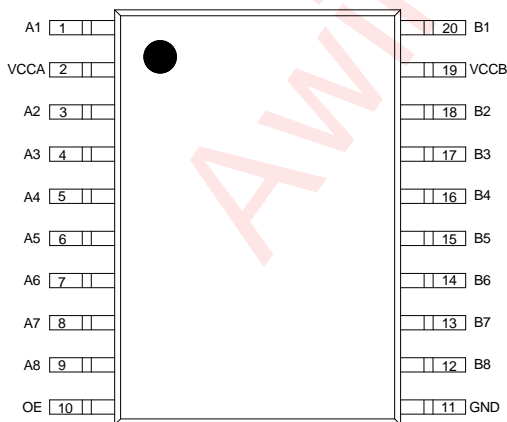


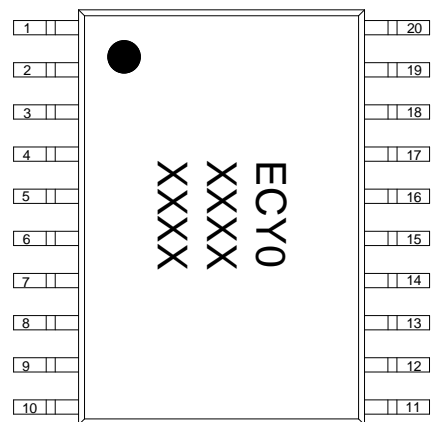
Figure 1 Typical Application Circuit of AW39128

Pin Configuration And Top Mark

AW39128SPR
(Top View)



AW39128SPR Marking
(Top View)



ECY0—AW39128SPR
XXXX/XXXX—Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	A1	Input/output A1.
2	VCCA	A-port supply voltage. $1.1V \leq VCCA \leq 3.6V$, $VCCA \leq VCCB$.
3	A2	Input/output A2.
4	A3	Input/output A3.
5	A4	Input/output A4.
6	A5	Input/output A5.
7	A6	Input/output A6.
8	A7	Input/output A7.
9	A8	Input/output A8.
10	OE	Output enable.
11	GND	Ground.
12	B8	Input/output B8.
13	B7	Input/output B7.
14	B6	Input/output B6.
15	B5	Input/output B5.
16	B4	Input/output B4.
17	B3	Input/output B3.
18	B2	Input/output B2.
19	VCCB	B-port supply voltage. $1.65V \leq VCCB \leq 5.5V$.
20	B1	Input/output B1.

Functional Block Diagram

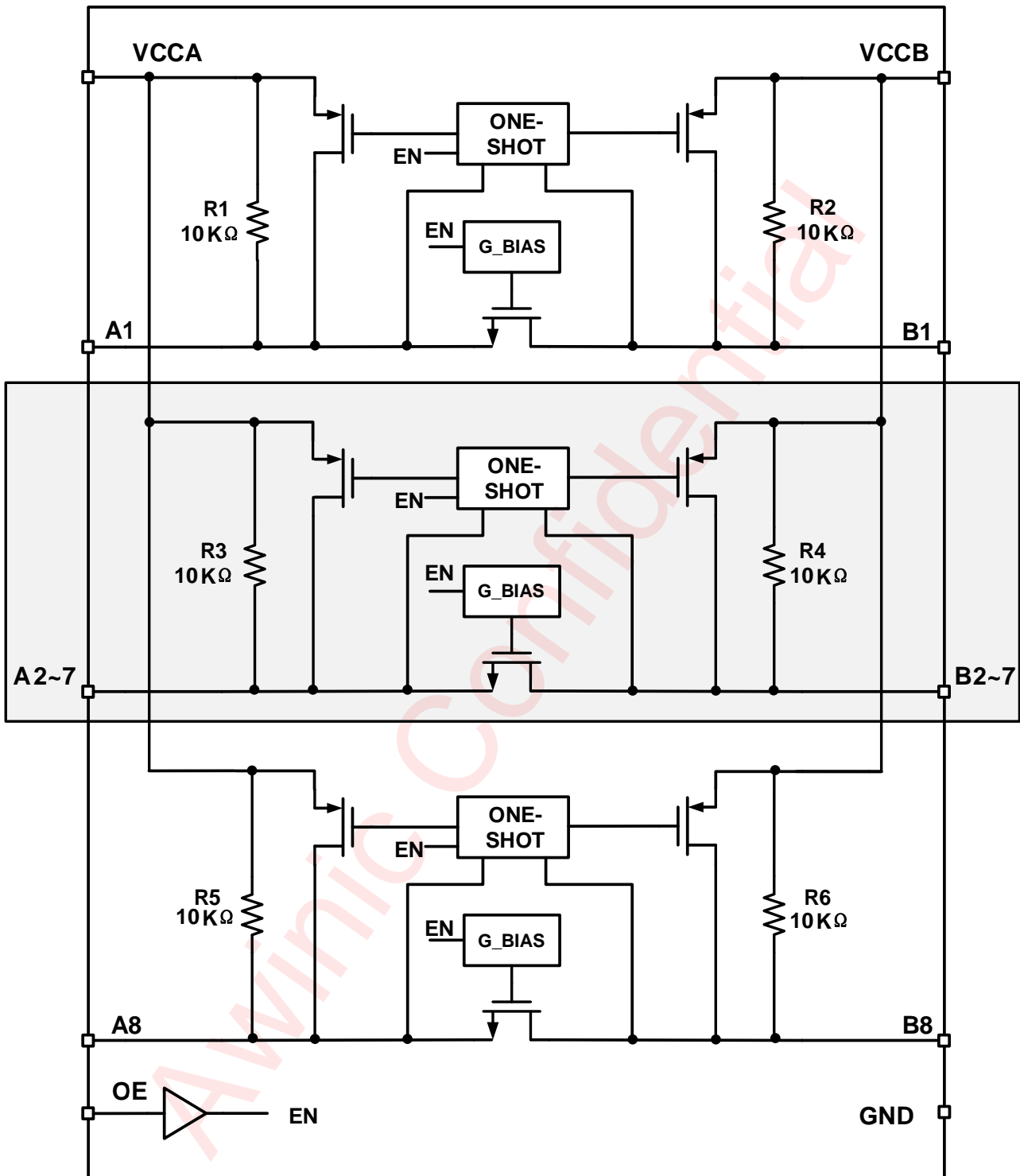


Figure 3 AW39128 Function Block

Typical Application Circuits

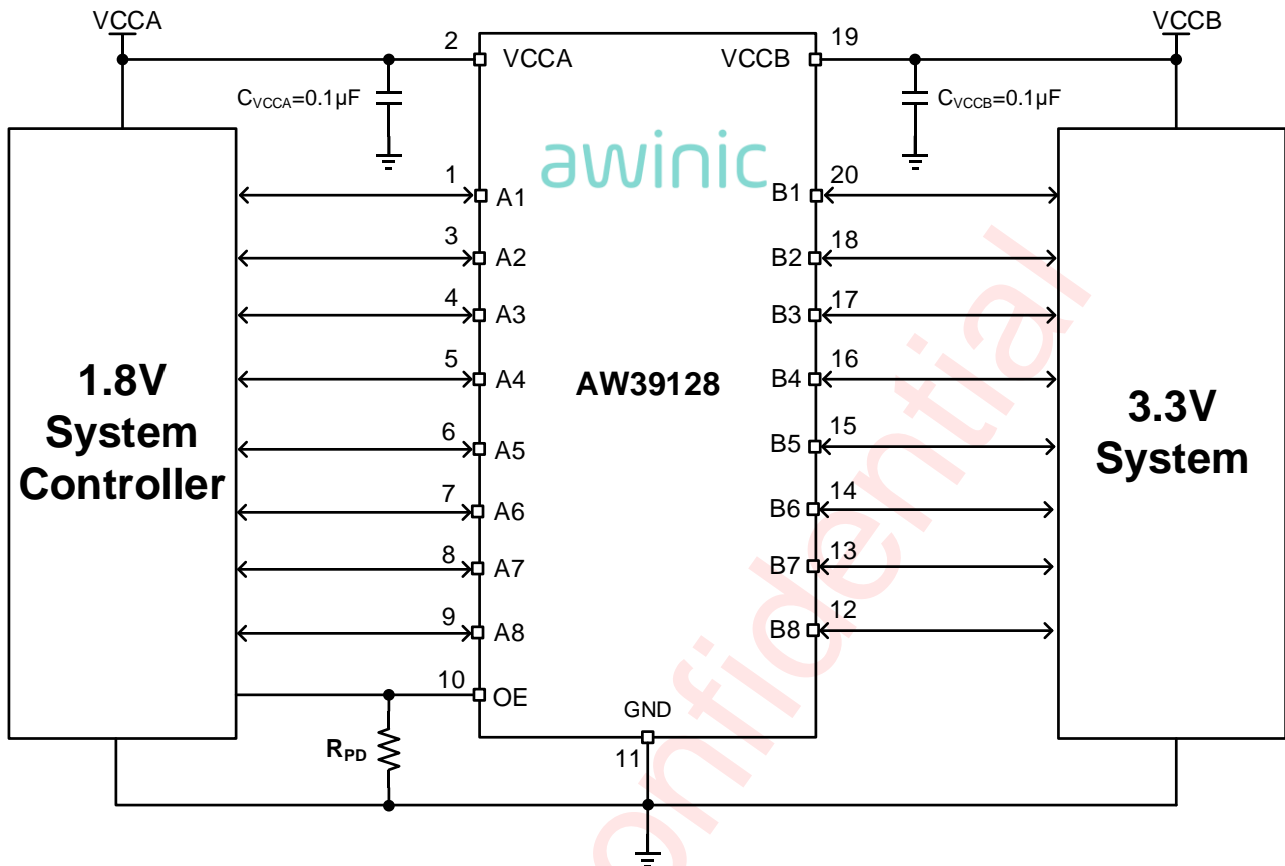


Figure 4 AW39128 Application Circuit

Notice for typical application circuits:

1. In any case, the A/B Ports Voltage cannot be higher than the VCCA/VCCB voltage. Otherwise, the leakage current will flow from A/B Ports to VCCA/VCCB.
2. The device driving the A/B ports must have the driving capacity at least ± 1 mA.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39128SPR	-40°C ~ 125°C	WBTSSOP 6.5mmx4.4mm- 20L	ECY0	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CCA} ^(NOTE2)		-0.5V to 5V
Supply voltage range V_{CCB} ^(NOTE2)		-0.5V to 6V
Input voltage range, V_I ^(NOTE2)	A port	-0.5V to 5V
	B port	-0.5V to 6V
Output voltage range in high or low state, V_O ^(NOTE2)	A port	-0.5V to 5V
	B port	-0.5V to 6V
Input clamp current, I_{Ik}	$V_I < 0$	-50mA
Output clamp current, I_{Ok}	$V_O < 0$	-50mA
Junction-to-ambient thermal resistance θ_{JA}		74.58°C /W
Operating free-air temperature range		-40°C to 125°C
Operating junction temperature T_J		-40°C to 150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM ^(NOTE 3)	A port	±4kV
	B port	±4kV
CDM ^(NOTE 4)	A port	±1kV
	B port	±1kV
Latch-Up ^(NOTE 5)		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: With respect to GND.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2023

NOTE4: Test method: ANSI/ESDA/JEDEC JS-002-2022

NOTE5: Test method: JEDEC JESD78F.01-2022

Recommended Operating Conditions

Symbol	Parameters	Conditions	Min.	Max.	Unit	
V _{CCA}	Supply voltage for A port		1.1	3.6	V	
V _{CCB}	Supply voltage for B port		1.65	5.5	V	
V _{IH}	High-level input voltage	A-port	V _{CCA} =1.1V~1.95V V _{CCB} =1.65V~5.5V	V _{CCI} -0.2	V _{CCI}	V
			V _{CCA} =2.3V~3.6V V _{CCB} =1.65V~5.5V	V _{CCI} -0.4	V _{CCI}	V
		B-port	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V	V _{CCI} -0.4	V _{CCI}	V
		OE input	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V	V _{CCA} ×0.65	5.5	V
V _{IL}	Low-level input voltage	A-port	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V	0	0.15	V
		B-port	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V	0	0.15	V
		OE input	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V	0	V _{CCA} ×0.35	V
Δt/ΔV	Input transition rise or fall rate	A-port (NOTE6)	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V		10	ns/V
		B-port (NOTE6)	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V		10	ns/V
		Control input	V _{CCA} =1.1V~3.6V V _{CCB} =1.65V~5.5V		10	ns/V
T _A	Operating free-air temperature T _A		-40	125	°C	

NOTE6: The parameter is defined for push-pull driving.

Electrical Characteristics

DC ELECTRICAL CHARACTERISTICS

Operating under recommended conditions, $V_{CCA} \leq V_{CCB}$, $T_A=25^\circ\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	$V_{CCA}(\text{V})$	$V_{CCB}(\text{V})$	MIN	TYP	MAX	UNIT		
V_{OHA}	Port A output high voltage	$I_{OH} = -20\mu\text{A}$ $V_{IB} \geq V_{CCB} - 0.4\text{V}$	1.1~3.6	1.65~5.5	$V_{CCA} \times 0.67$			V		
V_{OLA}	Port A output low voltage	$I_{OL} = 1\text{mA}$ $V_{IB} \leq 0.15\text{V}$						0.4	V	
V_{OHB}	Port B output high voltage	$I_{OH} = -20\mu\text{A}$ $V_{IA} \geq V_{CCA} - 0.2\text{V}$					$V_{CCB} \times 0.67$		V	
V_{OLB}	Port B output low voltage	$I_{OL} = 1\text{mA}$ $V_{IA} \leq 0.15\text{V}$						0.4	V	
I_I	OE input leakage current	$V_I = V_{CCI}$ or GND, $T_A = 25^\circ\text{C}$					-1		1	μA
		$V_I = V_{CCI}$ or GND, $T_A = -40^\circ\text{C}$ to 125°C					-2		2	μA
I_{OZ}	A or B port output current	$OE = V_{IL}$ $V_I = \text{GND}$, $T_A = -40^\circ\text{C}$ to 125°C					-2		2	μA
		$OE = V_{IL}$ $V_I = V_{CCI}$, $T_A = -40^\circ\text{C}$ to 125°C					-1		1	μA
I_{CCA}	VCCA supply current	$OE = V_{CCA}$ $V_I = V_O = \text{Open}$, $I_O = 0$ $T_A = 25^\circ\text{C}$	1.1~3.6	1.65~5.5			1	μA		
			3.6	0			1	μA		
			0	5.5			-1	μA		
		$OE = V_{CCA}$ $V_I = V_O = \text{Open}$, $I_O = 0$ $T_A = 125^\circ\text{C}$	3.6	5.5		0.04		μA		
			3.6	0		0.16		μA		
			0	5.5		-0.03		μA		
I_{CCB}	VCCB supply current	$OE = V_{CCA}$ $V_I = V_O = \text{Open}$, $I_O = 0$ $T_A = 25^\circ\text{C}$	1.1~3.6	1.65~5.5		2.5	18	μA		
			3.6	0			-1	μA		
			0	5.5			1	μA		
		$OE = V_{CCA}$ $V_I = V_O = \text{Open}$, $I_O = 0$ $T_A = 125^\circ\text{C}$	3.6	5.5		4.9		μA		
			3.6	0		-0.01		μA		
			0	5.5		0.09		μA		
I_{CCB+} I_{CCA}	Combined supply current	$V_I = V_O = \text{Open}$ $I_O = 0$	1.1~3.6	1.65~5.5			20	μA		
R_{PU}	Resistor pull-up value	$T_A = 25^\circ\text{C}$	1.1~3.6	1.65~5.5	8	10	12	k Ω		
R_{NPASS}	The resistor of NMOSFET between A port and B port	$OE = V_{CCI}$, $V_I = 0.15\text{V}$ $I_{source} = 10\text{mA}$, $T_A = 25^\circ\text{C}$	1.8	3.3		27		Ω		

TIMING REQUIREMENTS (NOTE1)Output load: $C_L=15\text{pF}$, push-pull driver, and $T_A=-40^\circ\text{C}$ to 125°C .

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
$V_{CCA}=1.1\text{V}\pm 0.15\text{V}$					
Data Rate	Push-pull driving	$V_{CCB}=1.8\text{V}\pm 0.2\text{V}$		16	Mbps
		$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		16	
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		10	
	Open-drain driving	$V_{CCB}=1.8\text{V}\pm 0.2\text{V}$		2	
		$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		2	
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		2	
$V_{CCA}=1.65\text{V}\pm 0.15\text{V} / 2.5\text{V}\pm 0.2\text{V}$					
Data Rate	Push-pull driving	$V_{CCB}=1.8\text{V}\pm 0.2\text{V}$		40	Mbps
		$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		40	
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		40	
	Open-drain driving	$V_{CCB}=1.8\text{V}\pm 0.2\text{V}$		2	
		$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		2	
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		2	
$V_{CCA}=3.3\text{V}\pm 0.3\text{V}$					
Data Rate	Push-pull driving	$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		70	Mbps
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		70	
	Open-drain driving	$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$		2	
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$		2	
t_w	Pulse Duration	$V_{CCB}=2.5\text{V}\pm 0.2\text{V}$	45		ns
		$V_{CCB}=3.3\text{V}\pm 0.3\text{V}$	40		
		$V_{CCB}=5\text{V}\pm 0.5\text{V}$	40		

NOTE1: The parameter's variation is guaranteed by design, not production tested.

SWITCH CHARACTERISTICSOutput load: $C_L=15\text{pF}$, $T_A=25^\circ\text{C}$ for typical values (unless otherwise noted), $V_{CCA}=1.1\text{V}$

PARAMETER	TEST CONDITION		$V_{CCB}=1.65\text{V}$	$V_{CCB}=3.3\text{V}$	$V_{CCB}=5\text{V}$	UNIT
			TYP	TYP	TYP	
t_{PHL} (NOTE2)	A to B	Push-pull	6.1	7.5	9.5	ns
		Open-drain	1.5	2.8	4.2	
t_{PLH} (NOTE2)	A to B	Push-pull	14.06	11.3	12.9	ns
		Open-drain	60.8	49.9	42.7	
t_{PHL} (NOTE2)	B to A	Push-pull	5.04	5.5	5.8	ns
		Open-drain	1.7	2.7	3.4	
t_{PLH} (NOTE2)	B to A	Push-pull	-0.2	-2.2	-3.2	ns
		Open-drain	-64.4	-53.3	-41.7	
t_{en} Enable time	OE to A or B		62	24.9	14.7	ns
t_{dis} disable time	OE to A or B		106.4	79.6	77.5	ns

PARAMETER	TEST CONDITION		V _{CCB} =1.65V	V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	TYP	
t _{rA} output rise time	A port rise time	Push-pull	19.5	12.8	6.3	ns
		Open-drain	171.2	105.9	77.1	
t _{rB} output rise time	B port rise time	Push-pull	18.2	13.6	12.4	ns
		Open-drain	164.7	79.1	41.2	
t _{fA} output fall time	A port fall time	Push-pull	4.3	4.9	7.4	ns
		Open-drain	1.4	2.4	1.7	
t _{fB} output fall time	B port fall time	Push-pull	7.7	10.3	13.9	ns
		Open-drain	3.3	5.3	8.2	
t _{SK} Skew time output	Channel to channel skew		0.1	0.1	0.1	ns

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), V_{CCA}=1.8V.

PARAMETER	TEST CONDITION		V _{CCB} =1.8V	V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	TYP	
t _{PHL} (NOTE2)	A to B	Push-pull	3.7	2.7	3.1	ns
		Open-drain	1.2	1.3	1.9	
t _{PLH} (NOTE2)	A to B	Push-pull	5.2	5.2	5	ns
		Open-drain	1.4	4.4	6.4	
t _{PHL} (NOTE2)	B to A	Push-pull	3.7	4.2	5.1	ns
		Open-drain	1.6	2.2	3	
t _{PLH} (NOTE2)	B to A	Push-pull	-0.7	-1.5	-2.3	ns
		Open-drain	-5.3	-5.5	7.5	
t _{en} Enable time	OE to A or B		28.2	20	13.4	ns
t _{dis} disable time	OE to A or B		83.5	72.9	67.9	ns
t _{rA} output rise time	A port rise time	Push-pull	9.5	8.5	7.1	ns
		Open-drain	112.5	88.5	59.7	
t _{rB} output rise time	B port rise time	Push-pull	10.6	8.9	7	ns
		Open-drain	104.1	73.5	34.1	
t _{fA} output fall time	A port fall time	Push-pull	5	4.3	5.4	ns
		Open-drain	1.4	4.2	6.1	
t _{fB} output fall time	B port fall time	Push-pull	7.2	8.1	8.8	ns
		Open-drain	1.1	1.6	2.7	
t _{SK} Skew time output	Channel to channel skew		0.1	0.1	0.1	ns

Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), V_{CCA}=2.5V

PARAMETER	TEST CONDITION		V _{CCB} =2.5V	V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	TYP	
t _{PHL} (NOTE2)	A to B	Push-pull	4.3	0.7	0.6	ns
		Open-drain	1.3	1.1	1.4	
t _{PLH} (NOTE2)	A to B	Push-pull	0.3	1.9	3.2	ns
		Open-drain	0.1	0.2	0.23	
t _{PHL} (NOTE2)	B to A	Push-pull	3.5	3.2	4.3	ns
		Open-drain	1.6	1.9	2.7	
t _{PLH} (NOTE2)	B to A	Push-pull	0.7	-0.6	-1.9	ns
		Open-drain	-0.1	-0.2	-0.3	
t _{en} Enable time	OE to A or B		33.1	24.2	23.4	ns

PARAMETER	TEST CONDITION		V _{CCB} =2.5V	V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	TYP	
t _{dis} disable time	OE to A or B		90.6	85.9	87.1	ns
t _{rA} output rise time	A port rise time	Push-pull	8.7	7.6	6.4	ns
		Open-drain	111.2	89.8	62.4	
t _{rB} output rise time	B port rise time	Push-pull	9.1	7.9	6.1	ns
		Open-drain	121.1	90.6	43.6	
t _{fA} output fall time	A port fall time	Push-pull	5.6	5.3	4.4	ns
		Open-drain	1.7	2	1.8	
t _{fB} output fall time	B port fall time	Push-pull	6.3	6.9	8.1	ns
		Open-drain	1.6	1.5	2.7	
t _{SK} Skew time output	Channel to channel skew		0.3	0.2	0.3	ns

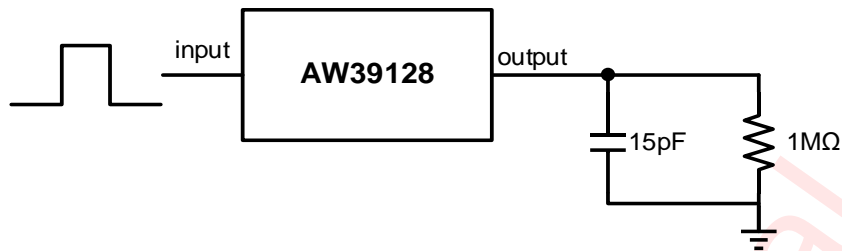
Output load: C_L=15pF, T_A=25°C for typical values (unless otherwise noted), V_{CCA}=3.3V

PARAMETER	TEST CONDITION		V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	
t _{PHL} (NOTE2)	A to B	Push-pull	3.2	-0.9	ns
		Open-drain	1.2	1.2	
t _{PLH} (NOTE2)	A to B	Push-pull	0.3	2.2	ns
		Open-drain	-0.1	0.2	
t _{PHL} (NOTE2)	B to A	Push-pull	2.7	3.5	ns
		Open-drain	1.7	4	
t _{PLH} (NOTE2)	B to A	Push-pull	0.6	-1.3	ns
		Open-drain	0.01	-0.2	
t _{en} Enable time	OE to A or B		17.5	11.2	ns
t _{dis} disable time	OE to A or B		71.1	67.9	ns
t _{rA} output rise time	A port rise time	Push-pull	6.9	5.7	ns
		Open-drain	92.9	63.7	
t _{rB} output rise time	B port rise time	Push-pull	7.6	6.1	ns
		Open-drain	100.2	54.3	
t _{fA} output fall time	A port fall time	Push-pull	5.8	4.8	ns
		Open-drain	2.1	1.9	
t _{fB} output fall time	B port fall time	Push-pull	6.2	7.3	ns
		Open-drain	1.8	2.5	
t _{SK} Skew time output	Channel to channel skew		0.1	0.2	ns

NOTE2: t_{PHL} presents propagation delay from high to low, and t_{PLH} presents propagation delay from low to high.

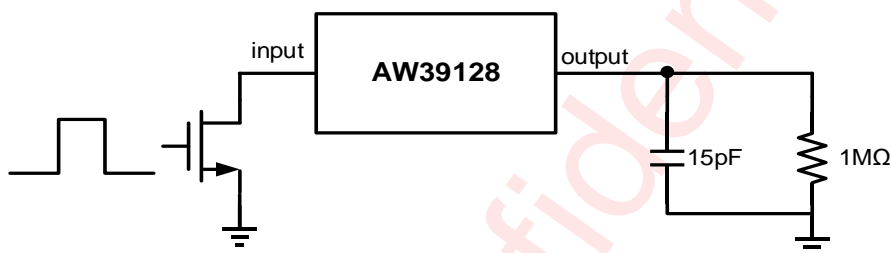
Typical Characteristics

TEST INFORMATION



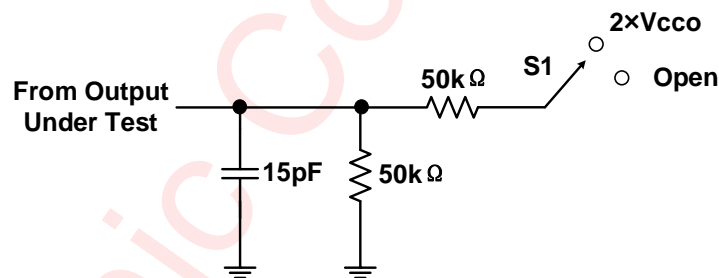
Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

Figure 5 Load Circuit of Push-Pull Driver



Test Circuit for Date Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

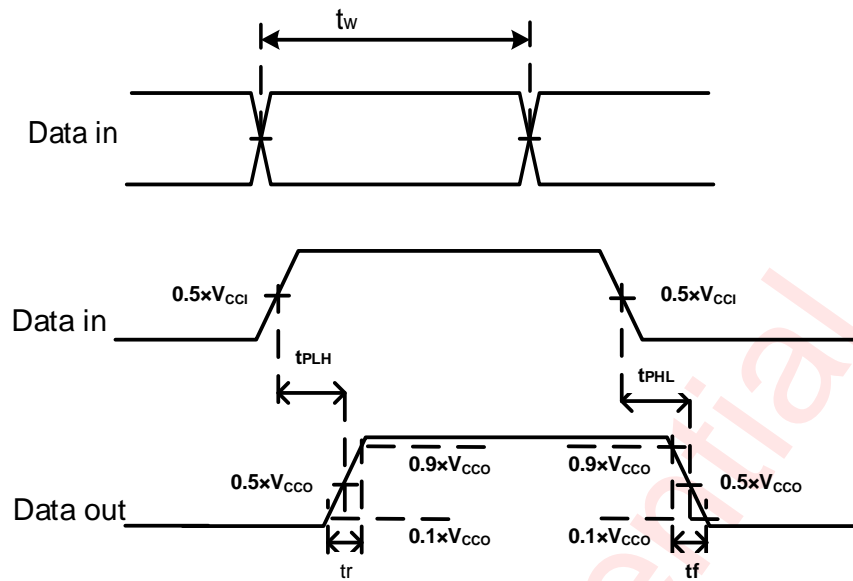
Figure 6 Load Circuit of Open-Drain Driver



TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open

1. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
2. t_{PZL} and t_{PZH} are the same as t_{en} .
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.
5. The resistance and Capacitance values at output notes above are the total effective values.

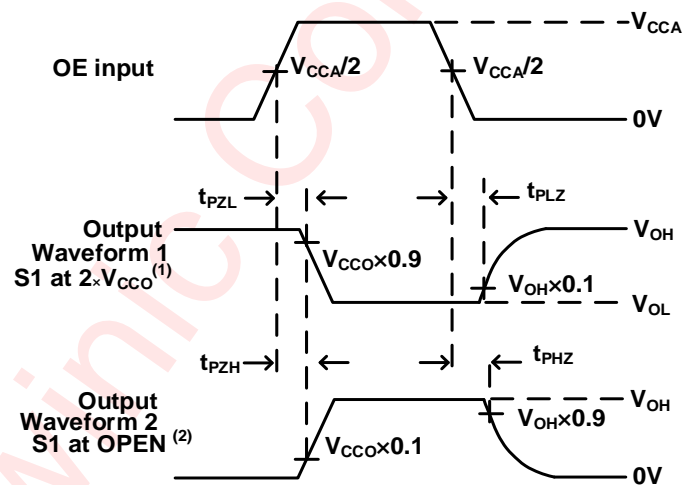
Figure 7 Load Circuit for Enable-Time and Disable-Time Measurement



The input pulses should have the following characteristics:

1. $f_{IN} \leq 10\text{MHz}$.
2. $dv/dt \geq 1\text{V/ns}$.

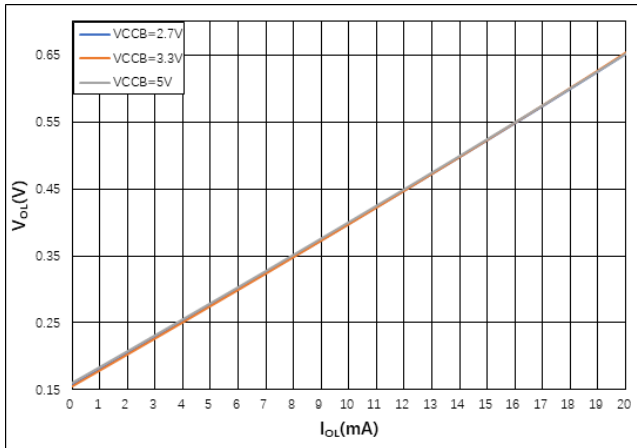
Figure 8 Timing Parameter Definition



1. The Waveform 1 is obtained under the condition that the input is low and S1 at $2 \times V_{CCO}$.
2. The Waveform 2 is obtained under the condition that the input and S1 at OPEN.

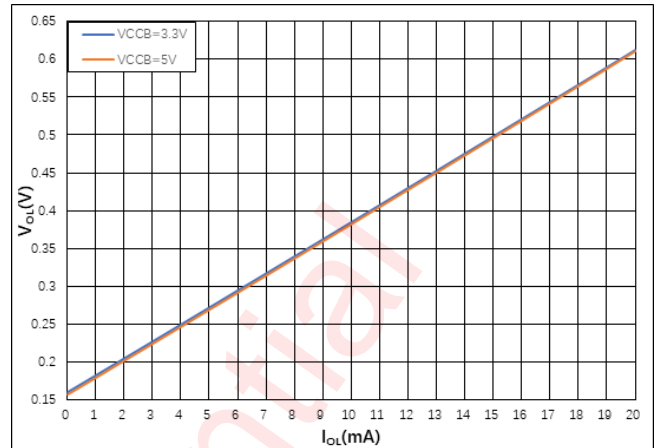
Figure 9 Enable and Disable Times

TYPICAL CURVE $T_A=25^\circ\text{C}$



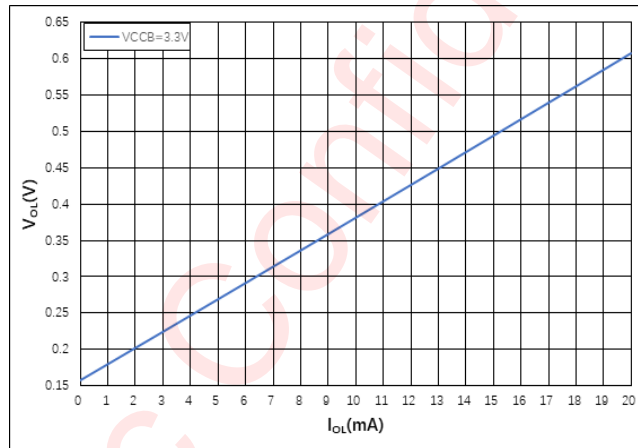
$V_{CCA}=1.8\text{V}$, $OE=V_{CCA}$, $V_{ILA}=0.15\text{V}$

Figure 10 Low-Level Output Voltage vs Low-Level Current



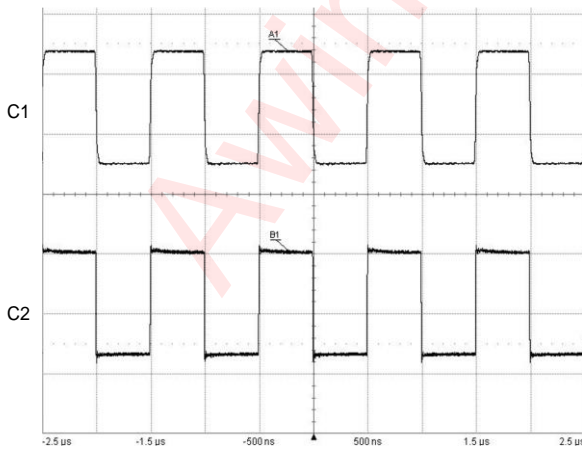
$V_{CCA}=2.7\text{V}$, $OE=V_{CCA}$, $V_{ILA}=0.15\text{V}$

Figure 11 Low-Level Output Voltage vs Low-Level Current



$V_{CCA}=3.3\text{V}$, $OE=V_{CCA}$, $V_{ILA}=0.15\text{V}$

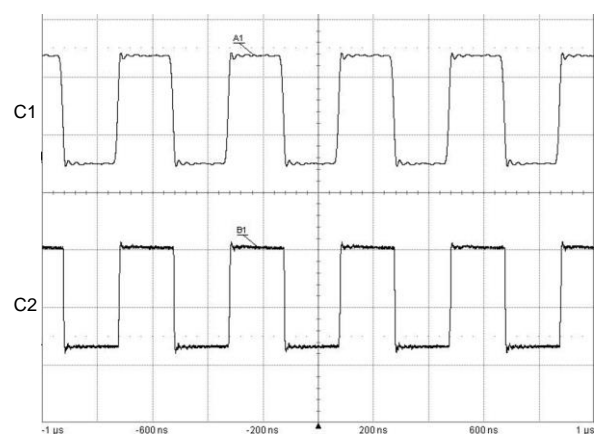
Figure 12 Low-Level Output Voltage vs Low-Level Current



C1: 1.00V/div C2: 2.00V/div

$V_{CCA}=1.8\text{V}$, $V_{CCB}=3.3\text{V}$, $OE=V_{CCA}$, Push-Pull Driver
Signal is translated from A port to B port

Figure 13 Level Translation of a 1MHz Signal



C1: 1.00V/div C2: 2.00V/div

$V_{CCA}=1.8\text{V}$, $V_{CCB}=3.3\text{V}$, $OE=V_{CCA}$, Push-Pull Driver
Signal is translated from A port to B port

Figure 14 Level Translation of a 2.5MHz Signal

Detailed Functional Description

AW39128 is a 8-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. Port A can support I/O voltages from 1.1 V to 3.6 V, while Port B is able to support I/O voltage range from 1.65 V to 5.5 V. The chip uses a transmission gate architecture with an rising edge rate accelerator (one-shot), to increase overall data rate. Also, 10k Ω pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

ONE-SHOT ACCELERATOR

The One-Shot rising edge accelerator circuit speeds up the rising edge to help increasing the chip's data rate. Once the chip has detected the rising edge of the input signal from low to high, the one-shot circuit generates a pulse signal of approximately 30ns, which enables the internal pull-up PMOS transistor between power supply and output, thereby accelerating the output port from low to high. During this acceleration phase, the output resistance of the driver is reduced from 10k Ω to approximately 60 Ω . While detecting the output has been turned up, the one-shot pulse signal is finished and pull-up PMOS transistor is quickly turned off. This architecture reduces the average dynamic power consumption of the chip while allowing it to meet different drive requirements.

GATE BIAS

For the bidirectional voltage translator AW39128, a NMOS switch transistor is used between the input and output. When translating high level, the NMOS transistor is turned off, and the input and output terminals are isolated so that they do not impact each other. When the low level is translated, the NMOS switch transistor is fully turned on, so that the output terminal can be quickly pulled down to the low voltage level. Therefore, the gate bias voltage of the NMOS switch transistor is set to a fixed value about $V_{CCA} + V_{TH}$. It is also because of this architecture that $V_{CCA} \leq V_{CCB}$ needs to be guaranteed in the applications.

ENABLE CONTROL

The AW39128's OE pin can disable the chip by setting OE to low voltage level, allowing all I/O to be pulled to the supply voltage through a 5M Ω internal pull-up resistor. The disable time (t_{dis}) represents the delay time from OE going low to the chip turns to OFF-state. And the enable time (t_{en}) indicates the delay from OE going high to the chip working in translation state. Meanwhile, OE is recommended to be tied to GND through an external pull-down resistor to ensure the ultra-low power-supply quiescent current. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

INPUT DRIVER

The rising edge time of the signal (t_{rA} , t_{rB}) and propagation delay from low to high (t_{PLH}) are determined by the rising edge rate of the input signal, the ONE-SHOT accelerator's pull-up capability, and the capacitive load of the port. The falling edge time of the signal (t_{fA} , t_{fB}) depends on the falling edge rate of the input signal, the output impedance of the external driver, and the capacitive load on the data line. Similarly, t_{PHL} and the maximum data rate also depend on the output impedance of the external driver. So, the test conditions for t_{rA} , t_{rB} , t_{fA} , t_{fB} , t_{PLH} , t_{PHL} and maximum data rate in the data sheet are that the output impedance of the external driver is less than 50 Ω .

OUTPUT LOAD

It is recommended that a PCB layout with short PCB layout length:

1. Avoid excessive capacitive load triggers ONE-SHOT circuit falsely;

2. It can ensure that the round trip delay of any reflection is less than a single ONE-SHOT duration;
3. Improve signal integrity.

Meanwhile, the pulse width of the ONE-SHOT circuit is approximately 30 ns, which determines the maximum output load capacitance that the chip can drive. For very heavy output capacitive loads, the one-shot accelerator will time-out before the output is fully pulled to high level, at which case the signal transmission will be distorted. So the ONE-SHOT duration design requires a trade-off between dynamic power consumption, capacitive load driving capability and maximum data rate. The signal t_w at the maximum translation rate should be greater than the maximum pulse width of the ONE-SHOT circuit, and the delay caused by the output capacitive load should be less than the maximum pulse width of the ONE-SHOT circuit.

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Application Information

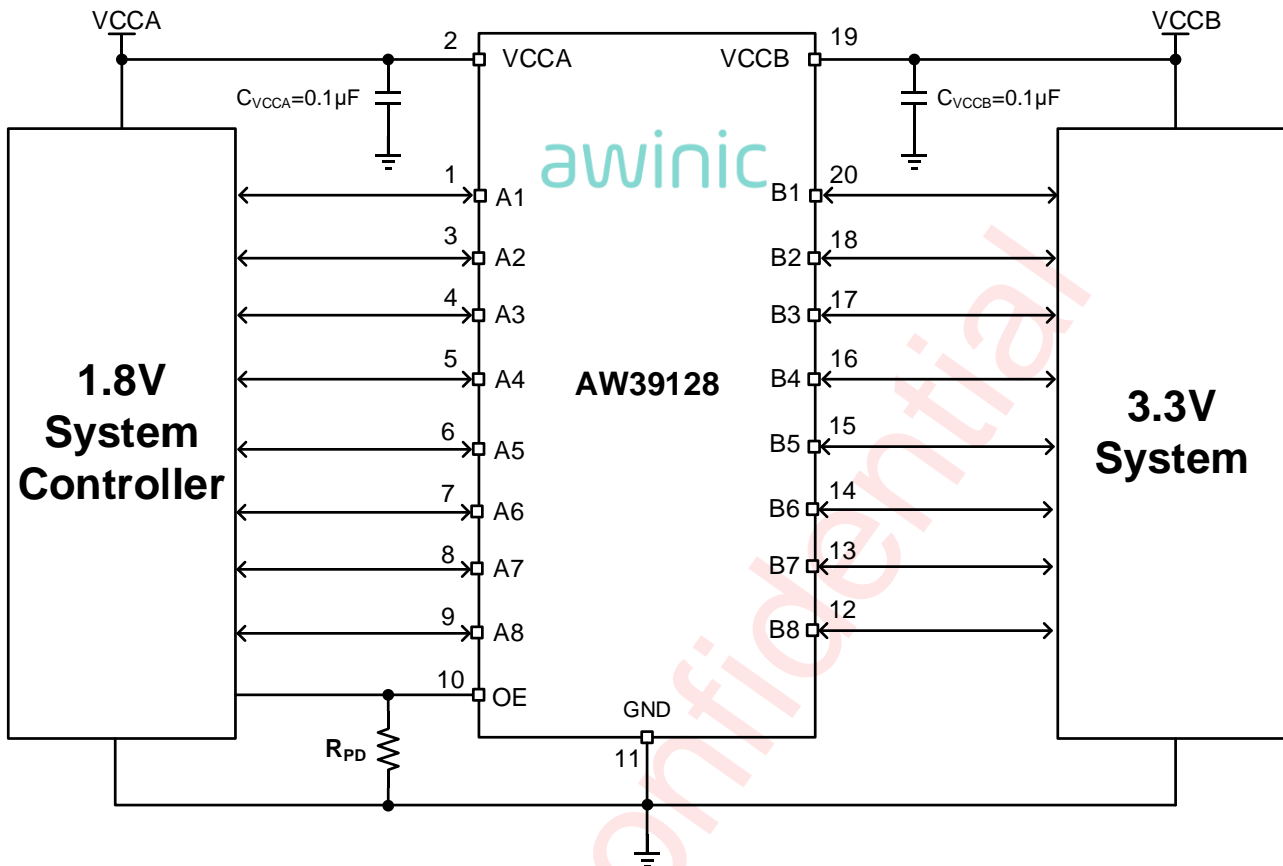


Figure 15 AW39128 Application Circuit

AW39128 is a 8-bit voltage-level translator without direction control signal, which is suitable for interfacing devices or systems operating at different interface voltages with one another. Port A can support I/O voltages from 1.1 V to 3.6 V, while Port B is able to support I/O voltage range from 1.65 V to 5.5 V. Also, 10kΩ pull-up resistors are integrated in the chip, which ensures the chip not only supports push-pull applications but also can be used in open-drain applications directly.

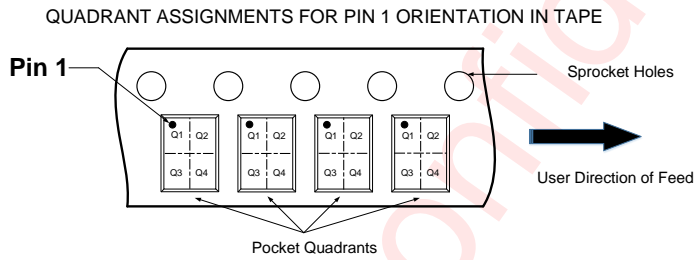
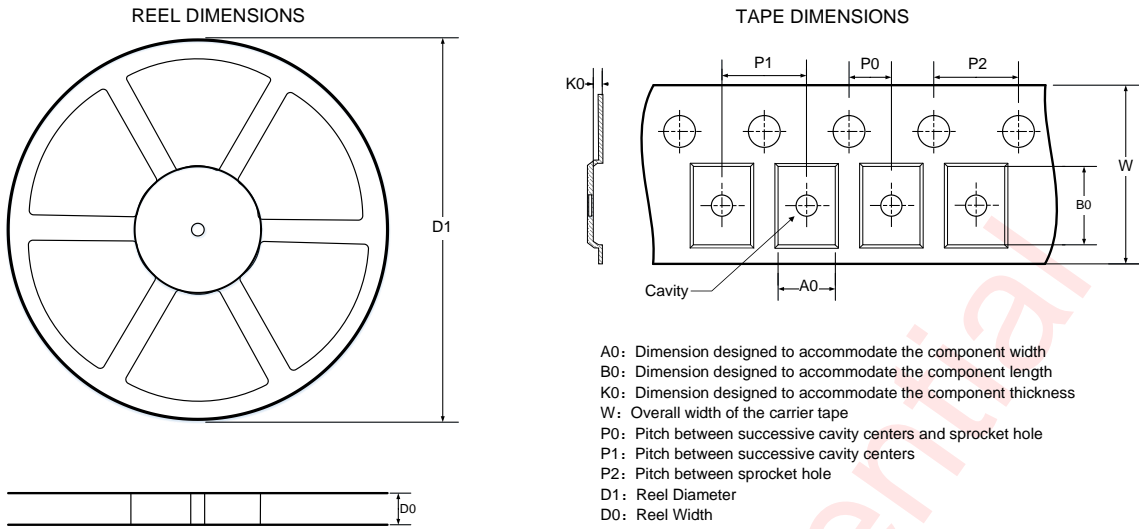
VCC CAPACITOR SELECTION

The device is a 8-bit high-performance voltage-level translator that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, recommend 0.1µF or larger than 0.1µF.

R_{PD} SELECTION

Drive OE pin HIGH to enable the device. If the voltage level of OE pin is low, all I/O are pulled to the supply voltage through a 5MΩ internal pull-up resistor. OE is recommended to be tied to GND through an external pull-down resistor to ensure the ultra-low power-supply quiescent current. OE pin is high impedance without internal pull down resistor, customer can choose the resistor value based on the source drive capability and current consumption.

Tape And Reel Information



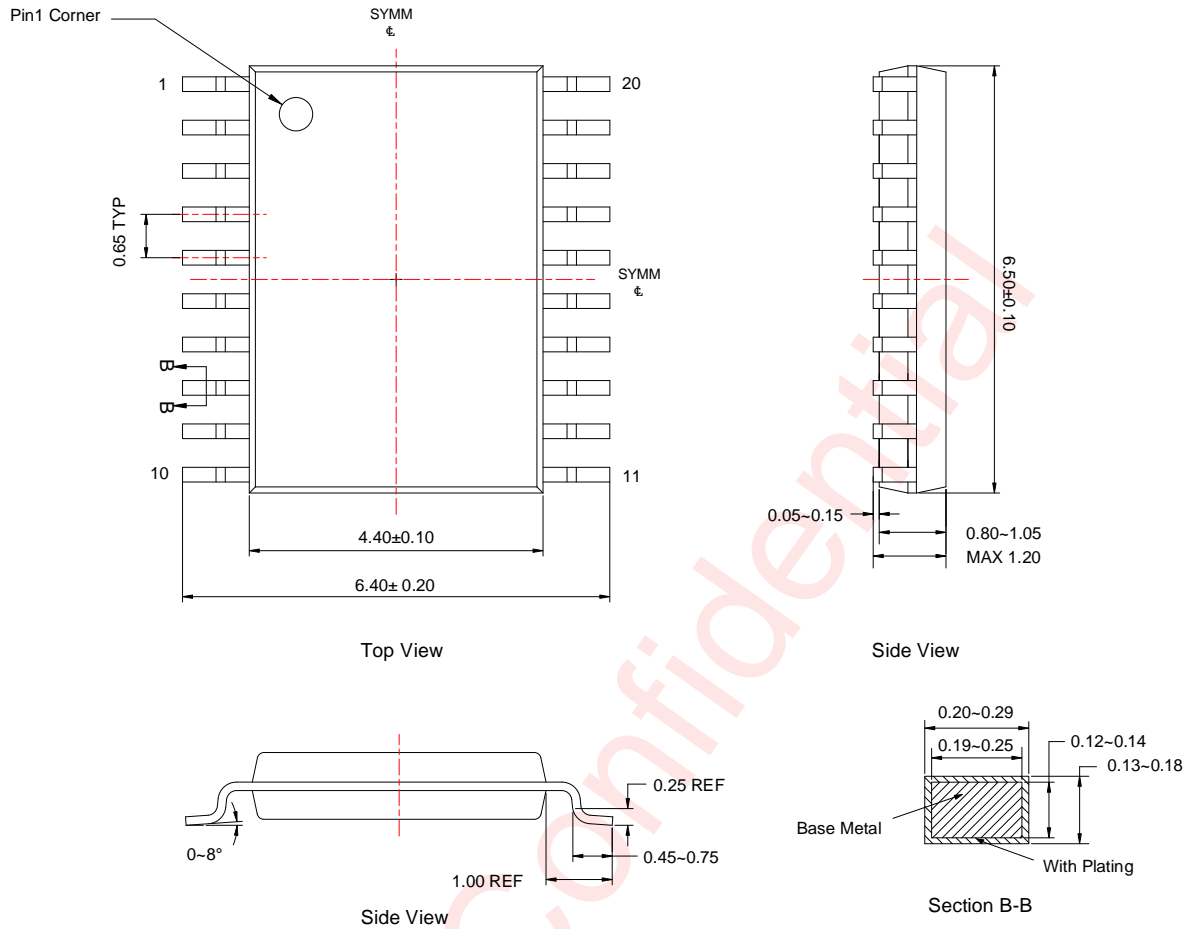
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	16.4	6.8	6.9	1.5	2	8	4	16	Q1

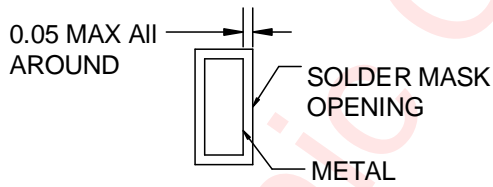
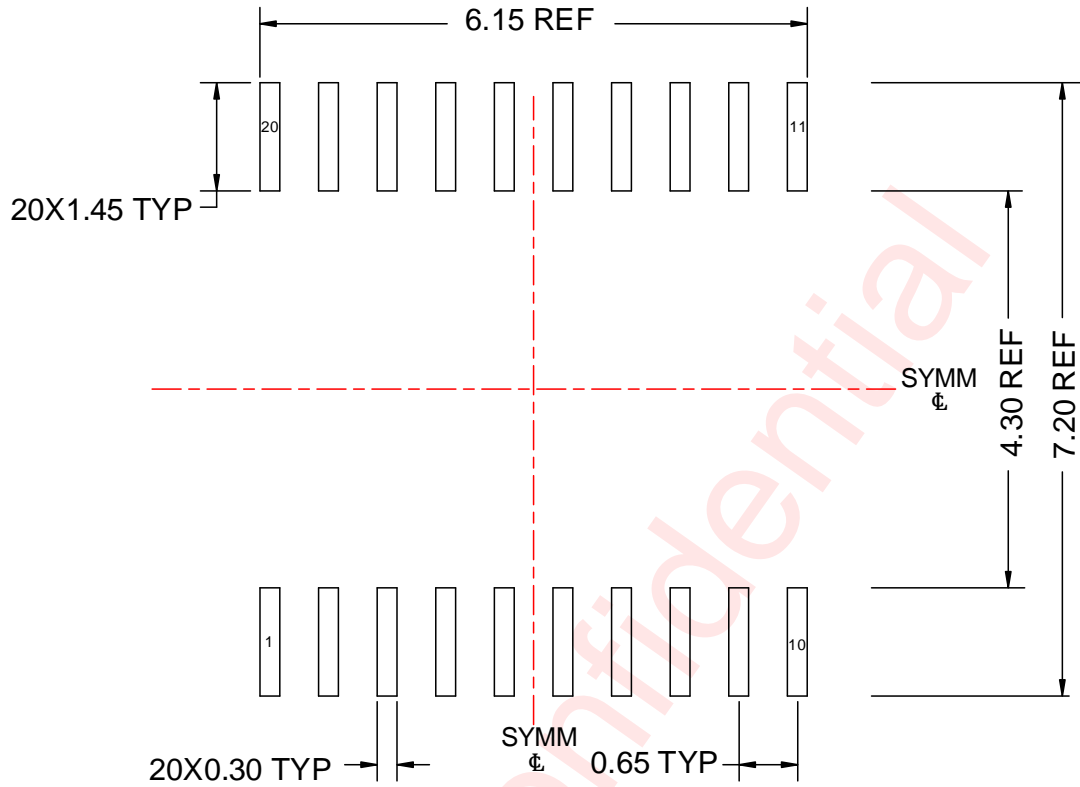
All dimensions are nominal

Package Description

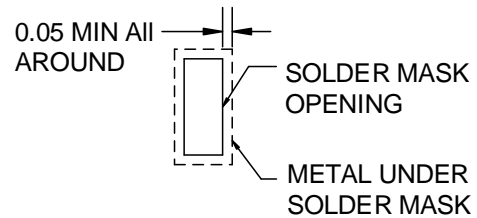


Unit: mm

Land Pattern Data



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2023	Officially released
V1.1	Apr. 2025	Update Land Pattern Data. (P20)

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