36V, 0.9MHz, General Purpose Op Amps

Features

- Supply Voltage: 3V(±1.5V) to 36V(±18V)
- Supply Current: 110μA per channel
- Differential Input Voltage Range to Supply Rail
- Input Rail to V-, Output Rail to Rail
- Bandwidth:0.9MHz
- Slew Rate:0.5V/μs
- Offset Voltage:±3mV Maximum
- 6KV HBM, 1.5KV CDM, ±200mA Latch Up
- -40°C to 125°C Operation Temperature Range

Applications

- Sensor Interface
- Motor Control
- Power Module
- Audio

General Description

The AWS72904 is high supply voltage amplifier with low offset, low power and stable frequency response. It incorporates AWINIC's proprietary and patented design techniques to achieve very good AC performance with 0.9MHz bandwidth,0.5V/μs slew rate and low distortion.

The input common-mode voltage range extends to V-, and the outputs swing rail-to-rail. The AWS72904 can be used as plug-in replacements for many commercially available op amps to reduce power and improve input/output range and performance.

The combination of features makes the AWS72904 ideal choices for Sensor Interface, industrial control, motor control and audio application.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS72904	MSOP - 8L	3.0mm ×3.0mm
AWS72904	SOP-8L	3.9mm × 4.9mm

Typical Application Circuit

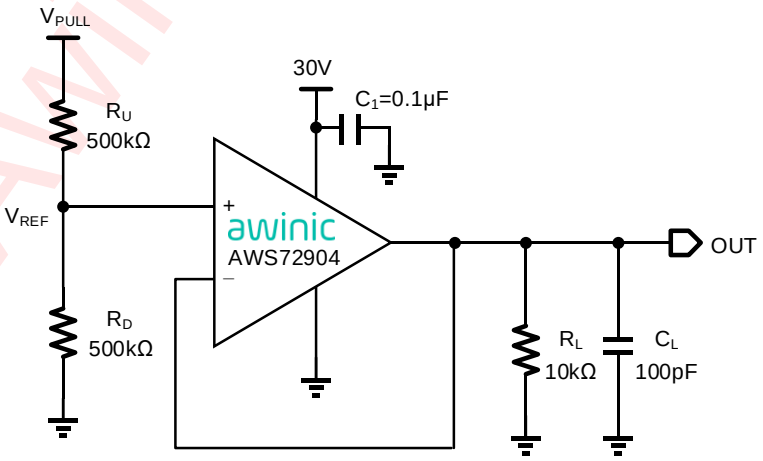
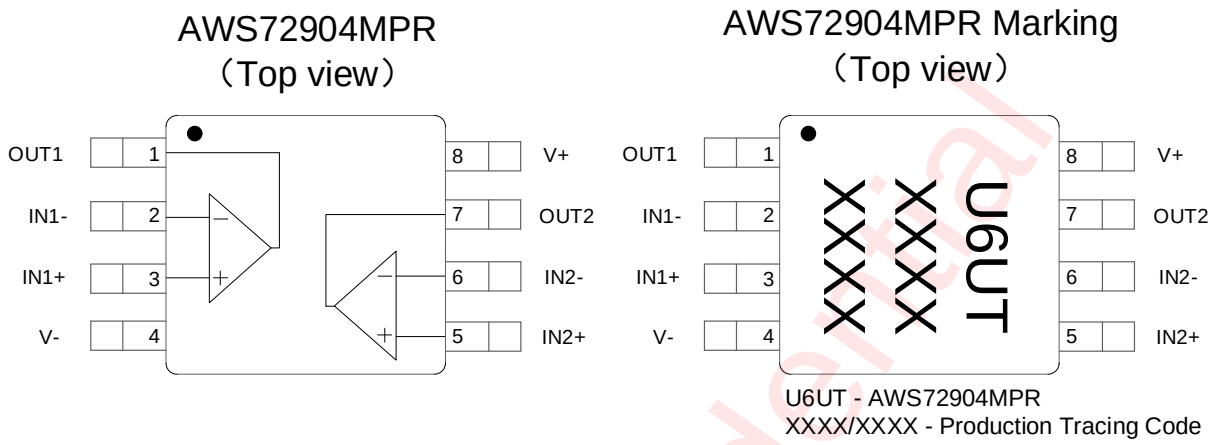


Figure 1 Typical Application of AWS72904

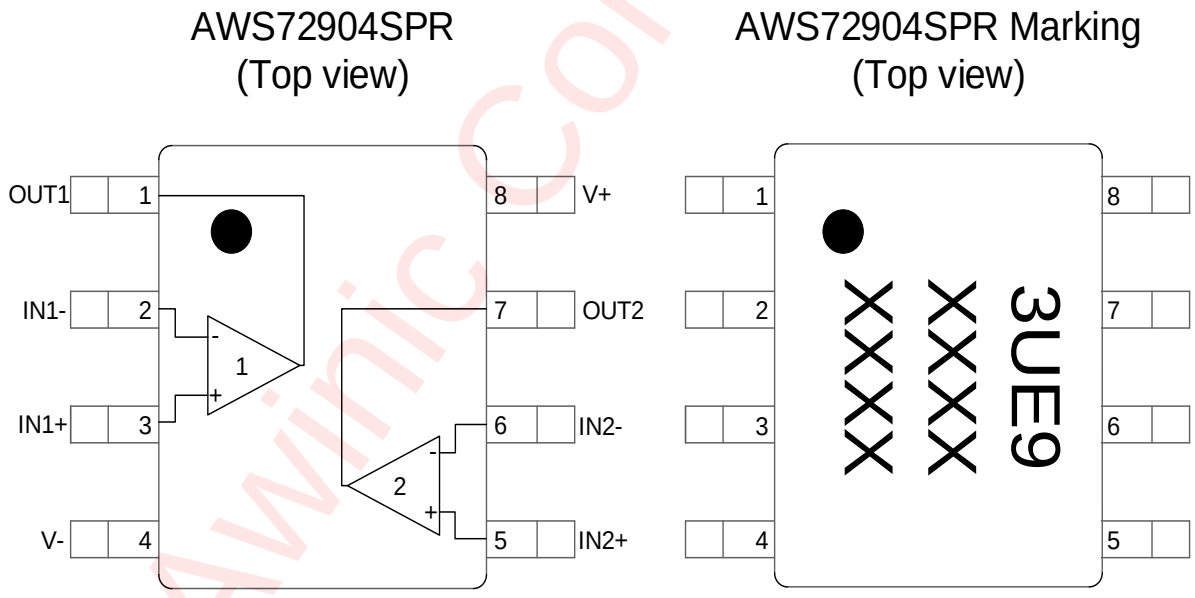
Pin Configuration And Top Mark

MSOP - 8L



U6UT - AWS72904MPR
XXXX/XXXX - Production Tracing Code

SOP-8L



3UE9 - AWS72904SPR
XXXX/XXXX - Production Tracing Code

Figure 2 Pin Configuration

Pin Definition

No.	NAME	DESCRIPTION
1	OUT1	Channel 1 output
2	IN1-	Channel 1 inverting input
3	IN1+	Channel 1 noninverting input
4	V-	Negative (low) supply or ground (for single-supply operation)
5	IN2+	Channel 2 noninverting input
6	IN2-	Channel 2 inverting input
7	OUT2	Channel 2 output
8	V+	Positive (high) supply

Functional Block Diagram

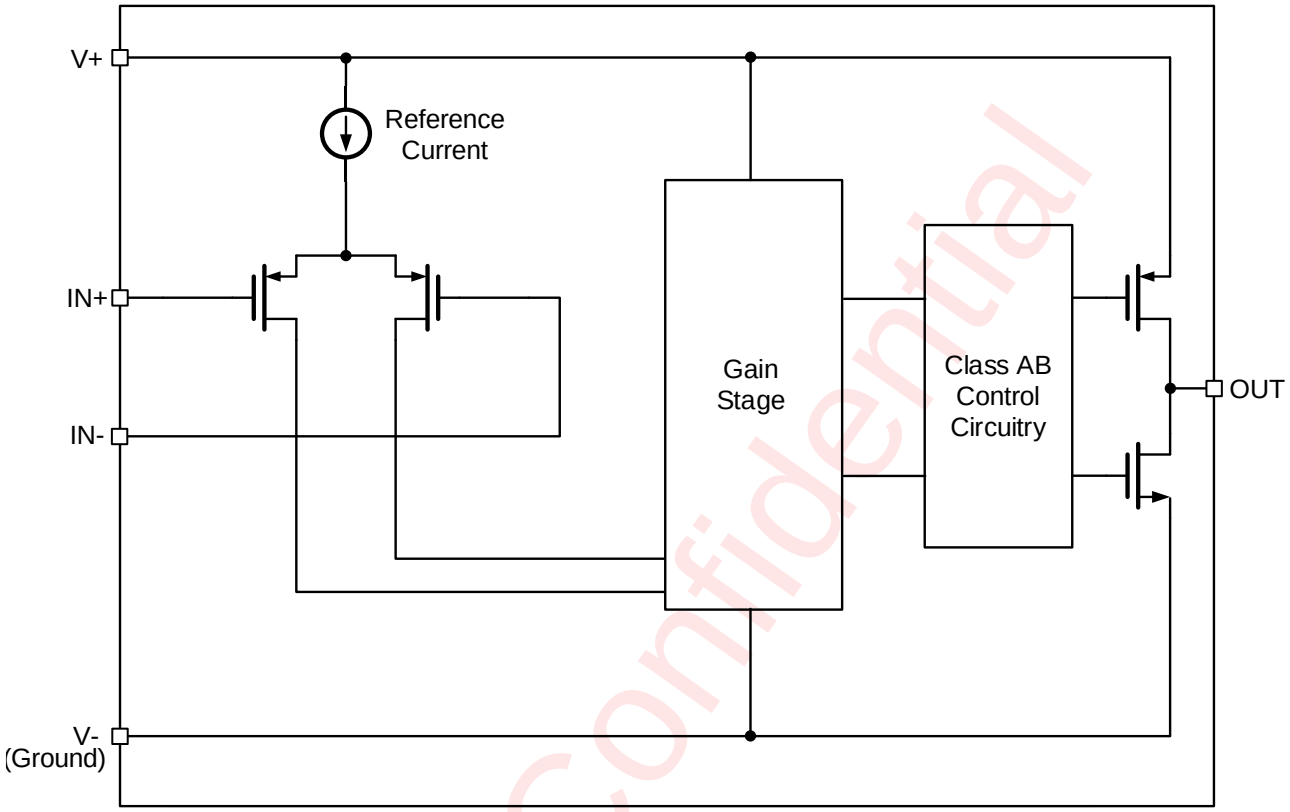


Figure 3 Functional Block Diagram

Typical Application Circuits

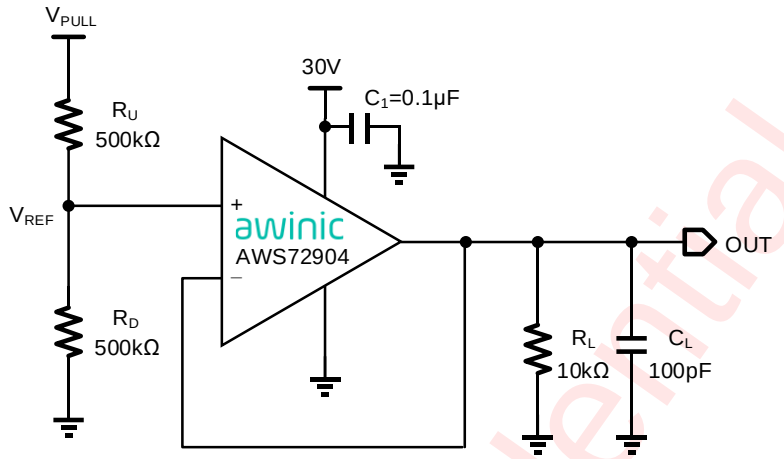


Figure 4 AWS72904 Application Circuit

- ***Notice for typical application circuits:***

1. Bypass capacitors C_1 is used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS72904MPR	-40°C ~ 125°C	MSOP - 8L	U6UT	MSL3	RoHS+HF	3000 units/ Tape and Reel
AWS72904SPR	-40°C ~ 125°C	SOP - 8L	3UE9	MSL3	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage, V_S = (V+) - (V-)		-0.3V to 40V
Signal input pins	Common-mode voltage (NOTE 2)	(V-) - 0.3V to (V+) + 0.3V
	Differential voltage (NOTE 2)	($+V_S$)- ($-V_S$)
	Current (NOTE 2)	-10mA to 10mA
Output short-circuit (NOTE 3)		Continuous
Operating free-air temperature range T_A		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *Input pins are diode-clamped to each power supply. Input signals that may extend more than 0.5V beyond the supply rails must be current limited to 10mA or less.*

NOTE3: *A heat sink may be required to keep the junction temperature below the absolute maximum.*

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 4)	±6	kV
CDM (NOTE 5)	±1.5	kV
Latch-Up (NOTE 6)	+IT: 200 -IT: -200	mA

NOTE4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023*

NOTE5: Test method: ESDA/JEDEC JS-002-2022

NOTE6: Test method: JESD78F

Thermal Information

THERMAL METRICS		AWS72904		UNIT
SYMBOL	PARAMETER	MSOP-8L	SOP-8L	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.6	179.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	111.6	121.9	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	35.3	101.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.2	36.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	109.2	121.3	°C/W

Electrical Characteristics

All test condition is V_S =30V, T_A = 25°C, R_L = 10kΩ connected to V_S/2, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			3 (±1.5)		36 (±18)	V
I_Q	Quiescent current per channel	V_S = 30V, I_O = 0A			110	200	μA
			-40~125°C			250	μA
		V_S = 5V, I_O = 0A			85	150	μA
			-40~125°C			200	μA
PSRR	Power-supply rejection ratio	V_S =3V to 36V		85	128		dB
			-40~125°C	80			dB
INPUT CHARACTERISTICS							
V_{OS}	Input offset voltage	V_S = 30V, V_{CM}=0V to 28V		-3	0.1	3	mV
		V_S = 30V, V_{CM}=28.5V		-3	0.1	3	mV
		V_S = 5V, V_{CM}=2.5V		-3	0.1	3	mV
V_{OS} TC	Input offset voltage Drift		-40~125°C		2.5		μV/°C
I_B	Input bias current				15		pA
			-40~125°C			1000	pA
I_{OS}	Input offset current				15		pA
C_{IN}	Input Capacitance	Differential Mode(1)			0.65		pF
		Common Mode			1		pF
Av	Open-loop Voltage Gain			95	110		dB
			-40~125°C	90			dB
V_{CMR}	Common-mode Input Voltage Range			(V-)		(V+) – 1.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 28V		75	118		dB
			-40~125°C	70			dB
OUTPUT CHARACTERISTICS							
V_{OH}	Output Swing from Positive Rail	R_L = 10kΩ to V_S/2			86	300	mV
			-40~125°C			700	mV

SYMBOL	PARAMETER	TEST CONDITION	T_A	MIN	TYP	MAX	UNIT
		R_L = 2kΩ to V_S/2			420	1300	mV
			-40~125°C			2000	mV
V_{OL}	Output Swing from Negative Rail	R_L = 10kΩ to V_S/2			75	300	mV
			-40~125°C			700	mV
		R_L = 2kΩ to V_S/2			380	1300	mV
			-40~125°C			2000	mV
I_{SC}	Output Short-Circuit Current			20	28		mA
			-40~125°C	10			mA
AC SPECIFICATIONS							
GBW	Gain-bandwidth product				0.9		MHz
SR	Slew rate	G=1,10V step			0.5		V/μs
t_{OR}	Overload recovery time	V_{IN} × gain > V_S			3.5		μs
t_S	Settling Time, 0.1%	G = -1, 10V step			5.5		μs
	Settling time, 0.01%(1)				6.5		μs
PM	Phase margin	V_S = 36V, R_L=10K, C_L=100pF			75		°
NOISE PERFORMANCE							
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz			3		μV_{RMS}
e_N	Input Voltage Noise Density	f = 1kHz			70		nV/ √ Hz
THD+N	Total harmonic distortion + noise	f = 1kHz, G =1, R_L = 10kΩ, V_{OUT}= 6V_{RMS}			0.002		%

(1)The values are guaranteed by design.

Typical Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = 10kΩ, unless otherwise specified.

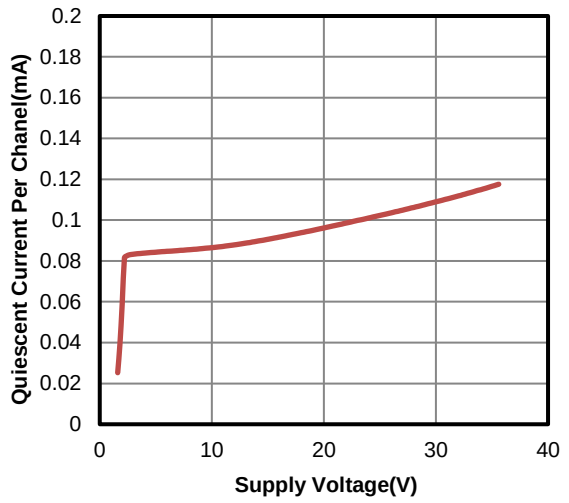


Figure 5 Quiescent Current vs. Supply Voltage

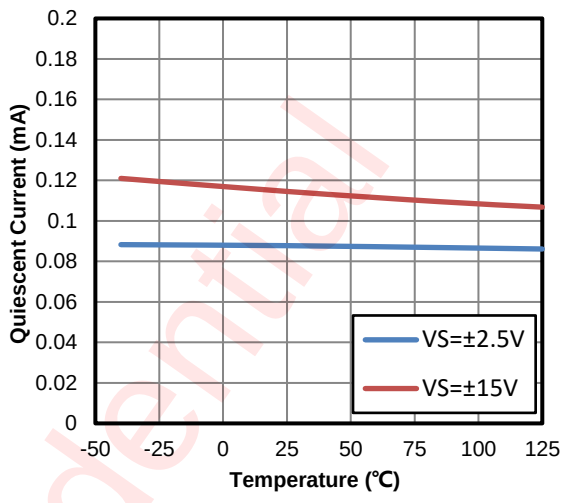


Figure 6 Quiescent Current vs. Temperature

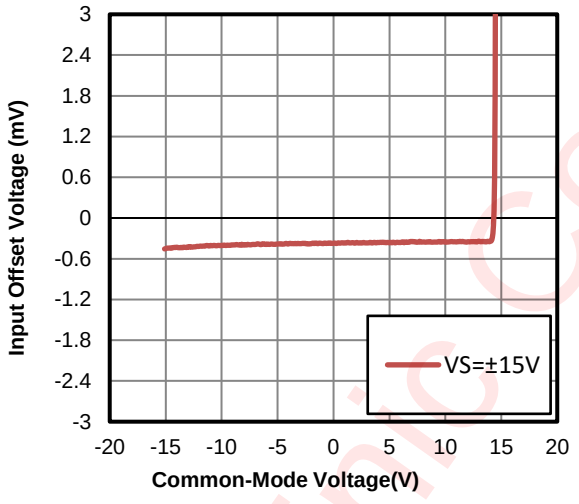


Figure 7 Input Offset Voltage vs. V_{CM}

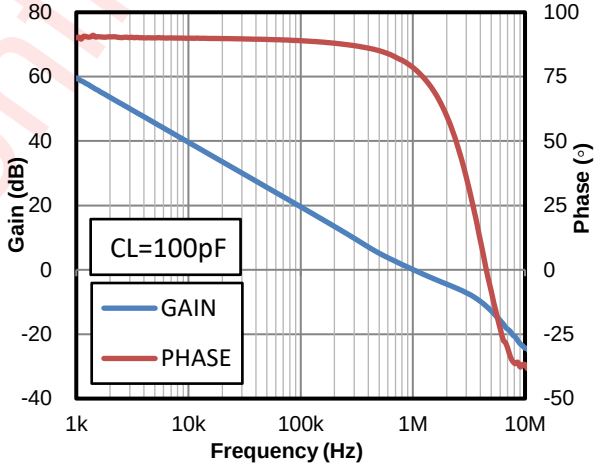


Figure 8 A_{OL} and Phase vs. Frequency

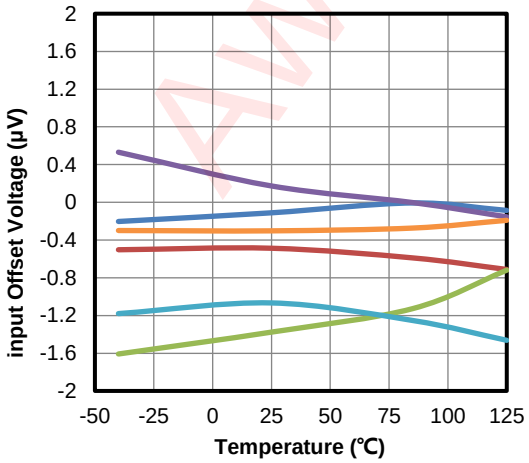


Figure 9 Offset Voltage vs. Temperature

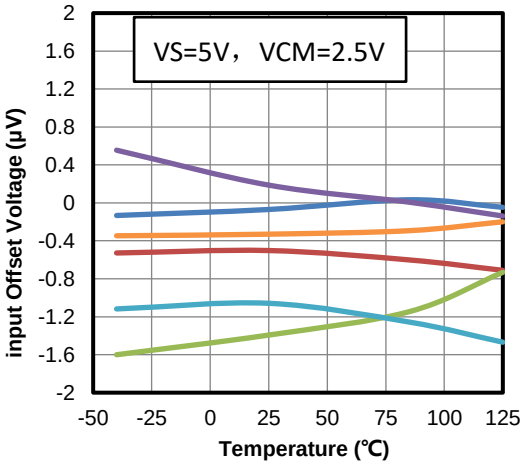


Figure 10 Offset Voltage vs. Temperature

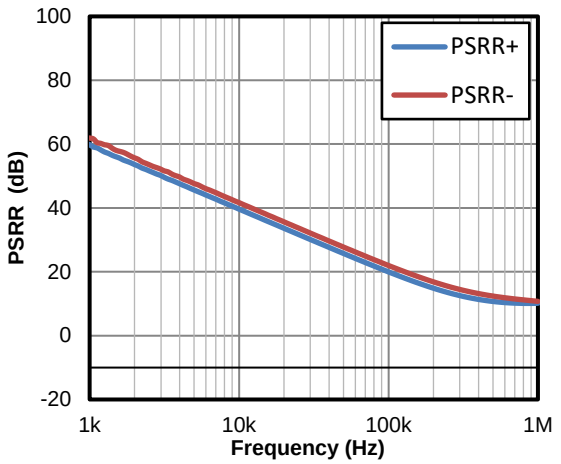


Figure 11 PSRR vs. Frequency

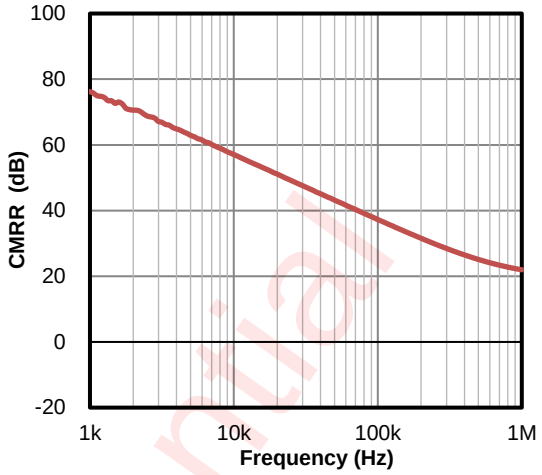


Figure 12 CMRR vs. Frequency

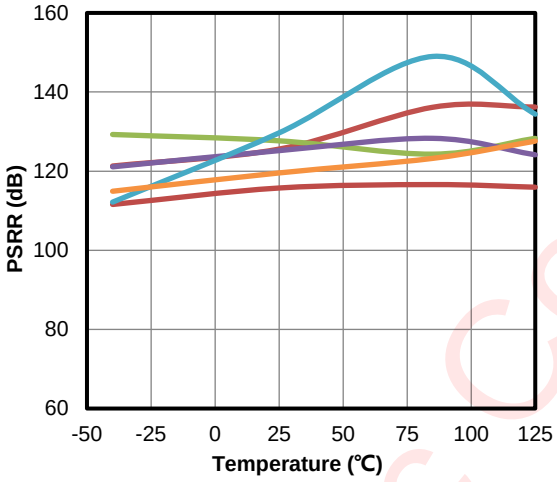


Figure 13 PSRR vs. Temperature

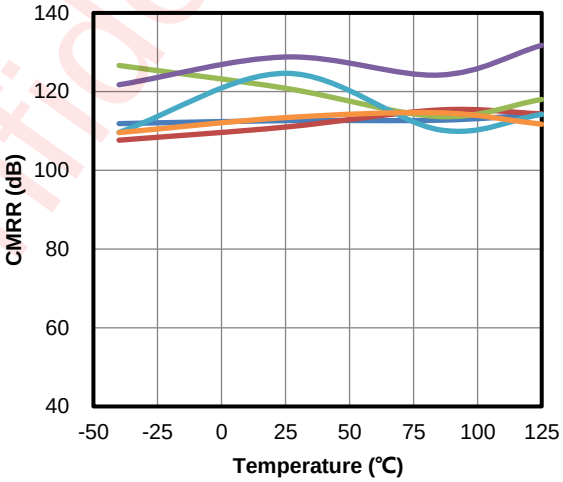


Figure 14 CMRR vs. Temperature

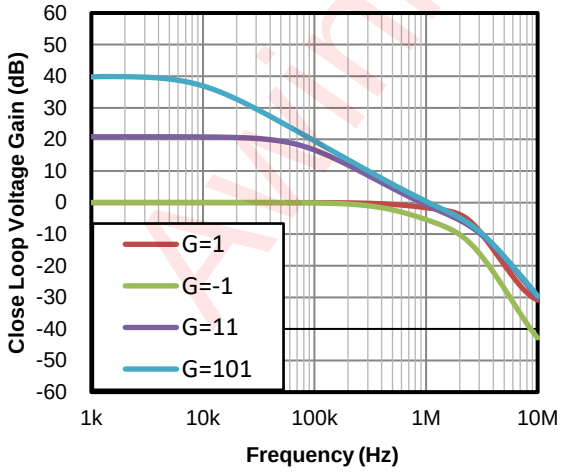


Figure 15 Close Loop Gain vs. Frequency

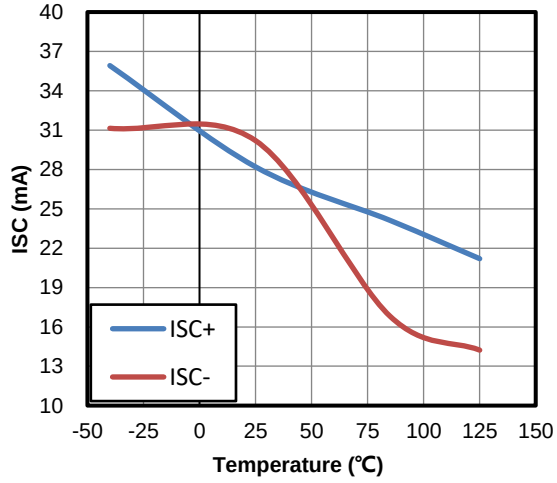


Figure 16 ISC vs. Temperature

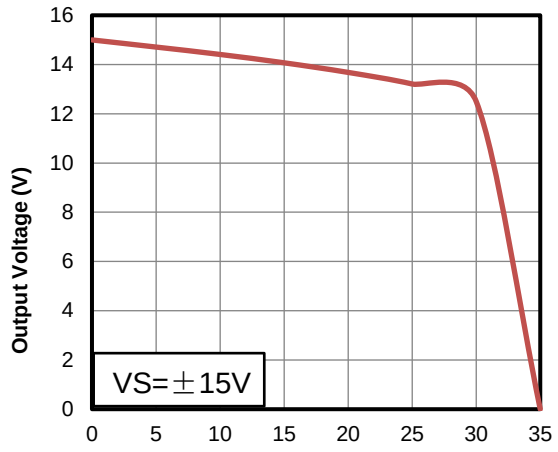


Figure 17 Output Voltage vs. Output Current

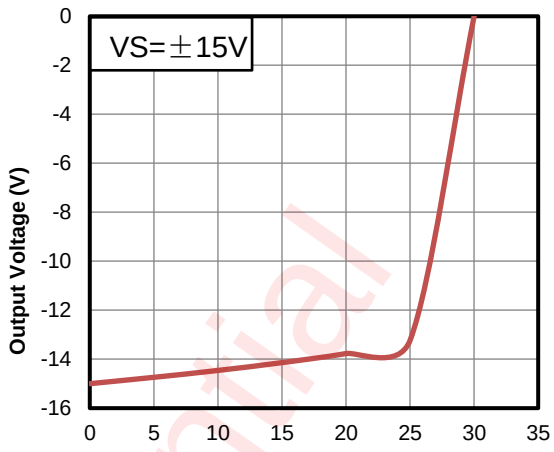


Figure 18 Output Voltage vs. Output Current

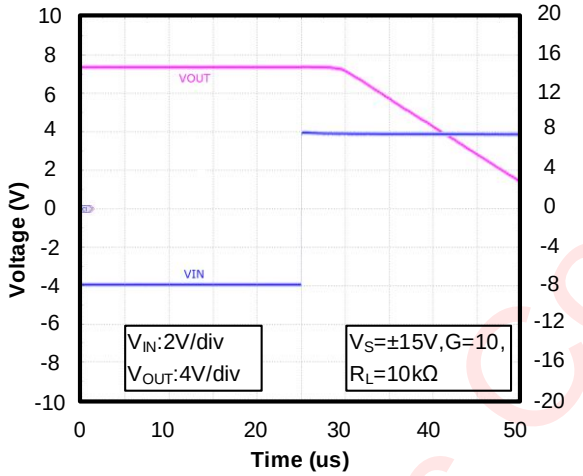


Figure 19 Positive Overload Recovery

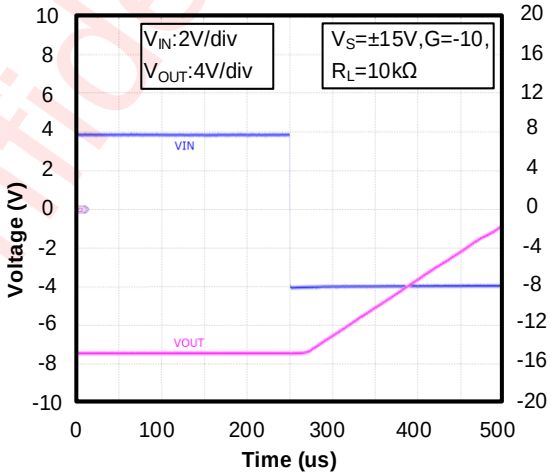


Figure 20 Negative Overload Recovery

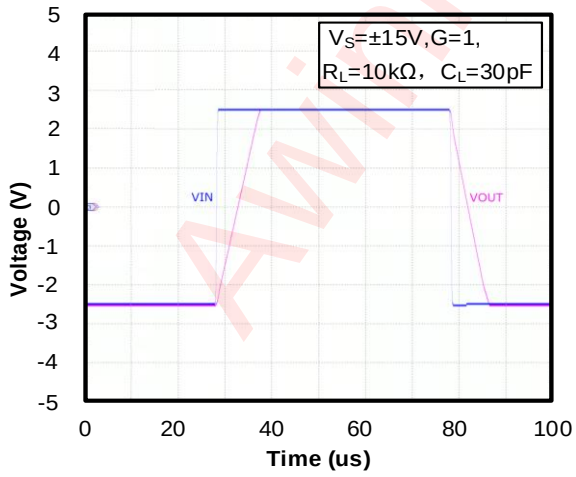


Figure 21 5V Signal Step Response

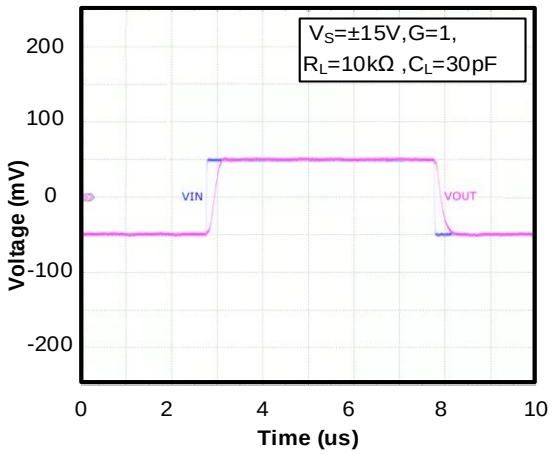


Figure 22 100mV Signal Step Response

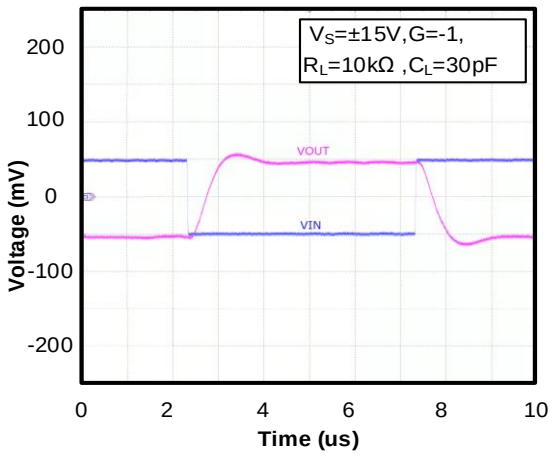


Figure 23 100mV Signal Step Response

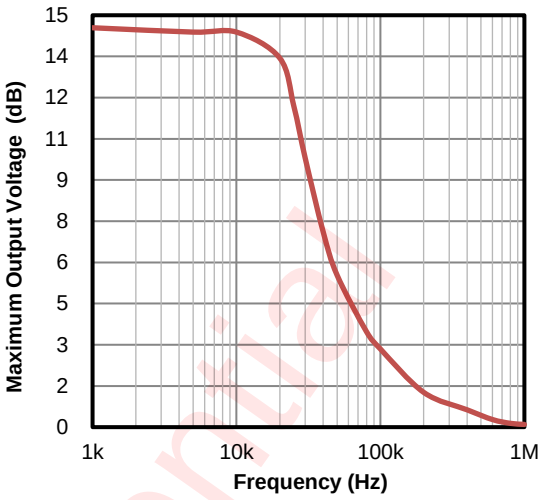


Figure 24 Maximum VOUT vs. Frequency

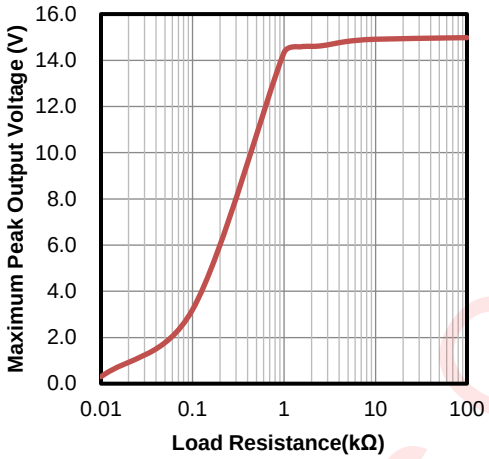


Figure 25 Maximum Output Voltage vs. Load Resistance

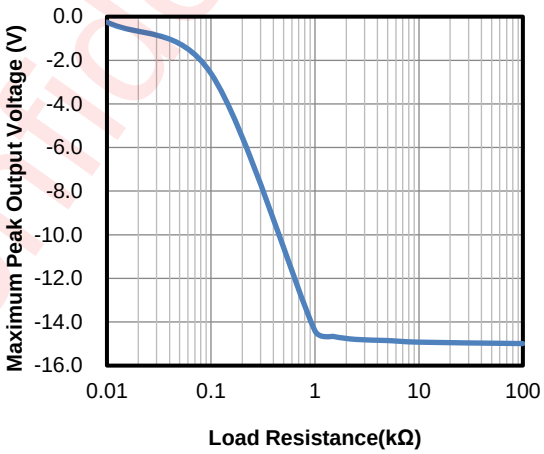


Figure 26 Maximum Peak Output Voltage vs. Load Resistance

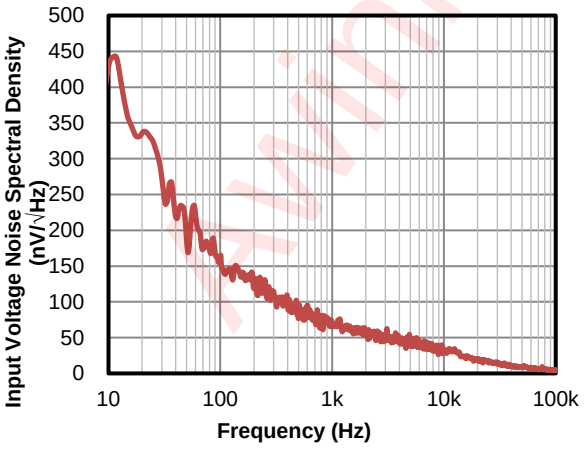


Figure 27 Voltage Noise Spectral Density vs. Frequency

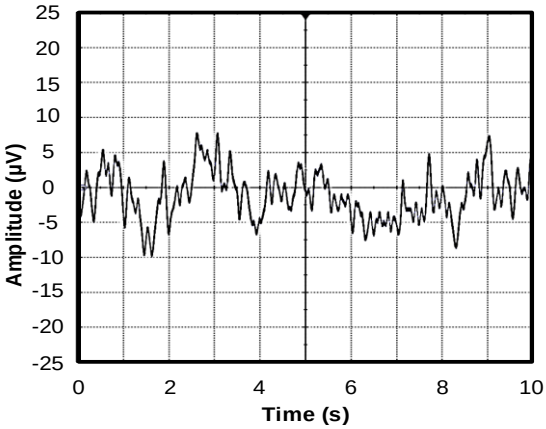


Figure 28 0.1-Hz to 10-Hz Integrated Voltage Noise

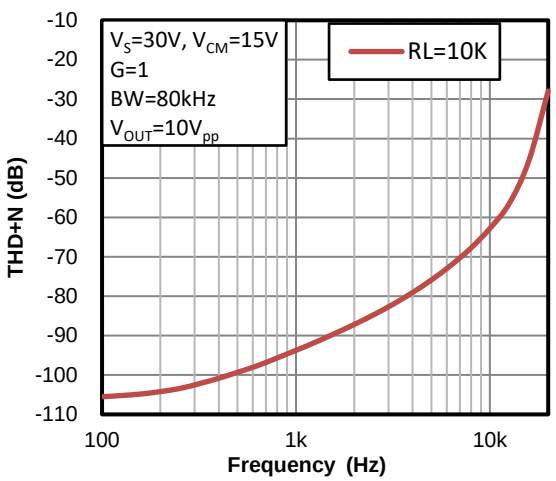


Figure 29 THD + N vs. Frequency

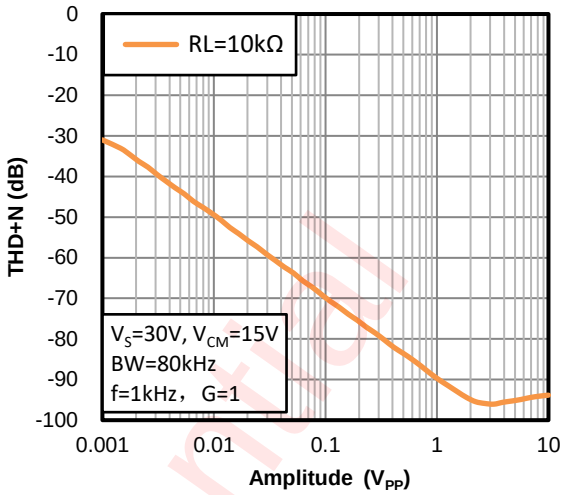


Figure 30 THD + N vs. Amplitude

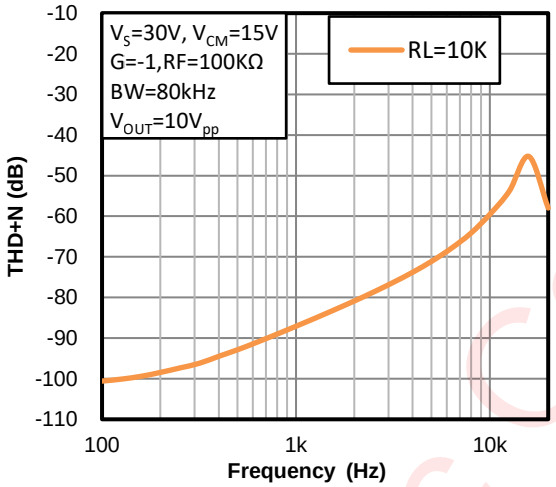


Figure 31 THD + N vs. Frequency

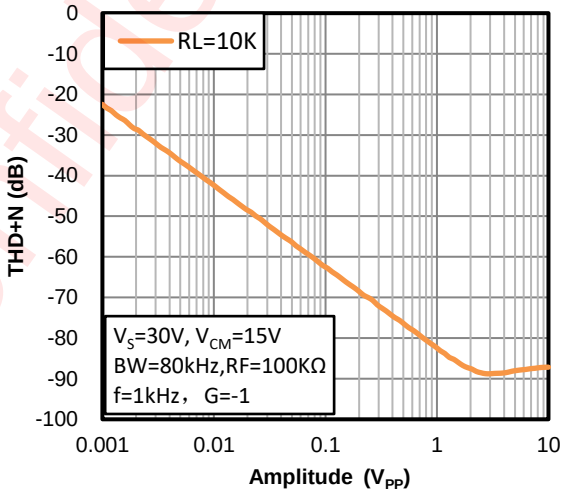


Figure 32 THD + N vs. Amplitude

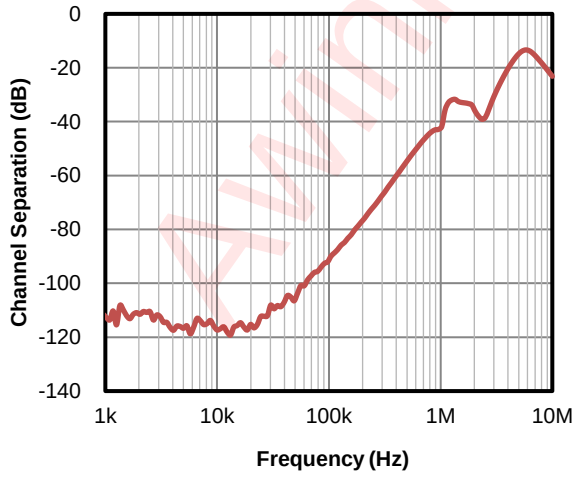


Figure 33 Channel Separation vs. Frequency

PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.
2. R_I is a balance resistor equals to R_G || R_F to reduce the influence of the input bias current on R_G and R_F, which can be shorted when unnecessary.
3. Separate grounding for analog and digital portions of circuitry for better noise suppression. Devote one or more layers on multilayer PCBs to ground planes, which help distribute heat and reduces EMI noise.
4. Run the input traces far away from the Vs supply or output traces to reduce the parasitic coupling. If not, cross these sensitive traces at a 90 degree instead of being parallel with the noisy trace.
5. The input traces are the most sensitive part of the circuit, so keep the length of input traces as short as possible. Place the external resistors and capacitors as close to device as possible, especially the R_F and R_G should be close to the inverting input to minimize the parasitic capacitance.
6. In differential applications, the trace of the inverting input and the non-inverting input should be symmetrical including the same layer, same length, same width and same line spacing.
7. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

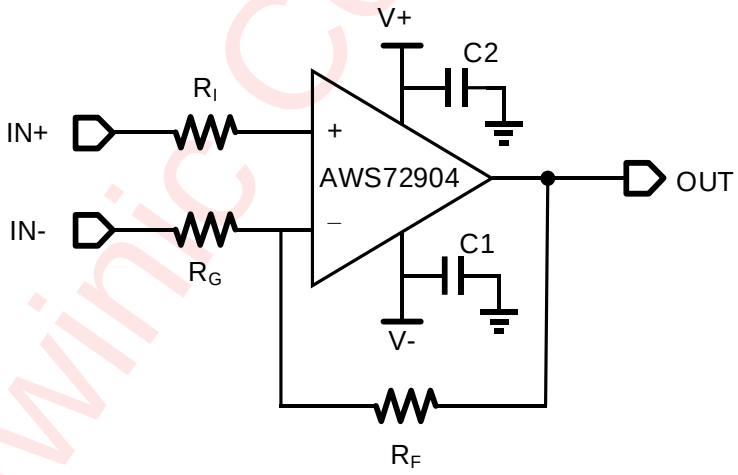
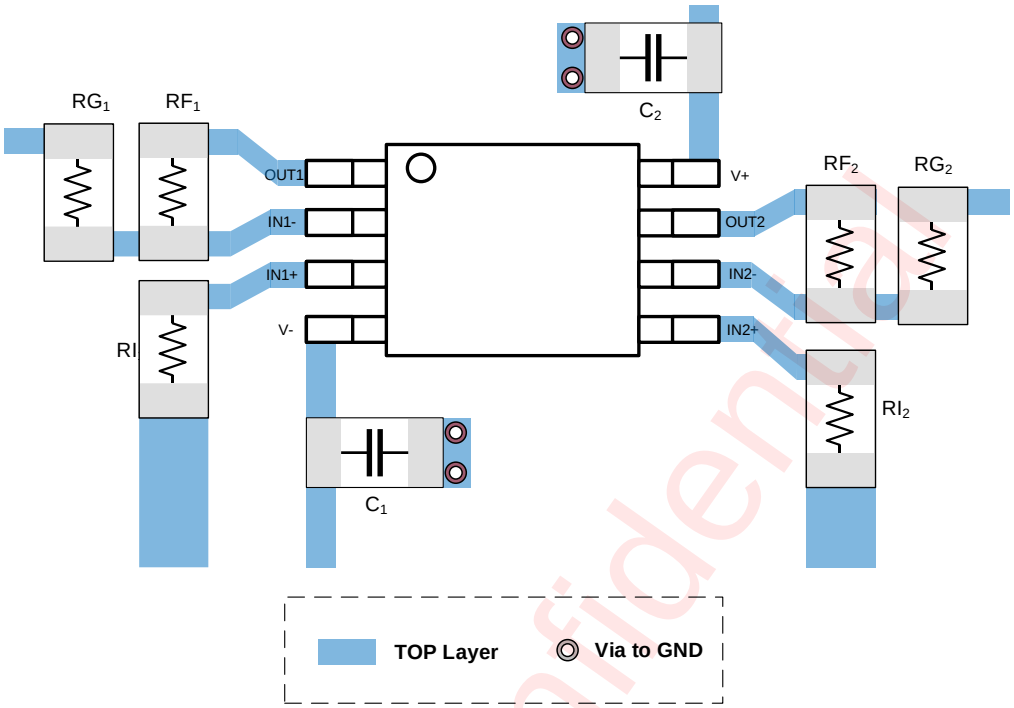


Figure 34 AWS72904 Schematic Example

MSOP-8L



SOP - 8L

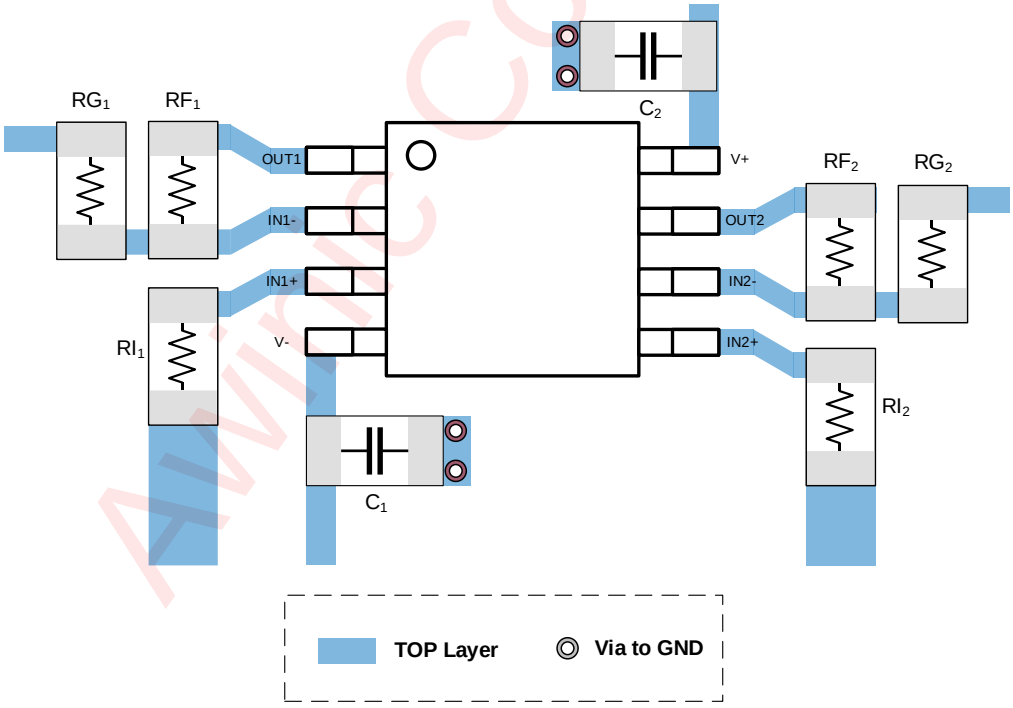


Figure 35 AWS72904 Layout Example

PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impendence node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting gain application，connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 36. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

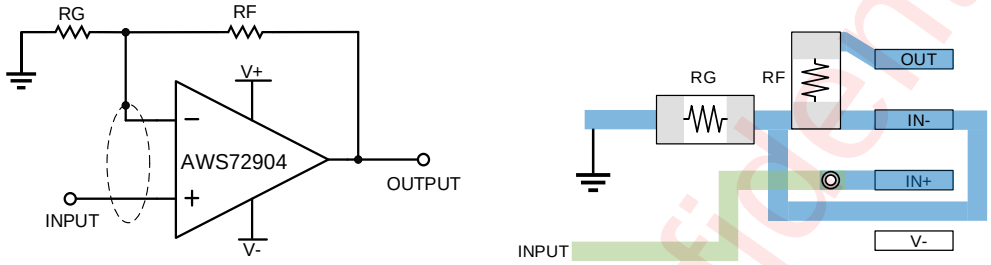


Figure 36 Non-inverting Gain Application Schematic and Layout Example

Similarly, for inverting gain application, connect the IN- to the input with traces not touching the PCB surface, for example, striding over with the input resistor in Figure 37. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS72904.

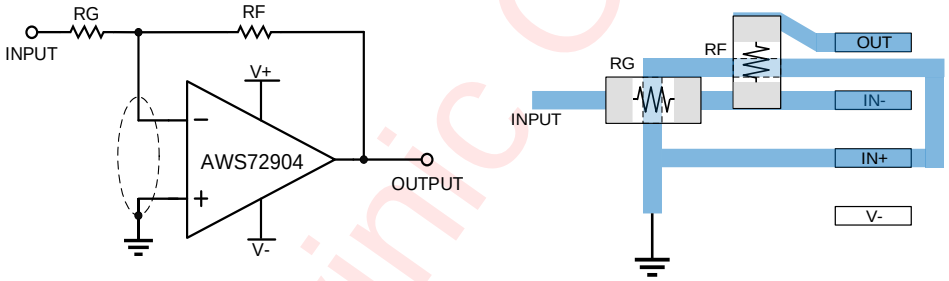
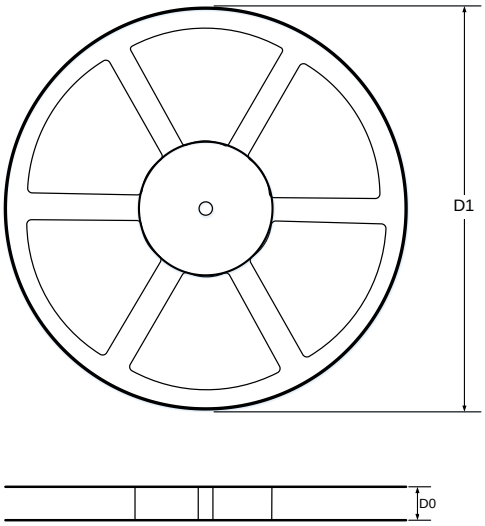


Figure 37 Inverting Gain Application Schematic and Layout Example

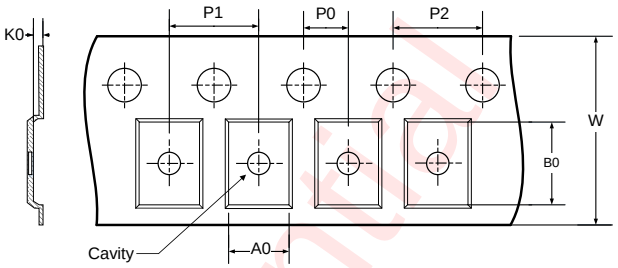
Tape And Reel Information

MSOP-8L

REEL DIMENSIONS

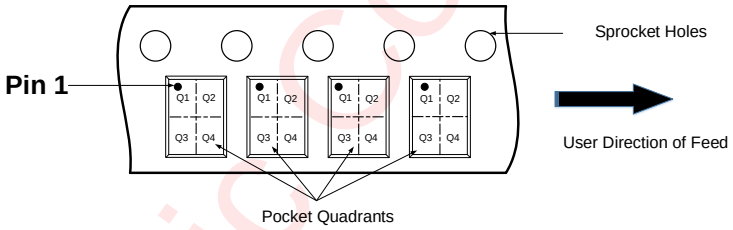


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	5.25	3.35	1.25	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

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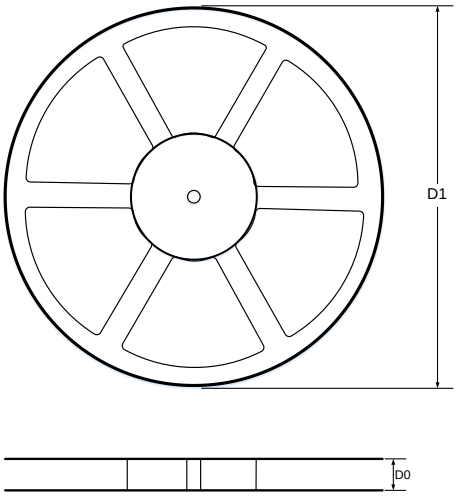
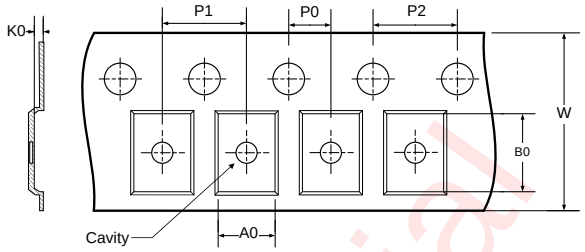
REEL DIMENSIONS

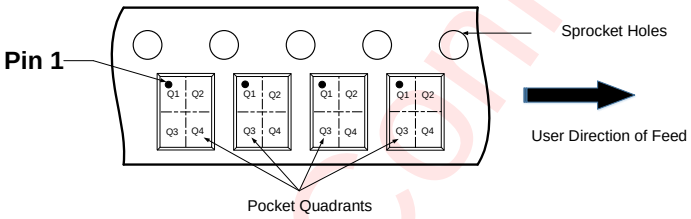


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	6.55	5.30	2.00	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

Package Description

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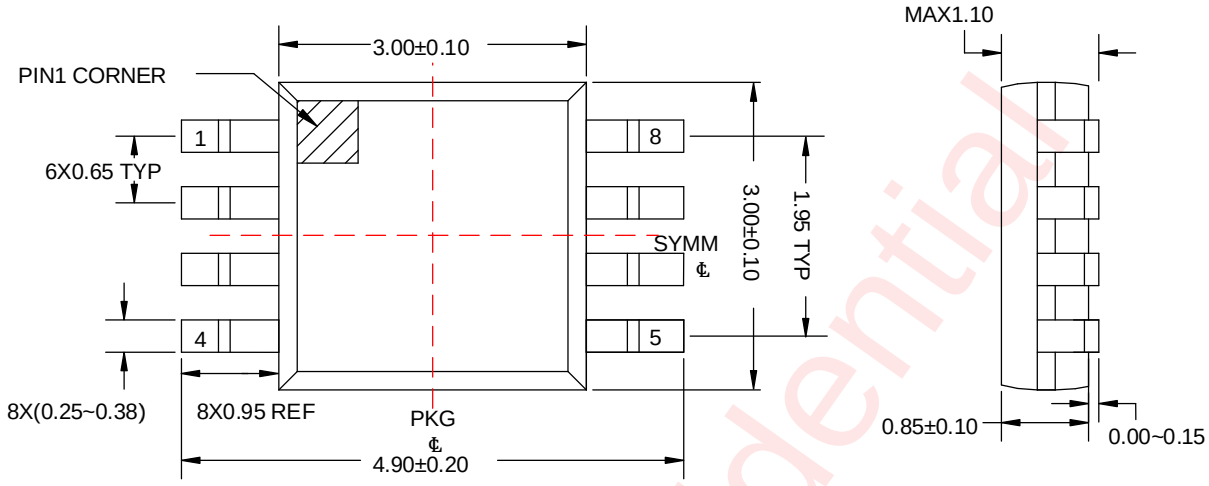
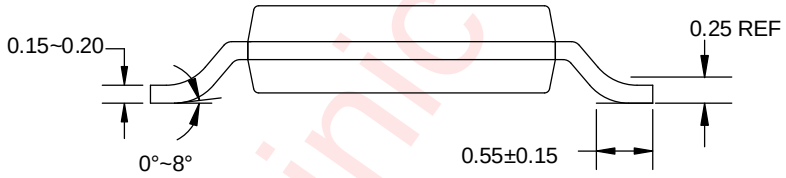


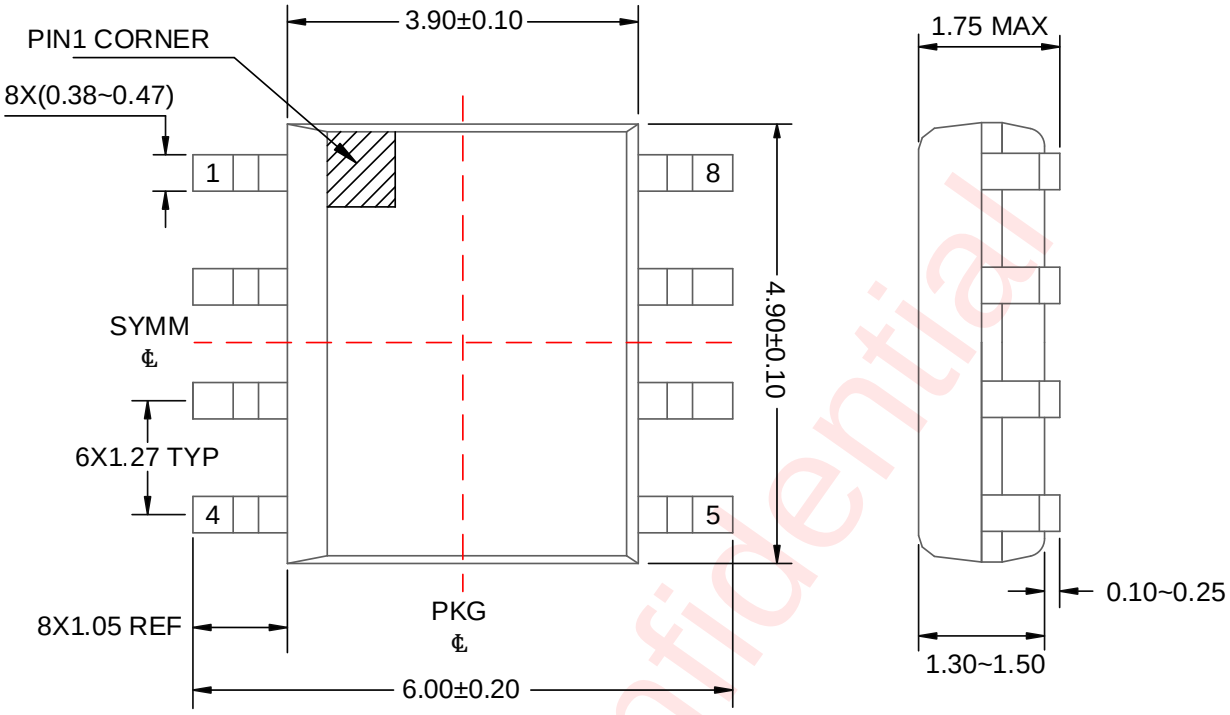
Top View **Side View**



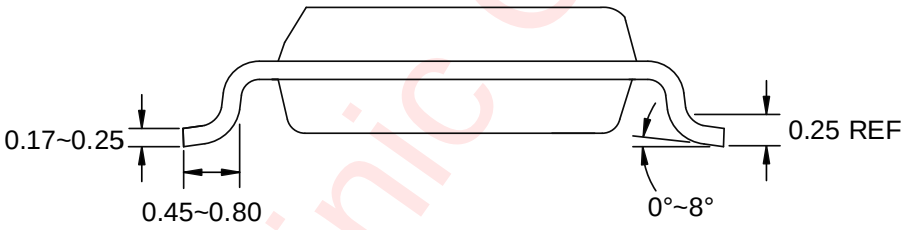
Side View

Unit: mm

SOP-8L



Top View **Side View**

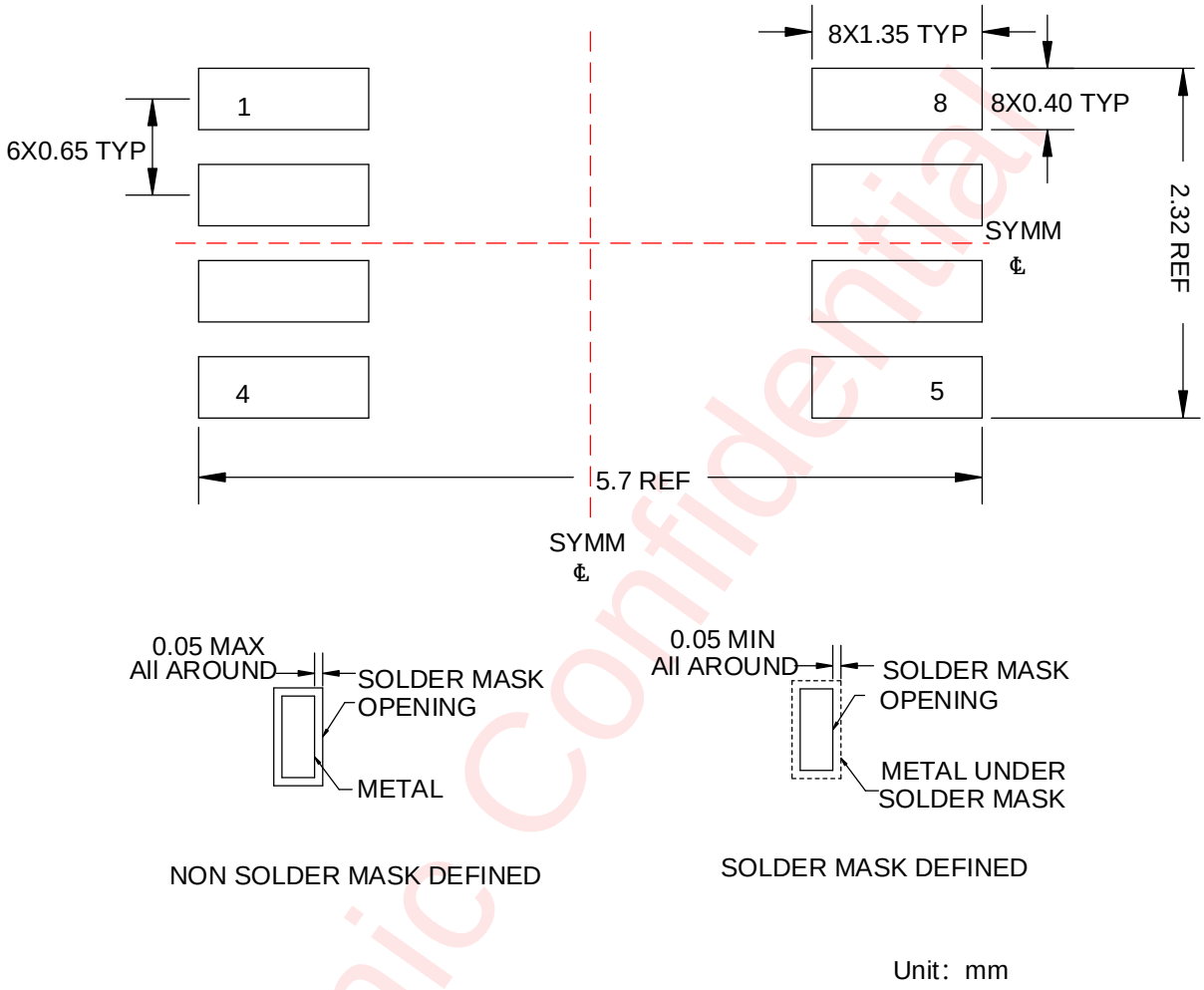


Side View

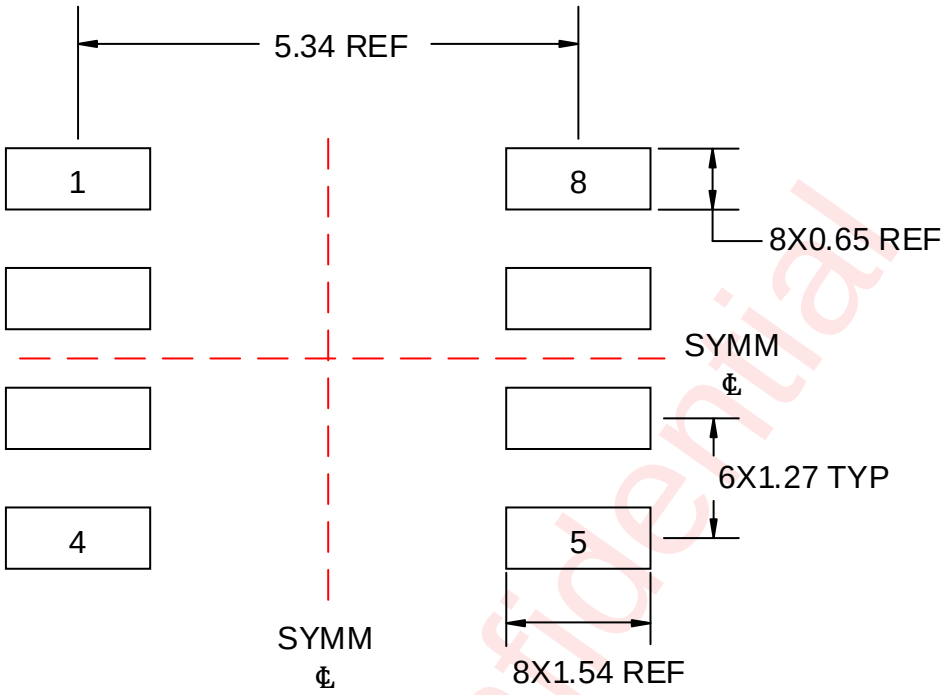
Unit: mm

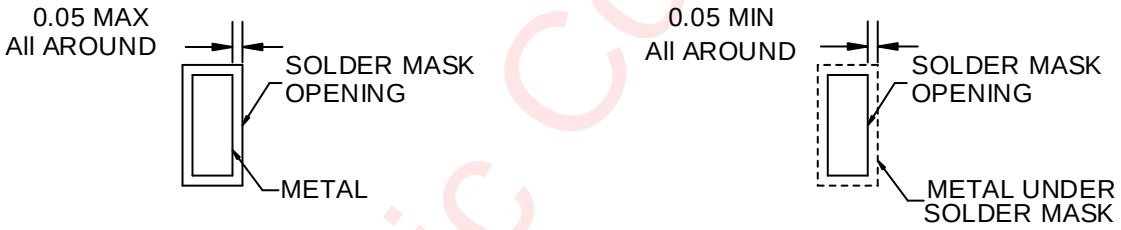
Land Pattern Data

MSOP-8L



SOP-8L





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2024	Official released

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