SI7913DN-VB Datasheet

Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 30	0.038 at V_{GS} = - 10 V	- 6.4
	0.060 at V_{GS} = - 4.5 V	- 5

FEATURES

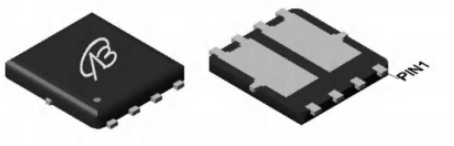
- **Halogen-free According to IEC 61249-2-21 Available**
- Trench Power MOSFET
- New Low Thermal Resistance Power Package

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

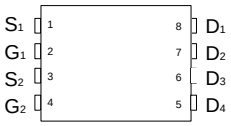
APPLICATIONS

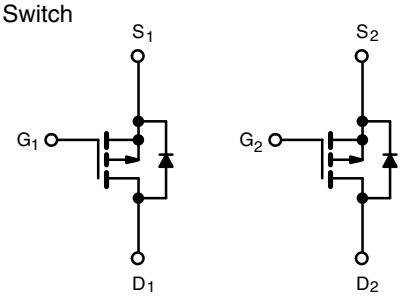
- Portable
  - Battery Switch
  - Load Switch

DFN 3*3



Top View　　Bottom View





P-Channel MOSFET　　P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	- 30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 6.4	- 4.3	A
	T_A = 85 °C		- 4.6	- 3.1	
Pulsed Drain Current		I_{DM}	- 20		
Continuous Source Current (Diode Conduction)[a]		I_S	- 2.3	- 1.1	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.8	1.3	W
	T_A = 85 °C		1.5	0.85	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	35	44	°C/W
	Steady State		75	94	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4	5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

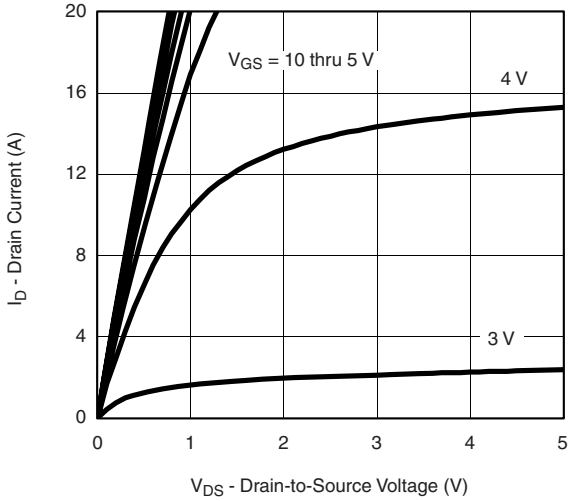
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.0		- 3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 6.4 A		0.038		Ω
		V_{GS} = - 4.5 V, I_D = - 5 A		0.060		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 6.4 A		13		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 2.3 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 6.4 A		14	21	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			3.8		
Gate Resistance	R_g			8.5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 15 Ω $I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 6 Ω		10	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	60	
Fall Time	t_f			28	45	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 2.3 A, dI/dt = 100 A/µs		20	40	

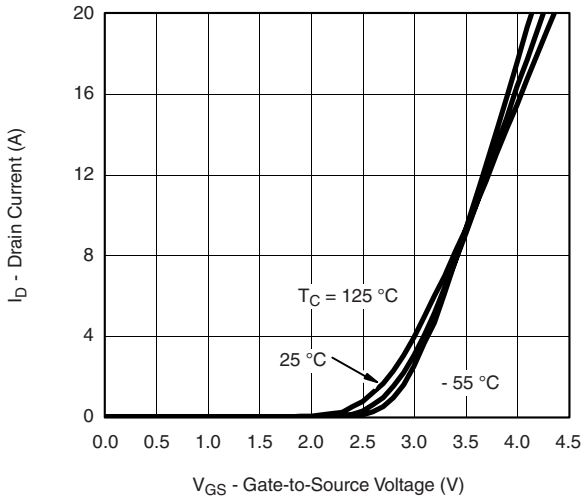
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

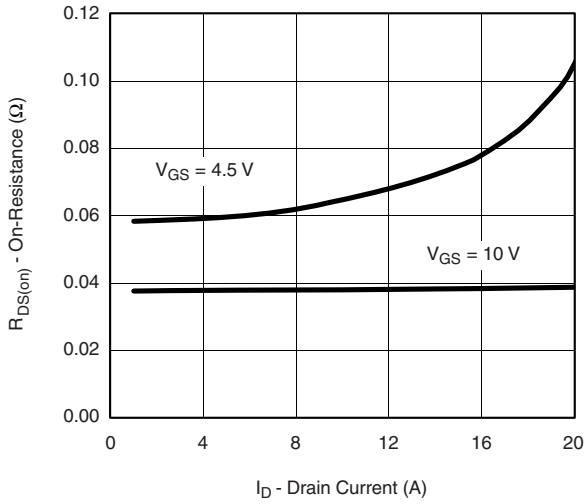


Output Characteristics

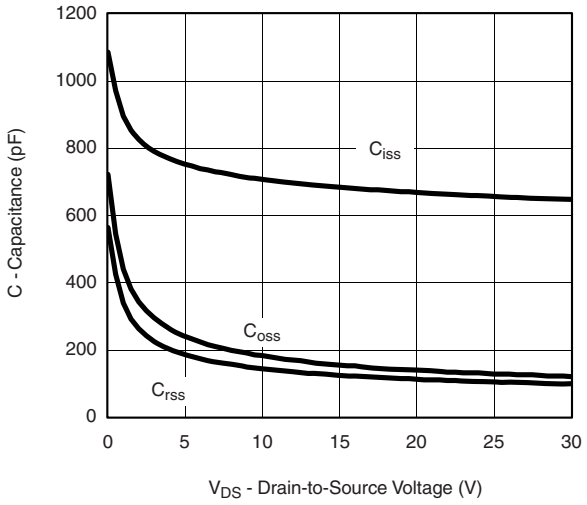


Transfer Characteristics

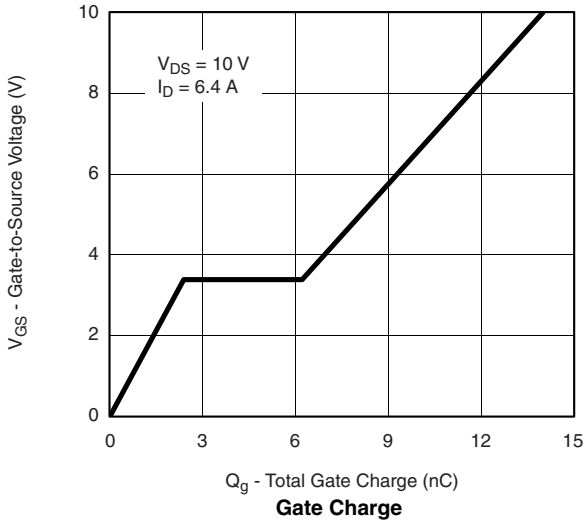
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



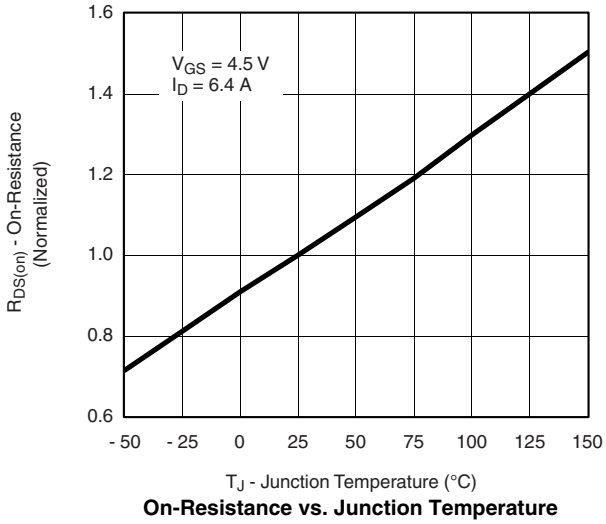
On-Resistance vs. Drain Current



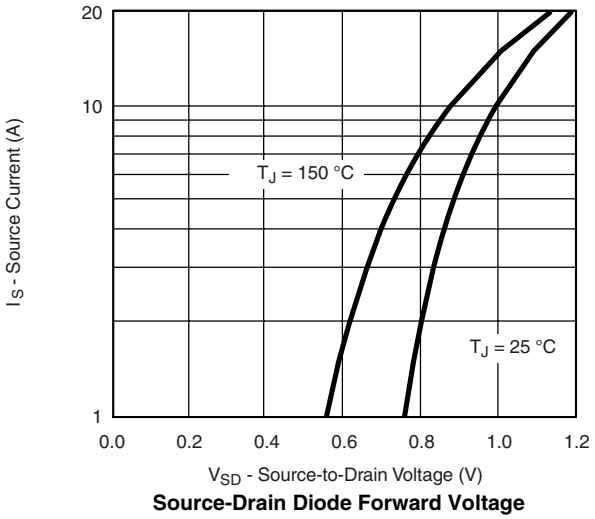
Capacitance



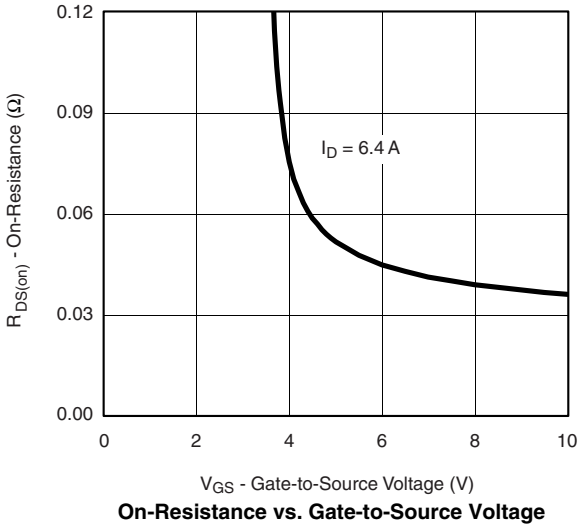
Gate Charge



On-Resistance vs. Junction Temperature

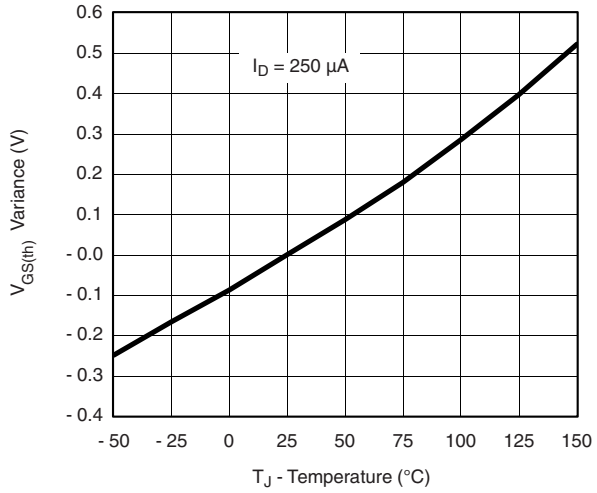


Source-Drain Diode Forward Voltage

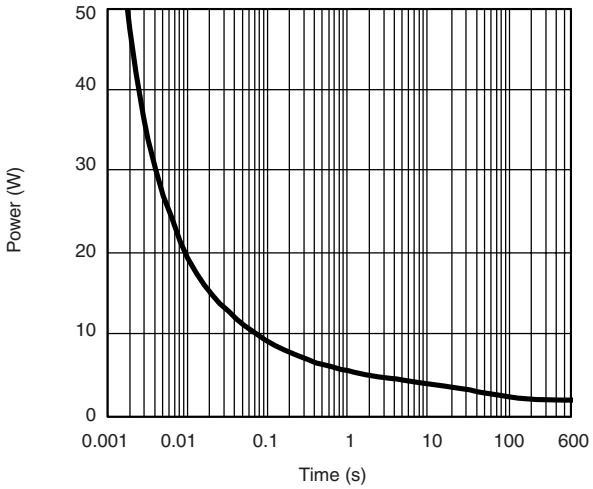


On-Resistance vs. Gate-to-Source Voltage

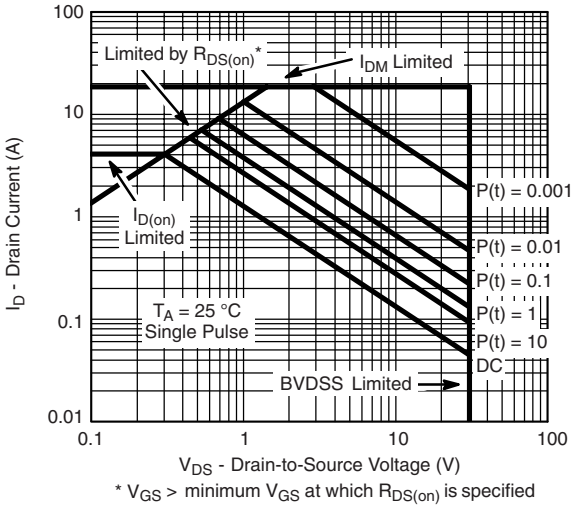
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage

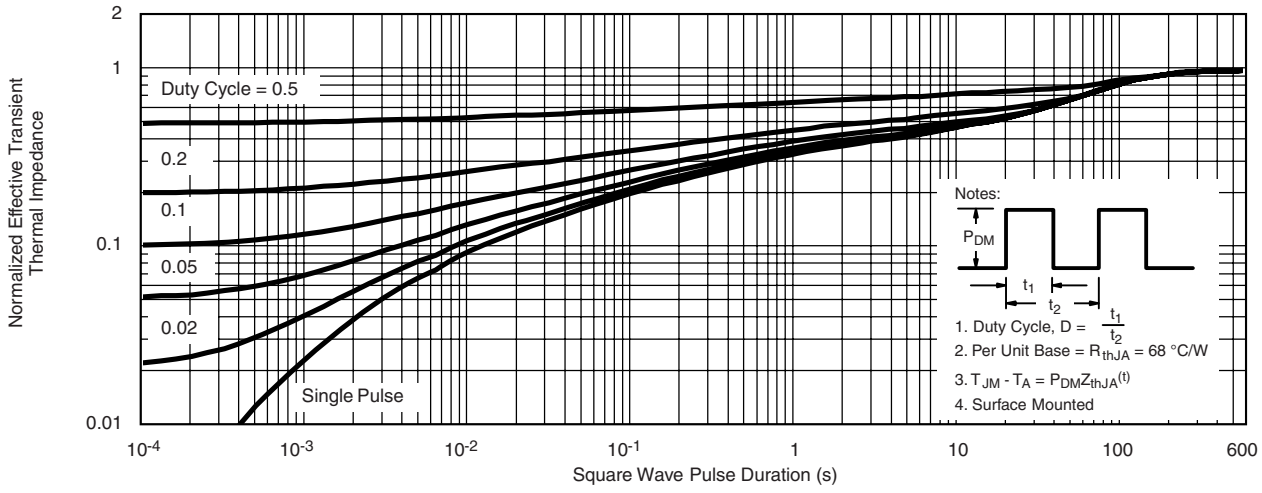


Single Pulse Power, Junction-to-Ambient



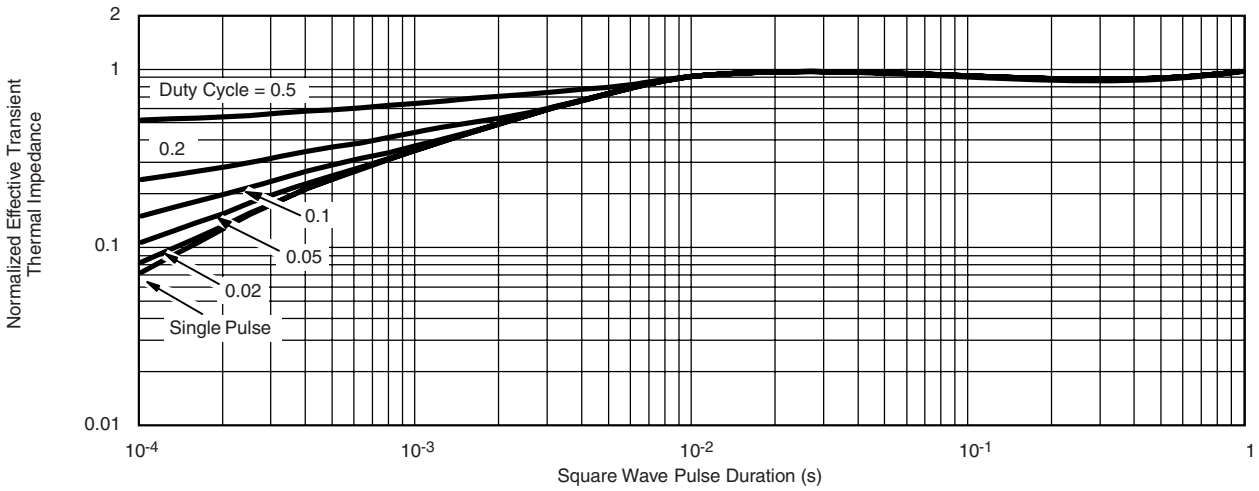
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



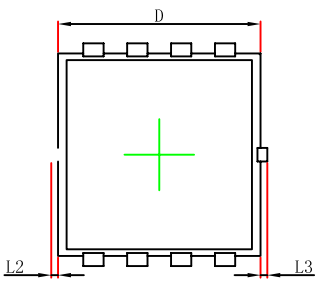
Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

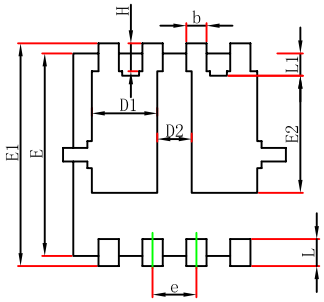


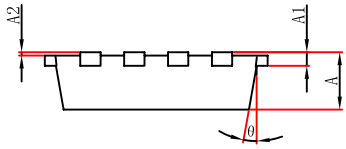
Normalized Thermal Transient Impedance, Junction-to-Case

PDFNWB3×3-8L-B Package Outline Dimensions



Top View
[顶视图]

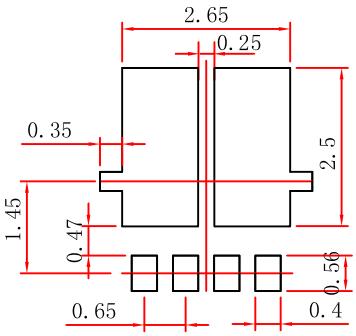




Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	0.935	1.135	0.037	0.045
D2	0.280	0.480	0.011	0.019
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3×3-8L-B Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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