XPC1132

2.7V to 5.5V Supply Voltage,
Scalable, 8.5MHz, 2A Step-down Regulator with LDC feature

FEATURES

- Advanced COT supports multi-phase applications
- Integrated low on-resistance MOSFETs for high conversion efficiency
- Up to 8.5MHz switching frequency
- 0.6-V ±1% voltage reference over temperature at zero load
- Forced PWM mode
- Logic enable input
- Programmable Line-Drop-Compensation (LDC)
- Monotonic start-up into pre-biased output
- Cycle by cycle current limitation and hiccup protection
- Over temperature protection
- RoHS compliance, Pb/Halogen free

APPLICATIONS

- Optical modules
- Cellular phones
- Portable instruments
- Security and surveillance
- Wearables and IoT

DESCRIPTION

The XPC1132 Micro-Point-of-Load is a very efficient, 2A, scalable, synchronous step-down current-mode DC-DC regulator.

Operating with 8.5MHz switching frequency, it allows the use of small external components in both value and form factor, reducing solution size.

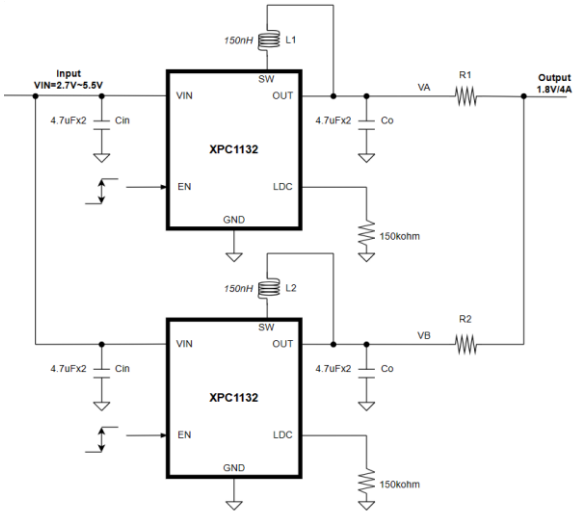
The XPC1132 solution has scalability and supports up to four-phase application, providing proprietary technology for current balance.

The XPC1132 implements Line-Drop-Compensation (LDC) feature, and the compensation slope of the reference voltage can be programmed by external resistor.

The output voltage is fixed and pre-set from 0.6V to 1.8V in 50mV steps with soft-start controlled monotonic ramp.

The XPC1132 comes in a compact 6-pin WLCSP package with minimum 0.4mm pin pitch and 1.5 x 1.15 x 0.6mm size.

TYPICAL APPLICATION



Note: R1 and R2 stand for the trace impedance on pcb.

REVISION HISTORY

Release	Rev	Changes	Date
Preliminary	0.6	Updates	3/5/2024

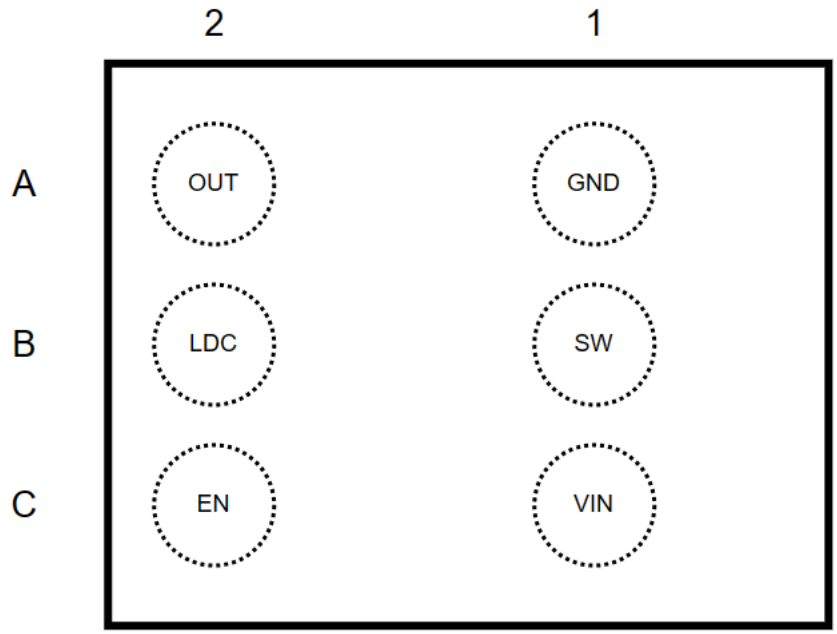
ORDERING INFORMATION

Part Number	Droop Feature	VOUT (V)	FSW (MHz)	Top Marking	MPQ
XPC1132AC06R080	Y	0.8V	8.5	A08	3,000
XPC1132BC06R080	N	0.8V	8.5	B08	3,000
XPC1132AC06R100	Y	1.0V	8.5	A10	3,000
XPC1132BC06R100	N	1.0V	8.5	B10	3,000
XPC1132AC06R120	Y	1.2V	8.5	A12	3,000
XPC1132BC06R120	N	1.2V	8.5	B12	3,000
XPC1132AC06R180	Y	1.8V	8.5	A18	3,000
XPC1132BC06R180	N	1.8V	8.5	B18	3,000

Note: Other output voltage versions (with or without droop feature) are available, however, an MOQ (Minimum Order Quantity) may be required.

MPQ = Minimum Package Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION



Top View (Not to scale)

Pin Configuration

Pin	Name	Description
A1	GND	IC ground. Connect it to larger copper areas or negative terminals of the input and output capacitors.
A2	OUT	Output voltage sense.
B1	SW	Switching node.
B2	LDC	Line-Drop-Compensation setting pin. Place a resistor at this pin to generate the compensation voltage. Leave this pin floated if line drop compensation feature is not needed.
C1	VIN	Power supply input.
C2	EN	Enable. Pull EN high to enable or low to disable the device.

ABSOLUTE MAXIMUM RATINGS(1)

Parameter	Min	Max	Units
DC Supply Voltage, VIN	-0.3	+7.0	V
SW	-0.3	V_{IN} + 0.3	V
SW (10ns transient)	-4.0	+8.0	V
Voltage on other pins, EN, LDC, OUT	-0.3	V_{IN} + 0.3	V
Storage Temperature Range	-40	+150	°C
Junction Temperature	-40	+150	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{IN}	2.7		5.5	V
Output Current (Single-phase)	I_{OUT}	0		2	A
Output Current (Four-phase)		0		8	A
Output Inductor	L		150		nH
Input Capacitor	C_{IN}		2x4.7		uF
Output Capacitor	C_{OUT}		2x4.7		uF
Operating Temperature, Junction	T_{OJ}	-40		+125	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	44	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	12	°C/W

ELECTRICAL SPECIFICATIONS

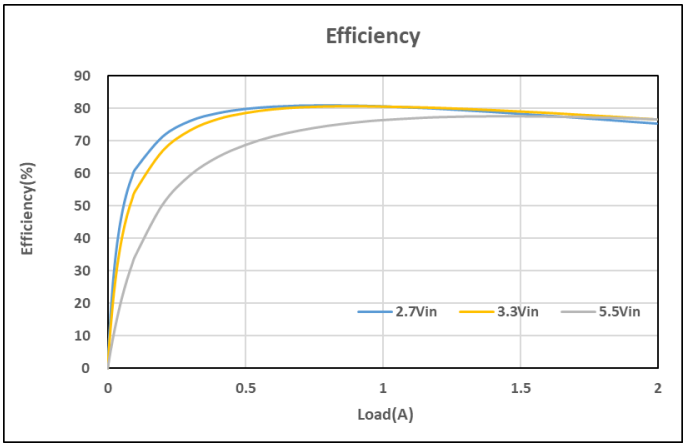
Typical values unless otherwise noted: V_{IN} = 3.3V, V_{OUT} = 1.2V, Ambient Temperature = +25°C.

Maximum and minimum values are: V_{IN} = V_{EN} = 2.7V to 5.5V, TJ = -40 to +125°C.

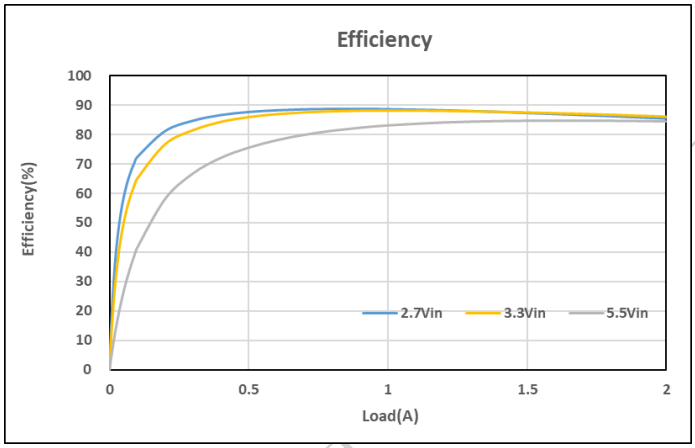
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Characteristics						
Supply Voltage	V_{IN}		2.7		5.5	V
Quiescent Current	I_Q	No Load, Not switching		550	600	µA
Shutdown Current	I_{SHDN}	EN = GND			5	µA
Under-Voltage Lockout Threshold	V_{UVLO}	Rising V_{IN}	2.4	2.5	2.7	V
Under-Voltage Lockout Hysteresis	$V_{UVLOHYST}$			300		mV
Thermal Shutdown	T_{TSD}			150		°C
Thermal Shutdown Hysteresis	T_{HYST}			25		°C
Logic Input: EN						
Logic High Voltage	V_{IH}		1.2			V
Logic Low Voltage	V_{IL}				0.4	V
Output Characteristics						
Switching Frequency	F_{SW}		7.5	8.5	9.5	MHz
Minimum Output Voltage	V_{OUT}	I_{OUT} =0A, LDC= V_{IN}, w/ droop	600	606	612	mV
		I_{OUT} =2A, LDC= V_{IN}, w/ droop	576			mV
		I_{OUT} =0A, LDC= V_{IN}, w/o droop	594	600	606	mV
Maximum Output Voltage	V_{OUT}	I_{OUT} =0A, LDC= V_{IN}, w/ droop	1.8	1.818	1.836	V
		I_{OUT} =2A, LDC= V_{IN}, w/ droop	1.728			
		I_{OUT} =0A, LDC= V_{IN}, w/o droop	1.782	1.8	1.818	V
Enable Turn-on Delay	T_{EN}			200		µs
Power Switches						
PMOS On Resistance	R_{DSONP}	V_{IN} = V_{GS} = 3.6V		25	35	mΩ
NMOS On Resistance	R_{DSONN}	V_{IN} = V_{GS} = 3.6V		15	25	mΩ
Minimum ON-time	Ton_min	Measured at 50% points on SW. IOUT=2A		10		ns
Minimum OFF-time	Toff_min	Measured at 50% points on SW. IOUT=2A		40		ns
Current Limit						
Low side current limit threshold	I_{LIM}		2	2.6		A
Vout threshold entering hiccup				V_{OUT}/2		
Delay time entering hiccup		fsw=8.5Mhz		120		us
Hiccup time		fsw=8.5Mhz		11.5		ms
Low side reverse current protection				1.5		A
Soft Start						
Soft start time		V_{IN}=3.3V		500		us

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

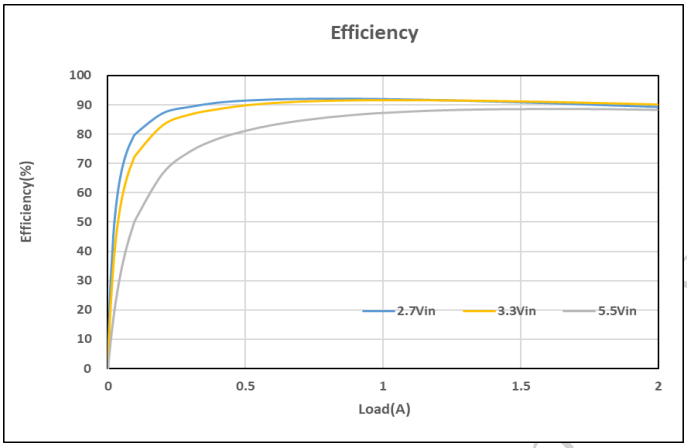
V_{IN} = 3.3V, V_{OUT} = 1.2V, L_{OUT} = 150nH, C_{OUT} = 2 x 4.7µF, f_{SW} = 8.5MHz, T_A = +25°C, unless otherwise noted.



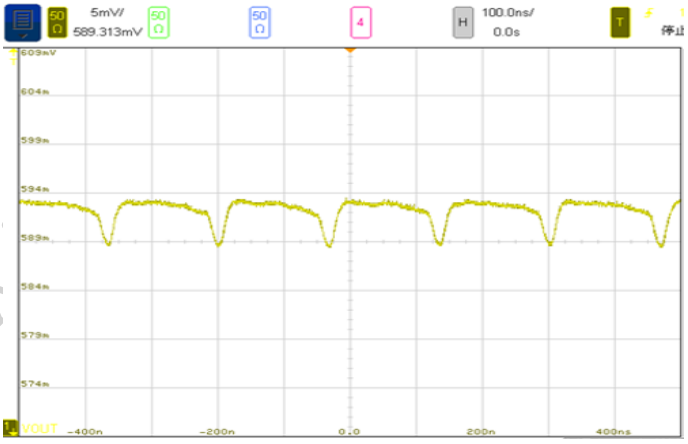
Efficiency, V_{OUT}=0.6V, F_{SW}=8.5MHz, DCR=31mohm



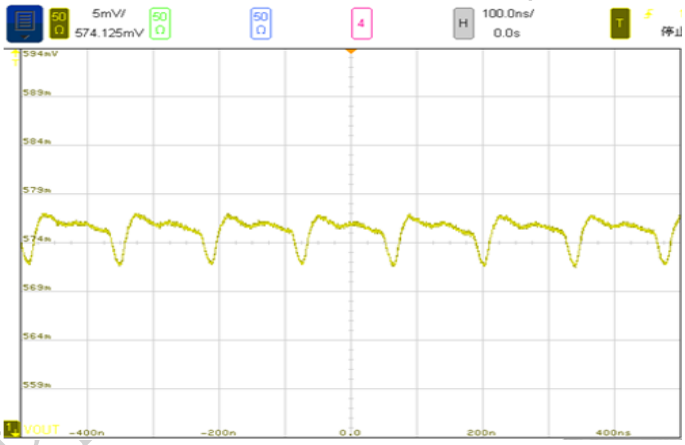
Efficiency, V_{OUT}=1.2V, F_{SW}=8.5MHz, DCR=31mohm



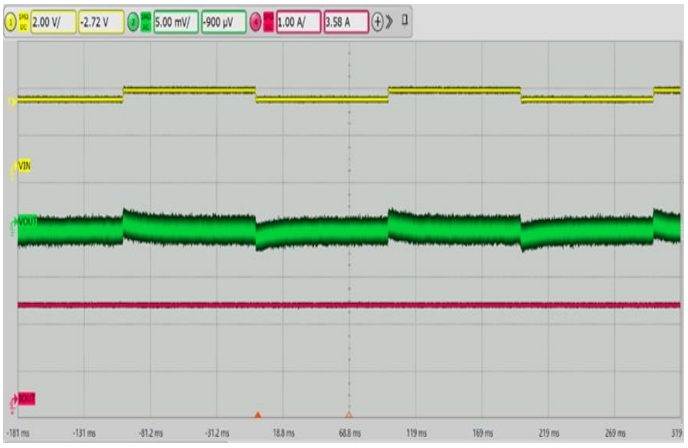
Efficiency, V_{OUT}=1.8V, F_{SW}=8.5MHz, DCR=31mohm



Ripple, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=0A



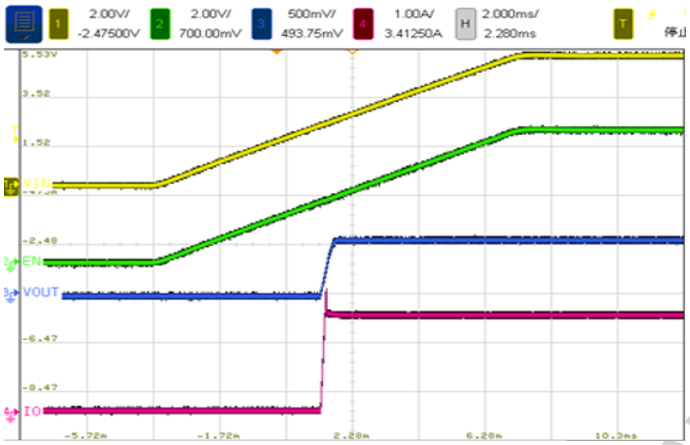
Ripple, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=2A



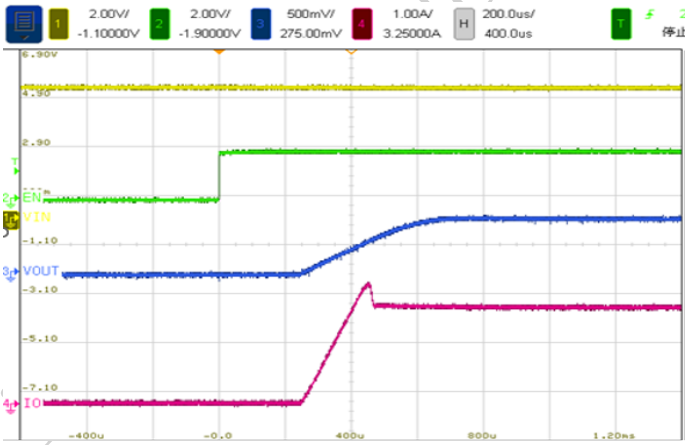
Line transient, V_{IN}=2.7V~3.3V, V_{OUT}=0.6V, I_O=2A

Load transient, V_{IN}=2.7V, V_{OUT}=0.6V (with droop), I_O=0A~1A

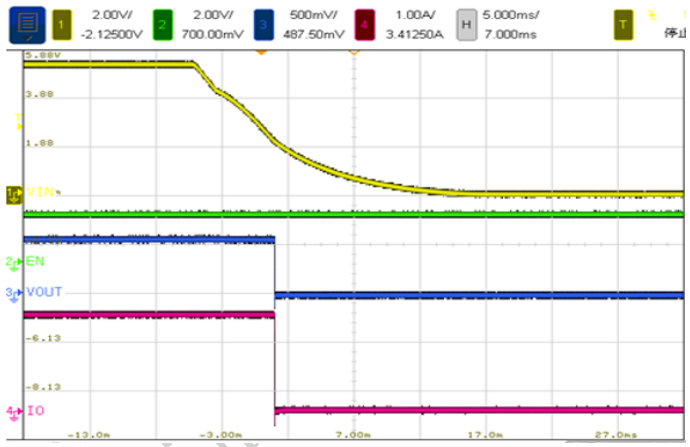
Load transient, V_{IN}=2.7V, V_{OUT}=0.6V (with droop), I_O=1A~2A



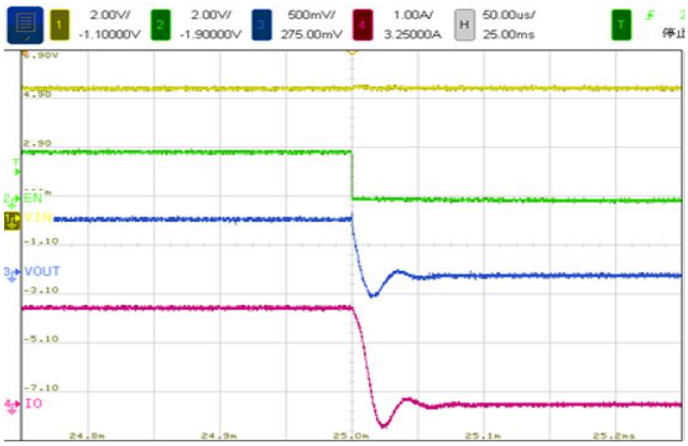
Power on, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=2A



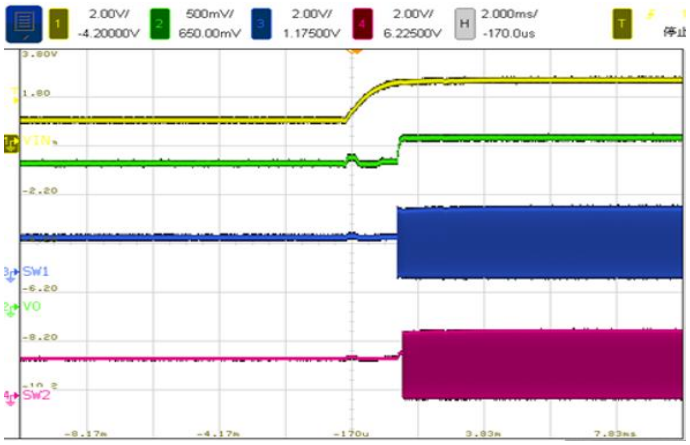
Enable on, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=2A



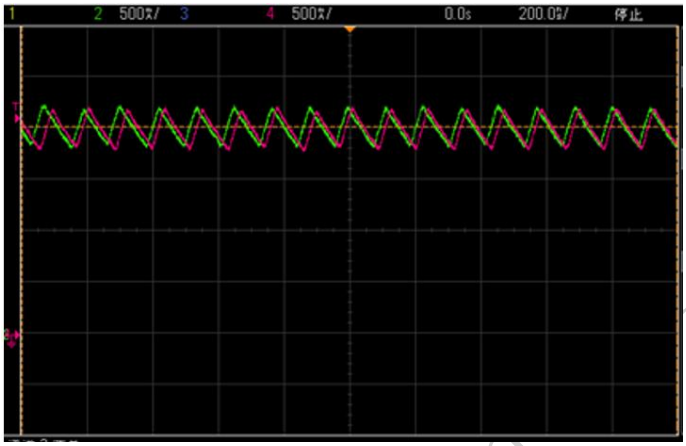
Power off, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=2A



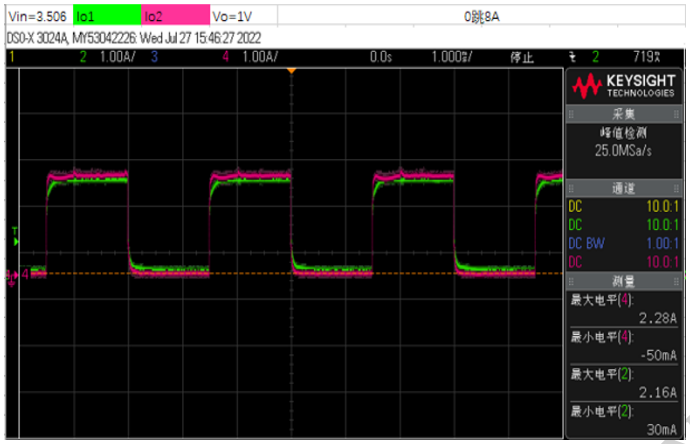
Enable off, V_{IN}=5.5V, V_{OUT}=0.6V, I_O=2A



Pre-biased start-up, dual-phase, V_{IN}=2.7V, V_{OUT}=1.8V, I_O=0A

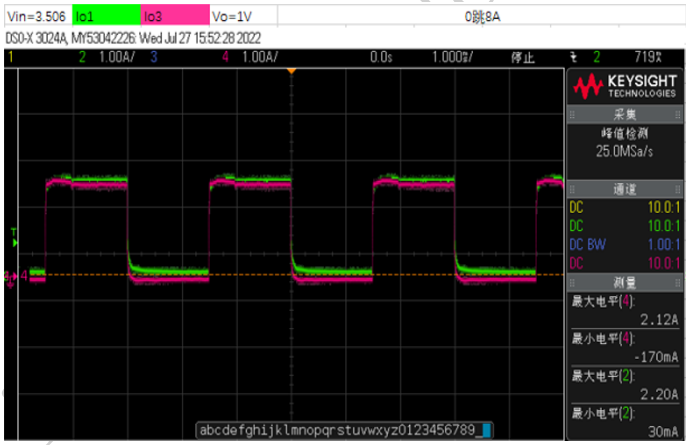


Dual-phase operation, V_{IN}=3.3V, V_{OUT}=1.0V, I_O=4A



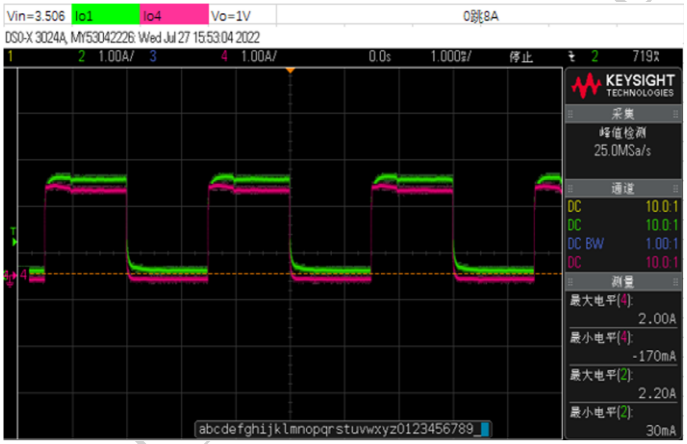
Four-phase operation, V_{IN}=3.5V, V_{OUT}=1.0V

Load transient 0~8A, Phase 1 and phase2



Four-phase operation, V_{IN}=3.5V, V_{OUT}=1.0V

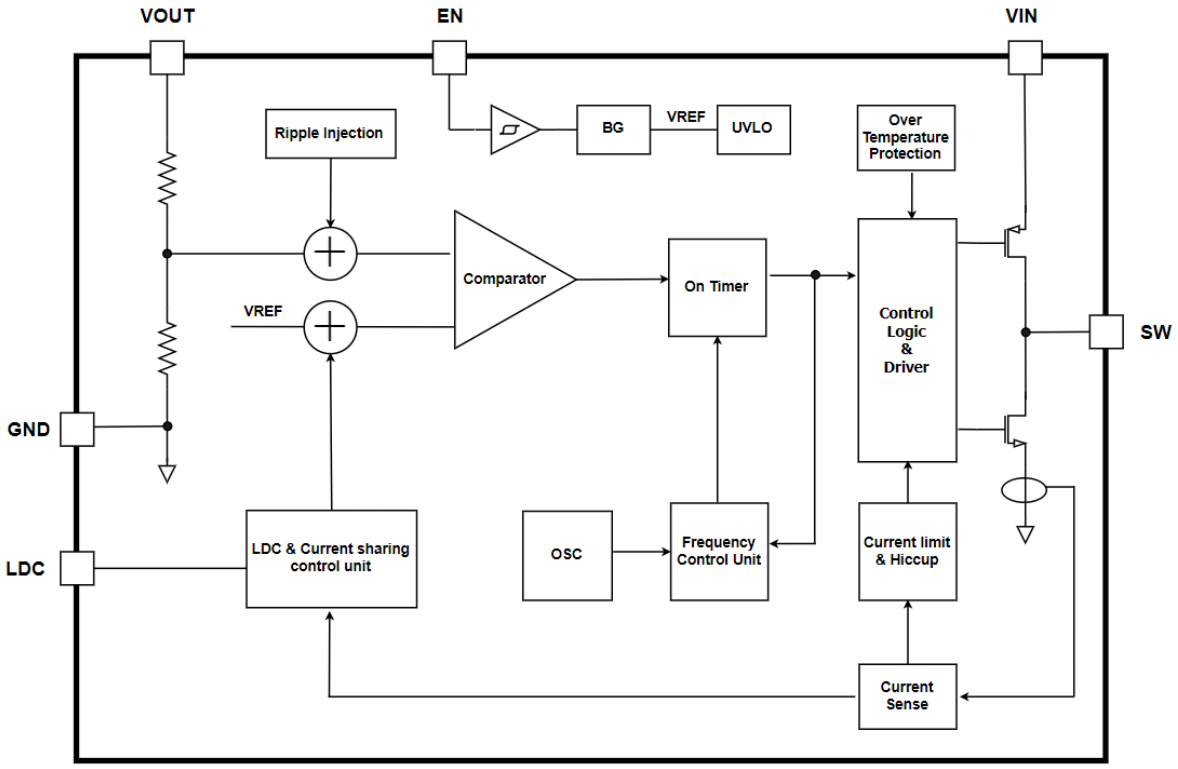
Load transient 0~8A, Phase 1 and phase3



Four-phase operation, V_{IN}=3.5V, V_{OUT}=1.0V

Load transient 0~8A, Phase 1 and phase4

FUNCTIONAL DESCRIPTION



Block Diagram

Overview

The XPC1132 is a synchronous, step-down, scalable DC/DC voltage regulator with 8.5MHz switching frequency. Operating from an input voltage between 2.7V and 5.5V, the regulator can deliver up to 2A of load current.

Once Droop feature enabled, the XPC1132 supports up to 4-phase operation in parallel to provide 8A of load current, without the need of additional external components.

The optional line drop compensation feature is ideal for those applications in which PoL is placed far away from the load. The compensation voltage is programmable with resistors.

Enable

Setting the EN pin to logic High enables the device, VOUT starts to ramp up after 150µs delay. Alternatively, the device is disabled when the EN voltage is set to logic Low. In this state the IC draws less than 1µA of current.

Under voltage lockout (UVLO)

The under-voltage lockout feature prevents the device from turning on if VIN is below 2.5V threshold. If the device is enabled under UVLO conditions, the internal circuitry will not turn on until input voltage is increased. Once active, the UVLO circuit has a 300mV of hysteresis and the device will turn off when VIN drops below 2.2V.

Soft start

When the device is enabled, internal soft-start circuitry ramps VOUT up over a period of 500us to limit inrush current. This feature protects a high impedance source from being pulled to a lower voltage as the device turns on.

Low-side overcurrent protection

XPC1132 continuously monitors the conduction current of low-side MOSFET. During normal operation, the low-side sources current into the load. When the sourcing current reaches the internally set low-side sourcing (forward) current limit, the high-side is not turned on. Under this condition, the low-side is kept on until the sourcing current becomes less than the internally set current limit and then the high-side is turned on if vout is less than the reference voltage. This ensures protection under an output short condition and small duty cycle condition; thereby, preventing current run-away. The low-side can also sink current from the load. If the low-side sinking (reverse) current limit is exceeded, the low-side is turned off immediately for the rest of the clock cycle. Under this condition, both the high-side and low side are off until the start of the next cycle.
When low-side overcurrent protection is trigged and vout voltage is less than 1/2 nominal value for more than 120us, the output will be disabled. After being disabled for 11.5ms, the device will be re-enabled, and a new soft-start cycle begins.

Thermal shut-down

The device thermal shutdown protection is enabled if the chip temperature exceeds 150°C. Once the temperature drops below 125°C, the device will be re-enabled, and a new soft-start cycle will begin.

Safe startup into prebiased output

The XPC1132 allows monotonic start-up into prebiased output. The low-side FET and high-side FET will keep turning off before the output voltage reaches the prebiased voltage.

When the converter sinks current through the low side FET and if the current exceeds the low-side sinking (reverse) current limit, the control circuit turns the low-side FET off. Due to the implemented pre-biased function, the low-side FET reverse current protection should not be reached, but it provides another layer of protection.

Line drop compensation (LDC)

XPC1132 provides optional line drop compensation for pcb trace and routing. The compensation slope of reference voltage can be programmed by external resistor that is connected to LDC pin.

$$Slop_{LDC} = \frac{1425}{R_{LDC}} mv/A$$

Below resistances are recommended for line drop compensation.

Resistance	Output voltage	Typical compensation at 1A load
150kohm	0.6V	10mV
	1.2V	20mV
	1.8V	30mV
180kohm	0.6V	8mV
	1.2V	16mV
	1.8V	24mV
240kohm	0.6V	6mV
	1.2V	12mV
	1.8V	18mV
300kohm	0.6V	5mV
	1.2V	10mV
	1.8V	15mV

When line drop compensation feature is not needed, leave LDC pin floating.

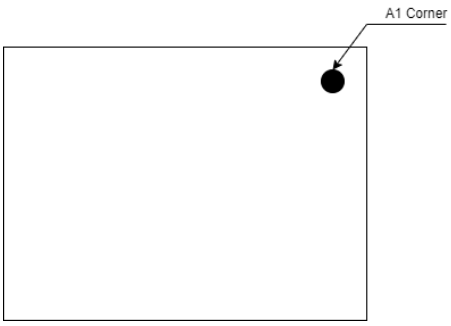
Current sharing for multi-phase application

XPC1132 has proprietary droop feature to make current sharing among multiple phases feasible. Up to four phases operation in parallel is supported with this droop feature.

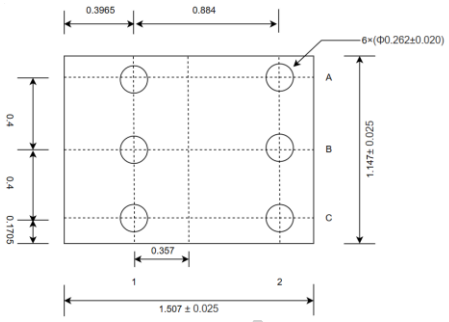
PHYSICAL DIMENSIONS

Units: mm

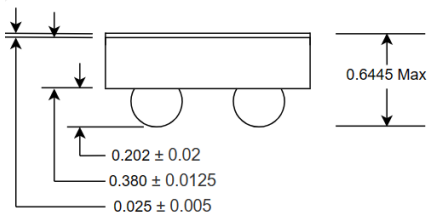
Top view



Bump view



Side view



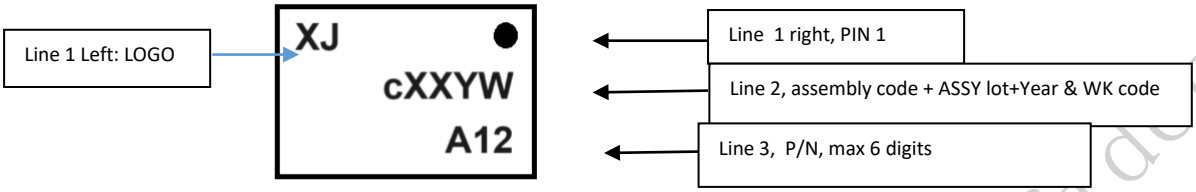
TOP MARKING

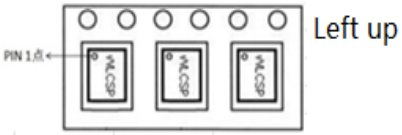
Package Marking & PQ information

XPC1132AC06R120 Marking

(CSP package marking)

Format:





Remark :

Font: Arial

Letter height of 160um, wide of 120um

Letter pitch of 50um

Line space of 50um

LOGO Line 1 leftt

Logo of XJ should be required and placed on assigned Logo position as upside illustration.

Pin 1 Line 1 right

Pin 1 should be designed at right of line 1 for recognition.

Traceability Code: Line 2 and Line 3

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code

a) 1st digit: Assembly location code: HEXIN: c
b) 2nd & 3rd digit: Assembly lot number

c)4nd digit: Year code.

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th digit: Week code, 1～9， A～Z（10~35)， a～z (36~53)

WK01 means the 1st Work Week based on XinJi's calendar.

WK01	WK02	WK03	WK04	WK05	WK06	WK07	WK08	WK09
1	2	3	4	5	6	7	8	9

WK10	WK11	WK12	WK13	WK14	WK15	WK16	WK17	WK18
A	B	C	D	E	F	G	H	I

WK19	WK20	WK21	WK22	WK23	WK24	WK25	WK26	WK27
J	K	L	M	N	O	P	Q	R

WK28	WK29	WK30	WK31	WK32	WK33	WK34	WK35	WK36
S	T	U	V	W	X	Y	Z	a

WK37	WK38	WK39	WK40	WK41	WK42	WK43	WK44	WK45
b	c	d	e	f	g	h	i	j

WK46	WK47	WK48	WK49	WK50	WK51	WK52	WK53
k	l	m	n	o	p	q	r

2.Product Number Code: Line 3

Product Name	P/N Code	Remark
XPC1132AC06R120	A12	Max. 6 digitals are defined for the device type .