

6MHz, 750mA Extremely Small DC-DC Buck Converter

Features

- 6MHz PWM Switching Frequency at Heavy Load
- Auto PFM/PWM – AW37418A/B/C
- Force PWM – AW37419A/B/C
- Output Voltage
0.9V – AW37418A, AW37419A
0.95V – AW37418B, AW37419B
1.1V – AW37418C, AW37419C
- 45 μ A PFM Quiescent Current at Light Load – AW37418A
- 750mA Output Current Capacity
- 1.5A Inductor Cycle-by-Cycle Peak Current Limit Protection
- <0.1 μ A Shutdown Current
- Small Chip Inductor in 0805 Case Size Allowed
- WLCSP 0.968mm \times 0.888mm - 5B Package

General Description

AW37418/9 series are 6MHz DC-DC step-down converters with extremely small package.

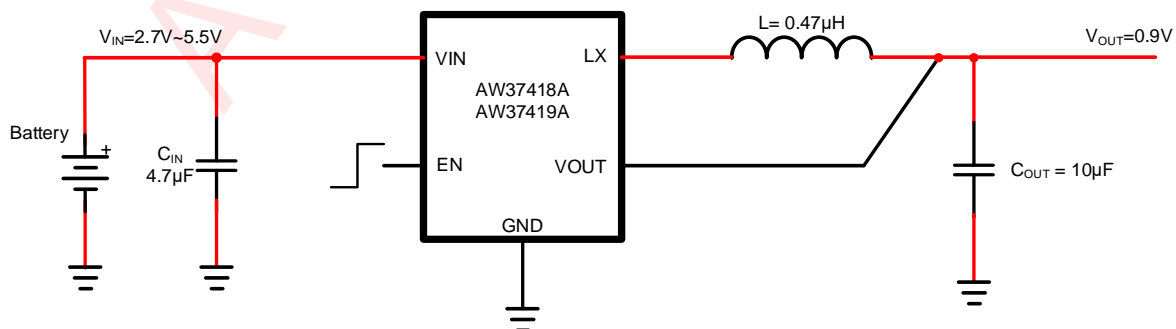
The AW37418 works in three operation modes. At heavy load, the device operates in 6MHz fixed frequency PWM mode. At light load, the AW37418 enters peak-current-control PFM mode automatically to reduce the switching losses. In PFM mode, the quiescent current consumed by the part is reduced to 45 μ A for the purpose to extend the battery life. The AW37419A works in forced PWM mode which can achieve extremely low output ripple throughout the load. The device is off in Shutdown mode and reduces the supply current to 0.1 μ A(typical).

AW37418/9 series are available in WLCSP-5B 0.968mm \times 0.888mm -5B Packages. The high switching frequency 6MHz allows the use of the economic size-saving external components, two ceramic capacitors and one 0.47 μ H inductor are required.

Applications

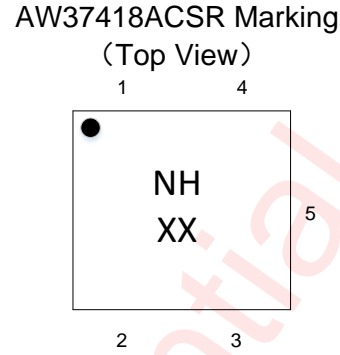
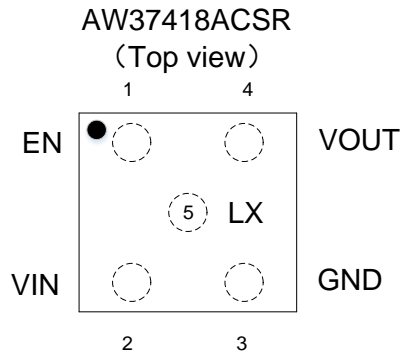
Smart phones / Mobile phones
Wireless earphone / Headset
Wearable devices
Power supply for module

Typical Application Circuit

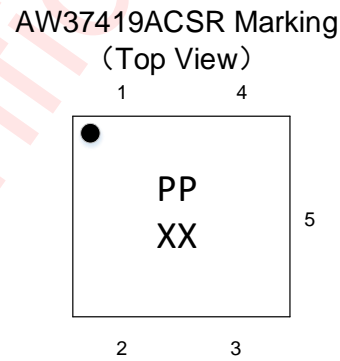
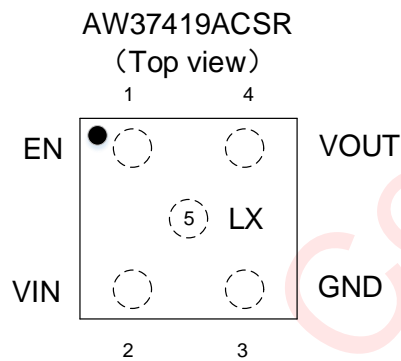


Typical Application Circuit

Pin Configuration and Top Mark



NH — AW37418ACSR
XX — Production Tracing Code



PP — AW37419ACSR
XX — Production Tracing Code

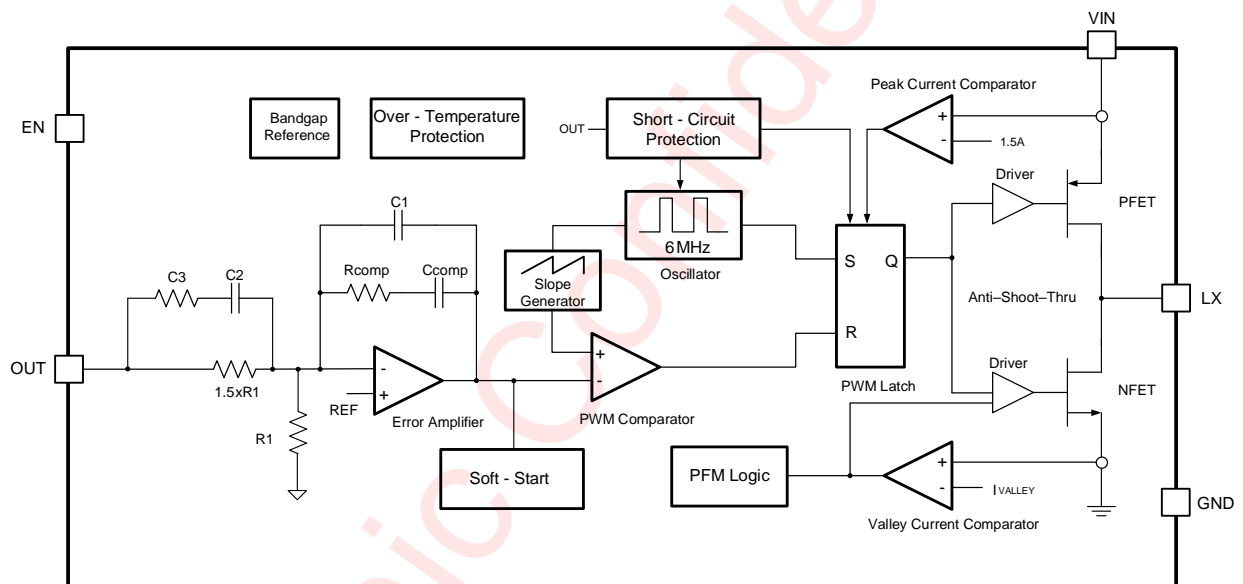
Pin Definition

No.	NAME	DESCRIPTION
1	EN	Enable Input. Set a digital input high to enable the part. Set low to shut down the IC. Do NOT leave the EN pin floating.
3	GND	Ground
5	LX	Switch pin of the converter, it is connected to the inductor.
2	VIN	Power Supply Input.
4	VOUT	Output Voltage Feedback Input. Connect this pin to output supply at the output inductor.

Device Comparison Table

Part Number	Operation Mode	Output Voltage
AW37418ACSR	Auto PFM/PWM	0.9V
AW37419ACSR	FPWM	0.9V
AW37418BCSR(In developing)	Auto PFM/PWM	0.95V
AW37419BCSR(In developing)	FPWM	0.95V
AW37418CCSR(In developing)	Auto PFM/PWM	1.1V
AW37419CCSR(In developing)	FPWM	1.1V

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37418ACSR	-40°C~85°C	WLCSP 0.968mm × 0.888mm -5B	NH	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37419ACSR	-40°C~85°C	WLCSP 0.968mm × 0.888mm -5B	PP	MSL1	ROHS+HF	3000 units/ Tape and Reel

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Absolute Maximum Ratings^(NOTE1)

Parameter		Range
Supply voltage range V_{IN}		-0.3V to 6V
Output voltage range	SW, VOUT, EN	-0.3V to $V_{IN}+0.3V$
Junction-to-ambient thermal resistance θ_{JA}		115°C/W
Operating free-air temperature range		-40°C to 85°C
Junction temperature range		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		160°C
Storage temperature T_{STG}		-65°C to 160°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)		
HBM ^(NOTE 2)		±2kV
CDM ^(NOTE 3)		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2022

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	0.9		1.1	V
I_{LOAD}	Load current			750	mA
$C_{IN}^{(1)}$	Input capacitor	4.7			μF
$C_{OUT}^{(1)}$	Total output capacitor	4.7	10	14.7	μF
L	Inductance		0.47		μH

(1) Capacitance of C_{IN} and C_{OUT} is nominal value.

Electrical Characteristics

All typical values are tested at $V_{IN}=3.6V$, $T_A=25^{\circ}C$ (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.05		V
	Hysteresis			250		mV
SUPPLY CURRENT						
I_{SD}	Supply current in shutdown mode	$EN=0V$, $V_{IN}=3.6V$			1	μA
I_Q	PFM mode quiescent current	$V_{IN}=3.6V$		45		μA
	PWM mode quiescent current (AW37419A)			8.5		mA
POWER SWITCH						
$R_{DSON(P)}$	P-type power switch on resistance	$I_{SW}=200mA$		170		m Ω
$R_{DSON(N)}$	N-type power switch on resistance	$I_{SW}=-200mA$		100		m Ω
I_{LIM}	P-type power switch peak current limit			1.5		A
		$V_{IN}=3.6V$, Open Loop Condition	1		1.7	A
f_{OSC}	Switching frequency			6		MHz
D_{MAX}	Maximum duty ratio				100	%
OUTPUT						
V_{OUT}	Output accuracy	$V_{OUT}=0.9V$, Load=10mA, PFM mode, AW37418A		0.890		V
		$V_{OUT}=0.9V$, Load=300mA, PWM mode, AW37418A		0.910		V
		$V_{OUT}=0.9V$, Load=10mA, AW37419A	0.882	0.900	0.918	V
T_{SS}	V_{OUT} step rise time from 0V to 0.9V			100		μs
T_{ON}	Turn on time(time for output voltage reaches 95% of final value after EN low to high transition)	$EN=low$ to high, $V_{IN}=3.6V$, $V_{OUT}=0.9V$, no load, $C_{OUT}=10\mu F$		220		μs
CONTROL LOGIC						
V_{EN_H}	EN pin logic high input threshold		1			V
V_{EN_L}	EN pin logic low input threshold				0.3	V
T_{OTP}	Over Temperature Protection			160		$^{\circ}C$
	Over Temperature Hysteresis			140		$^{\circ}C$

Electrical Characteristics

$V_{IN}=EN=3.6V$, $V_{OUT}=0.9V$, $C_{IN}=4.7\mu F$, $C_{OUT}=10\mu F$, $L=0.47\mu H$, $T_A=25^\circ C$, unless otherwise noted.

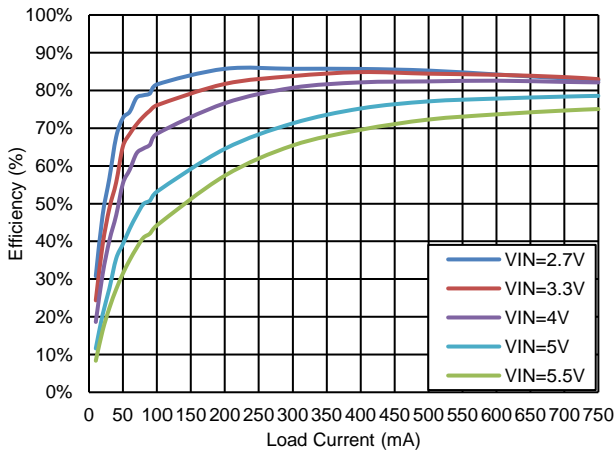


Figure 1. Efficiency vs. Load Current, AW37419A

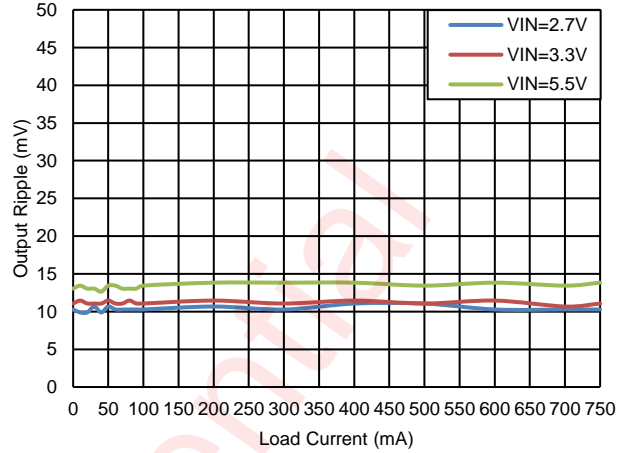


Figure 2. Output Ripple vs. Load Current, AW37419A

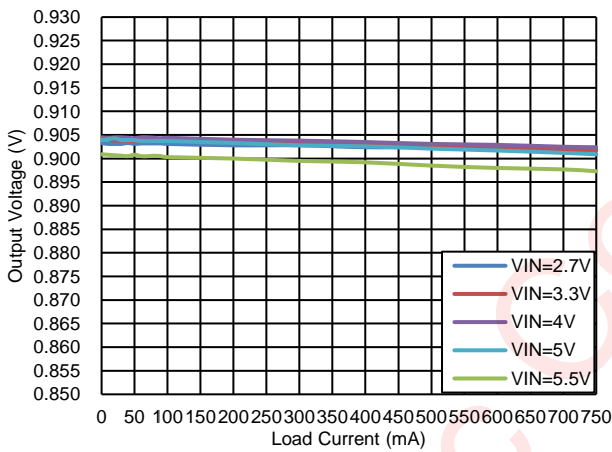


Figure 3. Output Voltage vs. Load Current, AW37419A

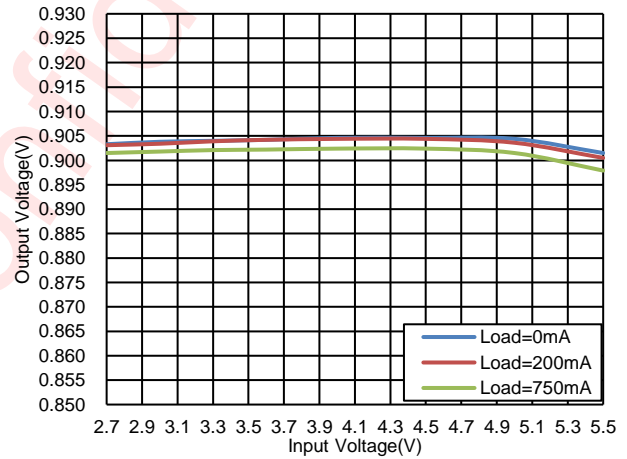


Figure 4. Output Voltage vs. Input Voltage, AW37419A

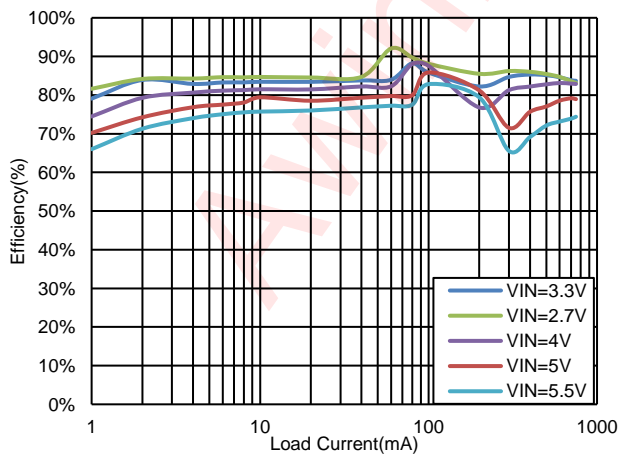


Figure 5. Efficiency vs. Load Current, AW37418A

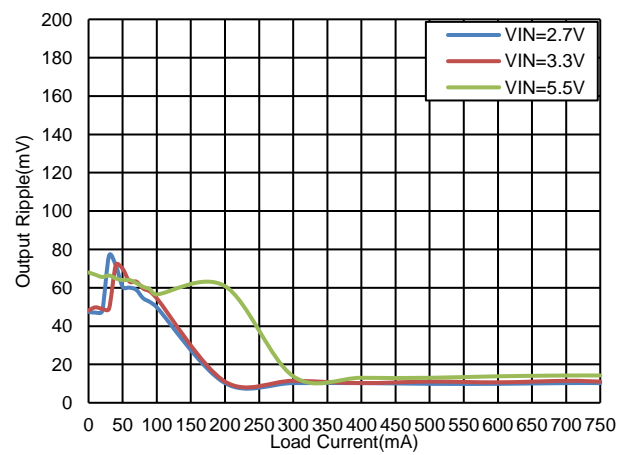


Figure 6. Output Ripple vs. Load Current, AW37418A

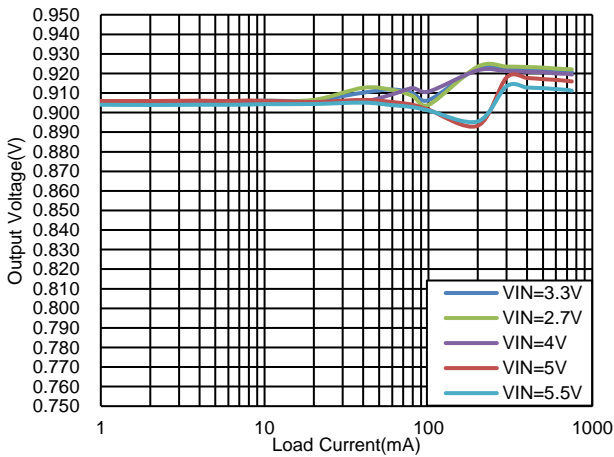


Figure 7. Output Voltage vs. Load Current, AW37418A

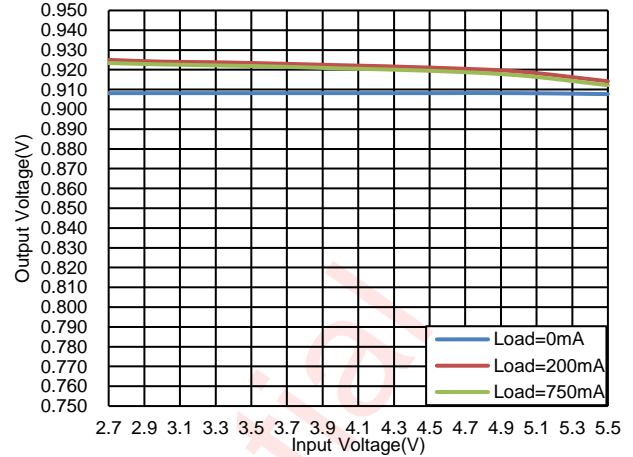


Figure 8. Output Voltage vs. Input Voltage, AW37418A

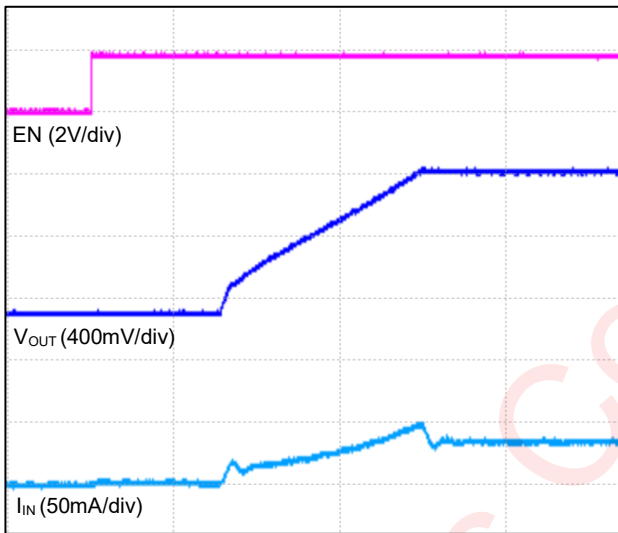


Figure 9. Start-up

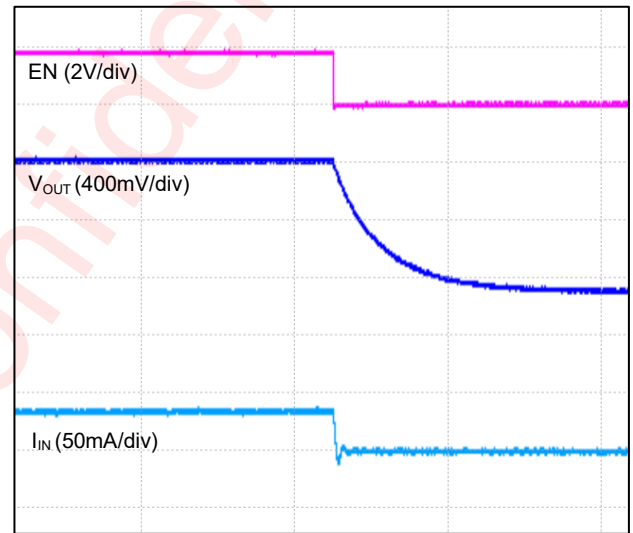


Figure 10. Shutdown

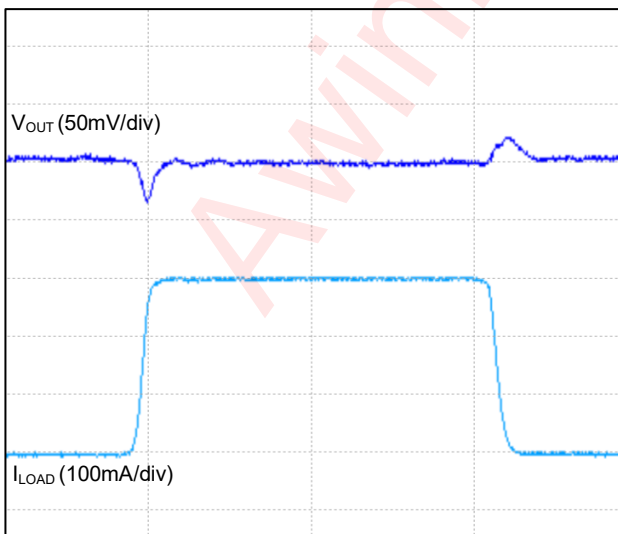


Figure 11. Load transient, 1mA-300mA-1mA, tr/tf=5µs, AW37418A

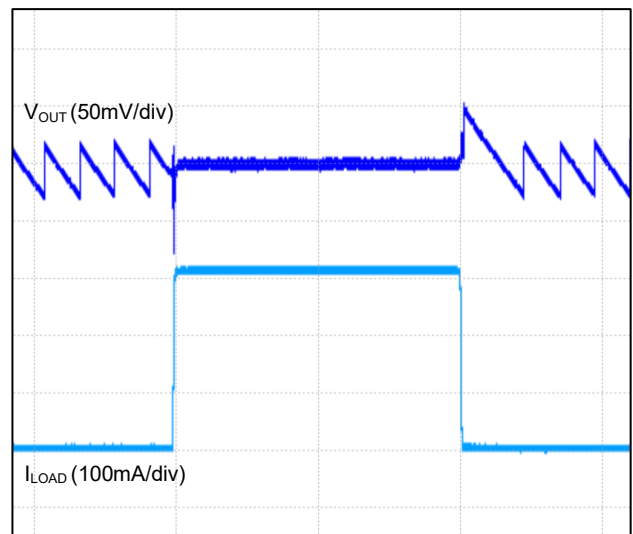


Figure 12. Load transient, 1mA-300mA-1mA, tr/tf=5µs, AW37418A

Detailed Functional Description

The AW37418 is a 6MHz single output step-down DC-DC converter with extremely small package. The AW37418 utilizes voltage-mode PWM control with synchronous rectification to provide maximum load current up to 750mA in high efficiency. The 6MHz switching frequency of AW37418 allows the utilization of small external components to reduce the size of the solutions. Maximum load range may vary from this depending on input voltage, output voltage, and the inductor chosen.

The AW37418 operates in three modes depending on load current demand: Pulse-Width-Modulation (PWM), Pulse-Frequency-Modulation (PFM) and Shutdown mode. In heavy load current condition, the AW37418 operates in PWM mode and automatically switches into PFM mode in light load condition. Shutdown mode turns off the device completely and reduces the current consumption to 0.1 μ A (typical).

High-side power PFET cycle-by-cycle current limit protection, low-side power NFET cycle-by-cycle sinking current limit, short-circuit-protection and on-chip thermal protection are also available on the AW37418.

The AW37418 is available in WLCSP-5B 0.888mm \times 0.968mm package. This package provides the smallest size for space-critical applications, while 6MHz operating switching frequency reducing the size of external components, only three external power components are required. Careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light.

Feature Description

Circuit Operation

At the beginning of each switching cycle, the 6MHz clock pulses set the PWM latch to turn on the internal high-side P-type power FET switch. The current flows from the input node to the output capacitor and loading through the PFET switch. The inductor limits the current to a ramp with a slope $(V_{IN}-V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, as the internal saw-tooth waveform voltage exceeds the output voltage of the error amplifier, the PWM comparator trips and resets the PWM latch to turn off the high-side PFET switch and to turn on the low-side NFET switch. As a result, the magnetic field of the inductor collapses, generating a voltage that forces the current from ground through the NFET switch to the output capacitor and load. The inductor current ramps down with a slope around V_{OUT}/L when the NFET switch is on.

By sending a duty-cycle modulated rectangular wave at SW to the inductor and output filter capacitor low-pass filter, the output voltage is regulated. The output voltage is equal to the average voltage at the SW pin.

Buck DC-to-DC Converter Operation

The AW37418 is a synchronous rectifier type buck converter with both high-side and low-side switches integrated on die. The AW37418 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

In PWM operation, the NFET synchronous rectifier is turned on in the second part of each cycle and turned off prior to the next cycle. No external transistors and diodes are required.

The device operates in three modes: Shutdown mode (EN=Low), PFM mode as operating at light load and PWM mode as operating at heavy load.

Shutdown Mode

The AW37418 enters shutdown mode as the voltage at EN pin below 0.3V or the input voltage below UVLO threshold voltage (2.05V). In shutdown mode, the typical current consumption of the whole chip is 0.1 μ A. Putting the voltage at the EN pin above 1V will enable the device.

PWM Mode Operation

In heavy load condition, the AW37418 operates in PWM mode from a fixed clock (6MHz). In PWM mode operation, the converter operates as a voltage-mode controller. The voltage mode PWM control allows the converter to achieve excellent load and line regulation. The output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET switch and turning on the PFET switch.

PFM Mode Operation

At light load condition, the AW37418 enters the PFM mode operation to save power and improve efficiency. During PFM mode operation, the AW37418 works in the peak-current-control, the inductor peak current is limited to 500mA. The output voltage is regulated by varying the switching frequency, proportional to loading current.

Inductor Peak Current Limitations

During PWM mode operation, peak inductor current is monitored and limited by the AW37418 current limiting circuitry. In PWM mode, the cycle-by-cycle current limit is 1500mA.

Short-circuit Protection

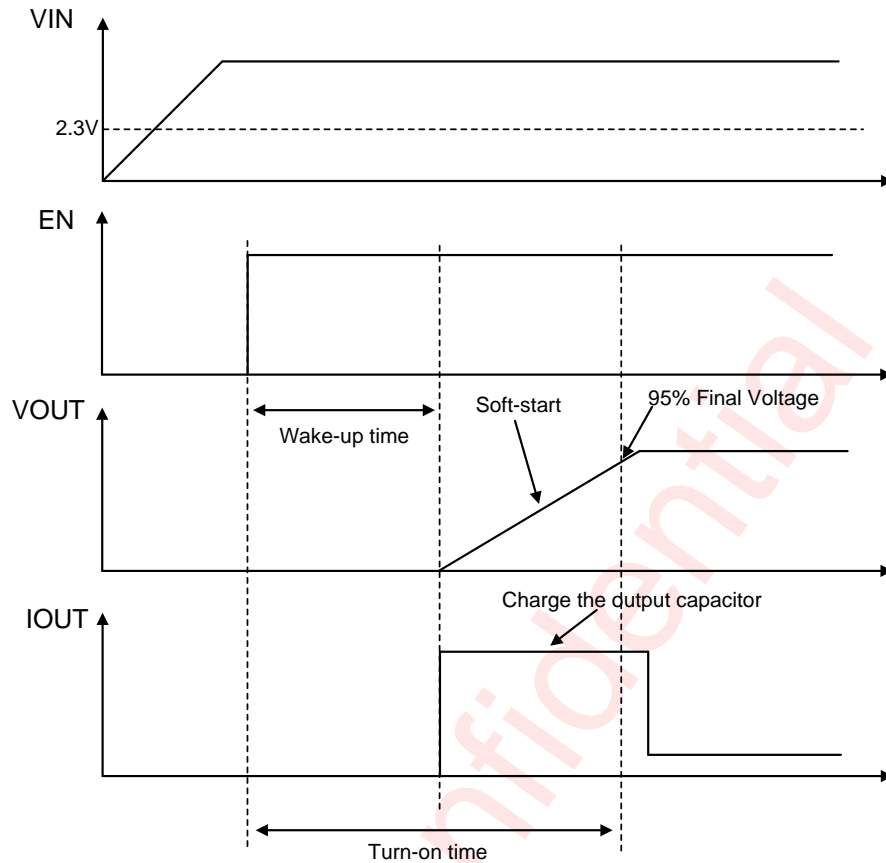
If an excessive load pulls the output voltage below 0.6V, AW37418 disables the NFET, the cycle-by-cycle current limit is reduced to 500mA, and the switching frequency decreases to 3MHz to protecting the part from excess current and thermal stress damages.

Thermal Protection

The thermal capability of IC can be exceeded due to buck converter output stage power level, therefore a thermal protection circuitry is implemented to prevent device from thermal damage. When the junction temperature exceeds around 160°C, the output rectifier stops switching, both PFET and NFET off. The AW37418 resumes switching as the junction temperature drops below 140°C.

Soft-start

The AW37418 features a soft-start circuit to limit inrush current during start-up. During start-up, the duty ratio of the SW voltage waveform is increased slowly until the output voltage reaches the setting value. Soft-start is activated if EN pin voltage goes from low to high after V_{IN} reaches 2.3V.



Application Information

Inductor Selection

Two main considerations must be considered when choosing an inductor: the inductor should not saturate and the inductor current ripple should be small enough to achieve the desired output voltage ripple.

The recommended value of inductance to ensure good performance is $1\mu\text{H}$ at bias current over the ambient temperature range. Shielding inductors radiates less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

$$I_{\text{SAT}} > I_{\text{OUT_MAX}} + I_{\text{RIPPLE}}$$

Where

- $I_{\text{OUT_MAX}}$ is the maximum load current (750mA)
- I_{RIPPLE} is the average-to-peak inductor current.

$$I_{\text{RIPPLE}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{2L} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times \frac{1}{f}$$

Where

- V_{IN} is the maximum input voltage in application.
- V_{OUT} is the output voltage

- L is the minimum inductor value including worst-case tolerances (30% drop can be considered)
- f is the minimum switching frequency

A more conservative and recommended approach is to choose an inductor that can support the maximum current limit of 1500mA.

Capacitor Selection

The AW37418 is designed for use with ceramic capacitors for its input and output filters. Use a 4.7μF ceramic capacitor for the input bypass filter and a 12.2μF ceramic for the output. The effective output capacitance should remain at least 8μF at DC bias and temperature conditions for stability reason. 25V of rated-voltage ceramic capacitors are suitable for full range output voltage applications. Ceramic capacitors type such as X5R, X7R are recommended for both filters. These types provide optimal balance between small size, cost, reliability, and performance for cell phones and similar applications.

The output filter capacitor absorbs the voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low equivalent series resistance (ESR) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple. The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be use. For a given peak-to-peak ripple current I_{LPP} in the inductor of the output filter, the output ripple across the output capacitor is the sum of three components as below.

$$V_{OUTPP} = V_{OUTPP(C)} + V_{OUTPP(ESR)} + V_{OUTPP(ESL)}$$

Where

- $V_{OUTPP(C)}$ is the ripple component coming from an equivalent total capacitance of the output capacitors.
- $V_{OUTPP(ESR)}$ is a ripple component from an equivalent ESR of the output capacitors.
- $V_{OUTPP(ESL)}$ is a ripple component from an equivalent ESL of the output capacitors.

In PWM operation mode, the three ripple components can be obtained by

$$V_{OUTPP(C)} = \frac{I_{LPP}}{8 \times C \times f_{sw}}$$

$$V_{OUTPP(ESR)} = I_{LPP} \times ESR$$

$$V_{OUTPP(ESL)} = \frac{ESL}{ESL + L} \times V_{IN}$$

And the peak-to-peak ripple current is:

$$I_{LPP} = \frac{(PV_{IN} - V_{OUT}) \times V_{OUT}}{PV_{IN} \times f_{sw} \times L}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUTPP(C)}$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUTPP} in PWM operation mode.

$$C_{MIN} = \frac{I_{LPP}}{8 \times V_{OUTPP} \times f_{sw}}$$

DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For C_{IN} , use of an 0603 size may also be considered if room is available on the system board.

The input filter capacitor supplies AC current drawn by the PFET switch of the AW37418 in the first part of each cycle and reduce the voltage ripple imposed on the input power source. One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better

decoupling in the input power supply rail. Ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding the input ripple voltage V_{INPP} is

$$C_{INMIN} = \frac{I_{LPP} \times (D - D^2)}{V_{INPP} \times f_{SW}}$$

Where $D=V_{OUT}/V_{IN}$.

In addition the input capacitor needs to be able to absorb the input current, which has a RMS value of:

$$I_{INRMS} = I_{OUTMAX} \times \sqrt{(D - D^2)}$$

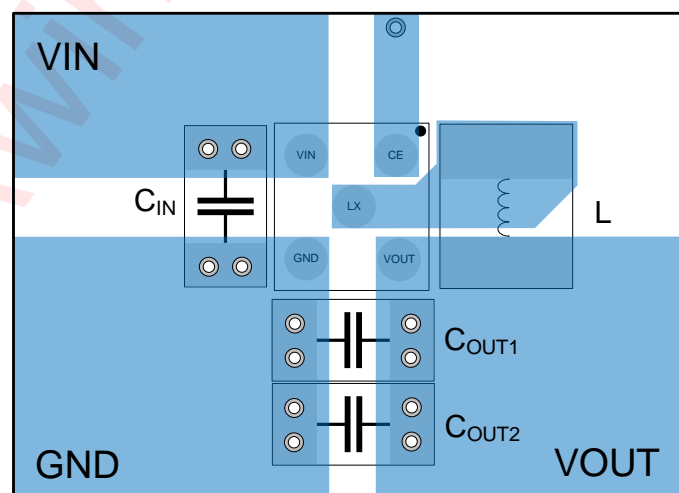
The input capacitor needs also to be sufficient to protect the device from over voltage spike and a minimum of 4.7 μ F capacitor is required. The input capacitor should be located as close as possible to the IC. PGND is connected to the ground terminal of the input cap which then connects to the ground plane. The PV_{IN} is connected to the V_{BAT} terminal of the input capacitor which then connects to the V_{BAT} plane.

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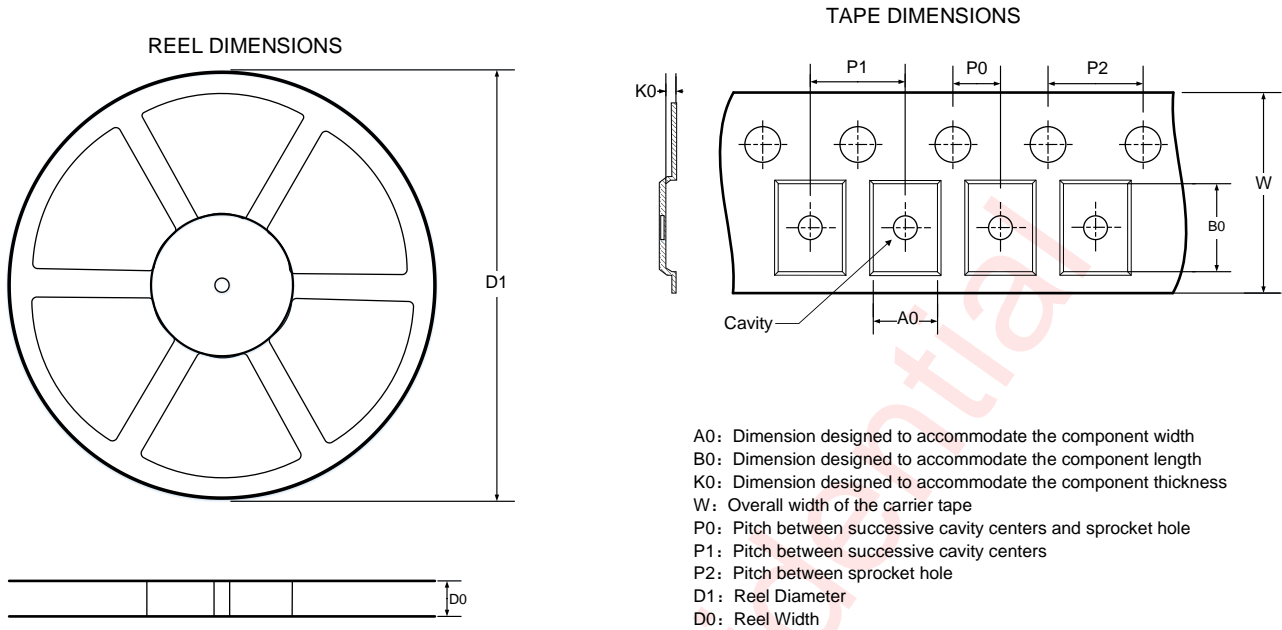
PCB Layout Consideration

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces, resulting in poor regulation or instability. To obtain the optimal performance, PCB layout should be considered carefully. Some guidelines:

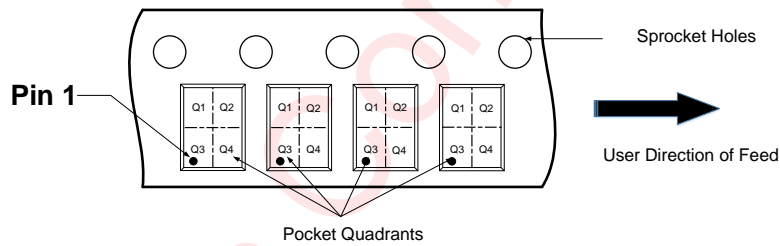
1. The V_{IN} and GND traces are especially recommended to be as wide as possible. The important criterion is symmetry to ensure the solder leads reflow evenly.
2. Place the AW37418, the inductor, and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise.
3. Place the input filter capacitor close to the V_{IN} and GND pads.
4. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the AW37418 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second of each cycle, current is pulled up from ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
5. Connect the ground pads of the AW37418 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane with several VIAs. This connection reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the AW37418 by giving it a low impedance ground connection.
6. Use side traces between the power components and for power connections to the DC-DC converter circuit which reduces voltage errors caused resistive losses across the traces.
7. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. The voltage feedback trace must remain close to the AW37418 circuit and should be routed directly from OUT to VOUT pin at the inductor and should be routed opposite to noise components. This trace placement allows fast feedback and reduces EMI radiated onto the voltage feedback trace of the DC-DC converter.



Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



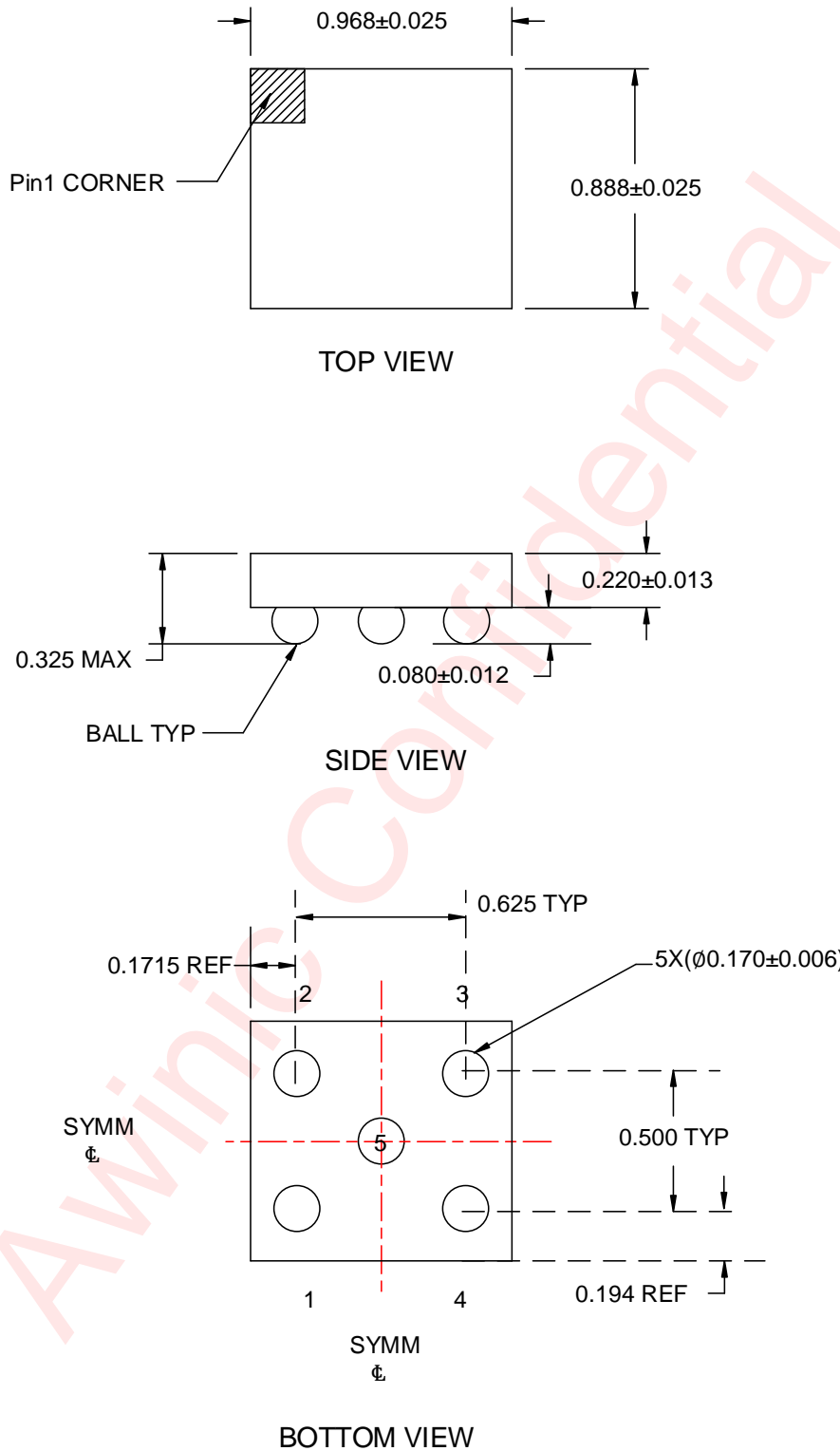
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0	8.40	0.98	1.07	0.40	2.00	2.00	4.00	8.00	Q3

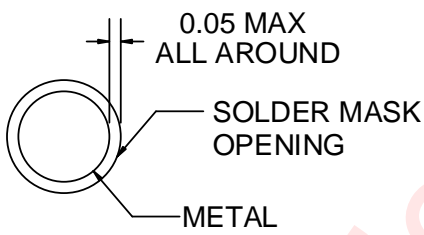
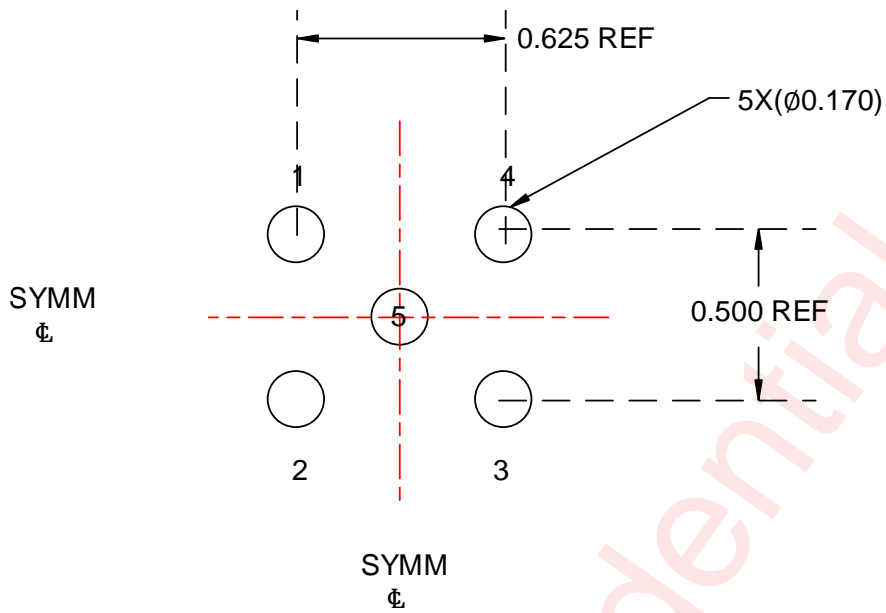
All dimensions are nominal

Package Description

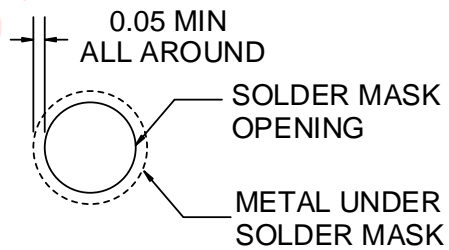


Unit:mm

Land Pattern Data



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2025	Officially released

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