钍地半导体
Tudi Semiconductor

# Product Specification

## TUDI-MAX3463/3464

+5V, Fail-Safe, 20Mbps, Profibus RS-485/
RS-422 Transceivers

网址 www.sztdbdt.com

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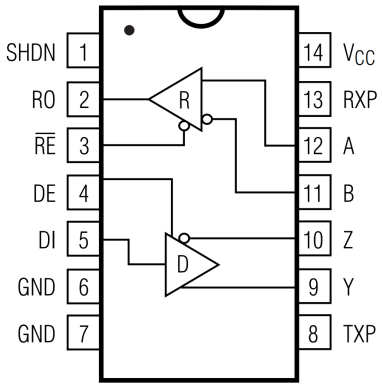
**semiconductor device manufacturer**

- Design
- research and development
- production
- and sales

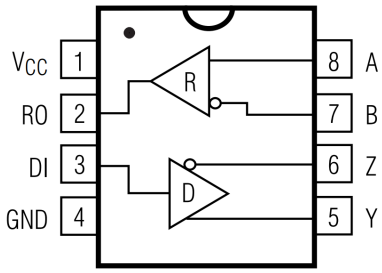
## Features

- Recommended for Profibus Applications
- Guaranteed 20Mbps Data Rate
- 20ns Transmitter and Receiver Propagation Delay
- 2ns Transmitter and Receiver Skew
- High Differential Driver Output Level (2.1V on 54Ω)
- Hot-Swap Versions
- 1μA Shutdown Supply Current
- Low Supply Current Requirements (2.5mA typ)
- Allow Up to 128 Transceivers on the Bus
- True Fail-Safe Receiver while Maintaining EIA/TIA-485 Compatibility
- Designed for Multipoint Transmissions on Long or Noisy Bus Lines
- Full Duplex and Half Duplex Versions Available
- Phase Controls to Correct for Twisted-Pair Reversal for 14-Pin Versions
- Current-Limiting and Thermal Shutdown for Driver Overload Protection

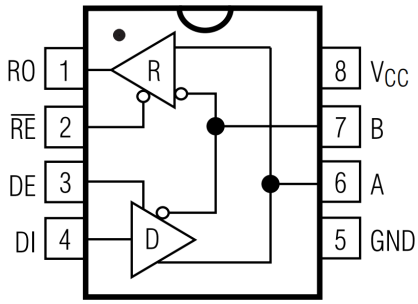
TOP VIEW




MAX3460
MAX3461




MAX3462




MAX3463
MAX3464

## Applications

High-Speed RS-485 Communications
High-Speed RS-422 Communications
Level Translators
Industrial-Control Local Area Networks
Profibus Applications

## General Description

The MAX3460 – MAX3464 are high-speed differential bus transceivers for RS-485 and RS-422 communications. They are designed to meet TIA/EIA-422-B, TIA/EIA-485-A, V.11, and X.27 standards. The trans-ceiver complies with the Profibus specification provid-ing +2.1V output level with a 54Ω load, 20Mbps data rate, and output skew less than 2ns. Each part contains one three-state differential line driver and one differen-tial input line receiver. The devices operate from a +5V supply and feature true fail-safe circuitry, which guaran-tees a logic-high receiver output when the receiver inputs are open or shorted. This enables all receiver outputs on a terminated bus to output logic highs when all transmitters are disabled.
All devices feature a 1/4 standard unit load receiver input impedance that allows 128 transceivers on the bus. Driver and receiver propagation delays are guar anteed under 20ns for multidrop,

clock distribution applications. Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry. The driver and receiver feature active-high and active-low enables, respective-ly, that can be connected together externally to serve as a direction control.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC}$) to GND .....-0.3V to +6V
Control Input Voltage ($\overline{RE}$, DE, DI, SHDN, TXP, RXP)
to GND.....-0.3V to ($V_{CC}$ + 0.3V)
Driver Output Voltage (Y, Z) to GND .....-8V to +13V
Receiver Input Voltage (A, B) to GND.....-8V to +13V
Differential Driver Output Voltage (Y - Z).....±8V
Differential Receiver Input (A - B).....±8V
Receiver Output Voltage (RO) to GND.....-0.3V to ($V_{CC}$ + 0.3V)
Output Driver Current (Y, Z) .....±250mA

Continuous Power Dissipation ($T_A$ = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin DIP (derate 9.09mW/°C above +70°C).....727mW
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
14-Pin DIP (derate 10mW/°C above +70°C).....800mW
Operating Temperature Range
MAX346_C__ .....0°C to +70°C
MAX346_E__.....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = +5V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Power-Supply Range | $V_{CC}$ | | | 4.75 | | 5.25 | V |
| **DRIVER** | | | | | | | |
| Differential Driver Output (no load) | $V_{OD}$ | Figure 5, R = ∞ | | | | $V_{CC}$ | V |
| Differential Driver Output | $V_{OD}$ | Figure 5, R = 27Ω | | 2.1 | | | V |
| Change in Magnitude of Differential Output Voltage | $\Delta V_{OD}$ | Figure 5, R = 50Ω or 27Ω (Note 2) | | | | 0.2 | V |
| Driver Common-Mode Output Voltage | $V_{OC}$ | Figure 5, R = 50Ω or 27Ω | | | | 3 | V |
| Change in Magnitude of Common-Mode Voltage | $\Delta V_{OC}$ | Figure 5, R = 50Ω or 27Ω (Note 2) | | | | 0.2 | V |
| Input High Voltage | $V_{IH}$ | DE, DI, $\overline{RE}$, SHDN | | 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | DE, DI, $\overline{RE}$, SHDN | | | | 0.8 | V |
| Input Hysteresis | $V_{HYS}$ | DE, DI, $\overline{RE}$, SHDN | | | 50 | | mV |
| Output Leakage (Y and Z) Full Duplex | $I_O$ | DE = GND, $V_{CC}$ = GND or +5.25V | $V_{IN}$ = +12V | | | +125 | µA |
| | | | $V_{IN}$ = -7V | -100 | | | |
| Input Current | $I_{IN}$ | DI, $\overline{RE}$, DE, SHDN | | | | ±1 | µA |
| Pulldown Current | | RXP = TXP = $V_{CC}$ | | 5 | 15 | 30 | µA |
| Driver Short-Circuit Output Current (Note 3) | $I_{OSD}$ | 0 ≤ $V_{OUT}$ ≤ 12V, output low | | | | +250 | mA |
| | | -7V ≤ $V_{OUT}$ ≤ $V_{CC}$, output high | | -250 | | | |
| Driver Short-Circuit Foldback Output Current (Note 3) | $I_{OSFD}$ | ($V_{CC}$ - 1V) ≤ $V_{OUT}$ ≤ 12V, output low | | +25 | | | mA |
| | | -7V ≤ $V_{OUT}$ ≤ 1V, output high | | | | -25 | |
| Thermal Shutdown Threshold | | | | | 140 | | °C |
| **RECEIVER** | | | | | | | |
| Differential Input Capacitance | $C_{A, B}$ | | | | 8 | | pF |
| Input Current (A and B) Full Duplex | $I_{A, B}$ | DE = GND, $V_{CC}$ = GND or 5.25V | $V_{IN}$ = +12V | | | 250 | µA |
| | | | $V_{IN}$ = -7V | -200 | | | |
| Receiver Differential Threshold Voltage | $V_{TH}$ | -7V ≤ $V_{CM}$ ≤ 12V | | -200 | -125 | -50 | mV |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = +5V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Receiver Input Hysteresis | $\Delta V_{TH}$ | $V_A + V_B = 0$ | | 20 | | mV |
| Receiver Output High Voltage | $V_{OH}$ | $I_O$ = -4mA, $V_A - V_B = V_{TH}$ | $V_{CC}$ - 1.5 | | | V |
| Receiver Output Low Voltage | $V_{OL}$ | $I_O$ = 4mA, $V_B - V_A = V_{TH}$ | | | 0.4 | V |
| Three-State Output Current at Receiver | $I_{OZR}$ | $0 \le V_O \le V_{CC}$ | | | ±1 | µA |
| Receiver Input Resistance | $R_{IN}$ | $-7V \le V_{CM} \le 12V$ | 48 | | | kΩ |
| Receiver Output Short-Circuit Current | $I_{OSR}$ | $0 \le V_{RO} \le V_{CC}$ | ±7 | | ±95 | mA |
| **SUPPLY CURRENT** | | | | | | |
| Normal Operation (static condition) | $I_Q$ | No load, DI = $V_{CC}$ or DI = GND | | 2.5 | 4 | mA |
| Supply Current in SHDN | $I_{SHDN}$ | DE = GND and $\overline{RE}$ = $V_{CC}$, or SHDN = $V_{CC}$ | | 1 | 10 | µA |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Driver Propagation Delay | $t_{PLH}$<br>$t_{PHL}$ | Figures 6 and 7, $R_{DIFF}$ = 54Ω, $C_L$ = 50pF | | | 20 | ns |
| Driver Differential Output Rise or Fall Time | $t_R$<br>$t_F$ | Figures 6 and 7, $R_{DIFF}$ = 54Ω, $C_L$ = 50pF | | | 20 | ns |
| Driver Output Skew $\lvert t_{PLH} - t_{PHL} \rvert$ | $t_{SKEW}$ | Figures 6 and 7, $R_{DIFF}$ = 54Ω, $C_L$ = 50pF, TXP = GND or floating | | | 2 | ns |
| Maximum Data Rate | | | 20 | | | Mbps |
| Driver Enable to Output High | $t_{ZH}$ | Figures 8 and 9, S2 closed, $R_L$ = 500Ω, $C_L$ = 50pF | | | 100 | ns |
| Driver Enable to Output Low | $t_{ZL}$ | Figures 8 and 9, S1 closed, $R_L$ = 500Ω, $C_L$ = 50pF | | | 100 | ns |
| Driver Disable Time from Low | $t_{LZ}$ | Figures 8 and 9, S1 closed, $R_L$ = 500Ω, $C_L$ = 50pF | | | 100 | ns |
| Driver Disable Time from High | $t_{HZ}$ | Figures 8 and 9, S2 closed, $R_L$ = 500Ω, $C_L$ = 50pF | | | 100 | ns |
| Receiver Propagation Delay | $t_{PLH}$<br>$t_{PHL}$ | Figure 10, $C_L$ = 15pF (Note 4) | | | 20 | ns |
| Receiver Output Skew $\lvert t_{PLH} - t_{PHL} \rvert$ | $t_{SKEW}$ | Figure 10, $C_L$ = 15pF, RXP = GND or floating (Note 4) | | | 2 | ns |
| Receiver Enable to Output Low | $t_{ZL}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S1 closed (Note 4) | | | 100 | ns |
| Receiver Enable to Output High | $t_{ZH}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S2 closed (Note 4) | | | 100 | ns |
| Receiver Disable Time from Low | $t_{LZ}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S1 closed (Note 4) | | | 100 | ns |
| Receiver Disable Time from High | $t_{HZ}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S2 closed (Note 4) | | | 100 | ns |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$ = +5V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Time to Shutdown | $t_{SHDN}$ | (Note 5) | 50 | | 800 | ns |
| Driver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | Figures 8 and 9, $R_L$ = 500Ω, $C_L$ = 50pF, S2 closed (Note 5) | | | 4 | µs |
| Driver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | Figures 8 and 9, $R_L$ = 500Ω, $C_L$ = 50pF, S1 closed (Note 5) | | | 4 | µs |
| Receiver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S2 closed (Notes 4, 5) | | | 4 | µs |
| Receiver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | Figures 8 and 11, $R_L$ = 1kΩ, $C_L$ = 15pF, S1 closed (Notes 4, 5) | | | 4 | µs |

**Note 1:** All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

**Note 2:** $\Delta V_{OD}$ and $\Delta V_{OC}$ are the changes in $V_{OD}$ and $V_{OC}$, respectively, when the DI input changes state.

**Note 3:** The short-circuit output current applies to peak current just prior to foldback-current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

**Note 4:** Capacitive load includes test probe and fixture capacitance.

**Note 5:** Shutdown is enabled by bringing $\overline{RE}$ high and DE low or by bringing SHDN high. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 800ns, the device is guaranteed to have entered shutdown.

## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX3460/ MAX3461 | MAX3462 | MAX3463/ MAX3464 | | |
| FULL DUPLEX | | HALF DUPLEX | | |
| 1 | — | — | SHDN | Shutdown. Drive SHDN high to enter low-power shutdown mode. |
| 2 | 2 | 1 | RO | Receiver Output. When $\overline{RE}$ is low and (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low. |
| 3 | — | 2 | $\overline{RE}$ | Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. |
| 4 | — | 3 | DE | Driver Output Enable. Drive DE high to enable driver output. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. |
| 5 | 3 | 4 | DI | Driver Input. With DE high, a low on DI forces the noninverting output low and the inverting output high. Similarly, a high on DI forces the noninverting output high and the inverting output low. |
| 6, 7 | 4 | 5 | GND | Ground |
| 8 | — | — | TXP | Transmitter Phase. Connect TXP to GND, or leave unconnected for normal transmitter phase/polarity. Connect TXP to $V_{CC}$ to invert the transmitter phase/polarity. TXP has an internal 15µA pulldown. |
| 9 | 5 | — | Y | Noninverting Driver Output |
| 10 | 6 | — | Z | Inverting Driver Output |
| 11 | 7 | — | B | Inverting Receiver Input |
| 12 | 8 | — | A | Noninverting Receiver Input |
| 13 | — | — | RXP | Receiver Phase. Connect RXP to GND, or leave unconnected for normal receiver phase/polarity. Connect RXP to $V_{CC}$ to invert the receiver phase/polarity. RXP has an internal 15µA pulldown. |
| 14 | 1 | 8 | $V_{CC}$ | Positive Supply: +4.75V ≤ $V_{CC}$ ≤ +5.25V. Bypass $V_{CC}$ to GND with a 0.1µF capacitor. |
| — | — | 7 | B | Inverting Receiver Input and Inverting Driver Output |
| — | — | 6 | A | Noninverting Receiver Input and Noninverting Driver Output |

## Function Tables

### MAX3460/MAX3461

| TRANSMITTING | | | | | |
|---|---|---|---|---|---|
| INPUTS | | | | OUTPUTS | |
| $\overline{RE}$ | DE | DI | SHDN | Z | Y |
| X | 1 | 1 | 0 | 0 | 1 |
| X | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | X | 0 | High-Z | High-Z |
| 1 | 0 | X | X | Shutdown | |
| X | X | X | 1 | Shutdown | |

| RECEIVING | | | | |
|---|---|---|---|---|
| INPUTS | | | | OUTPUT |
| $\overline{RE}$ | DE | A–B | SHDN | RO |
| 0 | X | ≥ -0.05V | 0 | 1 |
| 0 | X | ≤ -0.2V | 0 | 0 |
| 0 | X | Open/Shorted | 0 | 1 |
| 1 | 1 | X | 0 | High-Z |
| 1 | 0 | X | X | Shutdown |
| X | X | X | 1 | Shutdown |

### MAX3462

| TRANSMITTING | | |
|---|---|---|
| INPUT | OUTPUTS | |
| DI | Z | Y |
| 1 | 0 | 1 |
| 0 | 1 | 0 |

| RECEIVING | |
|---|---|
| INPUTS | OUTPUT |
| A–B | RO |
| ≥ -0.05V | 1 |
| ≤ -0.2V | 0 |
| Open/Shorted | 1 |

### MAX3463/MAX3464

| TRANSMITTING | | | | |
|---|---|---|---|---|
| INPUTS | | | OUTPUTS | |
| $\overline{RE}$ | DE | DI | B | A |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | High-Z | High-Z |
| 1 | 0 | X | Shutdown | |

| RECEIVING | | | |
|---|---|---|---|
| INPUTS | | | OUTPUT |
| $\overline{RE}$ | DE | A–B | RO |
| 0 | X | ≥ -0.05V | 1 |
| 0 | X | ≤ -0.2V | 0 |
| 0 | X | Open/Shorted | 1 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | Shutdown |

## Pin Configurations and Typical Operating Circuit

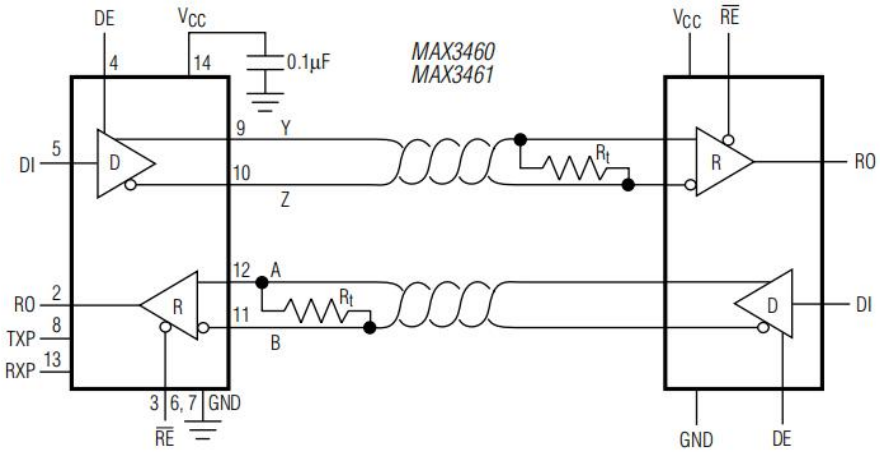



Figure 1. MAX3460/MAX3461 Pin Configuration and Typical Full-Duplex Operating Circuit

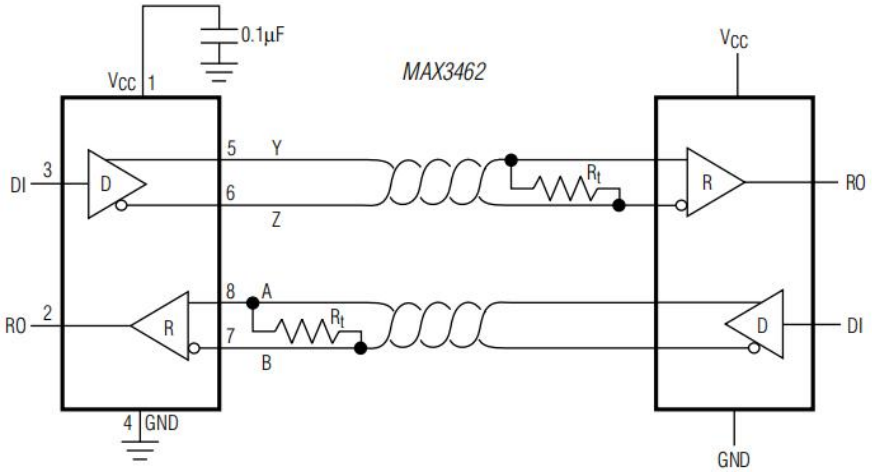
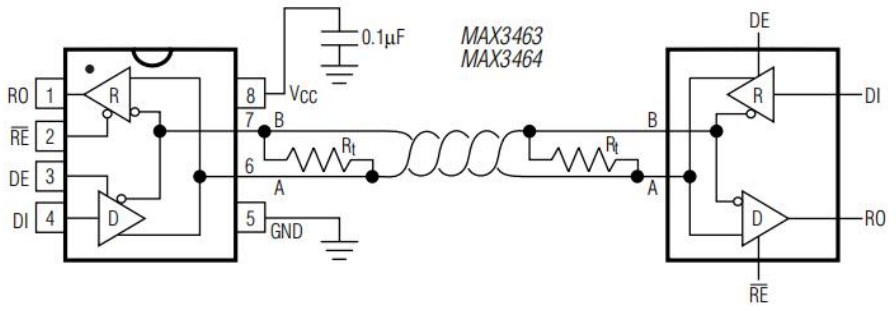



Figure 2. MAX3462 Pin Configuration and Typical Full-Duplex Operating Circuit




NOTE: PIN LABELS Y AND Z ON TIMING, TEST, AND WAVEFORM DIAGRAMS REFER TO PINS A AND B WHEN DE IS HIGH.

Figure 3. MAX3463/MAX3464 Pin Configuration and Typical Full-Duplex Operating Circuit

## Detailed Description

The MAX3460–MAX3464 high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). The MAX3460–MAX3464's driver slew rates allow transmit speeds up to 20Mbps.

The MAX3463 and MAX3464 are half-duplex transceivers, while the MAX3460, MAX3461, and MAX3462 are full-duplex transceivers. All of these parts operate from a single +5V supply. Drivers are output short-circuit current limited. Thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high-impedance state. The MAX3460 and MAX3463 devices have a hot-swap input structure that prevents disturbances on the differential signal lines when a circuit board is plugged into a "hot" backplane (see *Hot Swap* section). All devices have output levels that are compatible with Profibus standards.

### True Fail-Safe

The MAX3460–MAX3464 guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic high. If A - B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX3460–MAX3464, this results in a logic high with a 50mV minimum noise margin. Unlike previous true fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

### Hot-Swap Capability

#### Hot-Swap Inputs

When circuit boards are inserted into a "hot" or powered backplane, disturbances to the enable and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the output drivers are high impedance and are unable to drive the DE input of the MAX3460/MAX3463 to a defined logic level. Leakage currents up to 10µA from the high-impedance output could cause DE to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of $V_{CC}$ or GND to DE. These factors could improperly enable the driver.

When $V_{CC}$ rises, an internal pulldown circuit holds DE low for around 15µs. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

#### Hot-Swap Input Circuitry

The MAX3460/MAX3463 enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 4). When $V_{CC}$ ramps from 0, an internal 15µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a 100µA current sink, pull DE to GND through a 5.6kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 15µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever $V_{CC}$ drops below 1V, the hot-swap input is reset.

For $\overline{RE}$ there is a complimentary circuit employing two PMOS devices pulling $\overline{RE}$ to $V_{CC}$.

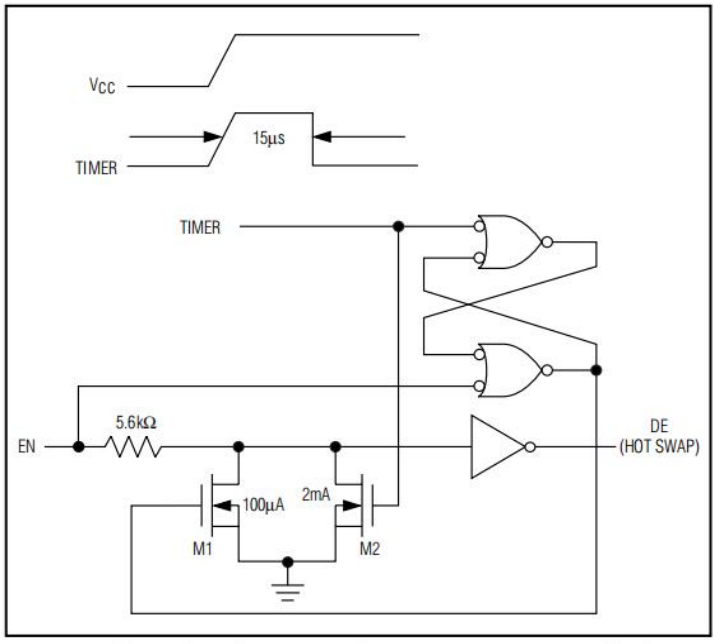



*Figure 4. Simplified Structure of the Driver Enable Pin (DE)*

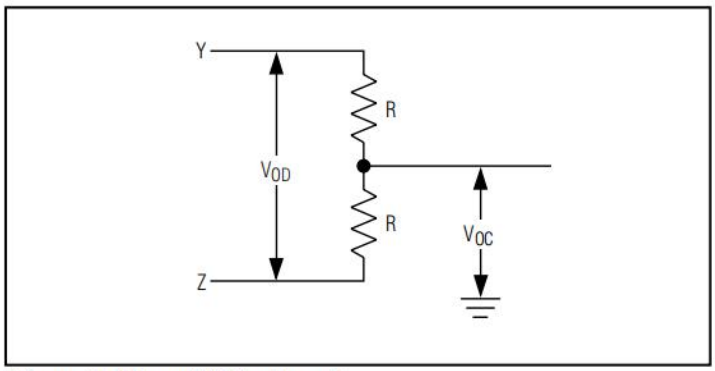



Figure 5. Driver DC Test Load

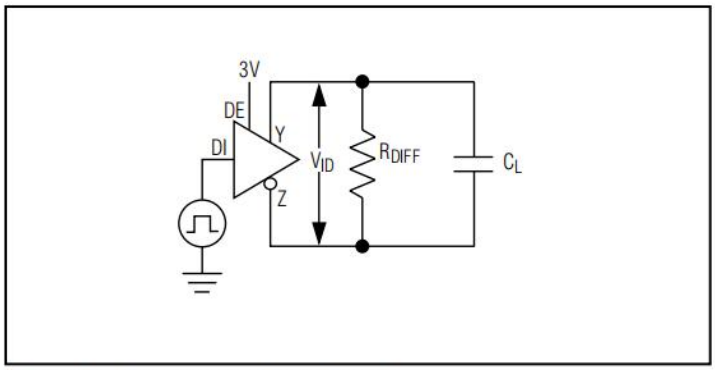



Figure 6. Driver Timing Test Circuit

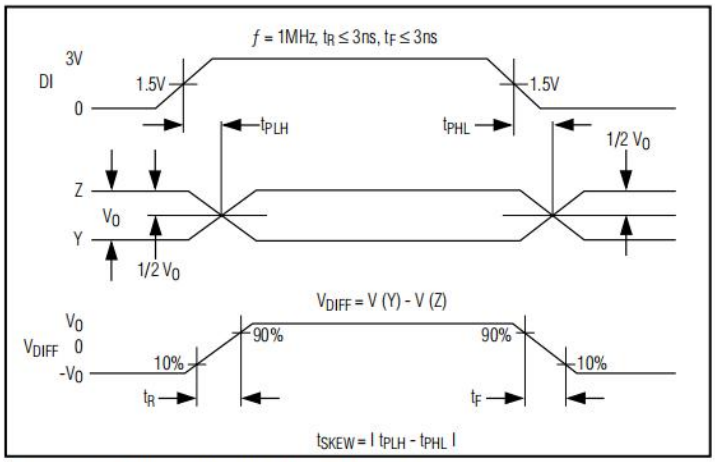



Figure 7. Driver Propagation Delays

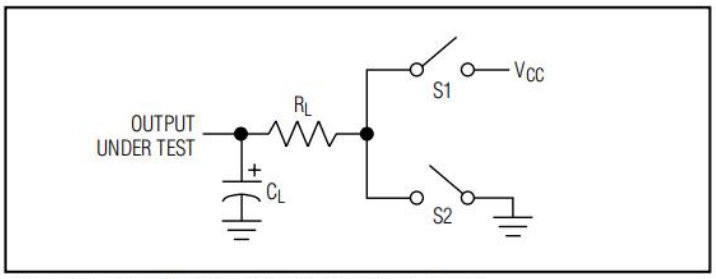



Figure 8. Enable/Disable Timing Test Load

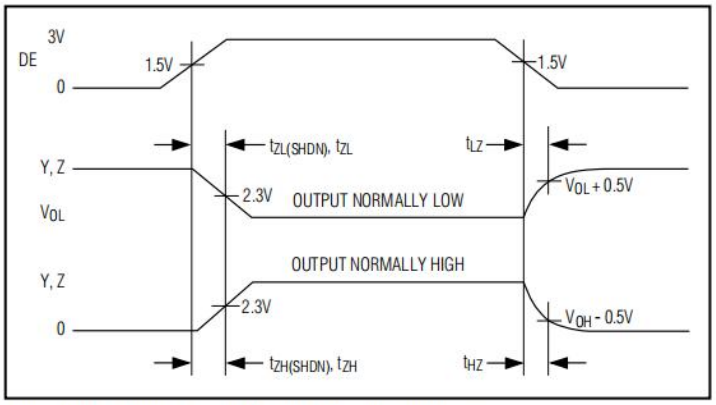



Figure 9. Driver Enable and Disable Times

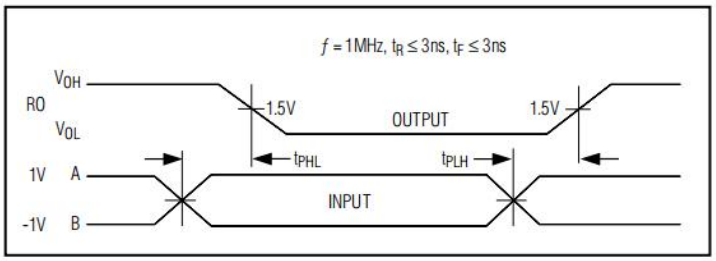



Figure 10. Receiver Propagation Delays

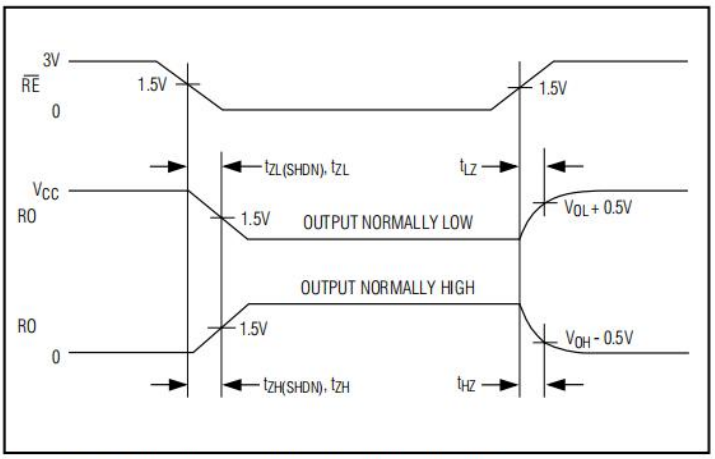



Figure 11. Receiver Enable and Disable Times

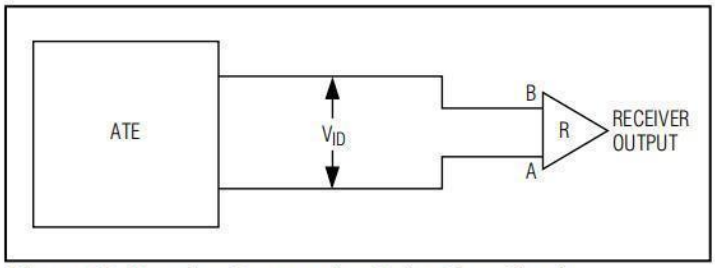



*Figure 12. Receiver Propagation Delay Test Circuit*

## Applications Information

### 128 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (one-unit load), and the standard driver can drive up to 32 unit loads. The MAX3460–MAX3464 family of transceivers has a 1/4-unit-load receiver input impedance (48kΩ), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

### Low-Power Shutdown Mode (except MAX3462)

Low-power shutdown mode is initiated by bringing SHDN high (MAX3460/MAX3461), or both $\overline{RE}$ high and DE low. In shutdown, the devices typically draw only 1µA of supply current. $\overline{RE}$ and DE can be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns, the parts are guaranteed to enter shutdown.

### Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +140°C.

### Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in the *Typical Operating Characteristics*. The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is a maximum of 2ns. The driver skew time $|t_{PLH} - t_{PHL}|$ is also a maximum of 2ns.

### Typical Applications

The MAX3460–MAX3464 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 13 and 14 show typical network applications circuits. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

### Profibus Termination

The MAX3460–MAX3464 are designed for driving Profibus termination networks. With a worst-case loading of two termination networks with 220Ω termination impedance and 390Ω pullups and pulldowns, the drivers can drive $V_{A-B}$> 2.1V output.

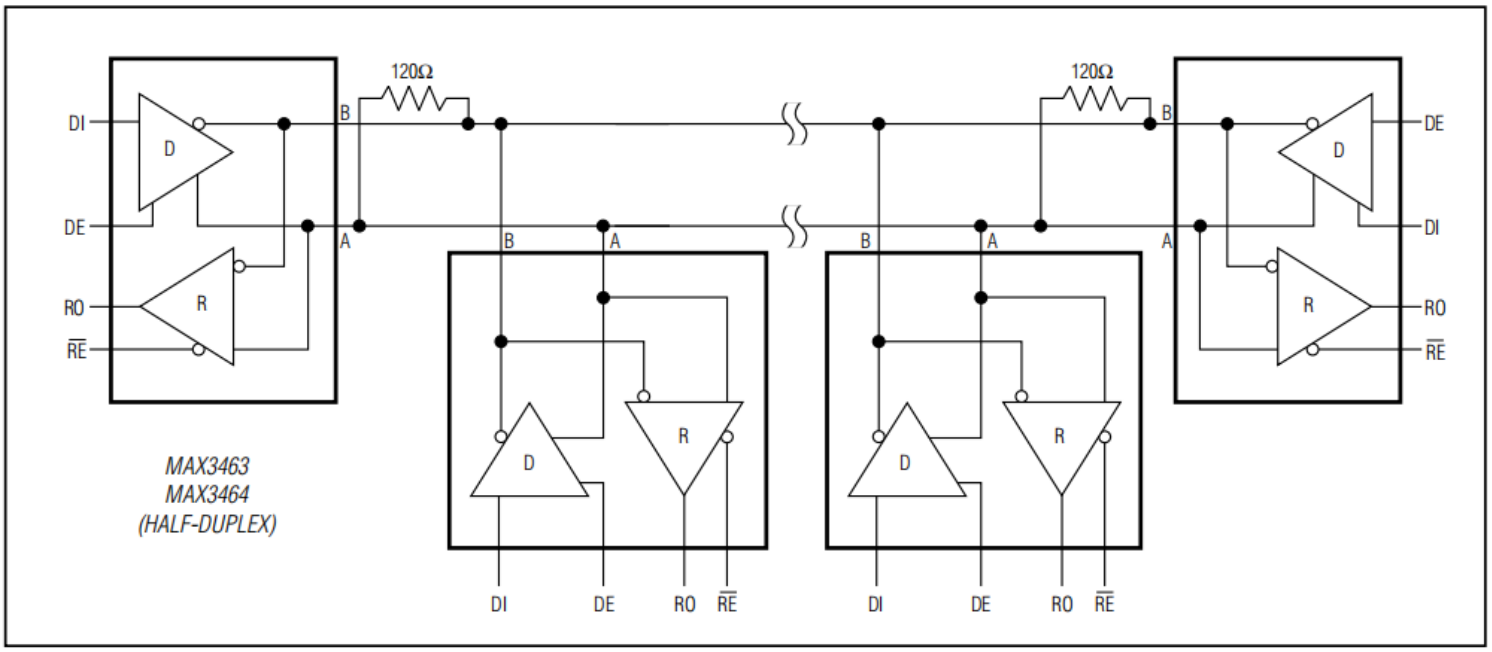



Figure 13. Typical Half-Duplex RS-485 Network

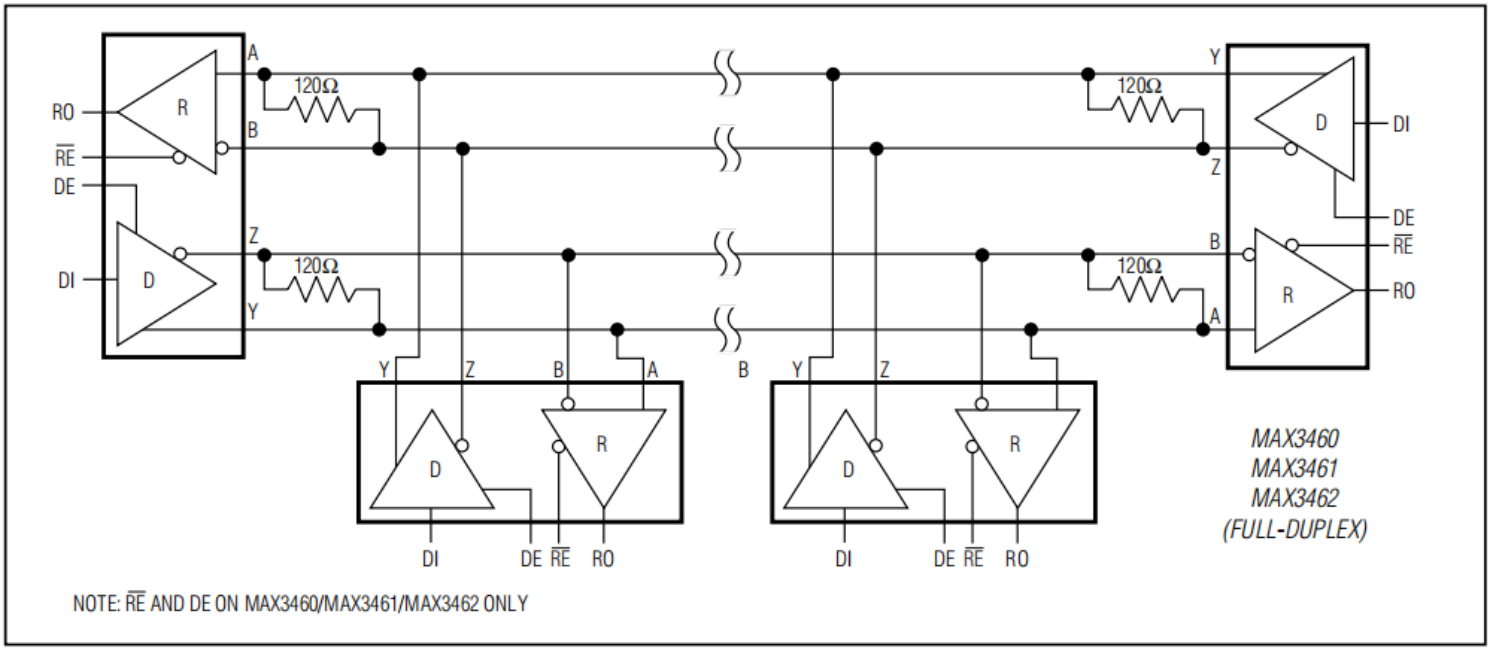
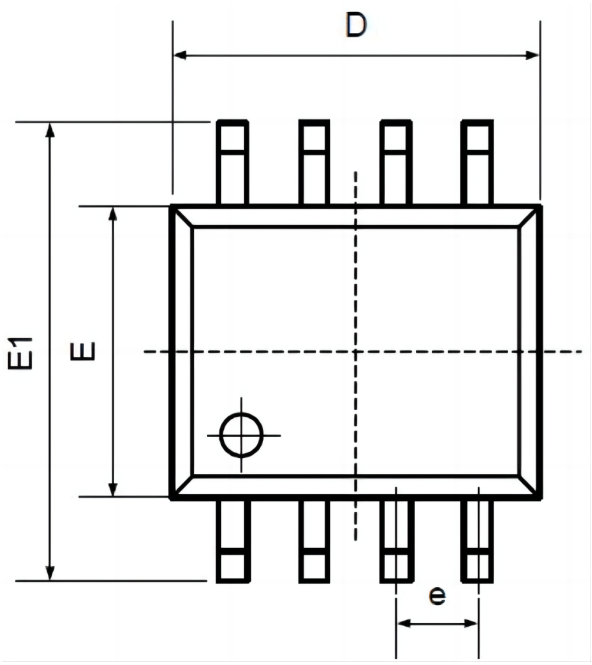


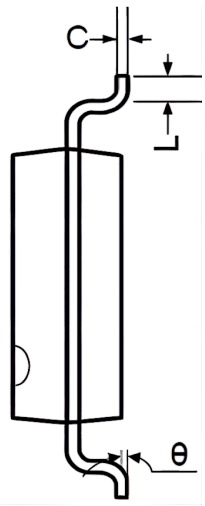

Figure 14. Typical Full-Duplex RS-485 Network

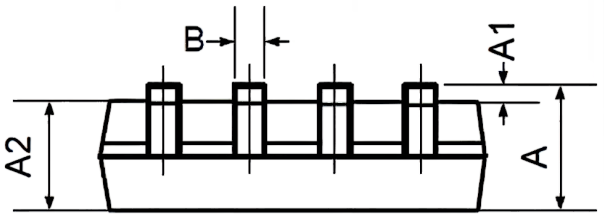
## ORDERING INFORMATION

| Order Number | Package | Package Quantity | Marking On The park |
|---|---|---|---|
| MAX3463CPA-TUDI | DIP8 | Tube,50,A box of 2000 | MAX3463CPA |
| MAX3463CSA-TUDI | SOP8 | Tape,Reel,2500 | MAX3463CSA |
| MAX3463EPA-TUDI | DIP8 | Tube,50,A box of 2000 | MAX3463EPA |
| MAX3463ESA-TUDI | SOP8 | Tape,Reel,2500 | MAX3463ESA |
| MAX3464CPA-TUDI | DIP8 | Tube,50,A box of 2000 | MAX3464CPA |
| MAX3464CSA-TUDI | SOP8 | Tape,Reel,2500 | MAX3464CSA |
| MAX3464EPA-TUDI | DIP8 | Tube,50,A box of 2000 | MAX3464EPA |
| MAX3464ESA-TUDI | SOP8 | Tape,Reel,2500 | MAX3464ESA |

# Package SOP8

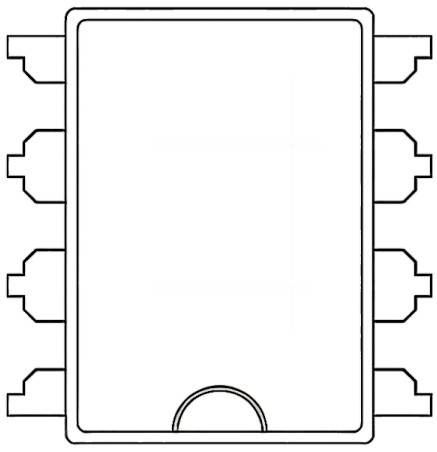


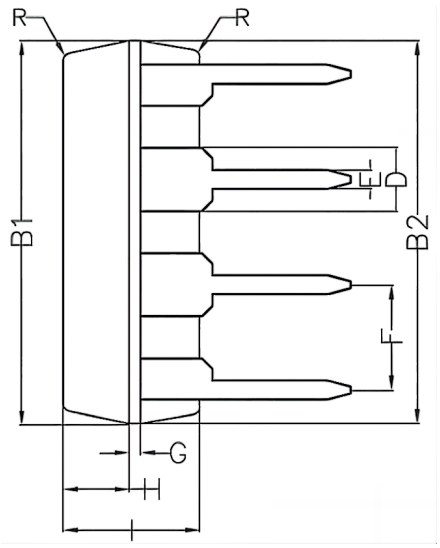



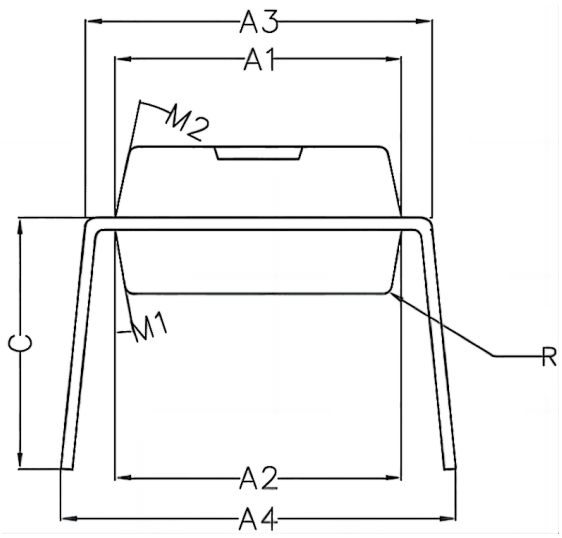




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# Package DIP8






| Symbol | Min | Non | Max |
|---|---|---|---|
| A1 | 6.28 | 6.33 | 6.38 |
| A2 | 6.33 | 6.38 | 6.43 |
| A3 | 7.52 | 7.62 | 7.72 |
| A4 | 7.80 | 8.40 | 9.00 |
| B1 | 9.15 | 9.20 | 9.25 |
| B2 | 9.20 | 9.25 | 9.30 |
| C | | 5.57 | |
| D | | 1.52 | |
| E | 0.43 | 0.45 | 0.47 |
| F | | 2.54 | |
| G | | 0.25 | |
| H | 1.54 | 1.59 | 1.64 |
| 工 | 3.22 | 3.27 | 3.32 |
| R | | 0.20 | |
| M1 | 9° | 10° | 11° |
| M2 | 11° | 12° | 13° |

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