



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-TPA321

0.85W MONO AUDIO POWER AMPLIFIER WITH DIFFERENTIAL INPUTS

网址 www.sztdbdt.com Q

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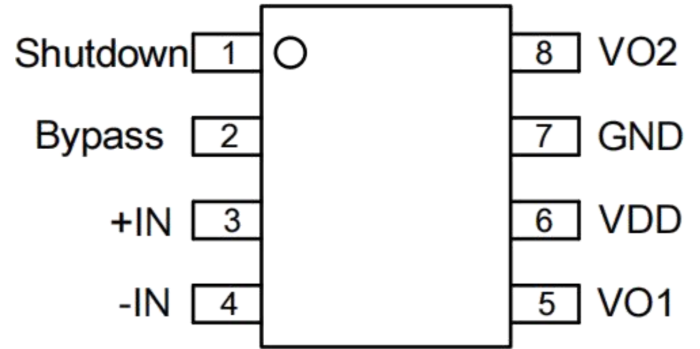
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- PO at 10% THD+N,1kHz
- TPA321 load 0.85W
- Shutdown Current 0.6uA(typ)
- Supply Voltage Range 2.0V to 5.5 V
- THD at 1kHz at 1W Continuous Average Output Power into 8Ω 0.5%(max)
- No Output Coupling Capacitors,Bootstrap Capacitors, or Snubber Circuits Required.
- Unity-gain Stable
- SOIC,or PDIP Packaging.
- External Gain Configuration Capability



TPA321 Pin Diagram

Description

The TPA321 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA321 can deliver 0.85W of continuous power into a BTL 8-Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment.

Applications

- Portable Computers
- Desktop Computers
- Low Voltage Audio Systems



Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage			6.0V
Supply Temperature			-65°C to +150°C
Input Voltage			-0.3V to VDD to +0.3V
Power Dissipation(3)			Internally Limited
ESD Susceptibility(4)			5000V
ESD Susceptibility ⁵⁾			250V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase(60 sec.)	215°C
		Infrared(15 sec.)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the TPA321, $T_{JMAX} = 150^\circ\text{C}$. For the θ_{JA} 's for different packages, please see the Application Information section or the absolute maximum ratings section.

(4) Human body model, 100pF discharged through a 1.5kΩ resistor.

(5) Machine Model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
Supply Voltage	$2.0\text{V} \leq V_{DD} \leq 5.5\text{V}$

Electrical Characteristics⁽¹⁾⁽²⁾

The following specifications apply for $V_{DD} = 5\text{V}$ and $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	TPA321			Units
			Min(3)	Typical	Limit(3)	
VDD	Supply Voltage			2	5.5	V
DD	Quiescent Power Supply Current	$V_{IN} = 0\text{V}, I_O = 0\text{A}$		6.5	10.0	mA
ISD	Shutdown Current	$V_{PIN1} = V_{DD}$		0.6	2	μA
Vos	Output Offset Voltage	$V_{IN} = 0\text{V}$		5.0	50	mV

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(2) All voltages are measured with respect to the ground pin, unless otherwise specified.

(3) Typicals are specified at 25°C and represent the parametric norm.



Electrical Characteristics⁽¹⁾⁽²⁾ (continued)

The following specifications apply for $V_{DD} = 5V$ and $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	TPA321			Units
			Min(3)	Typical(4)	Limit(3)	
P_o	Output Power	THD=1%, $f=1kHz$ $R_L=8\Omega$ (5)		2.38 2 1.2		W
		THD+N=10%, $f=1kHz$ $R_L=8\Omega$ (5)		3 2.5 1.5		W
THD+N	Total Harmonic Distortion+Noise	$20Hz \leq f \leq 20kHz$, $A_v=2$ $R_L=8\Omega$, $P_o=1W$		0.13 0.25		%
PSRR	Power Supply Rejection Ratio	$V_{DD}=4.9V$ to $5.1V$		60		dB

External Components Description

Components		Functional Description
1.	R_i	Inverting input resistance that sets the closed-loop gain in conjunction with R_f . This resistor also forms a high pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor that blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, Proper Selection of External Components , for an explanation of how to determine the value of C_i .
3.	R_f	Feedback resistance that sets the closed-loop gain in conjunction with R_i .
4.	C_S	Supply bypass capacitor that provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor that provides half-supply filtering. Refer to the section, Proper Selection of External Components , for information concerning proper placement and selection of C_B .

Chip Power Consumption

Power consumption is one of the key metrics for amplifiers. The maximum self-power consumption of a differential output amplifier is: $P_{D_{MAX}} = 4 \times (V_{DD})^2 / (2 \times \pi^2 \times R_L)$.

It must be noted that self-power consumption is a function of output power.

During circuit design, the internal chip temperature must not exceed $T_{J_{MAX}}$ ($150^\circ C$). The design should be based on the chip's thermal resistance Θ_{JA} , and heat dissipation performance can be enhanced by incorporating dedicated copper or platinum cooling fins.

If the chip still fails to meet the requirements, solutions include increasing the load resistance, reducing the power supply voltage, or lowering the ambient temperature.



Power Supply Bypass

In amplifier applications, the bypass design of the power supply is critical, particularly for noise performance and voltage rejection characteristics of the application. The design requires that the bypass capacitor be positioned as close as possible to the chip and power pins. A typical configuration consists of a 10 μF electrolytic capacitor connected in parallel with a 0.1 μF ceramic capacitor.

In the TPA321 application circuit, another capacitor CB (connected to the BYP pin) is also critical, as it influences PSRR and switching noise performance. Ceramic capacitors with capacitance values ranging from 0.1 μF to 1 μF are typically selected.

Shut Down Footwork Mode Selection

To conserve power, the amplifier can be turned off when not in use. The TPA321 features a shutdown control pin that determines whether the amplifier operates. The voltage level on this control pin must match the required interface control signal; otherwise, the chip may enter an unstable state. By applying one of three distinct voltage levels to the Shutdown pin, the chip switches between three different operating modes:

Low level: The chip is in normal operating mode. Therefore, during use, ensure this pin remains at a low level.

High level: The chip enters power-off operation mode, with the amplifier disabled and no output signal. Selecting this state effectively reduces energy consumption, achieving power-saving objectives.

Floating state: The chip remains in an unstable condition. It cannot enter power-saving mode, its self-power consumption does not decrease, and the energy-saving objective is unattainable; moreover, this state adversely affects the chip. Therefore, during prolonged operation, the chip must never be left in a floating state.

Selection of Peripheral Components

Proper selection of peripheral components is essential to ensure chip performance. Although the TPA321 offers substantial performance margin, correct component selection remains critical for optimal overall performance.

The TPA321 features stable unit gain, making it widely applicable. Unit-gain amplification is typically employed to reduce THD + N and maximize the signal-to-noise ratio. However, this requires the highest possible input voltage; standard CODECs can only provide an output voltage of 1 V_{rms}.

Additionally, the closed-loop bandwidth must be ensured, as the input coupling capacitance C_i (forming a first-order high-pass filter) determines the low-frequency response.



Select Input Coupling Capacitor

An excessively large input capacitor increases both cost and footprint, which is highly disadvantageous for applications with limited budget and space constraints. Clearly, determining the appropriate capacitance value for coupling is crucial. In practice, speakers often fail to reproduce low-frequency sounds below 100 – 150 Hz; thus, using a large capacitor does not improve system performance. Beyond system performance considerations, the suppression of switching noise depends on the capacitor size: a larger coupling capacitor results in greater delay in the feedback network, leading to pop noise. Therefore, a smaller coupling capacitor can reduce this noise. Additionally, the capacitance value of the CB capacitor must be considered. Selecting $C_B = 1 \mu\text{F}$ with C_i ranging from $0.1 \mu\text{F}$ to $0.39 \mu\text{F}$ will meet the system performance requirements.

Design Reference Example

Power Output	0.85 W _{rms}
Load Impedance	8Ω
Input Level	1 V _{rms}
Input Impedance	20 k Ω
Bandwidth	100 Hz-20 kHz ± 0.25 dB

First, Determine the Minimum Operating Voltage.

Based on the relationship between the output power of the TPA321 and the supply voltage, a supply voltage of 5.0 V should be selected. The voltage margin ensures that the output power can exceed 1 W without distortion. After selecting the voltage, consider the power consumption issue.

Determine Voltage Gain

The requirement is that AVD be greater than $\text{SQRT}(P_O \times R_L)/V_{IN}$, i.e., V_{orms}/V_{inrms} , with $R_f/R_i = AVD/2$. In this design, the minimum AVD calculated is 2.83; selecting $AVD = 3$ yields $R_i = 20 \text{ K}$ and $R_f = 30 \text{ K}$.

Other Precautions

The TPA321 offers stable unit gain; however, when the gain exceeds 10-fold (20 dB), an additional feedback capacitor C_f must be connected in parallel with resistor R_f to prevent high-frequency oscillation. The combined frequency of the poles formed by C_f and R_f must exceed f_H (300 kHz in this example). Using $C_f = 25 \text{ pF}$ yields a cutoff frequency of 320 kHz, which meets the requirement.



Finally, Determine the Input Capacitance Based on the Bandwidth Requirements.

The input low-frequency-3 dB bandwidth is 100 Hz, with the 1/5 low-frequency point approximately 0.17 dB below-3 dB and the 5-fold high-frequency point within the specification requirements. Let $f_L = 20$ Hz and $f_H = 100$ kHz; thus, C_i is approximately 0.39 μ F.

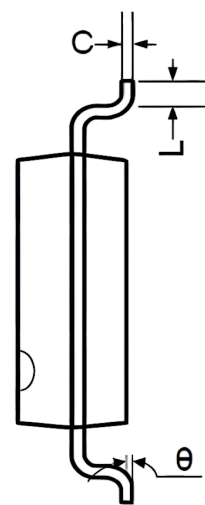
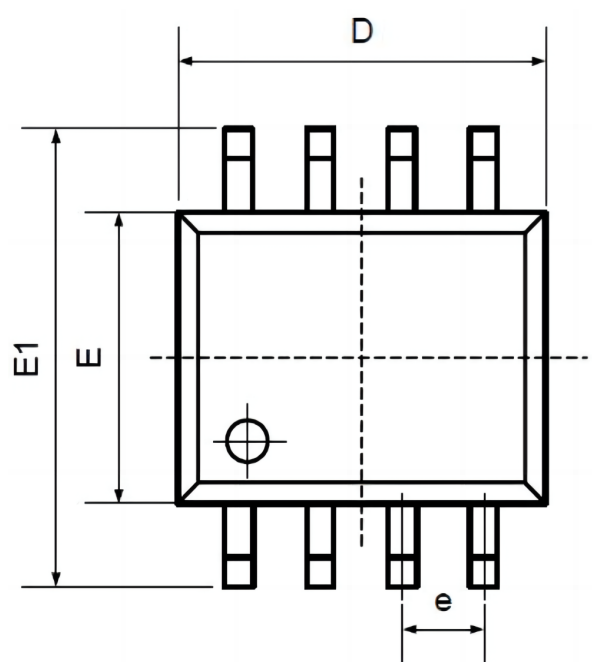
The high-frequency band f_H is determined by the amplifier's GBW, with a minimum requirement of $GBW > AVD \times f_H = 300$ kHz – significantly lower than the TPA321F's 2.5 MHz.

Order information

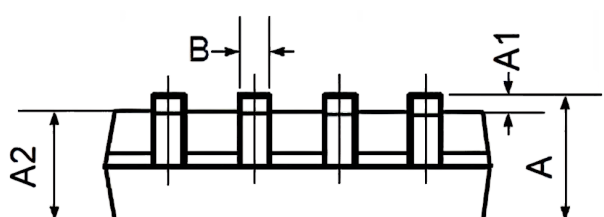
Order Number	Package	Package Quantity	Marking On The park	Temperature
TPA321DR-TUDI	SOP8	Tape,Reel,2500	TPA321	-40°C to 85°C
TPA321DGNR-TUDI	MSOP8	Tape,Reel,2500	AJB	
TPA321P-TUDI	DIP8	Tube,50,A box of 2000	TPA321P	



Package SOP8

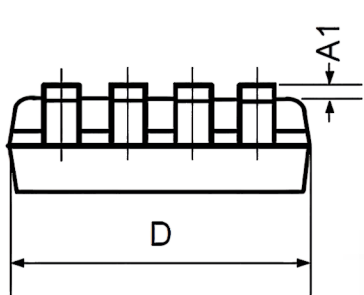
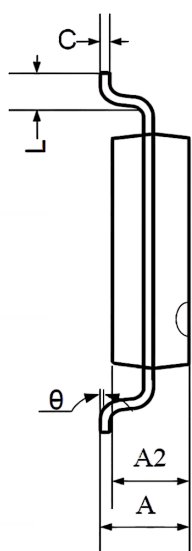
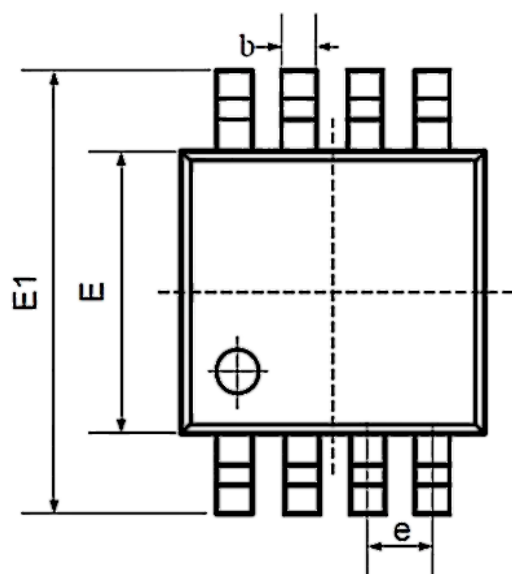


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



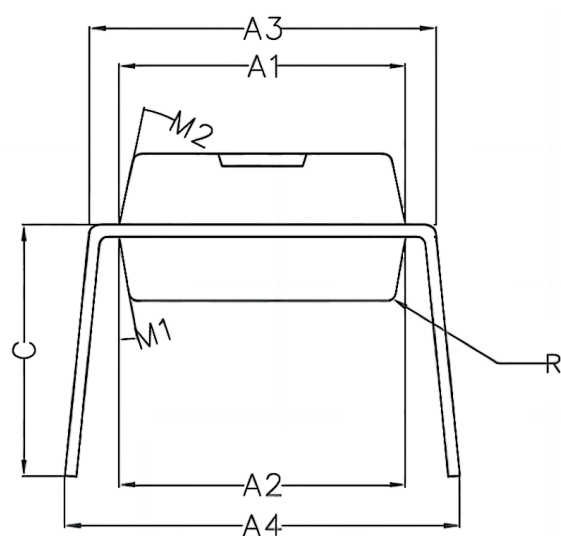
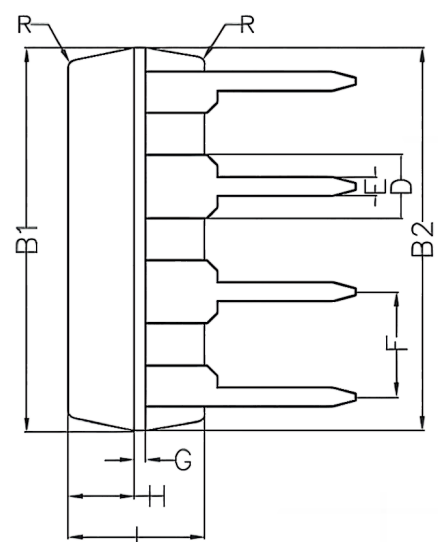
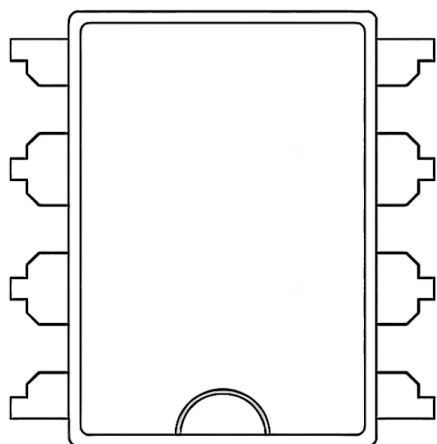


Package MSOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



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