SC5012
SC5012Q

High Efficiency 4-Ch, 150mA/Ch LED Driver with I²C Interface and Phase-Shifted PWM Dimming

POWER MANAGEMENT

Features

- Input Voltage — 4.75V to 45V
- Output Voltage — Up to 65V
- Step-up (Boost) Controller
  - Ultra-Fast Transient Response
  - Programmable Switching Frequency
  - External Sync Frequency for Boost Controller
- Linear Current Sinks
  - 4 Strings, up to 150mA/String
  - Current Matching ±1%
  - Current Accuracy ±2%
- PWM Dimming
  - String-by-String Phase Shifting
  - Dimming Frequency 100Hz-30kHz
  - User Selectable 9 or 10 Bits Dimming Resolution
  - Optional Synchronization to VSYNC/HSYNC Signal
- External Frequency Synchronization, FSYNC
- 8-bit Analog Dimming
- I²C Interface
  - Fault Status — Open/Short LED, OTP
  - Device Control: SYNC Freq, PLL Setting
- Protection Features
  - Open/Shorted LED(s) and adjustable OVP
  - Over-Temperature
- 4mm X 4mm 24 Ld QFN Package
- AEC-Q100 Qualified Version Available

Applications

- Medium-sized LCD Panel
- Automotive Car Navigation/Information Display
- LCD Monitors
- Automotive AEC-Q100 Qualified Application

Description

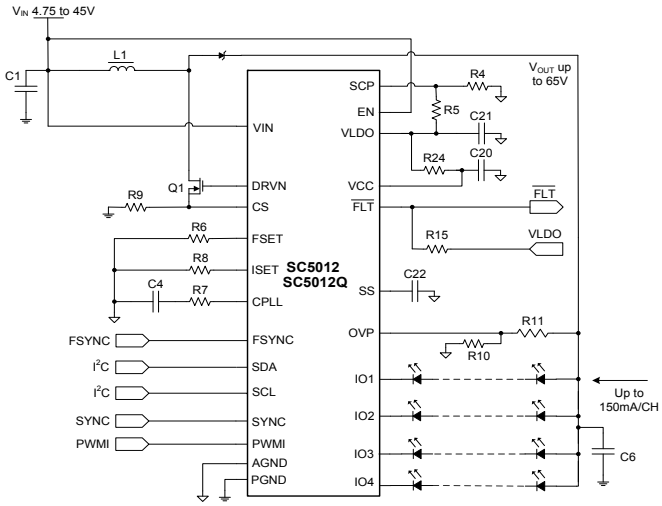
The SC5012/Q is a 4-channel high-precision, high-efficiency step-up (Boost) HB LED driver designed for backlight applications. It features wide input voltage range (4.75V to 45V) , flexible output configuration, wide analog and PWM dimming range, phase shifting, optional fading, external boost controller frequency synchronization (FSYNC), I²C interface, and numerous protection features.

The boost controller, with programmable switching frequency from 200kHz to 2.2MHz, can maximize efficiency by dynamically minimizing the output voltage while maintaining LED string current accuracy. It provides excellent line and load response with no external compensation components. Each linear current sink is matched within ±1% for superb lighting uniformity, and the accuracy of each string current is ±2%. An external resistor adjusts the current from 40-150mA per string. It also features PWM dimming resolution of 9 or 10 bits (user selectable) over a dimming frequency from 100Hz to 20kHz, synchronized to the SYNC signal or the boost oscillator. String-by-string phase shifting reduces the demand on the input/output capacitance, decreases EMI, and improves dimming linearity.

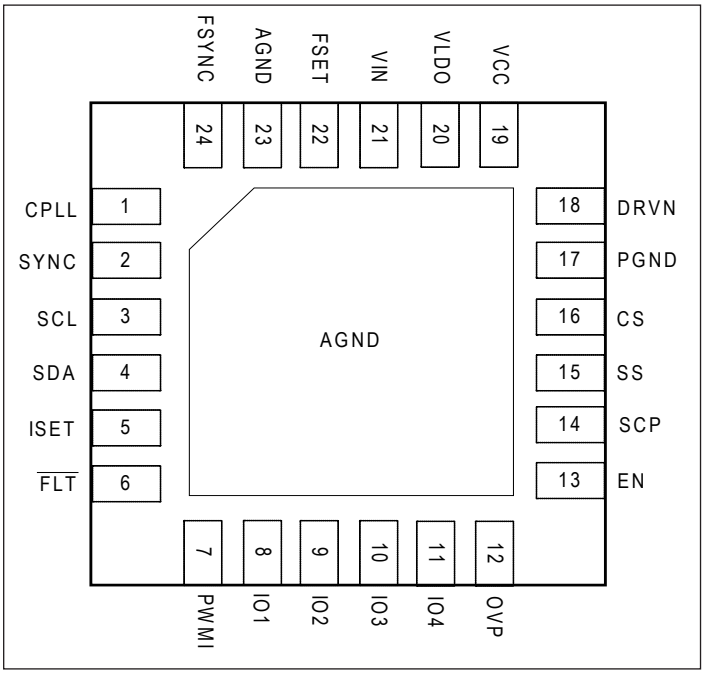
SC5012/Q is available in 4mm X 4mm 24 Ld QFN package.

The SC5012Q is an AEC-Q100 qualified version.

Typical Application Circuit



Pin Configuration

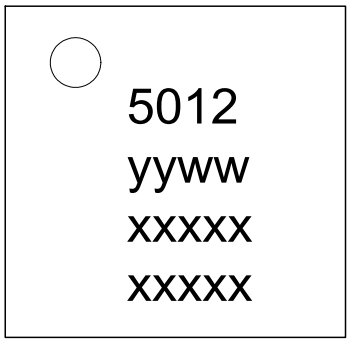


Ordering Information

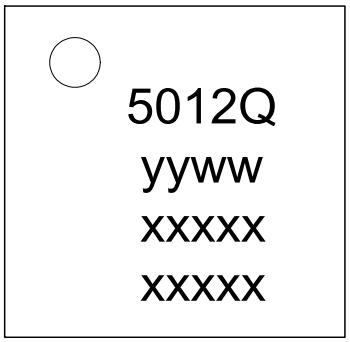
Device	Package
SC5012MLTRT[1][2]	MLPQ-24 4×4
SC5012QMLTRT[1][2][3]	MLPQ-24 4×4
SC5012EVB	Evaluation Board
SC5012QEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen free.
(3) Device is AEC-Q100 qualified.

Marking Information



nnnn = Part Number Code
yyww = Datecode
xxxxx = Semtech Lot No.
xxxxx = Semtech Lot No.



nnnn = Part Number Code
yyww = Datecode
xxxxx = Semtech Lot No.
xxxxx = Semtech Lot No.

Absolute Maximum Ratings

VCC, SYNC, FSYNC (V) ..... -0.3 to +6.0
EN(V) ..... -0.3 to VIN
VIN, IO1 to IO4(V) ..... -0.3 to +48
DRVN, OVP, CS, SS, SCP, VLDO, $\overline{FLT}$ (V) ..... -0.3 to +6.0
FSET, CPLL, SCL, SDA, ISET, PWMI(V) ..... -0.3 to +6.0
PGND to AGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \leq T_A \leq +85$
VIN (V) ..... 4.75 to 45
IO1 to IO4 Current per String (mA) ..... up to 150

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) ... 30
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in.), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless noted otherwise, T_A = 25°C for typical, -40°C < T_A < 85°C for min and max. V_{CC} = 5V, R_{ISET} = 34kΩ, R_{FSET} = 100kΩ , V_{IN} = 12V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply						
V_{IN} Supply Voltage	V_{IN}		4.75		45	V
V_{IN} Quiescent Supply Current	$I_{IN(Q)}$	EN = high, Switching, No Load		2		mA
V_{IN} Supply Current in Shutdown	$I_{IN(SD)}$	EN = 0, V_{IN} =12V		6	10	µA
		EN = 0, V_{IN} =28V		14	25	µA
V_{CC} Supply Voltage	V_{CC}		4.5		5.5	V
V_{CC} Under-Voltage Lockout Threshold	$V_{CC-UVLO(TH)}$	V_{CC} Voltage Rising	4.0	4.15	4.3	V
V_{CC} Under-Voltage Lockout Hysteresis	$V_{CC-UVLO(HYS)}$	V_{CC} Voltage Falling		180		mV
Linear Regulator (LDO)						
VLDO Output Accuracy	$V_{LDO-ACC}$	LDO Load = 10mA	4.875	5	5.125	V
VLDO Current Limit	$I_{LDO-LIMIT(ST)}$	During Start-up		85		mA
	$I_{LDO-LIMIT(OP)}$	Operating Current Limit	65	100		mA
VLDO Droput Voltage	$V_{LDO-DROP}$	V_{IN} = 4.75V, Load = 50mA		250	500	mV
V_{LDO} Under-Voltage Lockout Threshold	$V_{LDO-UVLO(TH)}$	V_{LDO} Voltage Rising	4.0	4.15	4.3	V

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{LDO} Under-Voltage Lockout Hysteresis	$V_{LDO-UVLO(HYS)}$	V_{LDO} Voltage Falling		180		mV
External FET Gate Drive						
DRVN High Level	$V_{DRVN(H)}$	100mA from DRVN to GND	V_{CC} -0.5	V_{CC} -0.2		V
DRVN Low Level	$V_{DRVN(L)}$	-100mA from DRVN to V_{CC}		0.2	0.5	V
DRVN On-Resistance	R_{DRVN}	DRVN high or Low		1	3	Ω
DRVN Sink Current	I_{DRVN}	DRVN forced to 2.5V		1.9		A
DRVN Source Current	I_{DRVN}	DRVN forced to 2.5V		1.5		A
Boost Converter						
CS Current Limit Threshold	$V_{CS(ILIM)}$		0.36	0.40	0.44	V
Internal Soft-start Time (1)	t_{SS}	From EN to end of soft start, F_{SW}=1MHz		4.4		ms
External Soft-start Current	I_{SS}			10		µA
Boost Oscillator Frequency	F_{SW}	R_{FSET} = 100kΩ	0.95	1	1.05	MHz
Boost Oscillator Frequency	F_{OSC}	R_{FSET} Varies	0.2		2.2	MHz
Minimum duty cycle	D_{MIN}				0	%
Maximum duty cycle	D_{MAX}		85	90		%
FSYNC Input Frequency Range	F_{FSYNC}	SYNC Range From Boost Oscillator Frequency	-10		+10	%
Control Signals: EN						
High Voltage Threshold	V_{EN-IH}		1.4			V
Low Voltage Threshold	V_{EN-IL}				0.4	V
EN Leakage Current	$I_{EN-LEAK}$	V_{EN} = VIN = 28V		11	18	µA
Control Signals: SYNC, SDA, SCL, FSYNC						
High Voltage Threshold	V_{IH}		2.1			V
Low Voltage Threshold	V_{IL}				0.8	V
SDA Output Low	$V_{SDA(L)}$	-3mA from V_{CC} to SDA			0.4	V
Pin Leakage Current	I_{LEAK}	V_{EN} = 0V, V_{SYNC} = V_{SDA} = V_{SDL} = V_{FSYNC} = 5.0V	-1		1	µA
Control Signals: PWMI						
High Voltage Threshold	$V_{PWMI-IH}$		2.1			V

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low Voltage Threshold	$V_{PWMI-IL}$				0.8	V
Pin Leakage Current	$I_{PWMI-LEAK}$	$V_{EN} = 5V = V_{PWMI}$	-1		1	µA
		$V_{EN} = 0V$, $V_{PWMI} = 5V$		200		µA
PWM Dimming						
PWMI Input Dimming Frequency(1)	F_{PWMI}		100		30k	Hz
IOx Dimming Minimum Pulse Width	$T_{PWM(MIN)}$	$F_{PWM(LED)}$ = 100Hz - 30kHz		300		ns
SYNC Input Frequency	F_{SYNC}		30		100k	Hz
PWMI Input Resolution		100Hz < F_{PWMI} < 10kHz		10		bits
		10kHz < F_{PWMI} < 30kHz		9		bits
Over-Voltage Protection						
OVP Trip Threshold Voltage	$V_{OVP(TRIG)}$	OVP Rising	1.17	1.22	1.27	V
OVP Hysteresis	$V_{OVP(HYS)}$	OVP Falling		10		mV
OVP Leakage Current	$I_{OVP(LEAK)}$	OVP = 5V		0.1	1	µA
Current Sink (IO1 to IO4)						
ISET pin voltage	V_{ISET}			1.23		V
Regulation Voltage	$V_{IOn(REG)}$	Voltage of Regulating String		0.8		V
Current Sink Disable Threshold	$V_{IOn(DIS)}$	Checked at Power-up	0.6			V
Current Sink Rise/Fall Time (1)	$t_{RISE/FALL}$	Rising edge from 10% to 90% of $I_{O(n)}$		25		ns
LED Current Accuracy	$I_{On(ACC\%)}$	PWMI = 100%, T_A = 25°C	147	150	153	mA
		PWMI = 100%, T_A = -40°C ~ 85°C	144	150	156	mA
LED Current Matching (2)	$I_{On(MATCH)}$	PWMI = 100%; T_A = 25°C			±1	%
		PWMI = 100%; T_A = -40°C ~ 85°C			±3	%
I_{On} Off Leakage Current	$I_{On(LEAK)}$	PWMI = 0V, EN = 0V, V_{IO1} ~ V_{IO4} = 25V		0.1	1	µA
Phase Delay Time (IO1 to IO4)	t_{PD}	FAST_FREQ = 1 (Default Setting) t_{PD} = (1/4)*(1/$F_{PWM(IO)}$), 4 Strings On		11.6		µs

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PWM Output Resolution		$F_{PWM(IO)}$ = 10kHz		10		bits
		$F_{PWM(IO)}$ = 20kHz		9		
IO Switching Frequency	$F_{PWM(IO)}$	FAST_FREQ = 0		10.75		kHz
		FAST_FREQ = 1 (Default Setting)		21.50		
Fault Protection						
LED Short Circuit Protection Threshold	$V_{IOn(SCP)}$	R_4 and R_5 (3)	8.5xV_{SCP}	10xV_{SCP}	11.5xV_{SCP}	V
LED Open Circuit Protection Threshold	V_{IO_OCP}	T_A = 25°C		0.2		V
LED Short Circuit Fault Delay	$t_{SCP(DELAY)}$	V_{OVP} set to 1.5V, $\overline{FLT}$ goes low		1		µs
		PWM dimming		10		µs
$\overline{FLT}$ Pin Leakage Current	$I_{\overline{FLT}(LEAK)}$	V_{EN} = 0V, $V_{\overline{FLT}}$ = VLDO	-1		1	µA
$\overline{FLT}$ Output Low	$V_{\overline{FLT}(LOW)}$	-5mA from $\overline{FLT}$			0.5	V
Over-Temperature Protection						
Thermal Shutdown Temperature	T_{OTP}			150		°C
Thermal Shutdown Hysteresis	T_{OTP_HYS}			10		°C
I²C Control Interface: SDA, SCL Timing Specifications						
SCL Clock Frequency	F_{SCL}				400	kHz
SCL Clock Low Period	$t_{LOW(SCL)}$		1.3			µs
SCL Clock High Period	$t_{HIGH(SCL)}$		0.6			µs
Hold Time Start Condition	$t_{HD(START)}$		0.6			µs
SDA Setup Time	$t_{SU(SDA)}$		100			ns
SDA Hold Time	$t_{HD(SDA)}$		0		0.9	µs
Setup Time Stop Condition	$t_{SU(STOP)}$		0.6			µs
Bus Free Time between Stop & Start	t_{BF}		1.3			µs

Notes:

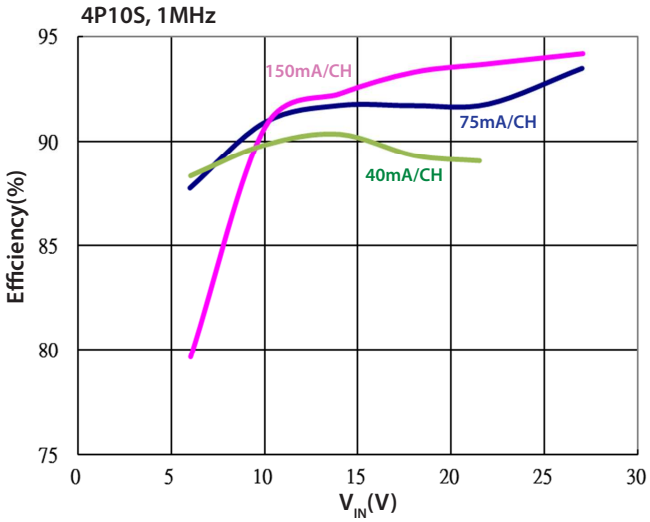
(1) Ensured by design and characterization, not production tested.

(2) LED current matching for 4 channels is defined as the largest of the two numbers, i.e., (MAX-AVG)/AVG and (AVG-MIN)/AVG; where MAX is the maximum LED channel current, MIN is the minimum LED channel current and AVG is the average of the 4 LED channel currents.

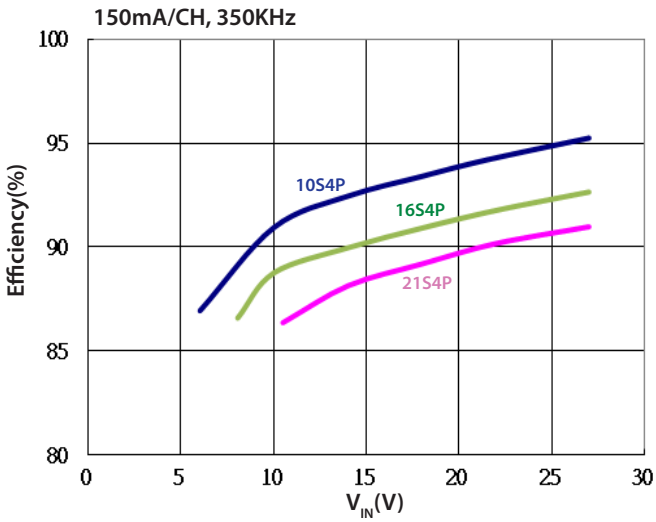
(3) Refer to the application circuit on page26, Figure 2.

Typical Characteristics

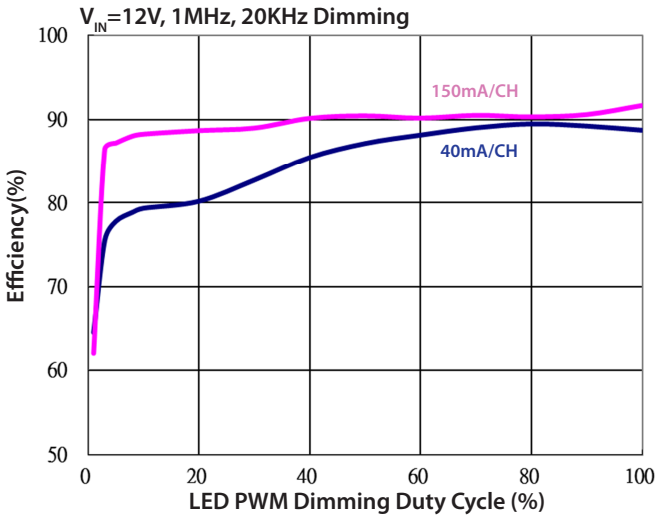
Backlight Efficiency vs. Input Voltage



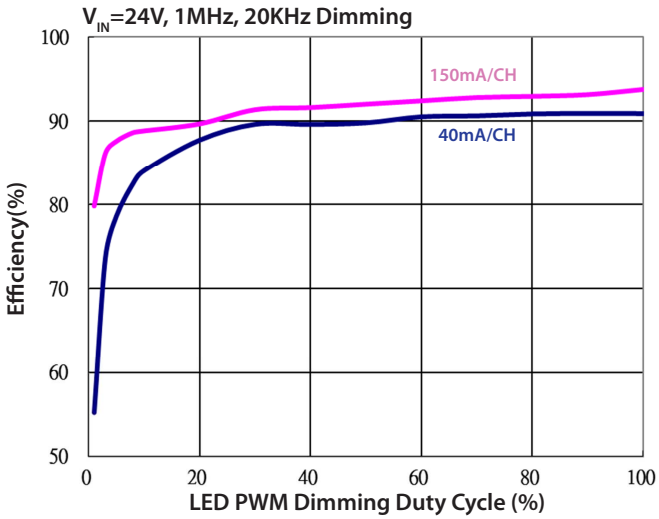
Backlight Efficiency vs. Input Voltage



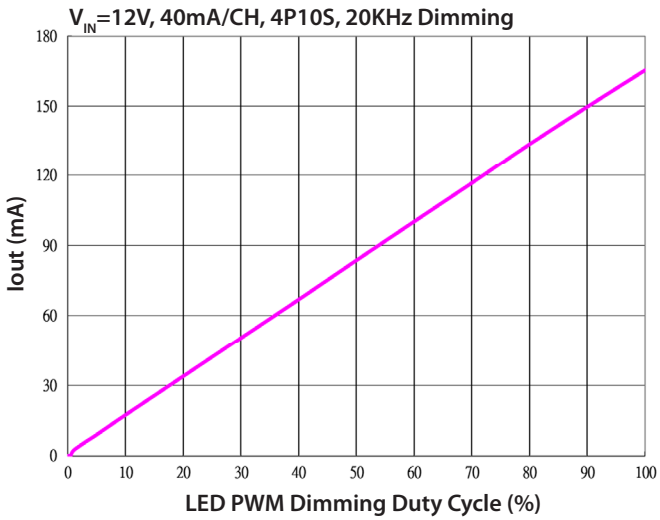
Backlight Efficiency vs. LED String Current



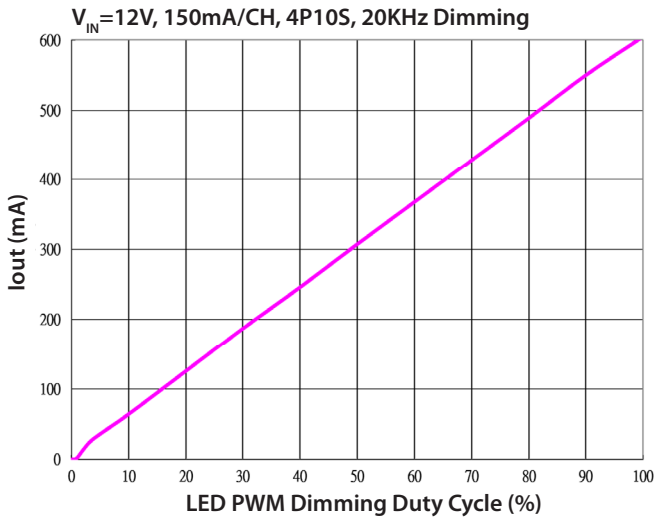
Backlight Efficiency vs. LED String Current



PWM Dimming Linearity with Phase Shift

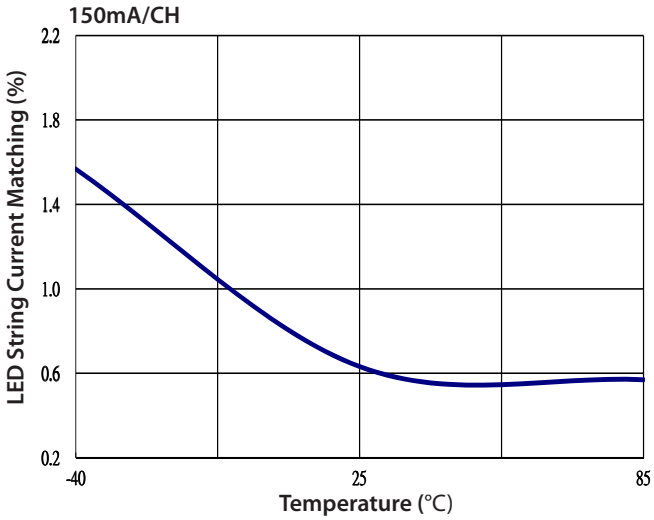


PWM Dimming Linearity with Phase Shift

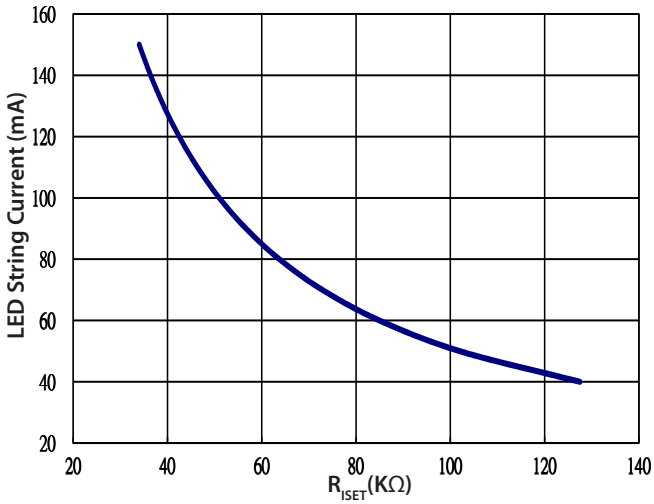


Typical Characteristics (continued)

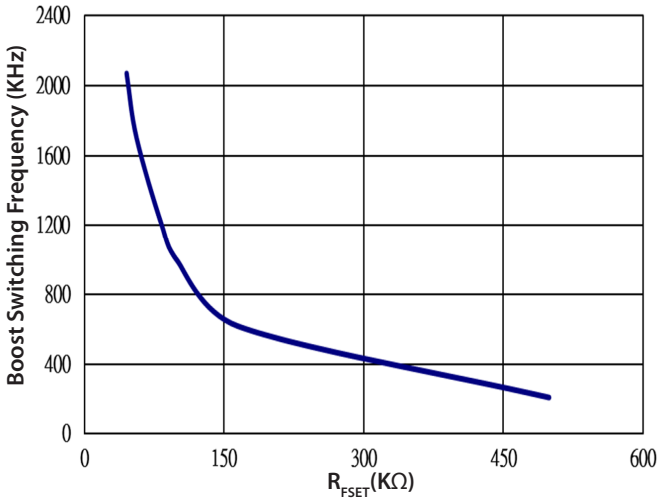
LED String Current Matching vs. Temperature



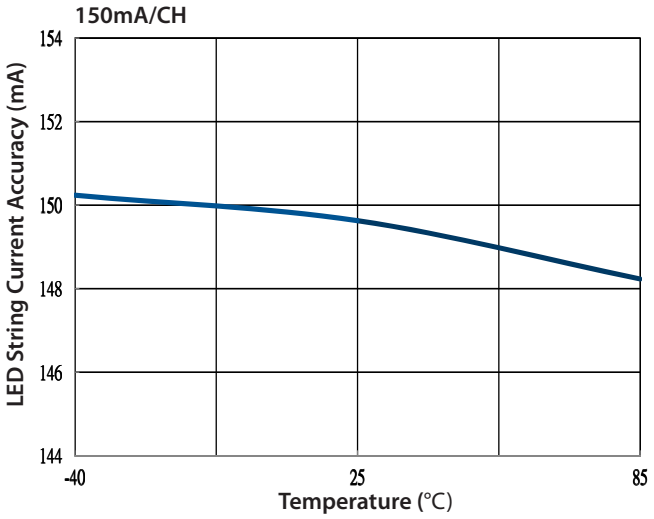
LED String Current vs. R_{ISET}



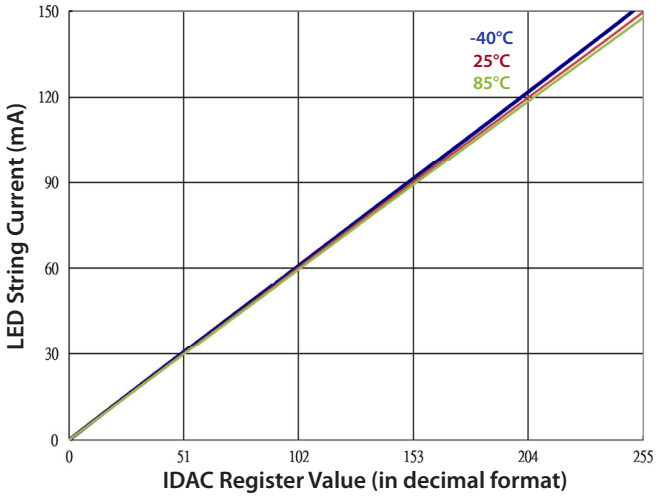
Switching Frequency vs. R_{FSET}



LED String Current Accuracy vs Temperature



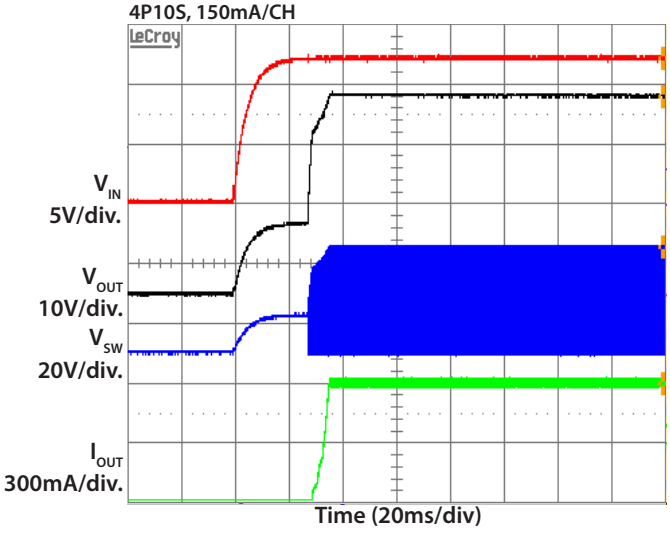
LED String Current vs. Analog Dimming Control Register (IDAC) Value



Typical Characteristics (continued)

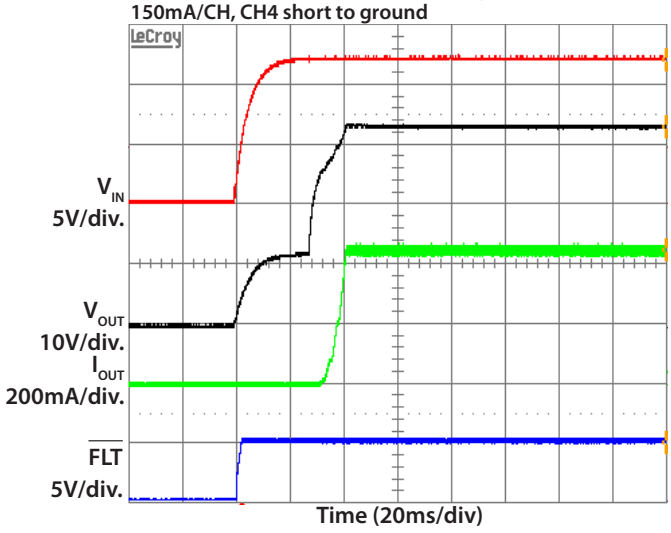
VIN Start Up

4P10S, 150mA/CH



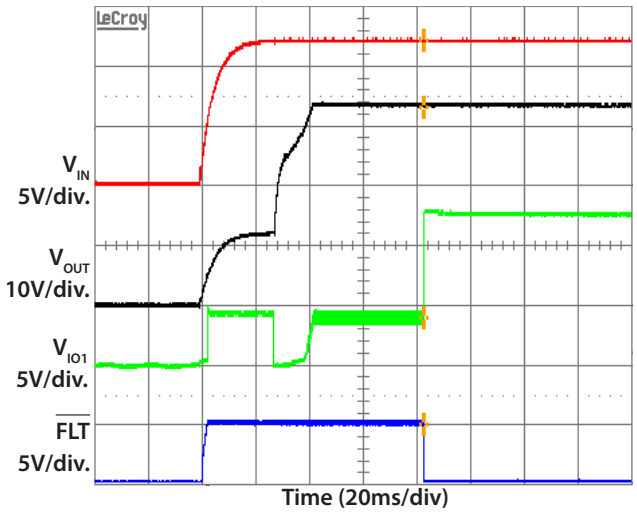
Unused String

150mA/CH, CH4 short to ground



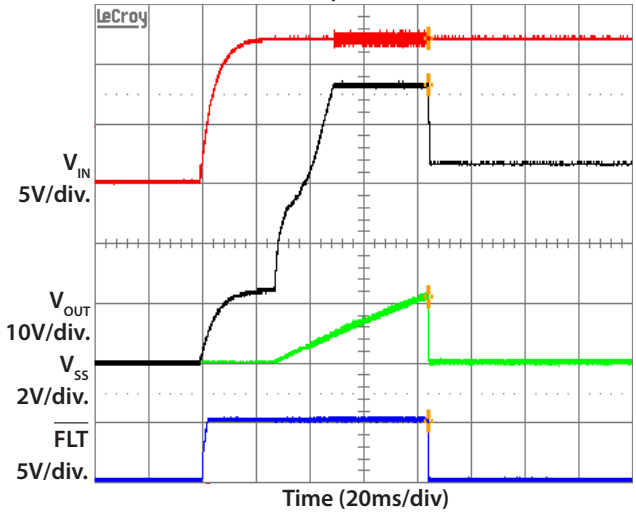
Start-up Into Short Circuit Protection

One LED short cicuit



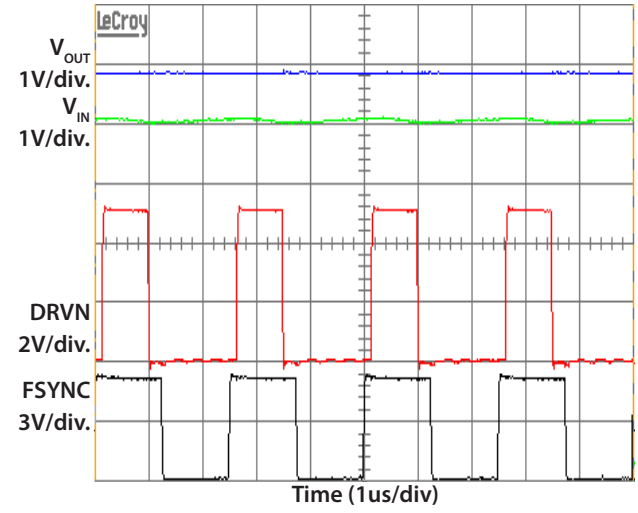
Start-up Into Open Circuit Protection

4P10S, 150mA/CH, CH4 Open



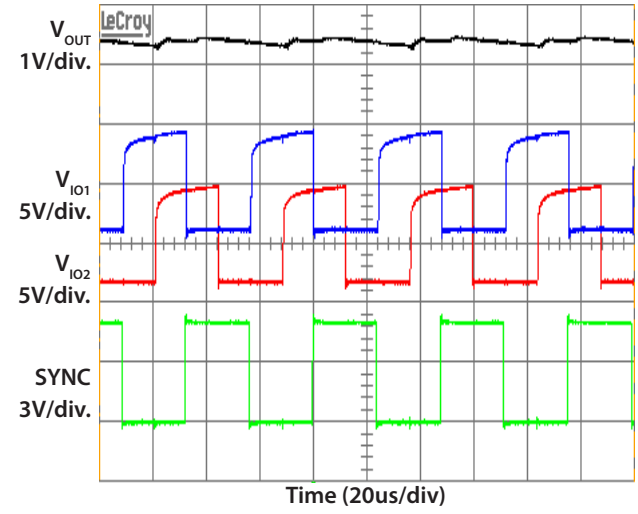
Synchronization of Switching Frequency

F_{SW} = FSYNC=400KHz



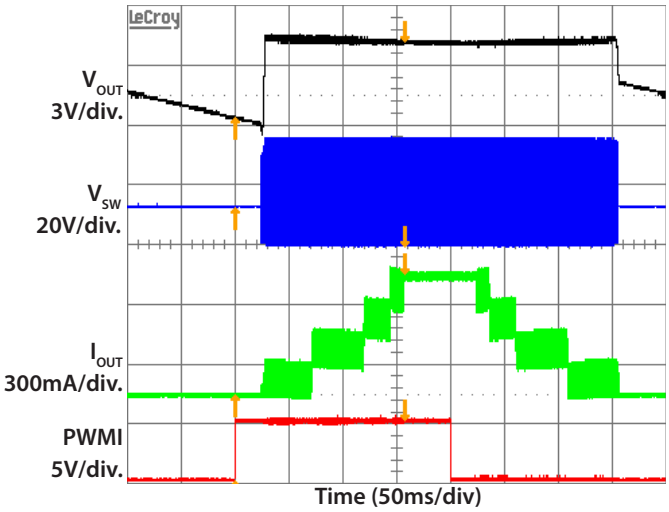
Synchronization of LED Dimming Frequency

SYNC=21KHz

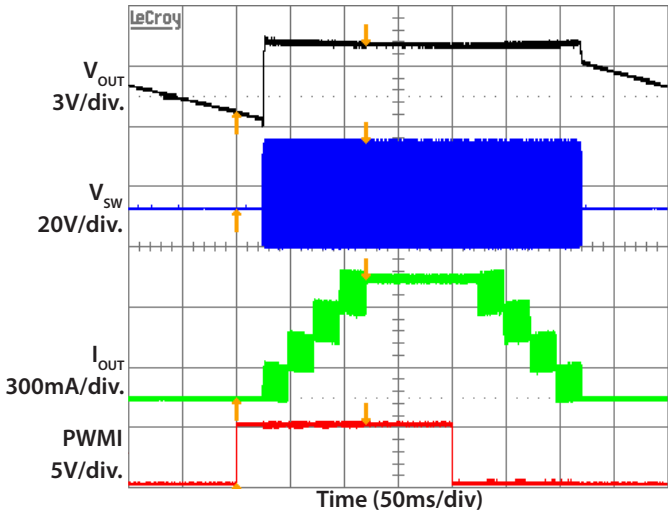


Typical Characteristics (continued)

Fade In/Out (Logarithmic)

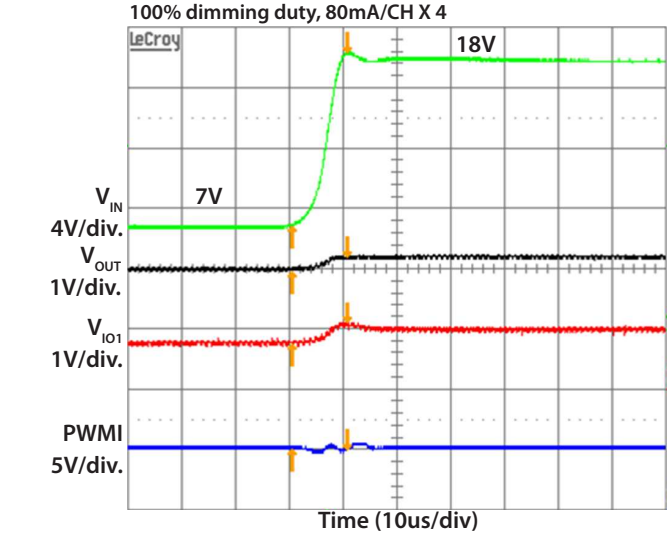


Fade In/Out (Linear)



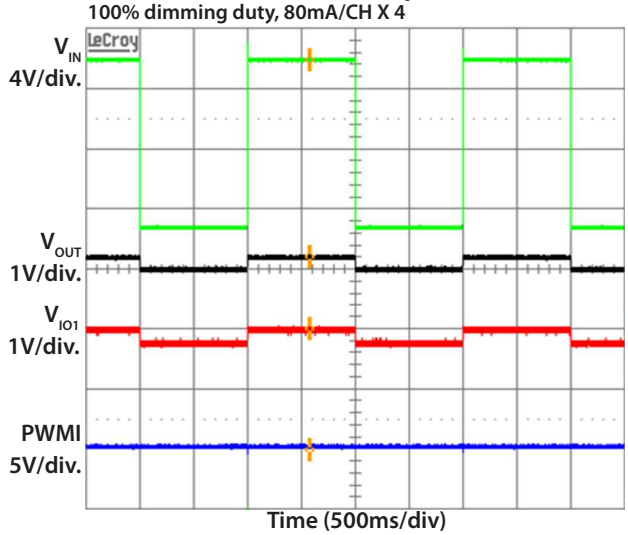
Line Transient Response

100% dimming duty, 80mA/CH X 4



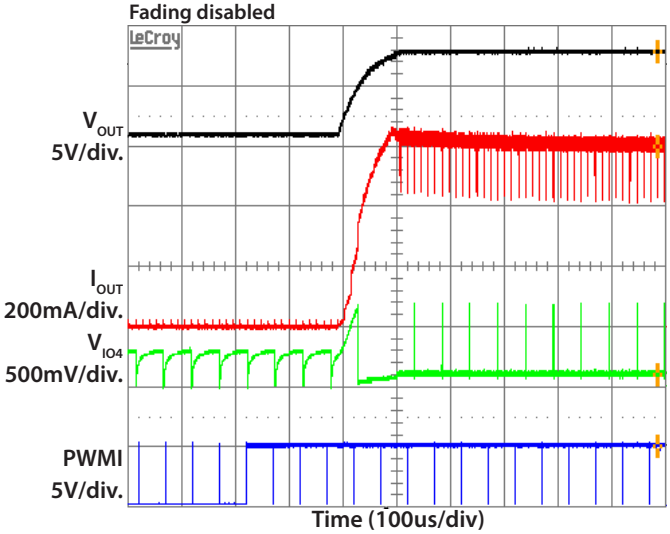
Line Transient Response

100% dimming duty, 80mA/CH X 4



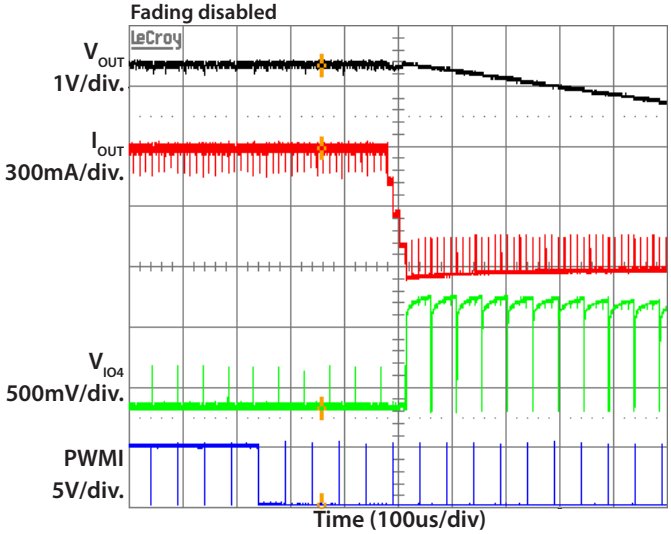
Load Transient Response

PWMI(20KHz)=0.5% to 99%, VIN=12V, 150mA/CH X 4
Fading disabled



Load Transient Response

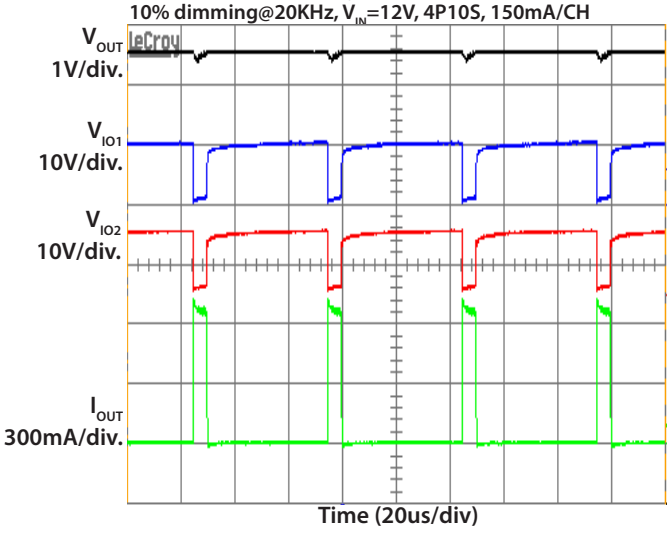
PWMI(20KHz)=99% to 0.5%, VIN=12V, 150mA/CH X 4
Fading disabled



Typical Characteristics (continued)

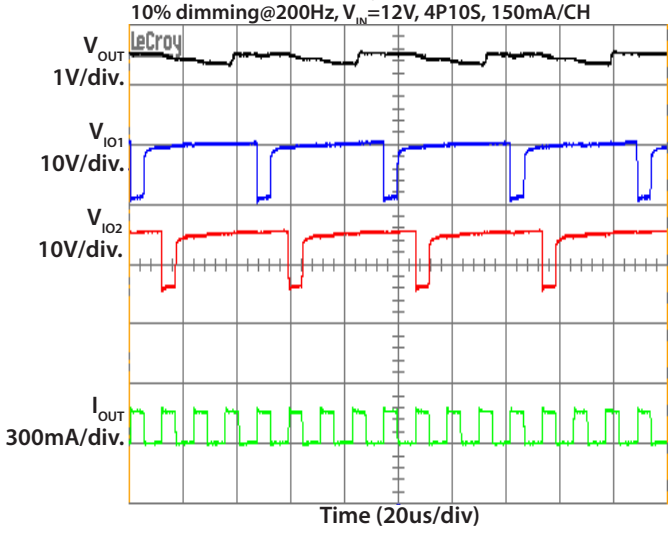
LED Dimming Without Phase Shift

10% dimming@20KHz, V_{IN}=12V, 4P10S, 150mA/CH



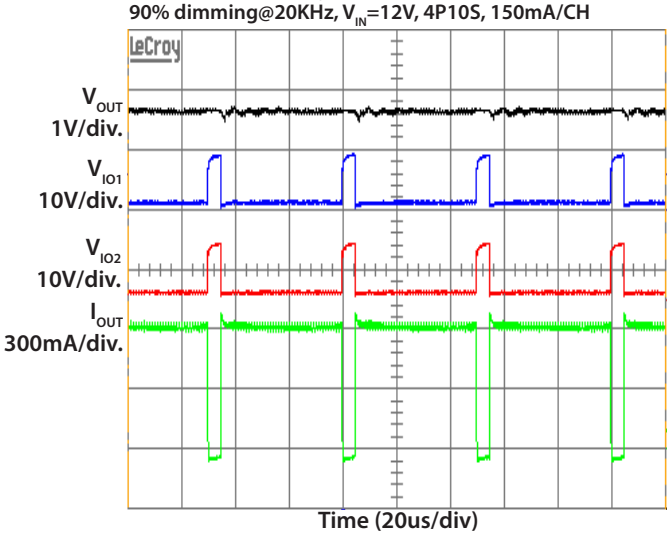
LED Dimming With Phase Shift

10% dimming@200Hz, V_{IN}=12V, 4P10S, 150mA/CH



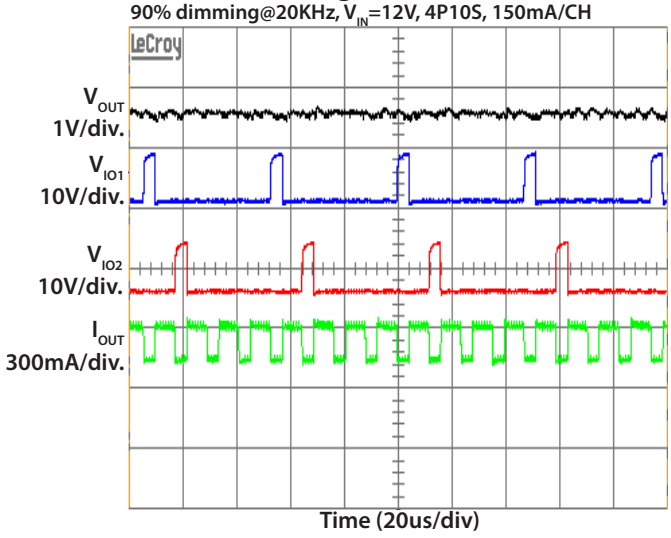
LED Dimming Without Phase Shift

90% dimming@20KHz, V_{IN}=12V, 4P10S, 150mA/CH



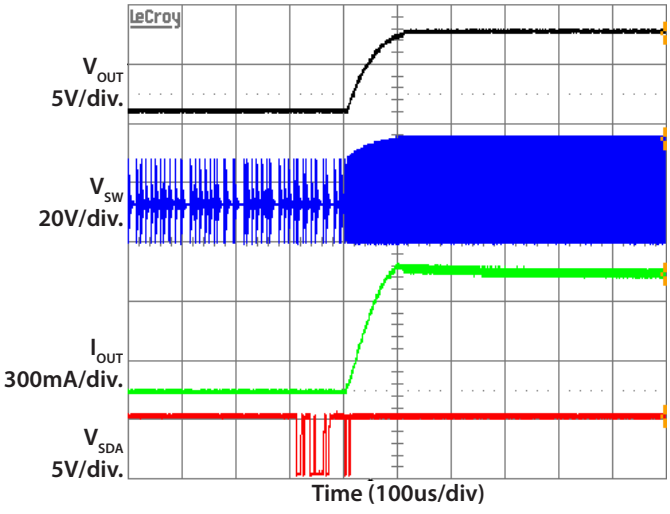
LED Dimming With Phase Shift

90% dimming@20KHz, V_{IN}=12V, 4P10S, 150mA/CH



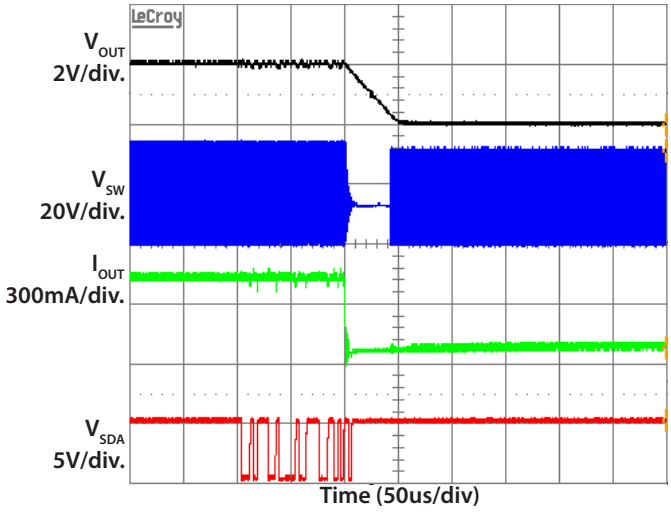
Analog Dimming Transient via I²C

0.39% to 100% dimming duty



Analog Dimming Transient via I²C

100% to 55.29% dimming duty



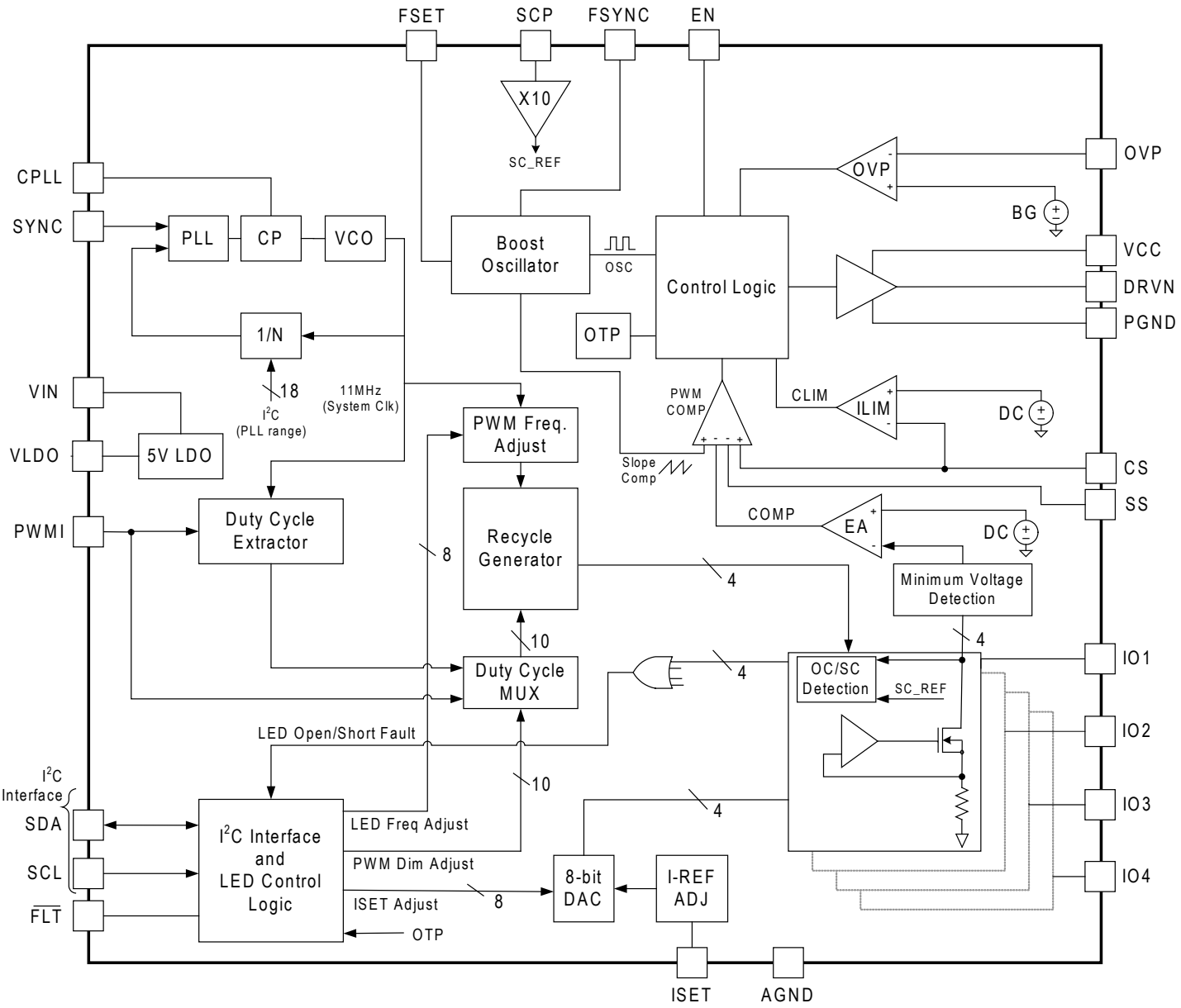
Pin Descriptions

Pin # (QFN)	Pin Name	Pin Function
1	CPLL	Compensation for the internal PLL — Connect a compensation resistor and capacitor from this pin to analog ground. This pin can be left floating if not used.
2	SYNC	SYNC input pin — Feeding the SYNC signal 30Hz to 100KHz to this input results in internal PLL being synchronized to the SYNC signal. This pin can be left floating if not used.
3	SCL	I^2C serial clock input — This pin must be connected to ground if not used.
4	SDA	I^2C serial data input — This pin must be connected to ground if not used.
5	ISET	LED current programming pin — Connect an external resistor to analog ground to program the peak current in the LED strings. For more details please refer to LED String Peak Current Programming on page 16.
6	$\overline{FLT}$	Logic low fault status pin — Open-drain output is latched low when fault condition is detected: Open/Short LED, Shorted String, OVP or OTP. Fault status can be reset by removing fault condition(s) and toggling the EN or VCC pin. This pin can be left floating if not used.
7	PWMI	LED string PWM dimming control input.
8	IO1	Regulated current sink LED channel 1 — Connect this pin to the cathode of the bottom LED in string 1. Connect pin to ground to disable this LED string during power on.
9	IO2	Regulated current sink LED channel 2 — Connect this pin to the cathode of the bottom LED in string 2. Connect pin to ground to disable this LED string during power on.
10	IO3	Regulated current sink LED channel 3 — Connect this pin to the cathode of the bottom LED in string 3. Connect pin to ground to disable this LED string during power on.
11	IO4	Regulated current sink LED channel 4 — Connect this pin to the cathode of the bottom LED in string 4. Connect pin to ground to disable this LED string during power on.
12	OVP	Over-voltage feedback pin — Over-voltage activated when pin exceeds 1.22V. Use a resistor divider tied to the output and analog ground to set the OVP level.
13	EN	Enable pin — Pull high to enable the device or pull low to disable and maintain low shutdown current.
14	SCP	Short circuit LED protection programming pin — Shorted LED protection disables the individual channel when the current sink voltage exceeds the programmed voltage threshold. Adding a resistor divider from this pin to VLDO and AGND programs the shorted-LED protection up to 10x the V_{SCP} voltage. Pulling the pin high disables the SCP feature on all channels.
15	SS	Soft-start pin — Connect a capacitor from this pin to analog ground.
16	CS	Step-up (boost) switch current sense pin — Connect a resistor from this pin to ground for current sense - utilized in peak current mode control loop and over-current sense circuitry.
17	PGND	Power ground — Tie this pin to the power ground plane close to input and output decoupling capacitors.
18	DRVN	Gate drive is connected to external step-up (boost) N-channel MOSFET.

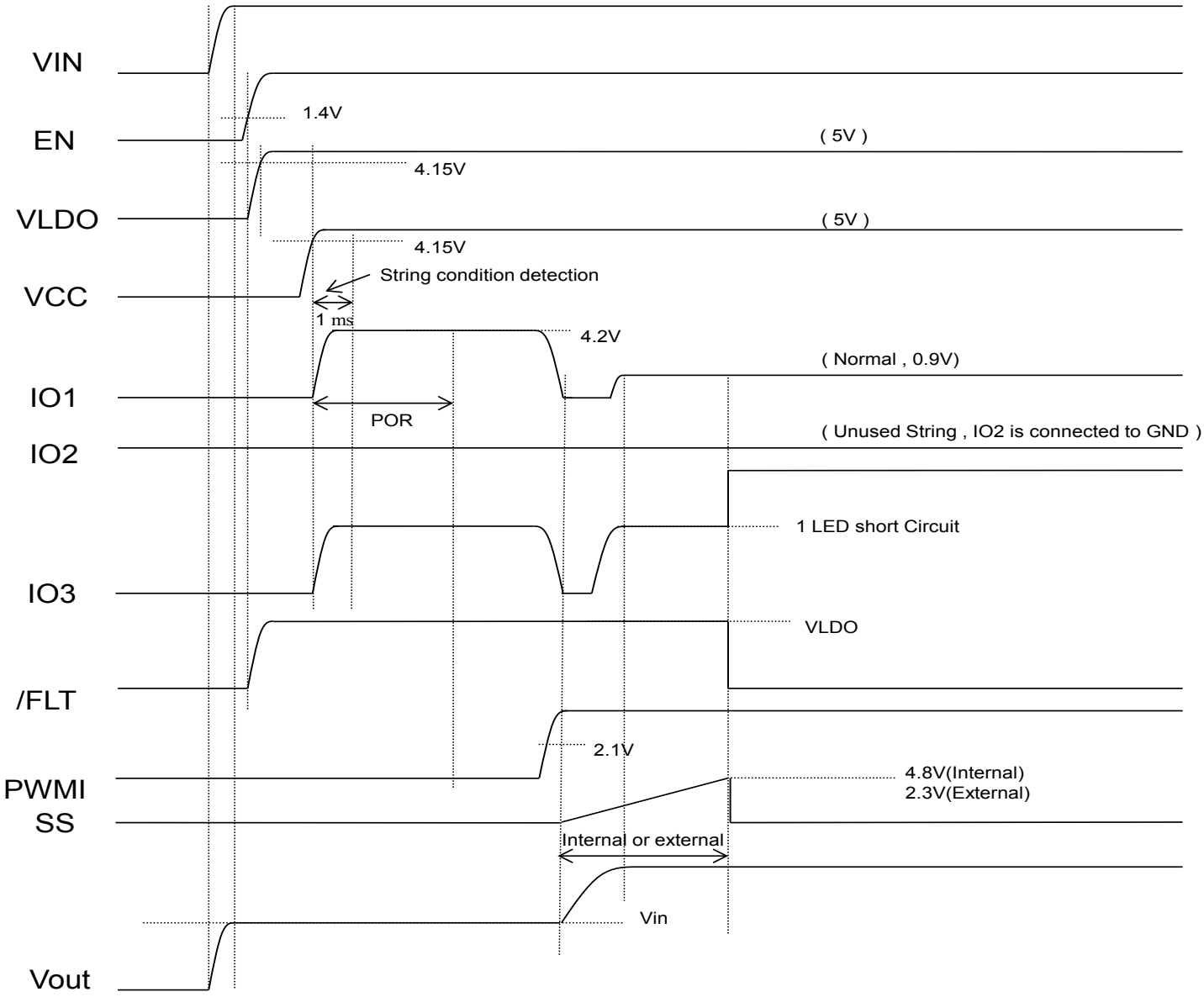
Pin Descriptions (continued)

Pin # (QFN)	Pin Name	Pin Function
19	VCC	Input bias voltage supply for the gate drive circuitry — Accepts 4.5-5.5V inputs. Add a 1µF or larger ceramic bypass capacitor from this pin to ground.
20	VLDO	On-chip 5V LDO output. A capacitor should be connected from this pin to analog ground.
21	VIN	Connect to the input power supply — Accepts 4.75V - 45V input. Usually add 2.2µF or larger ceramic bypass capacitor from this pin to analog ground.
22	FSET	Step-up (boost) frequency set pin. — Connect a resistor from this pin to analog ground to set the frequency from 200kHz to 2.2MHz.
23	AGND	Analog ground pin — Tie this pin to analog (quiet) ground isolated from step-up (boost) converter switching current path.
24	FSYNC	External clock synchronization pin — With an applied external clock signal, the boost converter will be synchronized with the rising edge of the external clock signal.
-	AGND	AGND thermal pad for heatsinking purposes — It should be connected to ground plane for proper circuit operation.

Block Diagram



Start-up Timing Diagram



SEMTECH

Applications Information

General Description

The SC5012/Q contains a high frequency, current-mode, internally compensated boost controller and four constant current sinks for driving LED strings. The LED peak current for all strings is programmed by an external resistor. The boost converter operates to maintain minimal required output voltage for regulating the LED current to the programmed value. A typical backlight application uses 3 to 14 LEDs per string, with current driven up to 150mA. The unique control loop of the SC5012/Q allows fast transient response in dealing with line and load disturbances. The SC5012/Q, operating with an external Power MOSFET, regulates the boost converter output voltage based on the instantaneous requirement of the 4 string current sources. This provides power to the entire lighting subsystem with increased efficiency and reduced component count. It supports PWM dimming frequencies from 100Hz to 30kHz and the supply current is reduced to 2mA typical when all LED strings are off. An external FSYNC pin provides the flexibility to apply an external clock signal to synchronize the boost converter switching.

Start-Up

When the EN pin is pulled high (>1.4V), the device is enabled and the internal 5V regulator output, VLDO, starts to turn on. VLDO powers most of the internal circuitry in the SC5012/Q, while the VCC input powers only the gate drive circuitry for DRVN. VCC is normally connected externally to VLDO through an RC filter, but can also be driven from a separate 5V power supply. VLDO and VCC have a fixed under-voltage rising and falling trip point and when both are higher than the UVLO threshold of 4.15V (typical), the SC5012/Q goes into a start-up sequence.

In this next phase, the SC5012/Q checks each IO pin to determine if the respective LED string is enabled. Each IO pin is pulled up with a 100uA current source and if any IO pin is connected to ground, it will be detected as unused and turned off. The unused string checking procedure typically takes 1mS and after this the SC5012/Q enters into a soft-start sequence.

The SC5012/Q has a fixed internal and programmable external soft-start function, where the slower of the two dominates. The soft-start function helps to prevent excess inrush current through the input rail during start-up. In the SC5012/Q, the soft-start is implemented by slowly ramping up the reference voltage fed to the error amplifier. This closed loop start-up method allows the output voltage to ramp up without any overshoot. The duration of the internal soft-start is controlled by an internal timing circuit, which is used during start-up and is based on the boost converter switching frequency. For example, with the switching frequency at 1MHz, it is 4mS typical and becomes 2mS typical when the switching frequency is 2MHz. For longer soft-start times an external capacitor can be placed from the SS pin to ground. A 10uA charging current flows from the SS pin through the external capacitor which sets the soft-start duration.

$$T_{SS} = \frac{C_{22} * \Delta V_{22}}{10uA},$$

If the PWM voltage goes low while the SC5012/Q is in soft-start operation, the SC5012/Q switches to standby mode, where the external power MOSFET and the LED current sources will be turned off immediately. The soft-start timers are turned off and the soft-start value is saved. When the PWM voltage goes high again, the soft-start resumes from the previously saved value.

Each LED current source (IO1 to IO4) tries to regulate the LED current to its set point. The control loop will regulate the output voltage such that all the IO pin voltages are at least 0.8V typical.

Shutdown

When the EN pin is pulled down below 0.4V, the device enters into shutdown mode. In this mode, all the internal circuitry is turned off and the supply current drops to 14µA typical.

In the scenario where the EN pin voltage is high, but either VLDO or VCC voltage falls below its respective UVLO threshold, the SC5012/Q goes into a suspend mode. In this mode, all the internal circuitry except the reference and the oscillator are turned off.

Thermal Shutdown (TSD)

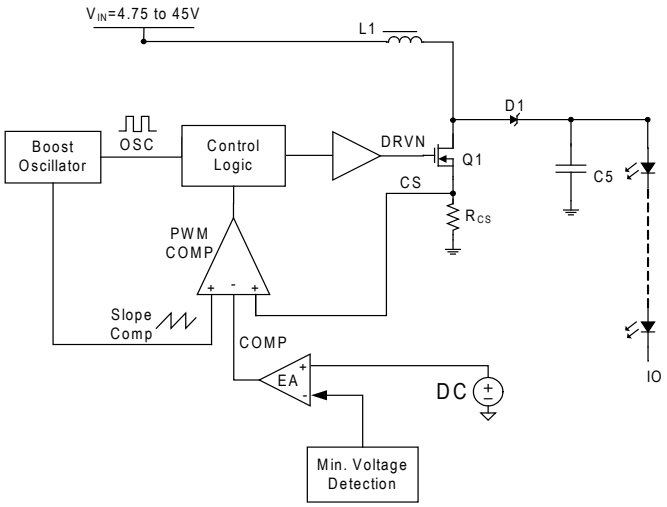
If the thermal shutdown temperature of typical 150°C is reached, the boost converter and all IO current sources are turned off. The $\overline{FLT}$ pin is forced low in this condition. When the temperature falls below the TSD trip point by 10°C, the SC5012/Q will restart following the start-up sequence as described before. The $\overline{FLT}$ pin is latched and will stay low, it is reset by cycling the EN or VCC.

Applications Information (continued)

Boost Converter Operation

The SC5012/Q includes a boost controller with programmable switching frequency. It applies a current-mode control method with an integrated compensation loop as shown in the diagram below. The clock (see block diagram on page 14) from the oscillator sets the latch and turns on the external power MOSFET, which serves as the main power switch. The current flowing through this switch is sensed by the current sense resistor in series with the switch. The sensed switch current is summed with the slope-compensated ramp and fed into the modulating input of the PWM comparator. When the modulating ramp intersects the error amplifier output (COMP), the latch is reset and the power MOSFET is turned off. The sense resistor also sets the peak current limit of the power MOSFET, I_{OCP} using the following equation:

$$I_{OCP}[A] = 0.4 / R_{CS}[\Omega]$$



The current-mode control system contains two loops. For the inner current loop, the error amplifier (EA) output (COMP) controls the peak inductor current. In the outer loop, the EA regulates the output voltage for driving the LED strings.

Boost Converter Switching Frequency Selection

The resistor between FSET and GND sets the boost converter switching frequency (200kHz to 2.2MHz) using the following equation:

$$f_{SW}[kHz] = 10^5 / R_{FSET}[k\Omega]$$

A higher switching frequency allows the use of low-profile height inductors for space-constrained and cost-sensitive applications.

FSYNC

The FSYNC function can be used to synchronize the boost switching frequency to an external clock signal applied to the FSYNC pin. The FSYNC frequency range is +/- 10 % of the free running frequency set by the FSET pin, with the rising edge of DRVN being synchronized with the rising edge of FSYNC.

Over-Voltage Protection (OVP)

SC5012/Q features programmable output over-voltage protection to prevent damage to the IC and output capacitor in the event of a LED string open-circuit. The boost converter output voltage is sensed at the OVP pin through the resistor voltage divider. The OVP trip threshold (refer to detailed application circuit) can be calculated using the following equation.

$$\text{Output OVP Trip Voltage [V]} = 1.22 \text{ X } (R_{11} + R_{10}) / R_{10}$$

When the OVP pin voltage exceeds 1.22V, the boost converter turns off and the $\overline{FLT}$ pin is pulled low. When the OVP pin voltage falls below the OVP threshold, the boost converter restarts and the $\overline{FLT}$ pin is released.

There is 10mV hysteresis between OVP pin threshold (falling) and OVP pin threshold (rising). This results in an output voltage hysteresis given by:

$$\text{Output OVP Hysteresis[mV]} = 10 \text{ X } (R_{11} + R_{10}) / R_{10}$$

LED Current Sink

The SC5012/Q provides 4 current sinks and each can sink up to 150mA current. It incorporates LED string short-circuit protection (trip-level programmable; can be disabled) and LED string open-circuit protection..

LED String Peak Current Programming

LED string peak current (at 100% dimming) can be set by selecting resistor R_{ISET}, connected between ISET and GND. The relationship between R_{ISET} resistance and single LED string peak current is calculated using the following equation:

Applications Information (continued)

I_{LED} [mA] = (4146 X 1.23) / R_{ISET} [kΩ]

V_{SCP_Trip} [V] = 10 X (VLDO X R_4) / (R_4 + R_5)

The LED string current can be programmed up to 150mA.

Unused Strings

The SC5012/Q may be operated with less than 4 strings. In this mode of operation, all unused IO pins should be connected to ground. During start-up, these unused strings are detected and disabled while other active strings work normally, and $\overline{FLT}$ does not be pulled low.

LED Short-Circuit Protection (SCP)

The SC5012/Q features a programmable LED short-circuit protection (SCP). This allows the part to be customized based on the LED forward voltage (VF) mismatches between the LED strings. If one or more LEDs are detected as short-circuited, the corresponding string will be latched off. The voltages on all IO pins are monitored to check if any IO pin exceeds the SCP trip point. The IO voltage for LED string(s) with faulty short-circuit LED(s) will be higher than other normal IO pin voltages. This LED short-circuit protection trip level (see detailed application circuit on page 26, Figure 2) is expressed by the following equation:

If any IO pin voltage exceeds the trip voltage, the IO current sink will be latched off and the $\overline{FLT}$ will go low. This latch can be reset by cycling VCC or EN. Other LED strings are unaffected and continue in normal operation. This protection will be disabled if SCP is pulled to high.

There is a typical 10µs SCP detection time in PWM dimming applications. If the PWM dimming on-time is less than the SCP detection time, the SCP cannot be enabled.

In many applications, LED strings are connected to the IO pins through a mechanical connector, which cannot support an electrical connection at specific times. This connection might cause noise on the IO pins. If this noise is large enough, it may trigger a false SCP mode. Under such condition, a ceramic decoupling capacitor (100pF ~ 8.2nF) between IO pin to ground can help prevent the SC5012/Q from entering the protection mode by false trigger. Or, simply disable this feature by connecting SCP pin to VLDO pin.

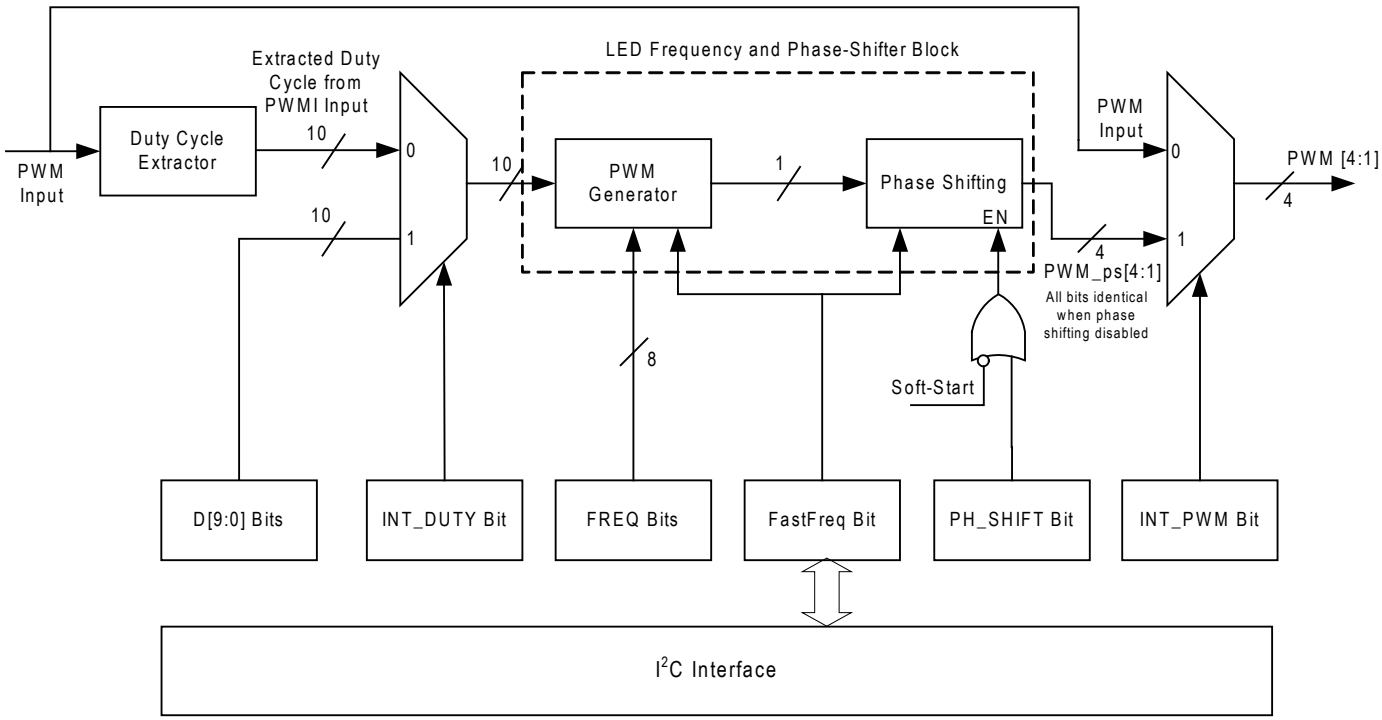


Figure 1— I²C Control Method

Applications Information (continued)

LED Open-Circuit Protection

If any LED string becomes open, the respective IO pin voltage will be pulled to GND. Consequently, the internal COMP node (output of error amplifier) is driven high, which causes the boost output voltage to increase. The output voltage will be eventually clamped to a voltage set by the OVP resistor divider. Under this condition, the faulty string is latched off and the $\overline{FLT}$ pin is pulled low. The boost voltage gets regulated to the voltage required to set all non-faulty IO pins above 0.8V. The remaining strings remain in normal operation. The $\overline{FLT}$ and the fault-out LED current sink latch-off can be reset by cycling VCC or EN.

LED Analog Dimming Control

The LED current in SC5012/Q can be dimmed via the 8-bit analog dimming register (register address: 0x02). The LED current can be adjusted in 256 steps from 0mA to maximum value, which is determined by the R_{ISET} resistor.

The SC5012/Q has a unique DAC architecture which allows it to have excellent LED current accuracy and string-to-string matching over the entire DAC range.

The analog dimming method can be used in conjunction with PWM dimming to increase the dimming resolution. The fast loop response of the SC5012/Q allows the LED current to transition to a new value within 160µs or so. Please refer to the graphs in the typical characteristics section.

LED PWM Dimming Control

The SC5012/Q supports three PWM dimming modes for controlling the brightness of the LEDs.

The dimming modes are:
(1) PWM direct,
(2) PWM indirect and
(3) I²C control

It provides flexibility in setting the duty cycle and frequency of the LED PWM signal. The PWM dimming mode is set through the device control register (register address: 0x01) DCR [1:0] bits. Refer to Table 1 for more details.

(1) PWM Direct Control

The PWM input needs to be held high for normal operation. PWM dimming can be achieved by cycling the PWM input at a given frequency where a "low" on the PWM input turns off all IO current sinks and a "high" turns on all IO current sinks. The PWM pin can be toggled by external circuitry to allow PWM dimming. In a typical application, a microcontroller sets a register or counter that varies the pulse width on a GPIO pin. The SC5012/Q allows dimming over a wide frequency range (100Hz-30kHz) in order to allow compatibility with a wide range of devices. This includes the newest dimming strategies that avoid the audio band by using high frequency PWM dimming. In this manner, a wide range of illumination can be generated while keeping the instantaneous LED current at its peak value for high efficiency and color temperature. The

Table 1 — Led Dimming Control Methods

PWM Dimming Mode	Register Settings DCR[1:0]	PWM Input Source	LED PWM Output		Phase Shift Option
			PWM Frequency	PWM Duty Cycle	
PWM Direct Control	00	PWMI Pin Input	Same as the PWMI input (Range 100 Hz to 30kHz	Same as the PWMI input	NO
PWM Indirect Control **(Default Option)**	01	PWMI Pin Input	Set via the FREQ Register (0x05) and FAST_FREQ bit 10kHz (max): FAST_FREQ=0 20kHz(max): FAST_FREQ=1	Same as the duty cycle of the PWMI input	YES
I²C Control	11	I²C Control	Set via the FREQ Register (0x05) and FAST_FREQ bit 10kHz (max): FAST_FREQ=0 20kHz(max): FAST_FREQ=1	Set via the Duty Cycle Control Register (0x03, 0x04) 10 bits @ 10kHz output 9 bits @ 20kHz output	YES

Applications Information (continued)

SC5012/Q provides a 1000:1 dimming range at 1kHz PWM frequency. The LED current sinks turn on/off very rapidly (<25ns, typical). This allows a wide dimming ratio. An additional advantage of PWM dimming is that it avoids in-rush currents when filling the boost output capacitor. Simply apply the PWM signal to the device at 10% duty for a millisecond or two, and in-rush current is reduced. This dimming time will vary based on the number of LEDs and the size of the output capacitor. This can be easily determined during testing and programmed into the microcontroller firmware.

(2) PWM Indirect Control

This is the default mode for LED PWM dimming in the SC5012/Q. In this mode, the input signal applied on the PWM pin is passed through a duty cycle extractor block after the system has detected two successive duty cycles that are the same. The extractor measures the duty cycle of the PWM input, and, depending on the value of FAST_FREQ, the duty cycle is converted to a 9-bit value (FAST_FREQ = 1) or a 10-bit value (FAST_FREQ = 0). This value is then passed to the PWM generator block as shown in Figure 1.

The LED PWM output frequency is set via the FREQ register (address 0x05) and the FAST_FREQ bit.

With FAST_FREQ = 0, low dimming frequency option is selected and the PWM dimming frequency will be according to the following equation:

$$\text{PWM Dimming Frequency} = \frac{11\text{MHz}}{1024 \times [\text{FREQ}[7:0]+1]} = 10.75\text{kHz(max)}$$

With FAST_FREQ = 1, the high dimming frequency option is selected and the PWM dimming frequency is shown by the following equation:

$$\text{PWM Dimming Frequency} = \frac{11\text{MHz}}{512 \times [\text{FREQ}[7:0]+1]} = 21.5\text{kHz(max)}$$

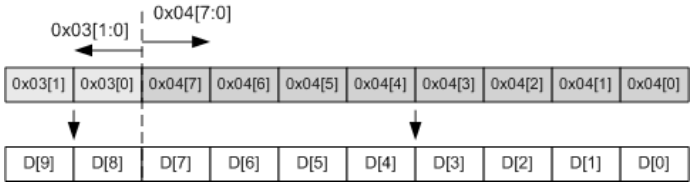
The default option is FAST_FREQ = 1. This gives 9-bit duty cycle resolution and up to 21.5kHz dimming frequency range. The PWM input is usually generated by the system graphics processor. This mode allows the user to set the PWM output dimming frequency independent of the PWMI input.

If the PWM signal has jitter, the SC5012/Q provides an option to filter it out. Hysteresis is also provided by selecting the WND[1:0] bits in the DCR register (address 0x01). WND[1:0] bits set the window comparator such that if a change in the duty cycle is detected which is smaller than the set window, then it is ignored.

(3) I²C Control

In I²C dimming mode (refer to Figure 1, page 17), both the output LED dimming duty cycle and the dimming frequency are set via the internal registers. The PWMI pin should be connected to ground. In this mode, the LED dimming duty cycle is set via the duty cycle registers (addresses 0x03, 0x04); and the dimming frequency is set via the FREQ register (address 0x05) and the FAST_FREQ bit.

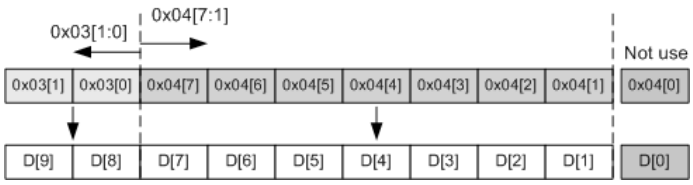
With FAST_FREQ = 0, the LED duty cycle can achieve 10-bit resolution, D[9:0], which is combined by two portions: (1) MSB portion - register address 0x03 [1:0] and (2) LSB portion - register address 0x04 [7:0] as shown below.



The dimming duty cycle with FAST_FREQ = 0 can be calculated as:

$$\text{LED Dimming Duty Cycle} = \{D[9:0]_{\text{decimal}}\}/2^{10}\text{-}1$$

With FAST_FREQ = 1, the LED duty cycle can achieve 9-bit resolution, D[9:1], which is combined by two portions: (1) MSB portion - register address 0x03 [1:0] and (2) LSB portion - register address 0x04 [7:1] as shown below.



Components Selection

The dimming duty cycle with FAST_FREQ = 1 can be calculated as:

$$\text{LED Dimming Duty Cycle} = \{D[9:1]_{decimal}\}/2^9\text{-}1$$

In both cases mentioned above, the duty cycle is fixed to be 0 when D[9:0] is set as 0x00.

The PWM dimming frequency is controlled the same way as in "Indirect Control".

Phase-Shift PWM Dimming

The SC5012/Q provides an option for phase-shifted LED PWM dimming. This option is available in both PWMI indirect control and I²C control. The phase-shift option is set by the PHASE_SHIFT bit in the Device Control Register (register address 0x01). This option delays the turn-on of the LED strings based on the number of the strings in operation (the number of the strings in operation is determined during the start-up). The delay time can be calculated by the following equation:

$$T_{\phi-phase} = \frac{1/f_{PWM}}{N},$$

N = number of strings in operation

f_{PWM} = LED PWM dimming frequency

Phase-shift mode is disabled during the soft-start period. This allows the output to ramp up to the correct voltage in a controlled fashion.

Phase-shifting reduces the peak input current, decreases EMI and improves the dimming linearity. The figures in the Typical Characteristics Section on page 7 show the improvement in dimming linearity with phase-shifted versus non-phase-shifted dimming.

Backlight Fade-in and Fade-out Options

The SC5012/Q features an option for fade-in and fade-out brightness control, which allows a smooth transition from one brightness level to another.

Registers associated with these fading functions are shown in this section.

1. Fade Option (register address 0x09) — sets fade enable options, fade time, fade type.
2. Fade Rate (register address 0x0A) — sets fade step size option.

The fade option register allows the user to select fading, choose between linear or logarithmic fading, and to set the fading time. The default setting is fading enabled with logarithmic mode. The fading time is determined by the LED PWM dimming frequency. The fade setting is shown in Table 2.

An example for calculating the linear fading time is shown in this section. Assuming LED PWM dimming frequency is 10kHz, then 10-bits are assigned for 1024 duty cycle settings.

Table 2 — Fade Setting

Duty Cycle Zone	Duty Cycle Range	Step Increment	Step Interval	Total Steps within the Range
1	0 to 511	1	2	512
2	512 to 767	1	1	256
3	768 to 1024	2	1	256

The time required to go from 10% (102/1024) to 90% (922/1024) duty cycle can be calculated using the following equation:

T_{PWM} = 100 µs (with 10kHz dimming frequency)

Cycle in Zone #1 = (511 - Starting Duty Cycle) x [(Zone #1 Step Interval) / (Zone #1 Step Increment)]

Cycle in Zone #2 = Total Steps in Zone #2 x [(Zone #2 Step Interval) / (Zone #2 Step Increment)]

Cycle in Zone #3 = (End Duty Cycle - 768) x [(Zone #3 Step Interval) / (Zone #3 Step Increment)]

In this case, the total cycle will be:

Total cycle = 2 x (511-102) + 1 x 256 + 0.5 x (922 - 768)
= 1151

Total Fading Time = Total Cycle x T_{PWM}
= 1151 x 100 µs = 115.1ms

Table 3 — Fault Protection Descriptions

Type of Fault	User Disable?	Fault Criteria	Action on Fault		Recovery	
			Device	$\overline{FLT}$ pin (latching / non-latching	Condition(s)	$\overline{FLT}$ pin
Input Under-voltage at VLDO	No	VLDO < 4.15V (rising)	No Startup	Not Active	VLDO > 4.15V (rising)	High
	No	VLDO < 4.0V (falling)	Shutdown	Not Active	VLDO > 4.15V (rising)	High
Input Under-voltage at VCC	No	VCC < 4.15V (rising)	No Startup	Not Active	VCC > 4.15V (rising)	High
	No	VCC < 4.0V (falling)	Shutdown	Not Active	VCC > 4.15V (rising)	High
Over-voltage Protection (OVP)	No	V_{OVP} > 1.23V (rising)	Regulate to OVP threshold: $I_{O(n)}$ = "on"	Low (non-latching)	V_{OVP} < 1.22V (falling)	High on removal of fault condition
Over-current Protection (OCP)	No	V_{CS} > 0.4V	Limit Q1 FET drain current < 0.4V/R9 (typ) (1)	High	V_{CS} < 0.4V	High
Shorted LED(s)	Yes, tie SCP to VLDO	$V_{IO(n)}$ > 10 x V_{SCP}	Device on: $I_{O(n)}$ = "off" Other $I_{O(All)}$ = "on"	Low (latching)	Replace Shorted LED(s) and Toggle EN or VCC	High
		$V_{IO(All)}$ > 10 x V_{SCP}	Device latch-off; $I_{O(All)}$ = "off"	Low (latching)	Replace Shorted LED(s) and Toggle EN or VCC	High
Open LED(s)	No	$V_{IO(n)}$ < 0.2V and OVP event	Device on: $I_{O(n)}$ = "off" Other $I_{O(All)}$ = "on"	Low (latching)	Replace Open LED(s) and Toggle EN or VCC	High
		$V_{IO(All)}$ < 0.2V and OVP event	Device latch-off; $I_{O(All)}$ = "off"	Low (latching)	Replace Open LED(s) and Toggle EN or VCC	High
Unused Strings	No	$V_{IO(All)}$ < 0.2V (start up)	Device on: $I_{O(n)}$ = "off" Other $I_{O(All)}$ = "on"	High		
Over-Temperature Protection (OTP)	No	T_J > 150°C (typ)	Device off; $I_{O(All)}$ = "off"	Low (latching)	Satisfy T_{HYS} > 10°C; Device On; $I_{O(All)}$ = "on"; Toggle EN, VCC	High

Components Selection (continued)

Time required to go from 10% (102/1024) to 90% (922/1024) duty cycle can be calculated using the following equation:

$$T_{PWM} = 100\,\mu s \text{ (PWM Dimming Period)}$$
$$\text{Total Cycle} = 2 \times (511 - 102) + 256 + \frac{1}{2} \times (922 - 768) = 1151$$
$$\text{Total Time} = 1151 \times T_{PWM} = 115.1\,ms$$

Optional Synchronization to SYNC Input

The SC5012/Q provides an option to synchronize the LED dimming to an external clock source connected to the SYNC pin. In certain applications, it may be beneficial to synchronize the LED drive signal to the LCD screen refresh signals such as VSYNC or HSYNC. This helps reduce or eliminate some of the problems associated with using LED backlights, such as flickering, shimmering, etc.

The phase lock loop available on the SC5012/Q can be programmed via I²C to synchronize the internal 11MHz oscillator to the SYNC input. Figures on page 9 show synchronization of SC5012/Q to a 21kHz SYNC signal applied on SYNC pin. The turn-on of the LED string IO1 (falling edge of V_{IO1}) is synchronized to the rising edge of the SYNC input. The turn-on of rest of the strings will be delayed based on the phase shifting algorithm.

Fault Protection

The SC5012/Q provides fault detection for low supply voltage, LED related faults, boost converter over-voltage and thermal shutdown. The open drain output pin ($\overline{FLT}$) indicates a system fault. The nature of the fault can be read from the fault status resistor (register address: 0x00) via I²C interface. Refer to Table 3 for a description of the Fault Protection Modes.

Other Possible Configurations

Depending on different application requirement, the SC5012/Q can also be easily configured to other topology such as SEPIC (Single-Ended Primary-Inductor Converter) configuration shown in Figure 3, page 27.

High Output Voltage Configuration

If high output voltage application is required, an additional external cascode MOSFET can be added on each IO pin to meet such requirement, please refer to Figure 4 on page 27 for reference.

In this case, the upper limit on the output voltage is mainly determined by the rating of the external MOSFET, heat dissipation, etc.

PCB Layout Considerations

The placements of the power components outside the SC5012/Q should follow the layout guidelines of a general boost converter. The Detailed Application Circuit is used as an example.

1. Capacitor (C20) should be placed as close as possible to the VCC pin and PGND to achieve the best performance. Place it next to the IC.
2. The decoupling capacitor (C17) for Pin VIN should return to AGND. Place it next to the IC.
3. Capacitor (C1) is the input power filtering capacitor for the boost. It needs to be tied to PGND.
4. The converter power train inductor (L1) is the boost converter input inductor. Use wide and short traces connecting these components.
5. The output rectifying diode (D1) uses a Schottky diode for fast reverse recovery. Transistor (Q1) is the external switch. Resistor (R9) is the switch current sensing resistor. To minimize switching noise for the boost converter, the output capacitor (C6) should be placed such that the loop formed by Q1, D1, C6 and R9, is minimized. The output of the boost converter is used to power up the LEDs. Use wide and short trace connecting Pin NDRV and the gate of Q1. The GNDs for R9 and C6 should be PGND. These components should be close to the SC5012/Q.
6. Resistor (R8) is the output current adjusting resistor for IO1 through IO4 and should return to AGND. Place it next to the IC.
7. Resistor (R6) is the switching frequency adjusting resistor and should return to AGND. Place it next to the IC.
8. The decoupling capacitor (C21) for Pin VLDO should return to AGND. Place it next to the IC.
9. Resistors (R4, R5) form a divider to set the SCP level, R4 should return to AGND. Place it next to the IC.
10. R11 and R10 form a divider to set the OVP level for VOUT, R10 should return to AGND. Place it next to the IC.

Components Selection (continued)

11. All the traces for components with AGND connection should avoid being routed close to the noisy areas.
12. An exposed pad is located at the bottom of the SC5012/Q for heat dissipation and analog ground. A copper area underneath the pad is used for better heat dissipation. On the bottom layer of the PCB another copper area, connected through vias to the top layer, is used for better thermal performance. The pad at the bottom of the SC5012/Q should be connected to AGND. AGND should be connected to PGND at a single point for better noise immunity.

Inductor Selection

The choice of the inductor affects the converter's steady state operation, transient response, and its loop stability. Special attention needs to be paid to three specifications of the inductor, its value, its DC resistance and saturation current. The inductor's inductance value also determines the inductor ripple current. The boost converter will operate in either CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) depending on its operating conditions. The inductor DC current or input current can be calculated using the following equation.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

I_{IN} - Input current;I_{OUT} – Output current;

V_{OUT} – Boost output voltage;

V_{IN} – Input voltage;

η – Efficiency of the boost converter.

Then the duty ratio under CCM is shown by the following equation.

$$D = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D}$$

V_D – Forward conduction drop of output rectifying diode

When the boost converter runs under DCM ($L < L_{boundary}$), it takes the advantages of small inductance and quick transient response; where as if the boost converter works under CCM ($L > L_{boundary}$), normally the converter has higher efficiency.

When selecting an inductor, another factor to consider is the peak-to-peak inductor current ripple, which is given by the following equation.

$$\Delta I_L = \frac{V_{IN} \times D}{f_{SW} \times L}$$

Usually this peak-to-peak inductor current ripple can be chosen between 30% to 50% of the maximum input DC current. This gives the best compromise between the inductor size and converter efficiency. The peak inductor current can be calculated using the following equation.

$$I_{L\text{-}peak} = I_{IN} + \frac{V_{IN} x D}{2 x f_{SW} x L}$$

For most applications, an inductor with value of 2.2µH to 22µH should be acceptable, (refer to the detailed application circuit on page26, Figure 2). The inductor peak current must be less than its saturation rating. When the inductor current is close to the saturation level, its inductance can decrease 20% to 35% from the 0A value depending on the vendor specifications. Using a small value inductor forces the converter in DCM, in which case the inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter's maximum output current and produces larger input voltage ripple. The DCR of the inductor plays a significant role for the total system efficiency and usually there is a trade-off between the DCR and size of the inductor. Table 4 lists some recommended inductors and their vendors.

Table 4. Recommended Inductors

Inductor	Website
HCM0703, 2.2uH~10uH	www.cooperindustries.com
IHLP-2525CZ-01, 4.7uH~10uH	www.vishay.com
MLPC0730L, 2.2uH~4.7uH	www.nec-tokin.com/english

Output Capacitor Selection

The next design task is targeting the proper amount of output ripple voltage due to the constant-current LED loads. Usually X5R or X7R ceramic capacitor is recommended. The ceramic capacitor minimum capacitance needed for a given ripple can be estimated using the following equation.

Components Selection (continued)

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times V_{RIPPLE}}$$

V_{RIPPLE} – Peak to peak output ripple.

The ripple voltage should be less than 200mV (pk-pk) to ensure good LED current sink regulation. For example, a typical application where 150mA/channel current is needed, the total output current for 4 channels will be 600mA, and 3x 10µF or 6x 4.7µF capacitors are recommended.

During load transient, the output capacitor supplies or absorbs additional current before the inductor current reaches its steady state value. Larger capacitance helps with the overshoot/undershoots during load transient and loop stability. Recommended ceramic capacitor manufacturers are listed in Table 5.

Table 5. Recommended Ceramic Capacitor Vendors

Vendor	Website
kemet	www.kemet.com
Vishay	www.vishay.com
TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

Input Capacitor Selection

X5R or X7R ceramic capacitor is recommended for input bypass capacitor. A 2.2µF capacitor is sufficient for the VCC input. Bypass the VIN input with a 10µF or larger ceramic capacitor.

Output Freewheeling Diode Selection

Schottky diodes are the ideal choice for SC5012/Q due to their low forward voltage drop and fast switching speed. Table 6 shows several different Schottky diodes that work properly with the SC5012/Q. Verify that the diode has a voltage rating greater than the maximum possible output voltage. The diode conducts current only when the power switch is turned off. The diode must be rated to handle the average output current. A diode rated for 1A average current will be sufficient for most designs.

Table 6. Recommended Rectifier Diodes

Rectifier Diode	Vendor Website
DFLS140	www.diodes.com
SS14/15/16, SS24/25/26	www.vishay.com

External Power MOSFET Selection

The boost converter in SC5012/Q uses an external power MOSFET to regulate the output voltage and output power to drive LED loads. This boost switching structure has an advantage in that the SC5012/Q is not exposed to high voltage. Only the external power MOSFET, freewheeling diode and the inductor will be exposed to the output voltage. The external power MOSFET should be selected with its voltage rating higher than the output voltage by minimum 30%. The current rating should be enough to handle the inductor peak current. Low R_{DS}(on) MOSFETs are preferred for achieving better efficiency.

The GD (gate driver) on SC5012/Q provides 1.5A (peak) current driving capability which is suitable for most MOSFETs for high frequency operation. The average current required to drive the mosfet is given by the following equation.

$$I_{GATE} = Q_G \times f_{SW}$$

Q_G — Gate charge

The $R_{DS(ON)}$ and its RMS current I_{S_RMS} of the power MOSFET will generate the conduction loss using the following equation.

$$P_{COND} = I_{S\_RMS}^2 \times R_{DS(on)}$$

The MOSFET's switch loss can be calculated using the following equation.

$$P_{SW} = ½ \times V_{IN} \times I_{L\_PEAK} \times f_{SW} \times (T_{ON} + T_{OFF})$$

Where T_{ON} and T_{OFF} are the MOSFET's on and off time and they can be estimated by the following equations.

$$T_{ON} = t_r + \frac{Q_{gd}}{(5 - V_{plateau}) / (5 + R_g)}$$

SEMTECH

Components Selection (continued)

$$T_{OFF} = t_f + \frac{Q_{gd}}{V_{plateau} / \ (5+R_g\ )}$$

Where t_r, t_f, Q_{gd} and $V_{plateau}$ can usually be found from datasheet of the selected MOSFET. R_g is the resistance of the optional resistor connected in serial on the gate of the MOSFET.

Current Sensing Resistor Selection

The switch current is sensed via the current sensing resistor, R_{CS}. The sensed voltage at this pin is used to set the peak switch current limit and also used for steady state regulation of the inductor current. The current limit comparator has a trip voltage of 0.4V. R_{CS} value is chosen to set the peak inductor and switch current using the following equation.

$$I_{SW(Peak)} = 0.4/R_{CS}$$

The power dissipation in R_{CS} can be calculated using the following equations.

$$P_{R\_CS} = I_{RMS}^2 \times R_{CS}$$

$$I_{RMS} = D \times [I_O/(1-D)]^2$$

I_O = Output DC Current, D = Duty Cycle

For the typical application circuit shown in the detailed application drawing(page26, Figure 2), the power dissipation on the sensing resistor is shown by the following equation.

Assuming V_{IN} = 12V and V_{OUT} = 33V, thus D = 63.6%,

$$I_{RMS} = 0.636 \times [0.6/0.364]^2 = 1.728(A)$$

$$P_{R\_CS} = 1.728^2 \times 0.11 = 0.328(W)$$

For this example, a 0.11 Ω 1% thick-film chip resistor rated at 1W can be used.

PLL Filter Component Selection

The Application Circuit shows the optimal R/C filter components for the PLL compensation. These are optimized for internal 1MHz switching frequency. Please contact Semtech application group if a different frequency is needed in a different system.

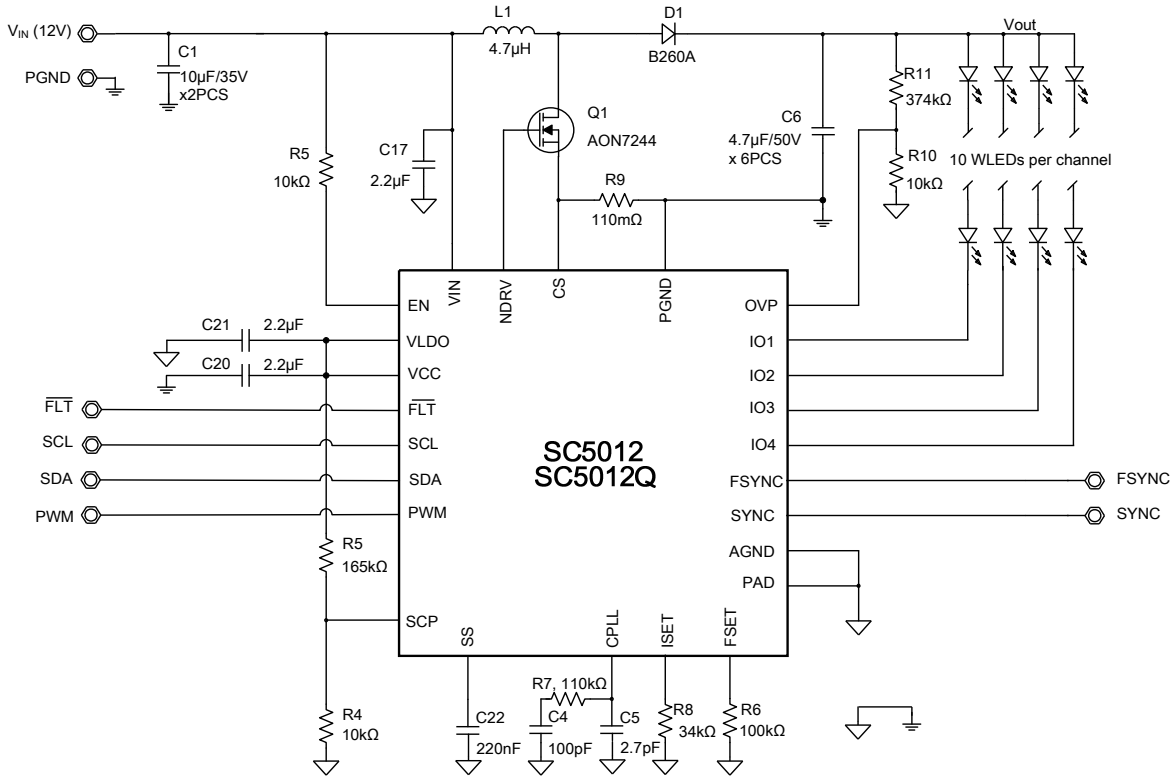


Figure 2— Application Circuit Example, 40 LED @ 150mA

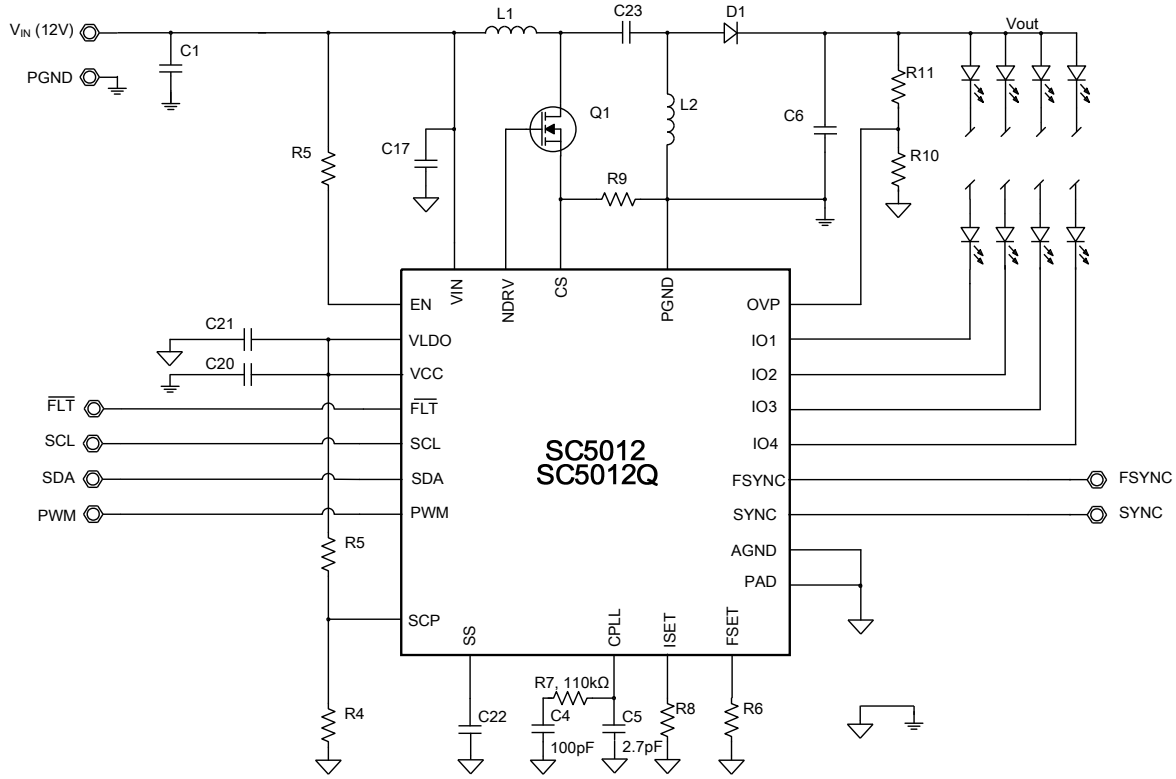


Figure 3— SEPIC Configuration

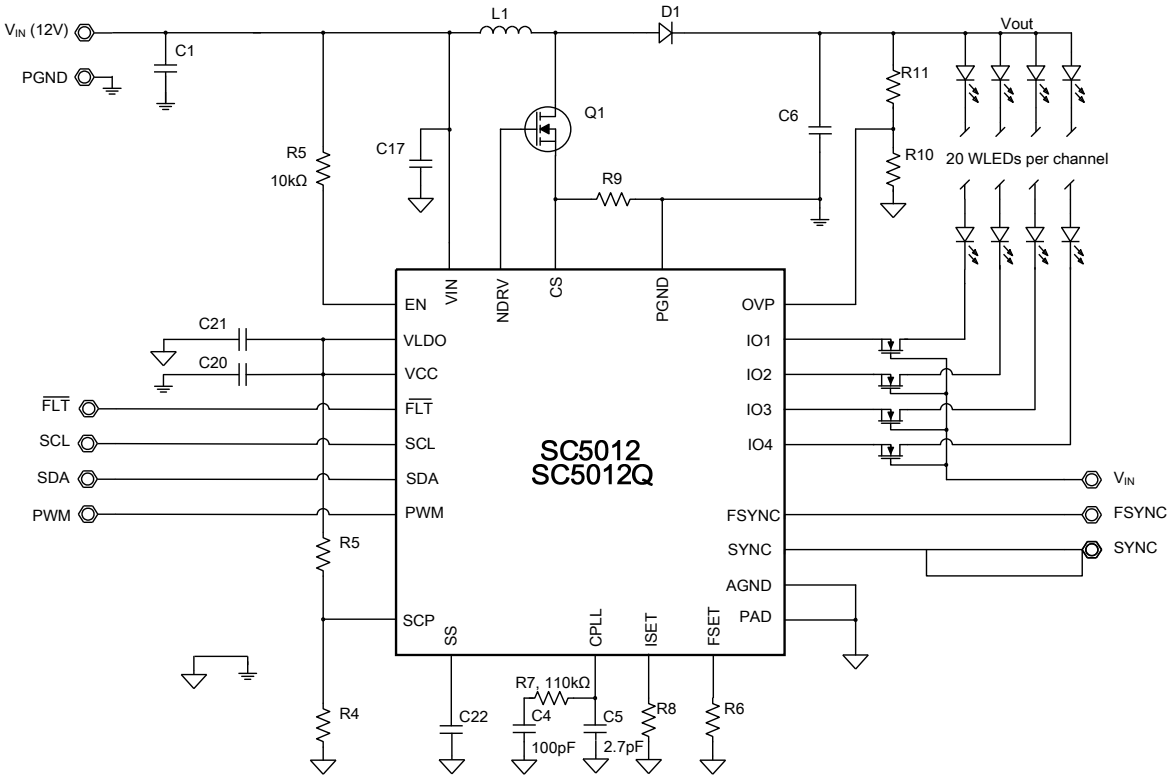


Figure 4— Cascode Configuration drives 80LEDs

Serial Interface

The I²C General Specification

The SC5012/Q is a read-write slave-mode I²C device and complies with the Philips I²C standard Version 2.1, dated January 2000. The SC5012/Q has 11 user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, supporting direct format for write operation. Read operations are supported on both combined format and stop separated format. While there is no auto increment/decrement capability in the SC5012/Q I²C logic, a tight software loop can be designed to randomly access the next register independent of which register you begin accessing. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

Limitations to the I²C Specifications

The SC5012/Q only recognizes seven bit addressing. This means that ten bit addressing and CBUS communication are not compatible. The device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s).

Slave Address Assignment

The 7-bit slave address is 0101 111x. The eighth bit is the data direction bit. 0x5F is used for read operation and 0x5E is used for write operation.

Supported Formats

The supported formats are described in the following subsections.

(1) Direct Format — Write

The simplest format for an I²C write is direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC5012/Q I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again, the slave acknowledges and the master terminates the transfer with the stop condition [P].

(2) Combined Format — Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC5012/Q I²C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the 8 bit data from the previously addressed register; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

(3) Stop Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The SC5012/Q then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the SC5012/Q with a read command. The device acknowledges this request and returns the data from the register location that had previously been set up.

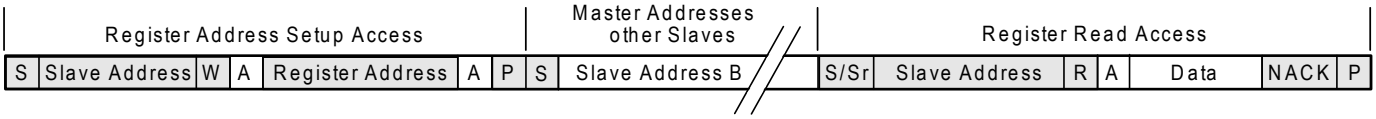
Serial Interface (continued)

I²C Direct Format Write

S – Start Condition
W – Write = '0'
A – Acknowledge (sent by slave)
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

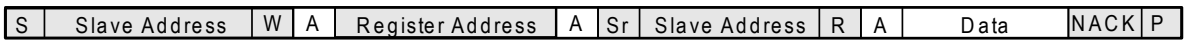
I²C Stop Separated Format Read



S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

I²C Combined Format Read



S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

Register Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value	Name
0x00	FSYNC_ GD	PLL_RDY	LED_ SHORT	LED_ OPEN	SYNC_ GD	OTP	OVP	FAULT/ CLF	0x00	Fault Status
0x01	WND1	WND0	FAST_ FREQ	FLT_EN	SYNC_EN	PHASE_ SHIFT	INT_ DUTY	INT_ PWM	0xB5	Device Control
0x02	IDAC7	IDAC6	IDAC5	IDAC4	IDAC3	IDAC2	IDAC1	IDAC0	0x1F	Analog Dimming Control
0x03	-	-	-	-	-	-	D9	D8	0x00	Dimming Duty Cycle Control 1
0x04	D7	D6	D5	D4	D3	D2	D1	D0	0x00	Dimming Duty Cycle Control 2
0x05	FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	0x00	Dimming Frequency Select
0x06	-	-	-	-	-	-	NPLL17	NPLL16	0x00	PLL Divider MSB
0x07	NPLL15	NPLL14	NPLL13	NPLL12	NPLL11	NPLL10	NPLL9	NPLL8	0x00	PLL Divider LSB2
0x08	NPLL7	NPLL6	NPLL5	NPLL4	NPLL3	NPLL2	NPLL1	NPLL0	0x08	PLL Divider LSB1
0x09	FADE_EN	FADE_ TYPE	-	-	-	STEP_ MUL2	STEP_ MUL1	STEP_ MUL0	0x80	Fade Options
0x0A	ARESYNC _EN	FADE_ RATE6	FADE_ RATE5	FADE_ RATE4	FADE_ RATE3	FADE_ RATE2	FADE_ RATE1	FADE_ RATE0	0x00	Fade Rate

Definition of Registers and Bits

Fault Status Register

This register monitors various fault conditions.

Bit Field	Definition	Read / Write	Description
0x00 [7]	FSYNC_GD	R	FSYNC status. (1 = FSYNC input is detected, 0 = no FSYNC signal detected)
0x00 [6]	PLL_RDY	R	PLL ready status
0x00 [5]	LED_SHORT	R	One or more LED strings faulted shorted
0x00 [4]	LED_OPEN	R	One or more LED strings faulted open
0x00 [3]	SYNC_GD	R	SYNC good signal. (1 = sync input is detected, 0 = no SYNC signal detected)
0x00 [2]	OTP	R	Thermal shutdown (1 = thermal OTP fault)
0x00 [1]	OVP	R	Output over-voltage fault (1 = OVP)
0x00 [0]	FAULT/CLF	R	OR of all fault conditions (0= no fault, 1 = fault condition)

Definition of Registers and Bits (continued)

Device Control Register

This register provides different control features of the device.

Bit Field	Definition	Read / Write	Description
0x01 [7:6]	WIN[1:0]	R/W	A modified duty cycle sent into the PWMI pin replaces the existing saved duty cycle when its deviation from the saved duty is outside the window for two consecutive samples. 00 = 0 bits (no window) 01 = ±1 bit window 10 = ±2 bit window 11 = ±3 bit window
0x01 [5]	FAST_FREQ	R/W	Determines the LED PWM dimming frequency selection: 1 = High PWM dimming frequency mode assuming 9-bit dimming duty cycle register D[8:0], dividing the system clock 11MHz / (512 x (FREQ+1)). 0 = Low PWM dimming frequency mode assuming 10-bit dimming duty cycle register D[9:0]; dividing the system clock 11MHz / (1024 x (FREQ+1)).
0x01 [4]	FLT_EN	R/W	This bit enables fault checking: 0 = LED_OPEN and LED_SHORT faults are not checked. 1 = LED_OPEN and LED_SHORT faults are checked.
0x01 [3]	SYNC_EN	R/W	Enables video signal synchronization with the PLL: 0 = SYNC is disabled. 1 = PLL tracks the VSYNC input signal.
0x01 [2]	PHASE_SHIFT	R/W	Enables String-by-String phase shifting. This is a don't care if INT_PWM=0. 0 = Phase shifting disabled. 1 = Phase shifting is enabled
0x01 [1]	INT_DUTY	R/W	Determines the duty cycle source. This is a don't care if INT_PWM = 0. 0 = LED duty cycle is set by the PWMI input 1 = LED duty cycle is set by the 10-bit duty cycle control registers
0x01 [0]	INT_PWM	R/W	Sets the LED PWM dimming source. 0 = PWM driven directly from the PWMI input source (direct PWM dimming) 1 = PWM driven from an internal oscillator (required for phase-shifted PWM dimming); enables the PLL.

Analog Dimming Control Register

This register is used to program the LED string current through the on-chip 8-bit DAC.

Bit Field	Definition	Read / Write	Description
0x02 [7:0]	IDAC [7:0]	R / W	8-bit analog dimming register — The LED current can adjusted in 256 (=2^8) steps from 0mA to max value determined by R_{ISET}.

Definition of Registers and Bits (continued)

Dimming Duty Cycle Control Register

These two registers (0x03 and 0x04) combine together as a 10-bit register for controlling the PWM dimming duty cycle.

Bit Field	Definition	Read / Write	Description
0x03 [1:0] 0x04 [7:0]	D [9:0]	R / W	10-bit PWM brightness setting — This value is spread over registers: 0x03 (MSB) and 0x04 (LSB). The LED PWM dimming duty cycle can be evenly adjusted by the 10-bit register from 0 to 100% with D[9:0] value changes from 0 to 0x3F.

Dimming Frequency Select Register

This register is used to program the LED PWM dimming frequency.

Bit Field	Definition	Read / Write	Description
0x05 [7:0]	FREQ [7:0]	R / W	This register sets the LED dimming frequency. FAST_FREQ = 1, then LED dimming frequency is equal to 11MHz / (512 x (FREQ+1)) FAST_FREQ = 0, then LED dimming frequency is equal to 11MHz / (1024 x (FREQ+1))

PLL Control Registers

This register is used to set the PLL divider value.

Bit Field	Definition	Read / Write	Description
0x06 [1:0] 0x07 [7:0] 0x08 [7:0]	NPLL [17:0]	R / W	These registers set the PLL divider value — The system clock is intended to run at 11MHz; this value divides the system clock down to a frequency comparable to the VSYNC signal's frequency to allow PLL synchronization. Typical values are shown below.

F_{IN}	PLL Divider N	Register Values	FPLL = (N+2) × F_{IN}
1 MHz	8	0x00 - 0x00 - 0x08	11MHz

Definition of Registers and Bits (continued)

Fade Options Registers

This register is used to select the fade in and fade out related features.

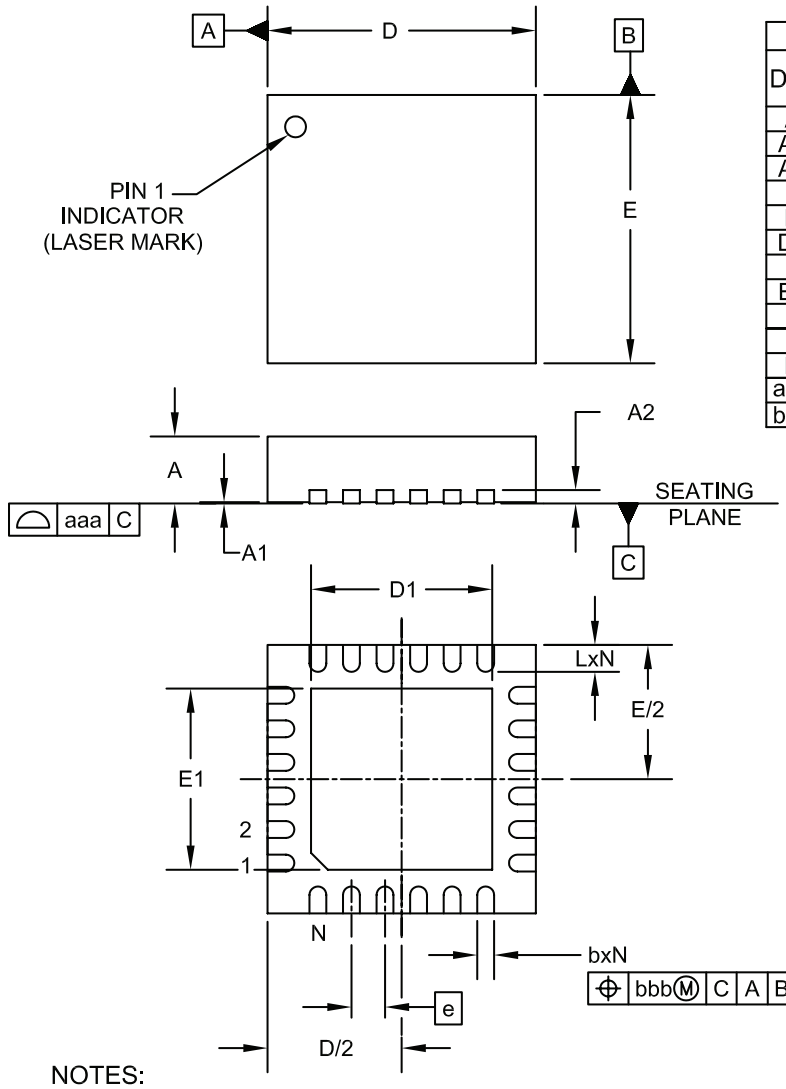
Bit Field	Definition	Read / Write	Description
0x09 [7]	FADE_EN	R/W	Enables the fading feature. FADE_EN = 0: No Fading; Jumps directly to new PWM value. FADE_EN = 1: Enables fading.
0x09 [6]	FADE_TYPE	R/W	Selects the fading type. FADE_TYPE = 0: Logarithmic Fading FADE_TYPE = 1: Linear Fading
0x09 [2:0]	STEP_MUL [2:0]	R/W	Used to speed up fade time, when selected LED PWM dimming frequency is low. Define a 2^N multiplier of the fade amount. STEP_MUL[2:0] = 000, N=0, multiplier = 1 STEP_MUL[2:0] = 001, N=1, multiplier = 2^1 = 2 STEP_MUL[2:0] = 010, N=2, multiplier = 2^2 = 4 STEP_MUL[2:0] = 011, N=3, multiplier = 2^3 = 8 STEP_MUL[2:0] = 100, N=4, multiplier = 2^4 = 16 STEP_MUL[2:0] = 101~111, N=5, multiplier = 2^5 = 32

Fade Rate Register

This register is used to program the rate of the duty cycle change during the fade in and fade out operation.

Bit Field	Definition	Read / Write	Description
0x0A [7]	ARBSYNC_ EN	R / W	Auto-resync enable bit. Synchronization of the PWM output to VSync is only enabled when VSYNC EN = 1
0x0A [6:0]	FADE_RATE [6:0]	R / W	Defines how often the duty is changed during a fade. Fade rate = PWM Output Rate / (1 + FADE_RATE[6:0])

Outline Drawing — MLPQ 4mm X 4mm, 24 Lead, EP 2.70mm X 2.70mm

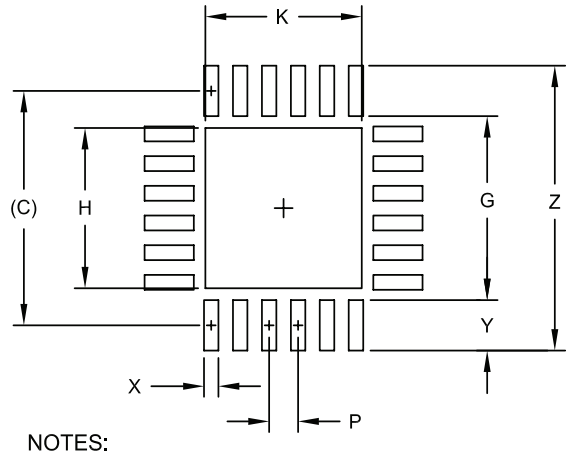


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.152	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.152	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ 4mm X 4mm, 24 Lead, EP 2.70mm X 2.70mm



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com