24/18-Channel Intelligent 12-Bit RGB LED Driver

Features

- 24/18-channel RGB LED Driver
- Independent 12-bit PWM modulation
  - Independent color mixing register per channel
  - Independent brightness register per RGB LED group
  - Linear or logarithmic brightness control
- Maximum output current: 25.5mA or 51mA
- Autonomous Breathing Mode
- Manual Breathing Mode
- High-precision current sinks
  - Device to device error：±5%
  - Channel to channel error：±5%
- LED Bank control
  - 3 banks for RGB LED color control
  - 1 bank for RGB LED brightness control
- Power save mode when all LED off > 30ms
- EMI reduction: slew rate control
- Over temperature protection
- 1.2V IO compatible
- Up to 1MHz I^2C interface, 4 independent addresses, 1 broadcast address
- Power supply: 2.7V to 5.5V
- QFN 4mm x 4mm x 0.85mm 32L package

Applications

- Smart speaker
- E-sports devices
- Smart home appliances

General Description

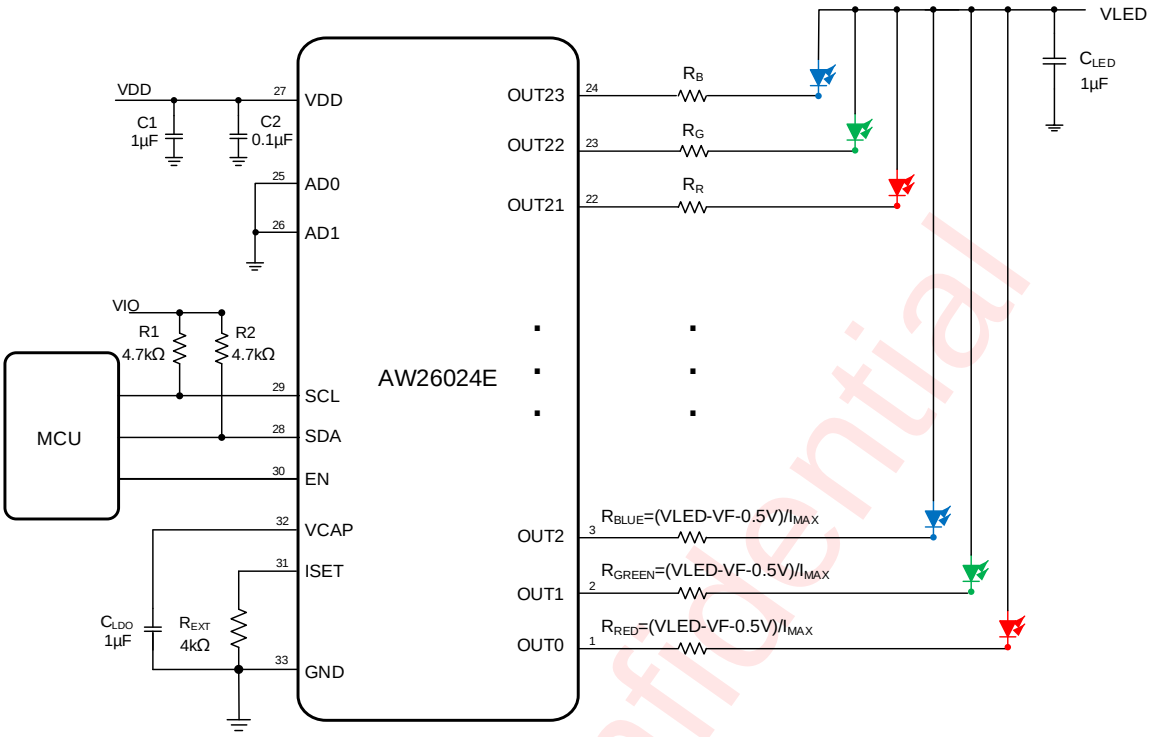
AW26024E/AW26018E is a 24/18-channel high precision constant current LED driver. AW26024E/AW26018E supports 5-bit globe current control. Each channel integrates independent 12-bit PWM generator which is composed of 8-bit brightness register and 8-bit color register. The maximum current of each channel is recommended to be configured via external resistor $R_{EXT.}$

AW26024E/AW26018E supports Auto-Breath-Pattern and has a flexible and efficient lighting effect programming function, which can reduce the resource occupation of the main controller.

AW26024E/AW26018E can be turned off with minimum current consumption by pulling the EN pin low. When EN pin pull high and all LEDs off >30ms, AW26024E/AW26018E enters power save mode.

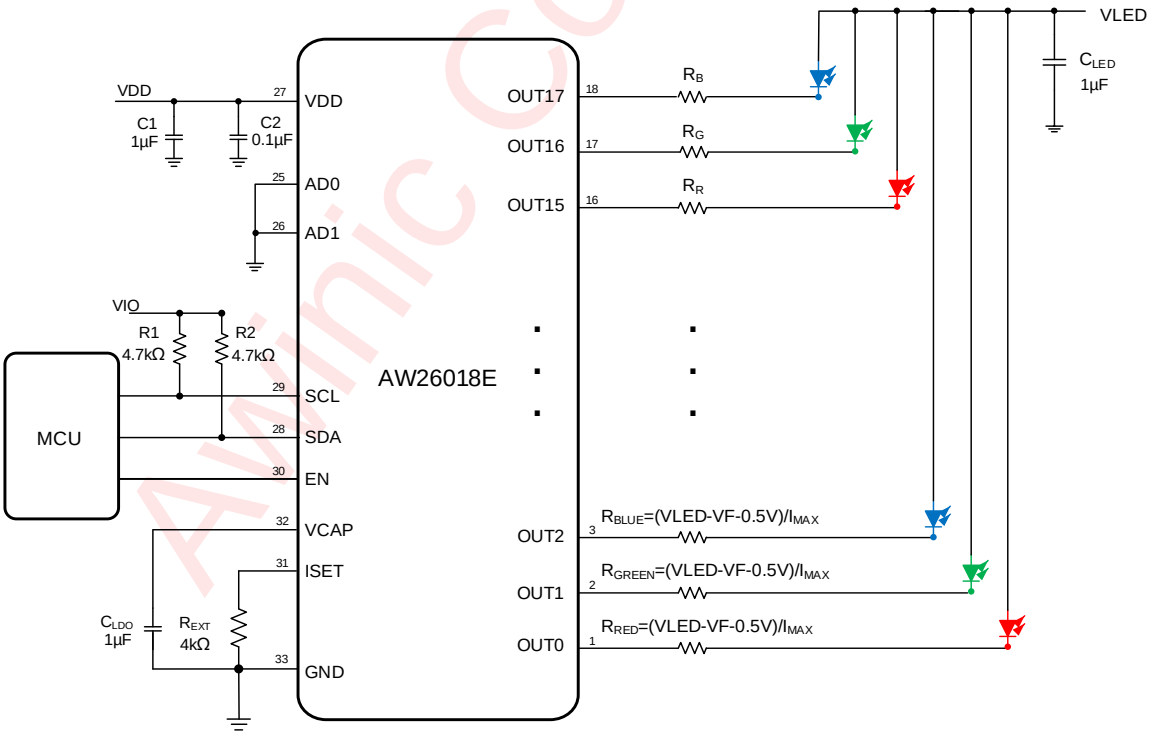
AW26024E/AW26018E is available in QFN 4mm x 4mm x 0.85mm-32L package. It operates from 2.7V to 5.5V over the temperature range of -40℃ to 105℃.

Typical Application Circuit



Note: The resistors(R_R, R_G, R_B) between LED and IC are only for thermal reduction. For more information, please refer to application information.

Figure 1 AW26024E Application Circuit

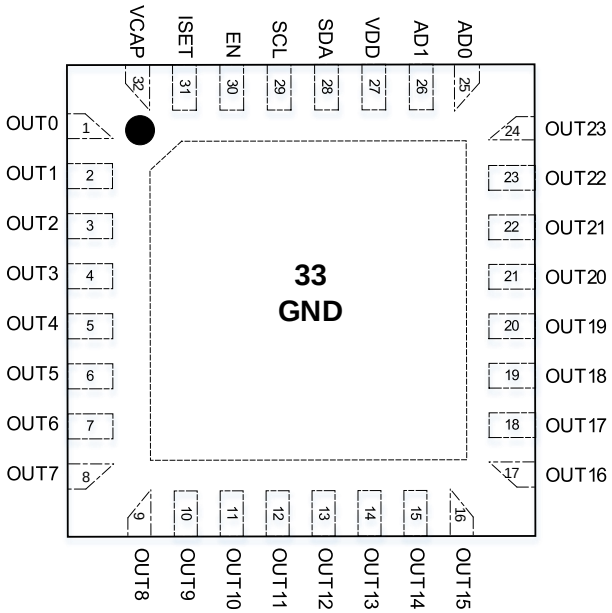


Note: The resistors(R_R, R_G, R_B) between LED and IC are only for thermal reduction. For more information, please refer to application information.

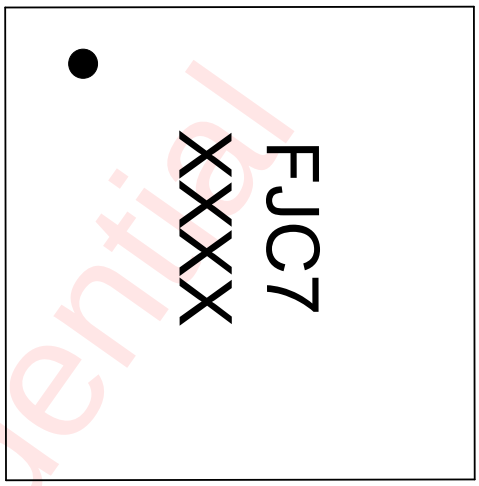
Figure 2 AW26018E Application Circuit

Pin Configuration And Top Mark

AW26024EQNR
(Top View)

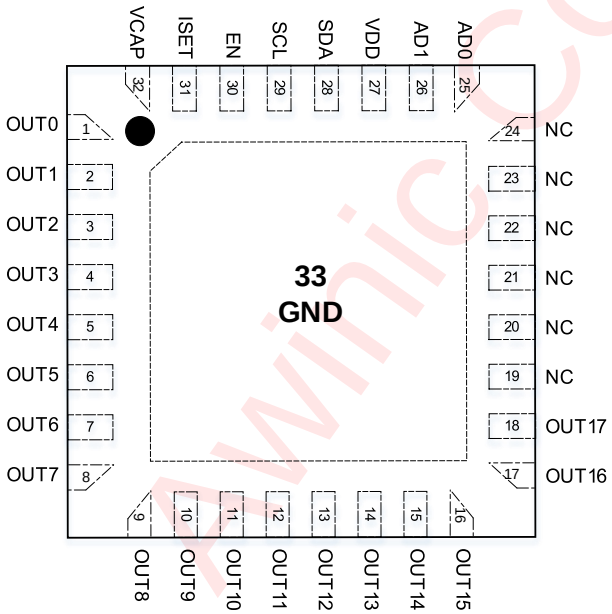


AW26024EQNR
(Top View)

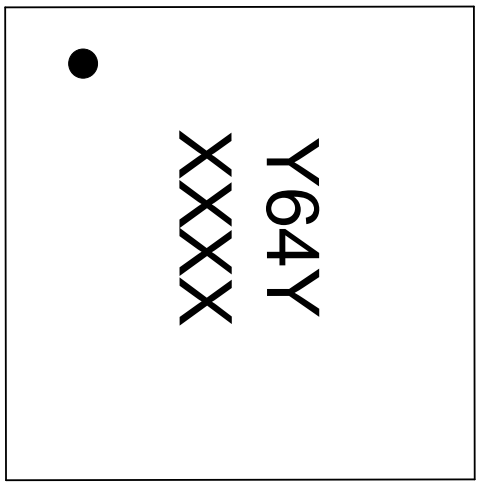


FJC7 – AW26024EQNR
XXXX – Production Tracing Code

AW26018EQNR
(Top View)



AW26018EQNR
(Top View)



Y64Y – AW26018EQNR
XXXX – Production Tracing Code

Figure 3 Pin Configuration and Marking

Pin Definition

No.	NAME	DESCRIPTION
1~24	OUT0~OUT23	Constant current sink, connect to LED's cathode
25~26	AD0, AD1	I²C address setting, connects to GND or VDD for different device address of I²C

27	VDD	Power supply
28	SDA	Serial data I/O for I²C interface
29	SCL	Serial clock input for I²C interface
30	EN	Shutdown the chip when pulled low.
31	ISET	Input terminal used to connect an external resistor. This regulates the global output current
32	VCAP	Connect a 1μF capacitor to GND.
33	GND	Ground

Functional Block Diagram

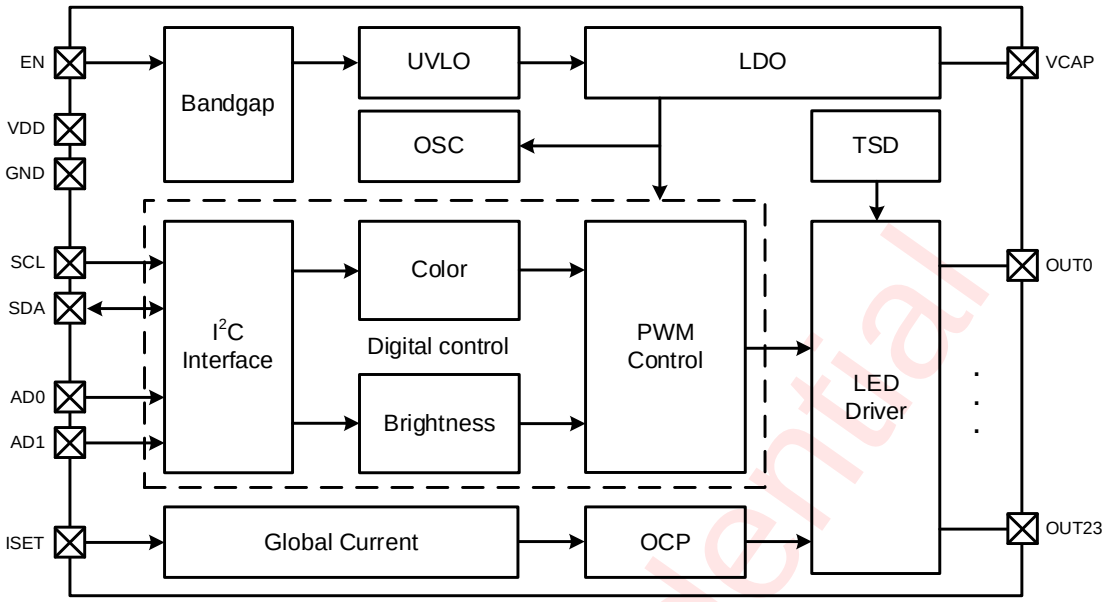


Figure 4 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW26024EQNR	-40℃～105℃	QFN 4X4-32L	FJC7	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW26018EQNR	-40℃～105℃	QFN 4X4-32L	Y64Y	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Over operating ambient temperature range (unless otherwise noted)(1)

PARAMETERS		RANGE
Supply voltage range V_{DD}		-0.3V to 6V
Input voltage range	EN, ADx, SCL, SDA	-0.3V to 6V
Output voltage range	OUTx, ISET	-0.3V to 6V
	VCAP	-0.3V to 2.5V
Junction-to-ambient thermal resistance θ_{JA}		36.4℃/W
Maximum operating junction temperature T_{J-MAX}		150°C
Storage temperature, T_{stg}		-65°C to 150°C
ESD (NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM test method: ESDA/JEDEC JS-001-2023, CDM test method: ESDA/JEDEC JS -002-2022.

Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	2.7		5.5	V
$V_{PULL-UP}$	SCL/SDA pull-up voltage	1.7		5.5	V
C_1, C_{LED}	Input capacitance	1			μF
C_2	Input capacitance	0.1			μF
C_{LDO}	Internal LDO capacitance	1			μF
R_{EXT}	Output current setting resistance	1.44			kΩ
T_A	Operating free-air temperature range	-40	25	105	°C

Electrical Characteristics

T_A=25°C, VDD=4.2V, R_{EXT}=2.94kΩ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{DD}	Supply voltage		2.7		5.5	V
I_{SD}	Shutdown supply current	V_{EN}=0		0.1	1	μA
I_{STB}	Standby supply current	V_{EN}=3.3V, CHIPEN=0		6	10	
I_{PS}	Power-save mode supply current NOTE(1)	V_{EN}=3.3V, CHIPEN=0,POWER_SAVE_EN=1, all the LEDs off duration>30ms(typical)		6	10	
I_{ACT}	Normal-mode supply current	I_{OUTx}=25mA, PWM=100%		1.8	3.5	mA
V_{UVR}	Undervoltage restart	V_{DD} rising			2.5	V
V_{UVF}	Undervoltage shutdown	V_{DD} falling	2			
V_{HYS}	UVLO hysteresis NOTE(1)			0.15		
I_{MAX}	Maximum output current	MAX_CUR_OPTION=0, V_{OUTX}=1V, PWM=100%			25.5	mA
		MAX_CUR_OPTION=1, V_{OUTX}=1V, PWM=100%			51	
I_{LIM}	Internal output current limit	MAX_CUR_OPTION=0, V_{OUTX}=1V, PWM=100%	35	50		
		MAX_CUR_OPTION=1, V_{OUTX}=1V, PWM=100% NOTE(1)	70	100		
I_{lkg}	Leakage current	PWM=0		0.1	1	μA
$I_{accuracy}$	Device to device current error, I_{ERR_DD}=(I_{AVE}-I_{SET})/I_{SET}x100%	I_{OUTx}=25mA, V_{OUTX}=1V, PWM=100%	-5%		5%	
I_{MATCH}	Channel to channel current error, I_{ERR_CC}=(I_{OUTX}-I_{AVE})/I_{AVE}x100%	I_{OUTx}=25mA, V_{OUTX}=1V, PWM=100%	-5%		5%	
V_{ISET}	ISET voltage			0.7		V
K_{IREF}	IREF ratio			105		
F_{PWM}	PWM switching frequency		25	29		kHz
$V_{Dropout}$	Voltage when LED current has dropped 5%	I_{OUTx}=51mA, PWM=100%		0.25	0.45	V
LOGIC INPUTS (EN, SCL, SDA, ADx)						
V_{IL}	Low level input voltage	LGC=0			0.36	V
V_{IH}	High level input voltage	LGC=0	0.84			
I_{LOGIC}	Input current		-1		1	μA
V_{SDA}	SDA output low level	I_{PULLUP}=10mA, LGC=0			0.4	V
PROTECTION CIRCUITS NOTE(1)						
$T_{(TSD)}$	Thermal shutdown junction temperature			160		℃
$T_{(HYS)}$	Thermal shutdown junction temperature hysteresis			15		

Note1：Guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C Interface Timing Requirements

Parameter		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

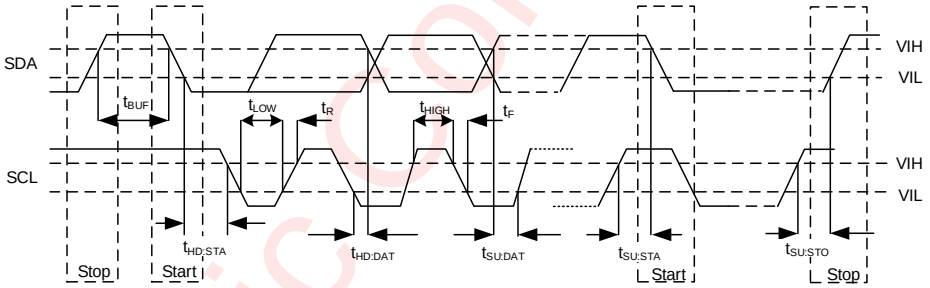


Figure 5 I²C Interface Timing

Detailed Functional Description

Reset

Power on Reset and Hardware Reset

After VDD powering on and the EN pin pulling up, I²C communication can be performed after 3ms.

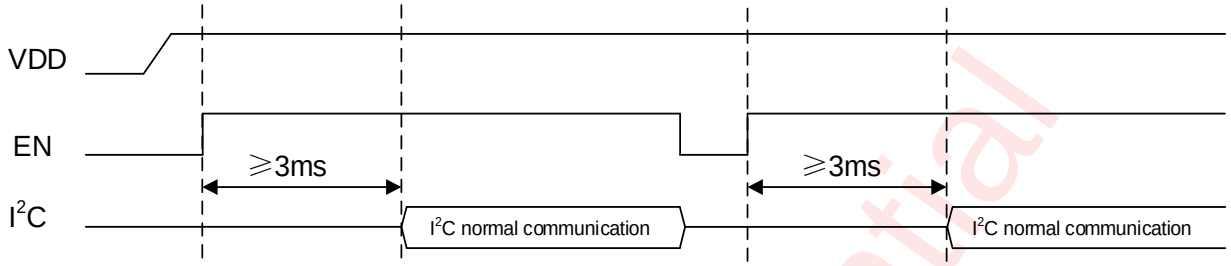


Figure 6 Power Up Timing

Soft Reset

Writing 0xFF into register RESET (address: 0x27), all configure registers will be reset. I²C communication can be performed after a delay of 3ms.

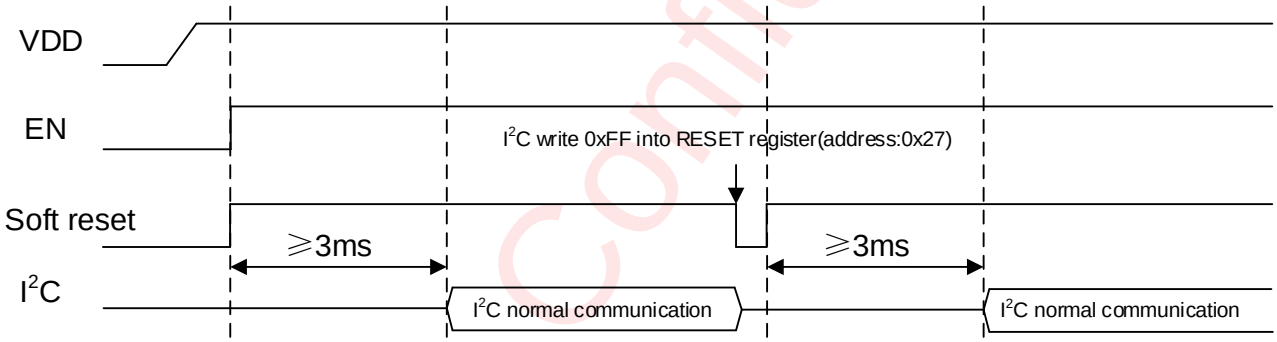


Figure 7 Software Reset Timing

Operation Mode

Shutdown

The device enters into shutdown mode automatically when EN is pulled low from any state, and all registers are reset and cannot be configured via I²C communication interface.

Initialization

The device enters initialization mode automatically from shutdown mode when EN is pulled high. If writing 0xFF into register RESET (address: 0x27) or UVLO is trigged from any state except shutdown, all configure registers will be reset, and the device will also enter initialization mode.

Standby

If the device completes initialization or the bit CHIPEN of register DEVICE_CFG0 (address: 0x00.bit6) is set to “0”, the device will enter standby mode. In this mode, the light control circuit is turned off, the power consumption is low, the registers data is retained, and the registers can be accessed through the I²C communication interface.

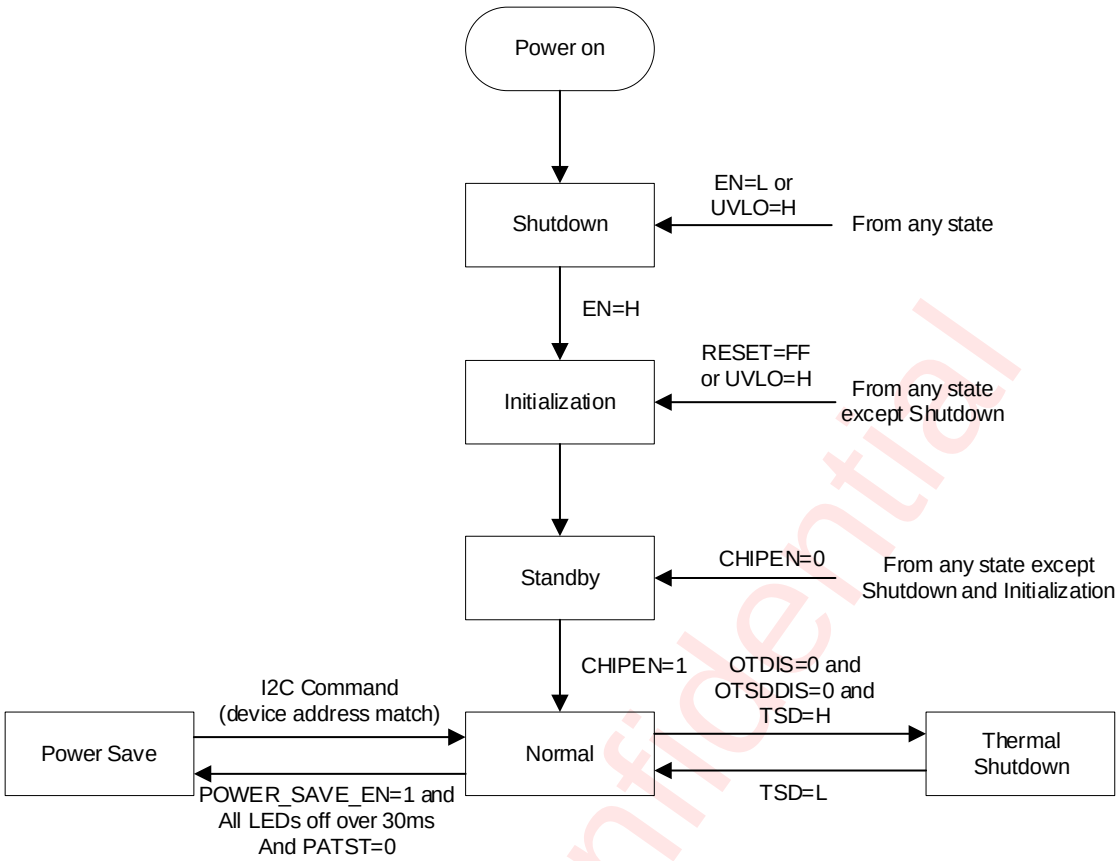


Figure 8 Operating Mode Transition

Normal

In the following three situations, the device will enter normal mode.

(1) In standby mode, the register CHIPEN is set to “1”;

(2) In thermal shutdown mode, the temperature reaches the recovery temperature;

(3) In power save mode, the device is accessed with I²C device address matching.

Power Save

If the bit POWER_SAVE_EN of register DEVICE_CFG1 (address: 0x01.bit4) is set to “1” and all LEDs off over 30ms and PATST=0 (address: 0x64.bit1), the device will enter power save mode. In this mode, the light control circuit is turned off, the power consumption is low, the registers data is retained, and the registers can be accessed through the I2C communication interface.

Thermal Shutdown

When the bits OTDIS and OTSDDIS of register OTCR (address: 0x6C.bit0 and bit1) are all set to “0” and the temperature is too high, the device will enter thermal shutdown mode. In this mode, LED driver will be turned off, and the registers data is retained.

PWM Control

The device supports independent color mixing and brightness control, providing smooth and rich lighting effects. Multiply the color mixing and brightness control data and modulate the output with a 9-bit precision PWM duty cycle. By configuring the bit PWM_DITHER_EN of register DEVICE_CFG1 (address: 0x01.bit2), 3-bit digital dither control can be performed on the basis of 9-bit precision to achieve 12-bit PWM output precision, which means increasing the brightness by 1 step every 8 PWM cycles, resulting in an average PWM duty cycle

increase of 1/8.

The frequency of the output PWM signal is about 29kHz, which is greater than the audible range and can eliminate audible noise.

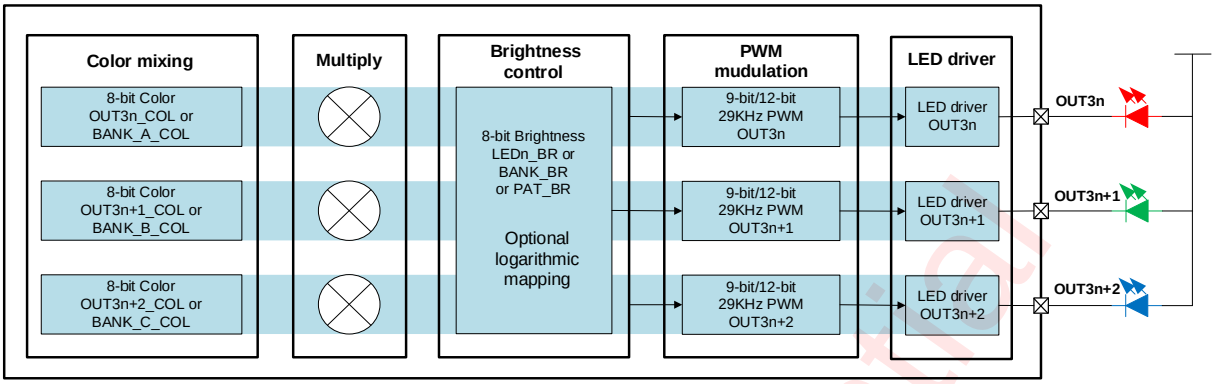


Figure 9 PWM Control

Independent Color Mixing

Each OUT channel has an independent 8-bit color mixing register OUT3n/3n+1/3n+2_COL (RGB，n=0~7, address: 0x0F~0x26). Each RGB LED can achieve 256 x 256 x 256 mixed color effects.

Independent Brightness

Each RGB LED has an independent 8-bit brightness control register LEDn_BR (n=0~7, address: 0x07 ~0x0E). When the color mixing configuration is fixed, using the independent brightness configuration can control each RGB LED to perform flexible dimming operations.

Logarithmic Brightness Mapping

By configuring the bit LOG_SCALE_EN of register DEVICE_CFG1 (address: 0x01.bit5), logarithmic curve mapping can be performed on the brightness control register LEDn_BR to achieve a more user-friendly visual effect of brightness changes. When the color mixing register is configured as 0xFF, the corresponding curve between the PWM duty cycle and the brightness control register is shown in the following figure.

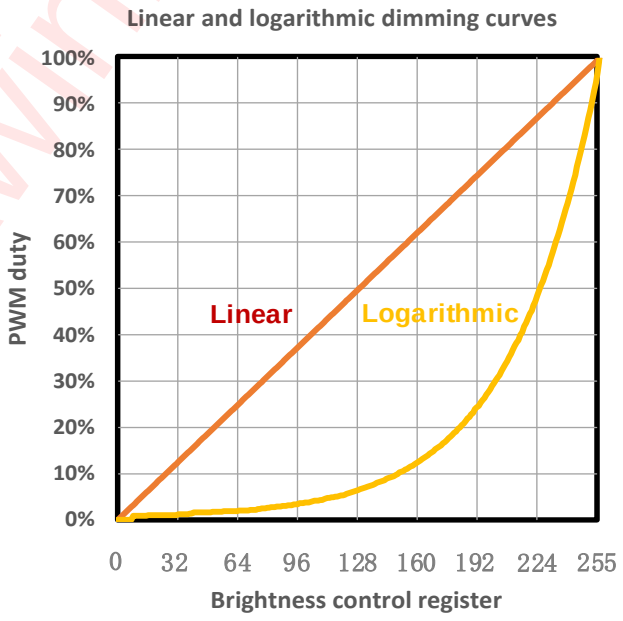


Figure 10 Linear and Logarithmic dimming curves

RGB LED Bank

For most LED animation effects, the brightness change process is basically the same, so the device provides a bank control mode that quickly achieves consistent color mixing and brightness control through simple register configuration updates.

Configure the bit LEDn_BANK_EN of register LED_CFG0 (n=0~7, address: 0x02.bit7~bit0) to select the corresponding RGB LED to join the bank mode. The brightness is controlled by the register BANK_BR_CFG (address: 0x03), and the RGB color mixing is controlled by registers BANK_A_COL_CFG (address:0x04), BANK_B_COL_CFG (address: 0x05), and BANK_C_COL_CFG (address: 0x06), respectively.

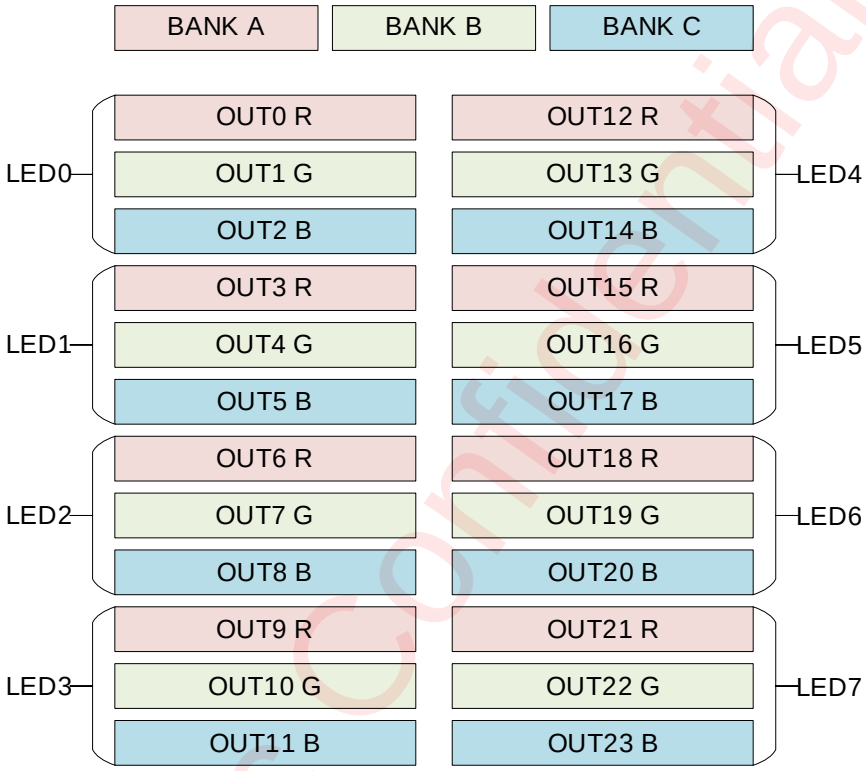


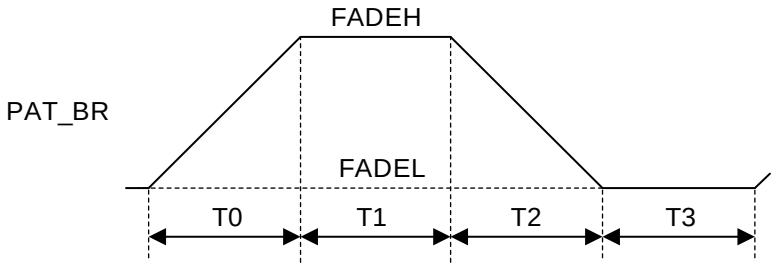
Figure 2 Bank Control

Autonomous Breathing Mode (ABM)

The device provides autonomous breathing mode. When the bit PATEN of register PATCFG (address: 0x63.bit0) is set to "1" and the bit PATMD of register PATCFG (address: 0x63.bit1) is set to "1", the autonomous breathing mode is enabled. On the basis of configuring the bit LEDn_BANK_EN of register LED_CFG0 as 0 , the corresponding RGB LED can be selected to join the autonomous breathing mode through configuring the bit LEDn_PAT_EN of register GCFG (address: 0x6B.bit7~bit0).

In this mode, the pattern controller will generate PAT_BR to control the brightness , and achieve a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 (address: 0x65, 0x66) define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off-time respectively. Register FADEH (address: 0x69) and FADEL (address: 0x6A) control the maximum and minimum brightness of the breathing respectively.

In this mode, color mixing is controlled by register OUT3n/3n+1/3n+2_COL (RGB , n=0~7, address: 0x0F~0x26).



Autonomous Breathing Mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3 through the bits LB of register PATT2 (address: 0x67.bit5~bit4). The end point of the loop can only be selected between the end of T0 and the end of T2 through the bits LE of register PATT2 (address: 0x67.bit7~bit6). The repeat times is determined by the end point defined. If LE is not “00”, the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If LE is “00”, the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times is decided by the bits RPT of registers PATT2 (address: 0x67.bit3~bit0) and PATT3 (address: 0x68). When setting RPT to “0”, the breathing pattern will run unlimited times.

After the breathing pattern is over, the status ENDFLAG of register PATGO (address: 0x64.bit2) will be set to “1”, and it will be cleared after reading out through I2C bus. Once breathing loop start again or set PATMD to “0”, the ENDFLAG will also be cleared.

When the bit PATRUN of register PATGO (address: 0x64.bit0) is set to “1”, breathing pattern is started. The full process of the autonomous breathing mode is as follows:

(1) Set OUT3n_COL, OUT3n+1_COL, OUT3n+2_COL, FADEH, FADEL parameter (n=0~7);

(2) Set LEDn_PAT_EN to select the LED in breathing pattern mode or not (n=0~7);

(3) Set T0~T3, LE, LB, RPT to determine breathing pattern;

(4) Set PATEN=1 to enable breathing pattern mode;

(5) Set PATMD=1 to select autonomous breathing mode;

(6) Set CHIPEN=1 to enable the chip;

(7) After waiting for at least 150us, set PATRUN=1 to start the autonomous breathing pattern.

Manual Breathing Mode (MBM)

The device provides manual breathing mode. When the bit PATEN of register PATCFG (address: 0x63.bit0) is set to “1” and the bit PATMD of register PATCFG (address: 0x63.bit1) is set to “0”, the autonomous breathing mode is enabled. On the basis of configuring the bit LEDn_BANK_EN of register LED_CFG0 as 0 , the corresponding RGB LED can be selected to join the manual breathing mode through configuring the bit LEDn_PAT_EN of register GCFG (address: 0x6B.bit7~bit0).

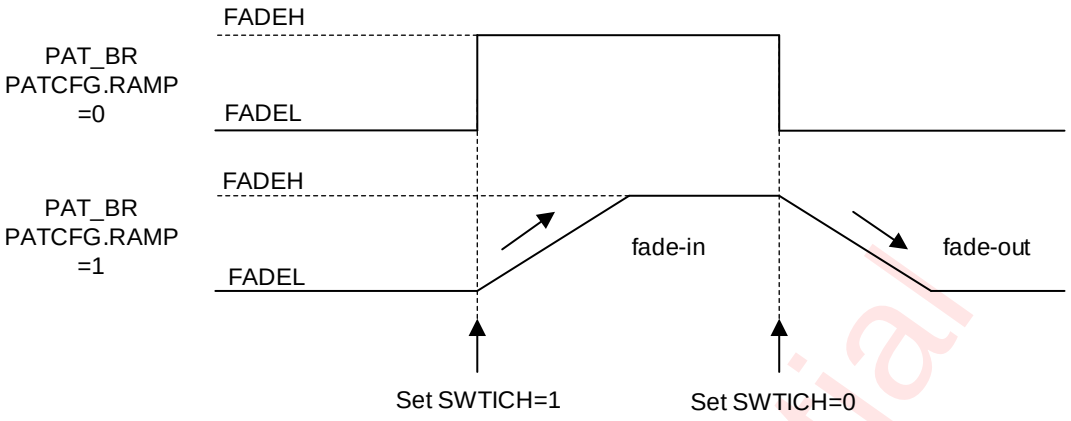
In this mode, the pattern controller will generate PAT_BR to control the brightness , and achieve a breathing lighting effect, which is configured by the user-defined timing parameter.

when the bit RAMP of register PATCFG (address: 0x63.bit2) is set to “1”, the smooth ramp up and ramp down will be enabled. At the same time, if the bit SWITCH of register PATCFG (address: 0x63.bit3) changes from “0” to “1”, PAT_BR will ramp up from FADEL to FADEH smoothly, and the ramp up time is controlled by the bits T0 of register PATT0 (address: 0x65.bit7~bit4). Similarly, if SWITCH changes from “1” to “0”, PAT_BR will ramp down from FADEH to FADEL smoothly, and the ramp down time is controlled by the bits T2 of register PATT1 (address: 0x66.bit7~bit4).

However, when the RAMP is set to “0”, if SWITCH changes from “0” to “1”, the output will directly change from FADEL to FADEH with no ramp. Similarly, if SWITCH changes from “1” to “0”, the output will directly change from FADEH to FADEL with no ramp.

In this mode, color mixing is controlled by register OUT3n/3n+1/3n+2_COL (RGB , n=0~7, address:

0x0F~0x26).



Manual Breathing Mode

The full process of the manual breathing mode is as follows:

(1) Set OUT3n_COL, OUT3n+1_COL, OUT3n+2_COL, FADEH, FADEL parameter (n=0~7);

(2) Set LEDn_PAT_EN to select the LED in breathing pattern mode or not (n=0~7);

(3) Set RAMP, T0 ,T2 to determine breathing pattern;

(4) Set PATEN=1 to enable breathing pattern mode;

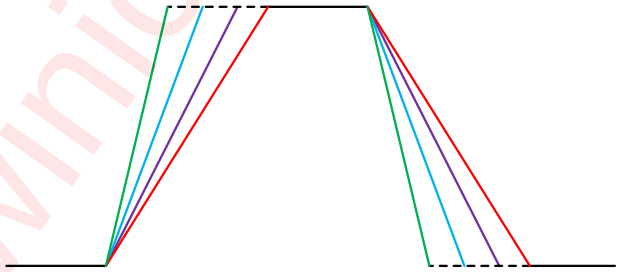
(5) Set PATMD=0 to select manual breathing mode;

(6) Set CHIPEN=1 to enable the chip;

(7) After waiting for at least 150us, alternately set SWITCH=1 or SWITCH=0 according to the lighting effect requirements.

Slew Rate

The device supports programmed slew rate control, which can change the transition time of the LED current sink on or off, so as to achieve the effect of reducing EMI. After writing 0xAA to the register SRCR_WREN_CFG (address: 0x60), the slew rate control is configured by the bits SRR and SRF of register SRCR (address: 0x61.bit1~bit0 and bit3~bit2).



Slew Rate Control

Maximum Current Setting

The maximum output current of OUTx is set by external resistor R_{ISET} and the bit GCC of register GCCR (address: 0x50.bit4~bit0). The current can be expressed by the following formula:

$$I_{OUTx\_MAX} = K \times \frac{V_{ISET}}{R_{ISET}} \times \frac{GCC+1}{32} \qquad x=0, 2, 3, \ldots, 23$$

Where V_{ISET}=0.7V, K=105

The device supports two levels of maximum output current (I_{MAX}).

When the bit MAX_CUR_OPTION of register DEVICE_CFG1 (address: 0x01.bit1) is set to “0”, the

recommended maximum current is 25.5mA.

When the bit MAX_CUR_OPTION of register DEVICE_CFG1 (address: 0x01.bit1) is set to "1", the recommended maximum current is 51mA.

If ISET pin is connected to a small resistor or shorted to ground. The max current is limit by internal OCP circuit. More information about current limit please refer to section OCP.

General I²C Operation

The device supports the I²C protocol in fast mode at 400kHz and fast mode plus at 1MHz. The two communication lines are a serial data line (SDA) and a serial clock line (SCL).The pull-up resistor for the SDA and SCL can be selected from 1k to 10kΩ. Usually, 4.7kΩ is recommended for 400kHz I²C.

Device Address

The device is defined by connecting GND or VDD to the AD0 and AD1 pins from the address. When GND or VDD is connected to the AD0 and AD1 pins, four independent device addresses can be combined (see Tables 1). Regardless of the settings of the AD0 and AD1 pins, the device will respond with a broadcast from the address. Perform global write operations on broadcast addresses to configure all devices simultaneously. This device supports global reading using broadcast addresses; However, the read data is only valid when all devices on the I²C bus contain the same value.

Table 1 I²C Device Address Configuration

AD1 Connection	AD0 Connection	Device Address	
		Independent	Broadcast
GND	GND	0x28	0x3C
GND	VDD	0x29	
VDD	GND	0x2A	
VDD	VDD	0x2B	

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

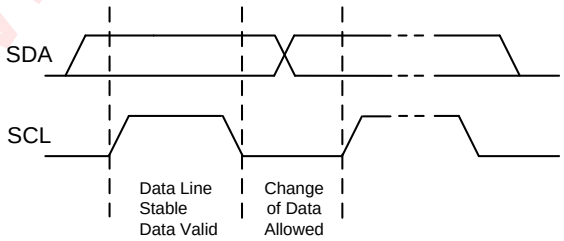


Figure 3 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

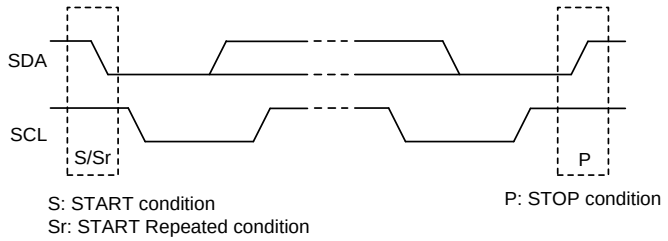


Figure 4 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

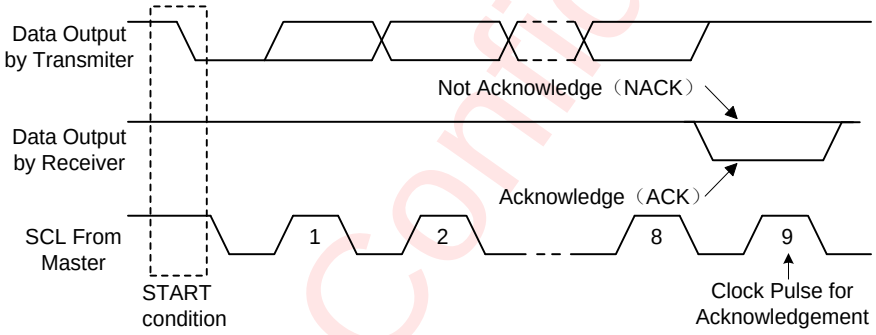


Figure 5 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal

h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)

i) Master generates STOP condition to indicate write cycle end

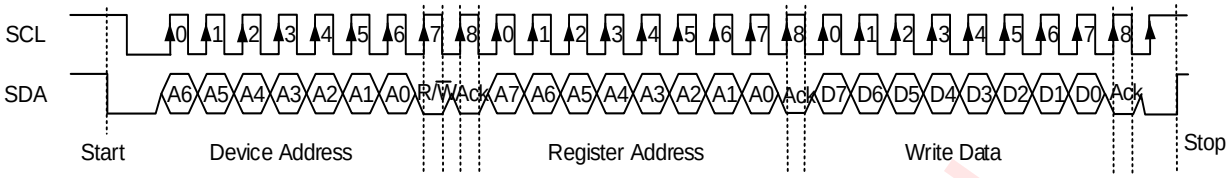


Figure 6 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

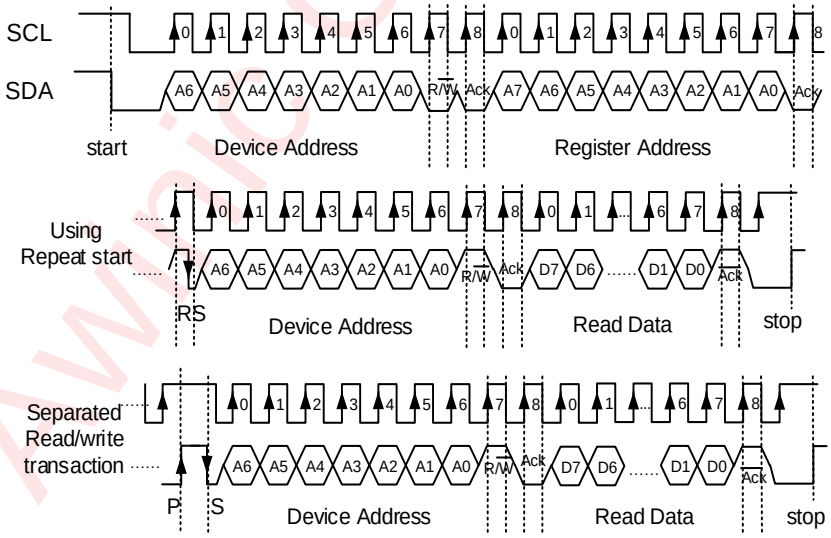


Figure 7 I²C Read Byte Cycle

Auto-Increment Feature

The auto-increment feature is enabled by default, when bit AUTO_INCR_EN of register DEVICE_CFG1 (address:0x01.bit3) is set to “0” , the feature is disabled. It allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the device, the internal address index counter is incremented by one, and the next register is written.

Under Voltage Lock Out (UVLO)

The device monitors the VDD voltage. If the voltage is higher than the rising voltage threshold, the device works normally. If the voltage is lower than the falling voltage threshold, UVLO will be triggered, and the device will be in initialization mode to avoid uncertain working conditions. Please refer to the electrical parameter table for specific parameters.

Over Temperature Protection (OTP)

The device monitors the junction temperature to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical), the device switches into thermal shutdown mode, LED driver will be turned off. The device releases thermal shutdown when the junction temperature of the device is reduced to 145°C (typical).

By configuring the bit OTDIS of register OTCR (address: 0x6C.bit0), the over temperature detection function can be enabled or disabled. By configuring the bit OTSDDIS of register OTCR (address: 0x6C.bit1), select whether to enter thermal shutdown mode when over temperature occurs.

Over Current Protection (OCP)

The device monitors the current of ISET pin. When the current above the threshold, the surplus portion cannot be mirrored to the output pin, thereby limiting the maximum current. Two configurable current limit threshold is provided, user can select the desired setting by configuring the bit MAX_CUR_OPTION of register DEVICE_CFG1 (address: 0x01.bit1). Please refer to the electrical parameter table for specific parameters.

REGISTER CONFIGURATION

REGISTER LIST

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	DEVICE_CFG0	RW	-	CHIPEN	-						0x00
0x01	DEVICE_CFG1	RW	-		LOG_SCALE_EN	POWER_SAVE_EN	AUTO_INCR_EN	PWM_DITHER_EN	MAX_CUR_OPTION	LED_GLOBAL_OFF	0x3C
0x02	LED_CFG0	RW	LED7_BANK_EN (only for AW26024E)	LED6_BANK_EN (only for AW26024E)	LED5_BANK_EN	LED4_BANK_EN	LED3_BANK_EN	LED2_BANK_EN	LED1_BANK_EN	LED0_BANK_EN	0x00
0x03	BANK_BR_CFG	RW	BANK_BR								0xFF
0x04	BANK_A_COL_CFG	RW	BANK_A_COL								0x00
0x05	BANK_B_COL_CFG	RW	BANK_B_COL								0x00
0x06	BANK_C_COL_CFG	RW	BANK_C_COL								0x00
0x07~0x0E	LED0_BR_CFG ~ LED7_BR_CFG	RW	LED0_BR~ LED7_BR (LED6/7_BR are only for AW26024E)								0xFF
0x0F~0x26	OUT0_COL_CFG ~ OUT23_COL_CFG	RW	OUT0_COL~ OUT23_COL (OUT18~23_COL are only for AW26024E)								0x00
0x27	RESET	WO	SOFT_RESET								0x00
0x50	GCCR	RW	-				GCC				0x1F
0x60	SRCR_WREN_CFG	RW	SRCR_WREN								0x00
0x61	SRCR	RW	-				SRR		SRF		0x00
0x62	LGCR	RW	LGC								0x00
0x63	PATCFG	RW	-				SWITCH	RAMP	PATMD	PATEN	0x00
0x64	PATGO	RW	-					ENDFLG	PATST	PATRUN	0x00
0x65	PATT0	RW	T0				T1				0x00
0x66	PATT1	RW	T2				T3				0x00

0x67	PATT2	RW	LE		LB		RPT_H			0x00
0x68	PATT3	RW	RPT_L							0x00
0x69	FADEH_CFG	RW	FADEH							0x00
0x6A	FADEL_CFG	RW	FADEL							0x00
0x6B	GCFG	RW	LED7_PAT_EN	LED6_PAT_EN	LED5_PAT_EN	LED4_PAT_EN	LED3_PAT_EN	LED2_PAT_EN	LED1_PAT_EN	LED0_PAT_EN	0x00
0x6C	OTCR	RW	-					OTST	OTSDDIS	OTDIS	0x00
0x6D	STAT	RO	-						OSC_OK	PUST	0x00
0x6E	CHIP_ID	RO	CHIPID								0xB0 0xB1
0x70	I²C_BROADCAST_DIS_CFG	RW	I²C_BROADCAST_DIS								0x00
0x71	I²C_TIMEOUT_EN_CFG	RW	I²C_TIMEOUT_EN								0x00

REGISTER DETAILED DESCRIPTION

DEVICE_CFG0: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RO	Not used	0x0
6	CHIPEN	RW	Chip enable 0 : Disable 1 : Enable	0x0
5:0	Reserved	RO	Not used	0x0

DEVICE_CFG1: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0x0
5	LOG_SCALE_EN	RW	Logarithmic PWM mapping selection 0 : Linear mapping 1 : Logarithmic mapping	0x1
4	POWER_SAVE_EN	RW	Power save mode enable 0 : Disable 1 : Enable	0x1
3	AUTO_INCR_EN	RW	I^2C register address automatic increment mode enable 0 : Disable 1 : Enable	0x1
2	PWM_DITHER_EN	RW	PWM precision selection 0 : 9bit PWM 1 : 12bit (9bit+3bit dither) PWM	0x1
1	MAX_CUR_OPTION	RW	Maximum current selection 0 : 25.5 mA 1 : 51 mA	0x0
0	LED_GLOBAL_OFF	RW	All LEDs off enable 0 : Diasble 1 : Enable	0x0

LED_CFG0: (Address 02h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	LED7_BANK_EN	RW	LED7 bank mode enable 0 : Disable 1 : Enable	0x0
6	LED6_BANK_EN	RW	LED6 bank mode enable 0 : Disable 1 : Enable	0x0
5	LED5_BANK_EN	RW	LED5 bank mode enable 0 : Disable 1 : Enable	0x0
4	LED4_BANK_EN	RW	LED4 bank mode enable 0 : Disable 1 : Enable	0x0
3	LED3_BANK_EN	RW	LED3 bank mode enable 0 : Disable 1 : Enable	0x0
2	LED2_BANK_EN	RW	LED2 bank mode enable 0 : Disable 1 : Enable	0x0
1	LED1_BANK_EN	RW	LED1 bank mode enable 0 : Disable 1 : Enable	0x0
0	LED0_BANK_EN	RW	LED0 bank mode enable 0 : Disable 1 : Enable	0x0

BANK_BR_CFG: (Address 03h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BANK_BR	RW	The brightness setting of bank mode applies to all bank enabled LEDs 00h : 0% of full brightness ... 80h : 50% of full brightness ... FFh : 100% of full brightness	0xFF

BANK_A_COL_CFG: (Address 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BANK_A_COL	RW	The color mixing setting of bank mode applies to all bank enabled OUT3n (n= 0~7) 00h : The color mixing rate is 0% ... 80h : The color mixing rate is 50% ... FFh : The color mixing rate is 100%	0x0

BANK_B_COL_CFG: (Address 05h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BANK_B_COL	RW	The color mixing setting of bank mode applies to all bank enabled OUT3n+1 (n= 0~7) 00h : The color mixing rate is 0% ... 80h : The color mixing rate is 50% ... FFh : The color mixing rate is 100%	0x0

BANK_C_COL_CFG: (Address 06h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	BANK_C_COL	RW	The color mixing setting of bank mode applies to all bank enabled OUT3n+2 (n= 0~7) 00h : The color mixing rate is 0% ... 80h : The color mixing rate is 50% ... FFh : The color mixing rate is 100%	0x0

LEDn_BR_CFG (n=0~7): (Address 07h~0Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	LEDn_BR	RW	LED0 brightness setting when LEDn bank mode disable and breathing mode disable 00h : 0% of full brightness ... 80h : 50% of full brightness ... FFh : 100% of full brightness	0xFF

OUT0_COL_CFG~OUT23_COL_CFG: (Address 0Fh~26h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	OUT0_COL~OUT23_COL	RW	OUT3n、OUT3n+1、OUT3n+2 color mixing setting when LEDn bank mode disable (n=0~7) 00h : The color mixing rate is 0% ... 80h : The color mixing rate is 50% ... FFh : The color mixing rate is 100%	0x0

RESET: (Address 27h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SOFT_RESET	WO	Soft reset, reset all register when FFh is written	0x0

GCC5: (Address 50h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:5	Reserved	RO	Not used	0x0
4:0	GCC	RW	Globle current control	0x1F

SRCR_WREN_CFG: (Address 60h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	SRCR_WREN	RW	Register SRCR write enable. Writting 0xAA to the register SRCR_WREN_CFG, and it will be set to "1", otherwise the register will be set to "0" 0 : Disable. 1 : Enable.	0

SRCR: (Address 61h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3:2	SRR	RW	Slew rate control for all LEDs output rising time, the bits SRR can be written only when SRCR_WREN = 1 b00: 3ns b01: 1ns b10: 10ns b11: 6ns	0
1:0	SRF	RW	Slew rate control for all LEDs output falling time, the bits SRF can be written only when SRCR_WREN = 1 b00: 1ns b01: 3ns b10: 6ns b11:10ns	0

LGCR: (Address 62h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	LGC	RW	Logic level selection of SDA/SCL. Writting 0xCC to the register LGCR, and it will be set to "1", otherwise the register will be set to "0" 0 : 0.84V/0.36V 1 : 1.4V/0.4V	0

PATCFG: (Address 63h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	Reserved	RO	Not used	0
3	SWITCH	RW	Switch on or off at MBM 0 : Controlled by FADEL_CFG 1 : Controlled by FADEH_CFG	0

2	RAMP	RW	Ramp enable at MBM 0 : Disable 1 : Enable	0
1	PATMD	RW	Breathing mode selection 0 : Manual breathing mode (MBM) 1 : Autonomous breathing mode (ABM)	0
0	PATEN	RW	Breathing mode enable 0 : Disable 1 : Enable	0

PATGO: (Address 64h)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RO	Not used	0
2	ENDFLG	RO	ABM loop end flag, read only and will be cleared after reading out, 0: ABM pattern is not over 1: ABM pattern is over	0
1	PATST	RO	ABM status 0: ABM pattern is stop 1: ABM pattern is running	0
0	PATRUN	RW	ABM pattern run control Write “1” to run ABM pattern after the CHIPEN has been configured to 1 and has waited at least 150us Note: You shall write “0” and then write “1” to this bit to restart a new ABM pattern.	0

PATT0: (Address 65h)

Bit	Symbol	R/W	Description	Default
7:4	T0	RW	ABM and MBM ramp rise time. The step from FADEL to FADEH is br_step and the change time is rise_time, A = FADEH - FADEL b0000 : br_step = A, rise_time = 0ms; If FADEH = 255, FADEL = 0, then rise_time = 0s b0001 : br_step = 8, rise_time = (4.37*A/8)ms; If FADEH = 255, FADEL = 0, then rise_time = 0.14s b0010 : br_step = 4, rise_time = (4.37*A/4)ms; If FADEH = 255, FADEL = 0, then rise_time = 0.28s b0011 : br_step = 2, rise_time = (4.37*64*A/171)ms ; If FADEH = 255, FADEL = 0, then rise_time = 0.42s b0100 : br_step = 2, rise_time = (4.37*A/2)ms; If FADEH = 255, FADEL = 0, then rise_time = 0.56s b0101 : br_step = 1, rise_time = (4.37*32*A/43)ms; If FADEH = 255, FADEL = 0, then rise_time = 0.83s b0110 : br_step = 1, rise_time = (4.37*A)ms; If FADEH = 255, FADEL = 0, then rise_time = 1.11s b0111 : br_step = 1, rise_time = (4.37*64*A/43)ms; If FADEH = 255, FADEL = 0, then rise_time = 1.66s b1000 : br_step = 1, rise_time = (4.37*2*A)ms; If FADEH = 255, FADEL = 0, then rise_time = 2.23s b1001 : br_step = 1, rise_time = (4.37*32*A/13)ms; If FADEH = 255, FADEL = 0, then rise_time = 2.74s b1010 : br_step = 1, rise_time = (4.37*32*A/11)ms; If FADEH =	0

			255, FADEL = 0, then rise_time = 3.24s b1011 : br_step = 1, rise_time = (4.37*A*4)ms; If FADEH = 255, FADEL = 0, then rise_time = 4.46s b1100 : br_step = 1, rise_time = (4.37*64*A/13)ms; If FADEH = 255, FADEL = 0, then rise_time = 5.49s b1101 : br_step = 1, rise_time = (4.37*64*A/11)ms; If FADEH = 255, FADEL = 0, then rise_time = 6.49s b1110 : br_step = 1, rise_time = (4.37*64*A/9)ms; If FADEH = 255, FADEL = 0, then rise_time = 7.93s b1111 : br_step = 1, rise_time = (4.37*A*8)ms; If FADEH = 255, FADEL = 0, then rise_time = 8.91s	
3:0	T1	RW	ABM hold on time b0000 : on_time = 0.05s b0001 : on_time = 0.14s b0010 : on_time = 0.28s b0011 : on_time = 0.42s b0100 : on_time = 0.56s b0101 : on_time = 0.84s b0110 : on_time = 1.12s b0111 : on_time = 1.68s b1000 : on_time = 2.24s b1001 : on_time = 2.80s b1010 : on_time = 3.36s b1011 : on_time = 4.48s b1100 : on_time = 5.6s b1101 : on_time = 6.72s b1110 : on_time = 7.84s b1111 : on_time = 8.95s	0

PATT1: (Address 66h)

Bit	Symbol	R/W	Description	Default
7:4	T2	RW	ABM and MBM ramp fall time. The step from FADEL to FADEH is br_step and the change time is fall_time, A = FADEH - FADEL b0000 : br_step = A, fall_time = 0ms; If FADEH = 255, FADEL = 0, then fall_time = 0s b0001 : br_step = 8, fall_time = (4.37*A/8)ms; If FADEH = 255, FADEL = 0, then fall_time = 0.14s b0010 : br_step = 4, fall_time = (4.37*A/4)ms; If FADEH = 255, FADEL = 0, then fall_time = 0.28s b0011 : br_step = 2, fall_time = (4.37*64*A/171)ms ; If FADEH = 255, FADEL = 0, then fall_time = 0.42s b0100 : br_step = 2, fall_time = (4.37*A/2)ms; If FADEH = 255, FADEL = 0, then fall_time = 0.56s b0101 : br_step = 1, fall_time = (4.37*32*A/43)ms; If FADEH = 255, FADEL = 0, then fall_time = 0.83s b0110 : br_step = 1, fall_time = (4.37*A)ms; If FADEH = 255, FADEL = 0, then fall_time = 1.11s	0

			b0111 : br_step = 1, fall_time = (4.37*64*A/43)ms; If FADEH = 255, FADEL = 0, then fall_time = 1.66s b1000 : br_step = 1, fall_time = (4.37*2*A)ms; If FADEH = 255, FADEL = 0, then fall_time = 2.23s b1001 : br_step = 1, fall_time = (4.37*32*A/13)ms; If FADEH = 255, FADEL = 0, then fall_time = 2.74s b1010 : br_step = 1, fall_time = (4.37*32*A/11)ms; If FADEH = 255, FADEL = 0, then fall_time = 3.24s b1011 : br_step = 1, fall_time = (4.37*A*4)ms; If FADEH = 255, FADEL = 0, then fall_time = 4.46s b1100 : br_step = 1, fall_time = (4.37*64*A/13)ms; If FADEH = 255, FADEL = 0, then fall_time = 5.49s b1101 : br_step = 1, fall_time = (4.37*64*A/11)ms; If FADEH = 255, FADEL = 0, then fall_time = 6.49s b1110 : br_step = 1, fall_time = (4.37*64*A/9)ms; If FADEH = 255, FADEL = 0, then fall_time = 7.93s b1111 : br_step = 1, fall_time = (4.37*A*8)ms; If FADEH = 255, FADEL = 0, then fall_time = 8.91s	
3:0	T3	RW	ABM ramp off time b0000 : off_time = 0.05s b0001 : off_time = 0.14s b0010 : off_time = 0.28s b0011 : off_time = 0.42s b0100 : off_time = 0.56s b0101 : off_time = 0.84s b0110 : off_time = 1.12s b0111 : off_time = 1.68s b1000 : off_time = 2.24s b1001 : off_time = 2.80s b1010 : off_time = 3.36s b1011 : off_time = 4.48s b1100 : off_time = 5.6s b1101 : off_time = 6.72s b1110 : off_time = 7.84s b1111 : off_time = 8.95s	0

PATT2: (Address 67h)

Bit	Symbol	R/W	Description	Default
7:6	LE	RW	End point of ABM loop pattern b00 : Pattern finally stop at OFF state b01-b11: Pattern finally stop at ON state	0
5:4	LB	RW	Start point of ABM loop pattern b00 : Start from RISE b01 : Start from ON b10 : Start from FALL b11 : Start from OFF	0
3:0	RPT_H	RW	4 MSB of ABM loop times	0

PATT3: (Address 68h)

Bit	Symbol	R/W	Description	Default
7:0	RPT_L	RW	8 LSB of ABM loop times Note: when RPT_H = 0 and RPT_L = 0, the pattern will run	0

			forever. In this case, you can switch ABM to MBM and then turn the pattern off.	

FADEH_CFG: (Address 69h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	FADEH	RW	Maximum brightness configure of ABM.	0

FADEL_CFG: (Address 6Ah)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	FADEL	RW	Minimum brightness configure of ABM.	0

GCFG: (Address 6Bh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	LED7_PAT_EN	RW	LED7 pattern group enable. If LED7_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
6	LED6_PAT_EN	RW	LED6 pattern group enable. If LED6_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
5	LED5_PAT_EN	RW	LED5 pattern group enable. If LED5_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
4	LED4_PAT_EN	RW	LED4 pattern group enable. If LED4_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
3	LED3_PAT_EN	RW	LED3 pattern group enable. If LED3_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
2	LED2_PAT_EN	RW	LED2 pattern group enable. If LED2_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
1	LED1_PAT_EN	RW	LED1 pattern group enable. If LED1_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0
0	LED0_PAT_EN	RW	LED0 pattern group enable. If LED0_BANK_EN = 0, the register is valid 0 : Disable 1 : Enable	0

OTCR: (Address 6Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:3	Reserved	RO	Not used	0
2	OTST	RO	Over temperature status, read only 0 : None over temperature 1 : Over temperature	0
1	OTSDDIS	RW	Thermal shutdown disable. If the register is enbale, when Over temperature event occurs, device will enter thermal shutdown mode. On the contrary, when Over temperature event occurs, device will not enter thermal shutdown mode 0 : Enable 1 : Disable	0
0	OTDIS	RW	Over temperature detect disable 0 : Enable 1 : Disable	0

STAT: (Address 6Dh)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RO	Not used	0
1	OSC_OK	RO	Oscillator stability flag, read only	0
0	PUST	RO	The event flag of power-on or EN pin pulled from low to high occur, will be cleared after reading out 0 : no occur 1 : occur	0

CHIP_ID: (Address 6Eh)

Bit	Symbol	R/W	Description	Default
7:0	CHIPID	RO	The CHIPID number. AW26024EQNR	0xB0
7:0	CHIPID	RO	The CHIPID number. AW26018EQNR	0xB1

I^2C_BROADCAST_DIS_CFG: (Address 70h)

Bit	Symbol	R/W	Description	Default
7:0	I^2C_BROADCAST_DIS	RW	I^2C broadcast device address disable. The register will be set to "1" only when firstly 0x55 is written and secondly 0x66 is written, otherwise the register will be set to "0" 0 : Enable 1 : Disable	0x0

I^2C_TIMEOUT_EN_CFG: (Address 71h)

Bit	Symbol	R/W	Description	Default
7:0	I^2C_TIMEOUT_EN	RW	I^2C abnormal timeout resolution enable. The register will be set to "1" only when firstly 0x77 is written and secondly 0x88 is written, otherwise the register will be set to "0". If the register is enable, SDA abnormal pull down for 25ms, automatically released 0 : Disable 1 : Enable	0x0

Application Information

R_{EXT}

The maximum output current of OUTx is set by external resistor R_{EXT} and can be expressed by the following formula:

$$I_{MAX} = K \times \frac{V_{ISET}}{R_{ISET}} \times \frac{GCC + 1}{32}$$

Where V_{ISET}=0.7V, K=105;

To set the LED current to 15mA, R_{EXT} should be set to 4.9kΩ, and the bit MAX_CUR_OPTION of register DEVICE_CFG1 (address: 0x01.bit 1) should be set to 0 or 1.

To set the LED current to 30mA, R_{EXT} should be 2.45kΩ, and the bit MAX_CUR_OPTION of register DEVICE_CFG1 (address: 0x01.bit 1) should be set to 1.

R_R, R_G, R_B

The resistance(R_X) used for thermal reduction can be calculated according to the following formula:

$$R_X = \frac{VLED - VF_x - V_{DROPOUT}}{I_{MAX}}$$

VLED: LED power supply voltage.

VF_X: LED forward voltage.

$V_{DROPOUT}$: Voltage on LEDx, recommended values is 0.5V.

I_{MAX}: Maximum output current.

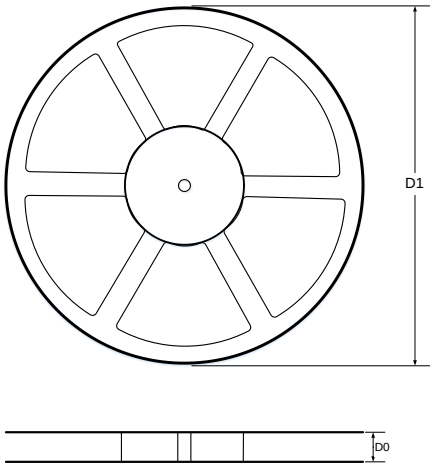
PCB Layout Consideration

AW26024E/AW26018E is a 24/18-channel LEDs driver programmed via I²C compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

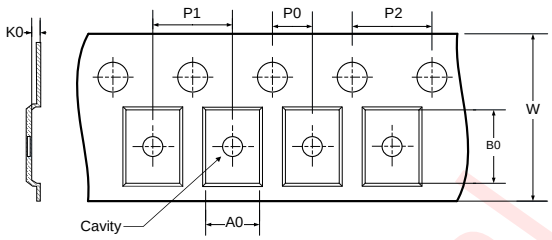
1. The C_1, C_2, C_{LED} should be placed as close to the chip as possible.
2. The C_{LDO} should be placed as close to the PIN 32 as possible.
3. The R_{EXT} should be placed as close to the PIN 31 as possible.
4. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

Tape And Reel Information

REEL DIMENSIONS

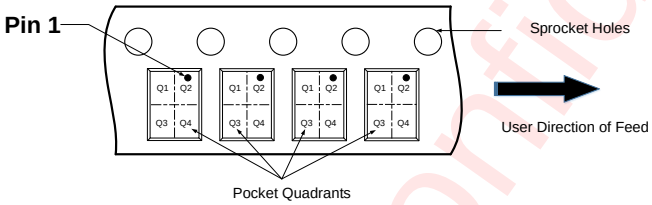


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

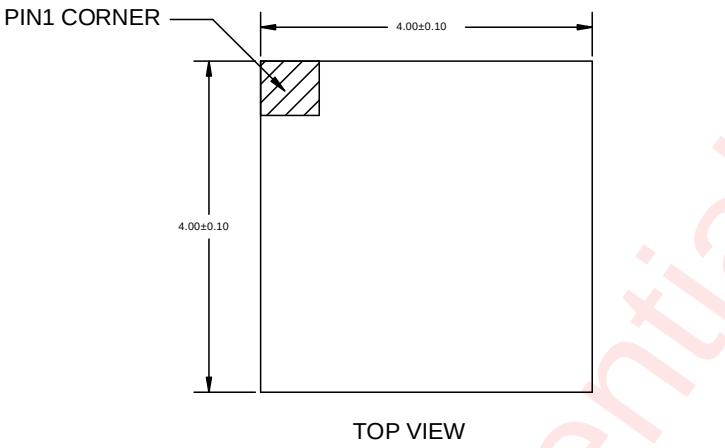


DIMENSIONS AND PIN1 ORIENTATION

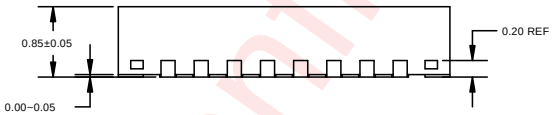
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q2

All dimensions are nominal

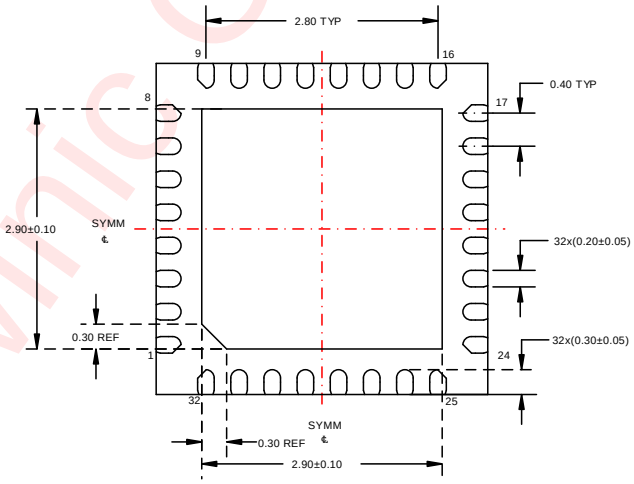
Package Description



TOP VIEW



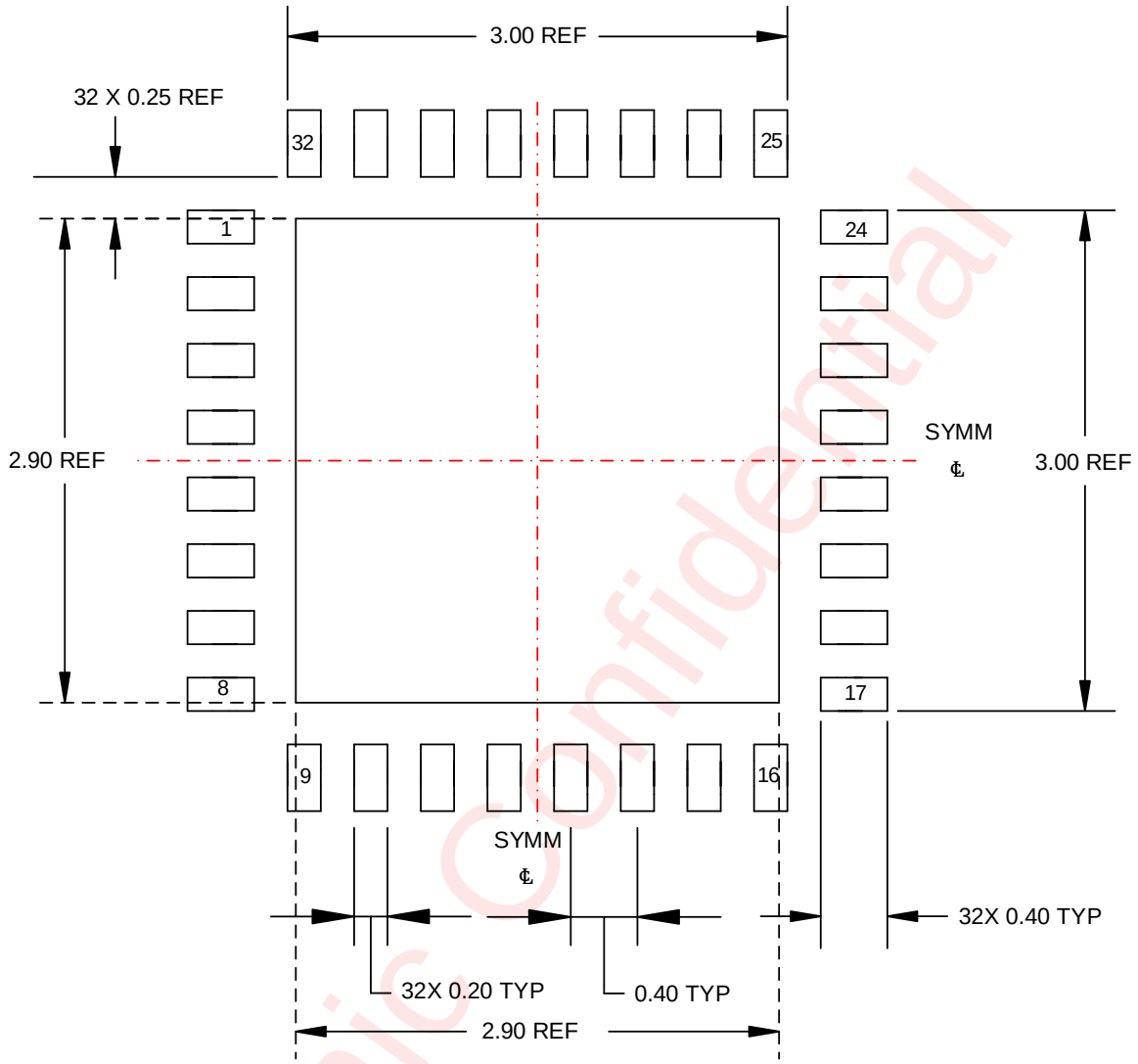
SIDE VIEW

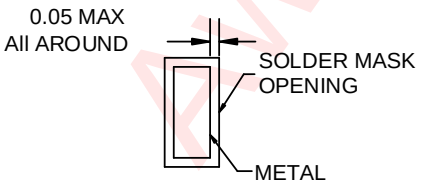


BOTTOM VIEW

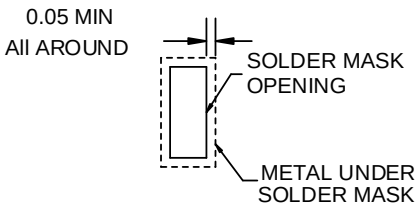
Unit：mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2025	Officially released

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