18×4 MATRIX LED DRIVER

Features

- Power Supply Voltage Range: 2.7V to 5.5V
- Operating Temperature Range: -40°C to 105°C
- Logic pins compatible with EN_VIO: 1.2V~5.5V
- LED matrix topology with high precision:
  - 18 constant current sinks with 4 scan switches for 72 LEDs
  - Configurable for 1 to 4 scan switches
  - Device-to-device error: ±4%
  - Channel-to-channel error: ±4%
- Ultra-low power consumption:
  - Shutdown mode: I_{CC}≤ 1μA when EN_VIO = Low
  - Standby mode: I_{CC} ≤ 2μA when EN_VIO = High and CHIP_EN = 0 (data retained)
  - Active mode: I_{CC} = 2.4mA (typ.) when channel current = 51mA
- Analog Dimming:
  - Global 8-bit current setting for all LED dots
  - Individual 8-Bit Current setting for each Current Sink
- Each LED dot features 12-Bit PWM Control Resolution
- Integrated Open/Short Detection
- De-ghosting
- EMI Reduction:
  - Spread spectrum
  - CS-Group delay
  - Slew-Rate adjustment
- Interface selection:
  - when IFS is low, 1MHz(max) I^2C
  - when IFS is high：
    - EN_VIO ≥ 3.6V, 20MHz(max) SPI
    - EN_VIO ≥ 1.8V, 12MHz(max) SPI
- Package: QFN 4X4-32L package

General Description

AW25072S is a universal high-performance LED driver IC designed to drive up to an 18×4 LED matrix.

The device integrates both analog dimming and PWM dimming control modes. For analog dimming, each current sink can be adjusted with 256 steps. For PWM dimming, each LED can be adjusted with 4096 steps.

The device supports Auto-Breath-Pattern and has a flexible and efficient lighting effect programming function, which can reduce the resource occupation of the main controller.

The device supports advanced EMI reduction techniques such as programmable analog CS slew rate adjustment, CS-Group delay and spread spectrum clock modulation. It also includes features like independent open/short detection, de-ghosting, over-temperature protection (OTP), and thermal roll-off for robust system operation.

The device has two communication interfaces: 1 MHz I^2C and 20 MHz SPI, enabling flexible system integration. It comes in a QFN 4X4-32L package and operates at 2.7V to 5.5V between -40°C and +105°C.

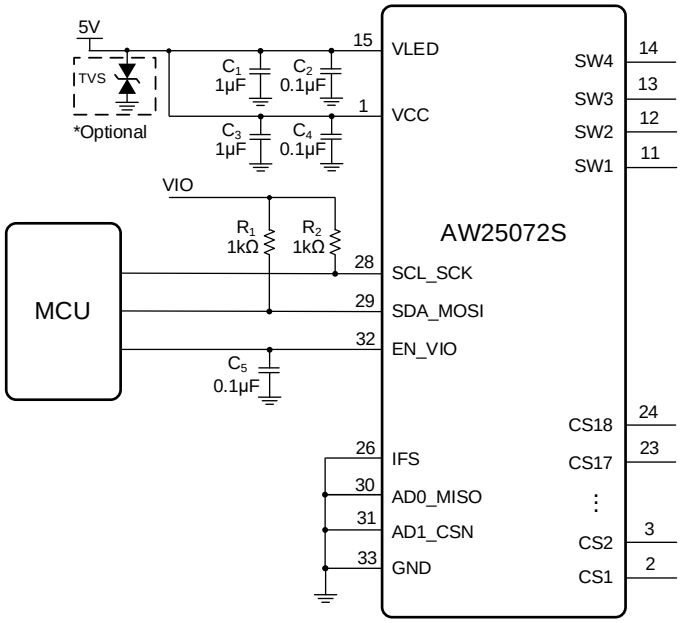
Applications

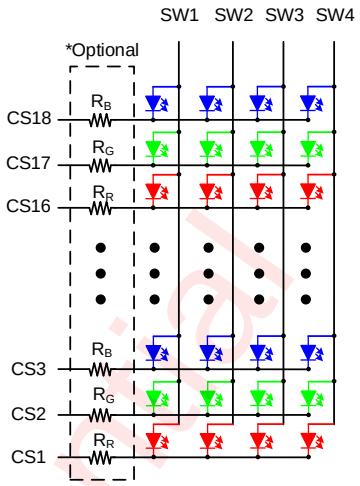
Smart speaker, Bluetooth speaker

Gaming device (Keyboard, Mouse etc.)

Mobile phone, PAD

Typical Application Circuit

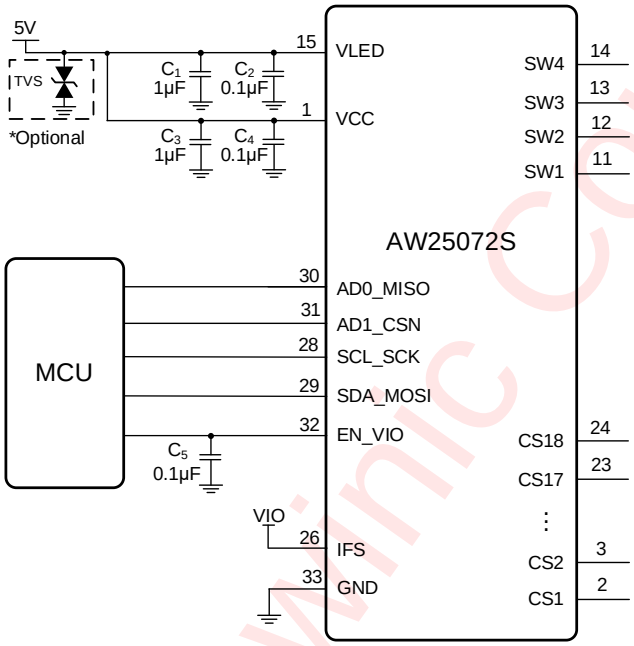


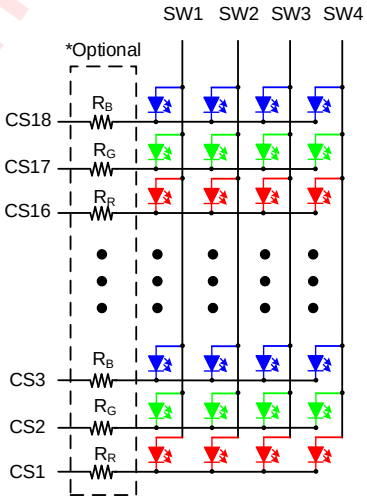


Note1: The resistance R_{LED} is determined by PVCC, VF of LED, ILED, VHR of CSx and SWx. R_{LED}=(VLED-VF-VHR_{CS}-VHR_{SW})/I_{MAX}.

Note2: EN_VIO pin need to be connected to MCU or VIO.

Figure 1 Application Circuit through I²C interface





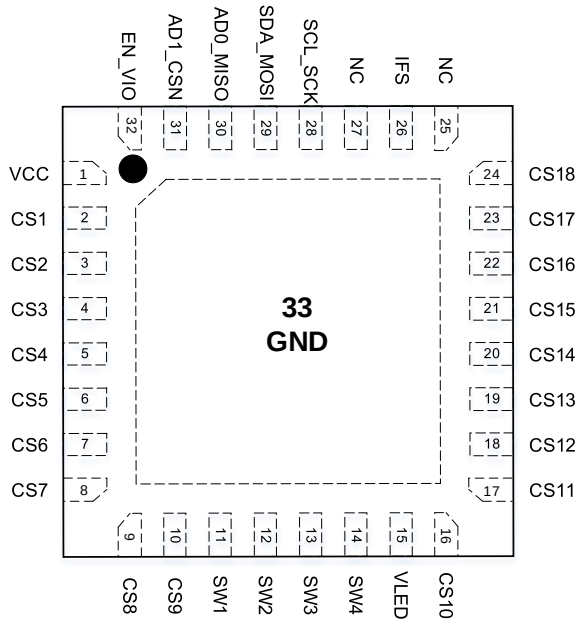
Note1: The resistance R_{LED} is determined by PVCC, VF of LED, ILED, VHR of CSx and SWx. R_{LED}=(VLED-VF-VHR_{CS}-VHR_{SW})/I_{MAX}.

Note2: EN_VIO pin need to be connected to MCU or VIO.

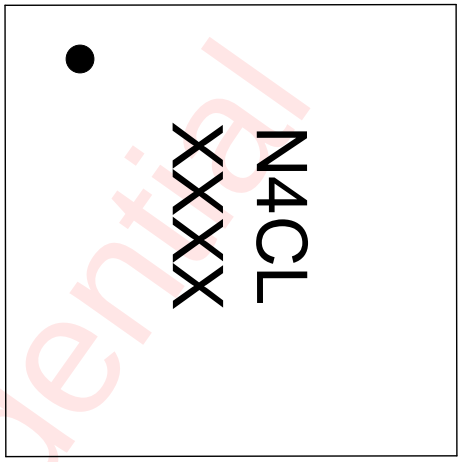
Figure 2 Application Circuit through SPI interface

Pin Configuration And Top Mark

AW25072SQNR
(Top View)



AW25072SQNR
(Top View)



N4CL – AW25072SQNR
XXXX – Production Tracing Code

Figure 3 Pin Configuration and Top Marking

Pin Definition

No.	NAME	DESCRIPTION
1	VCC	Power supply, 2.7V~5.5V. A 1-μF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
2~10	CS1~9	Current sinks, if not used, this pin must be left floating.
11~14	SW1~4	Current switches, if not used, this pin must be left floating.
15	VLED	Current source power supply, 2.7V~5.5V.
16~24	CS10~18	Current sinks, if not used, this pin must be left floating.
25	NC	No connection.
26	IFS	Communication interface select pin. I^2C is selected when IFS is low. SPI is selected when IFS is high. No floating.
27	NC	No connection.
28	SCL_SCK	I^2C clock input or SPI clock input. Pull up to VIO when configured as I^2C.
29	SDA_MOSI	I^2C data IO or SPI master output slave input. Pull up to VIO when configured as I^2C.
30	AD0_MISO	I^2C address select pin 0 or SPI master input slave output.
31	AD1_CSN	I^2C address select pin1 or SPI slave select.
32	EN_VIO	Standby the chip when EN_VIO is low, should be connected to MCU or VIO.
33	GND	Ground.

Functional Block Diagram

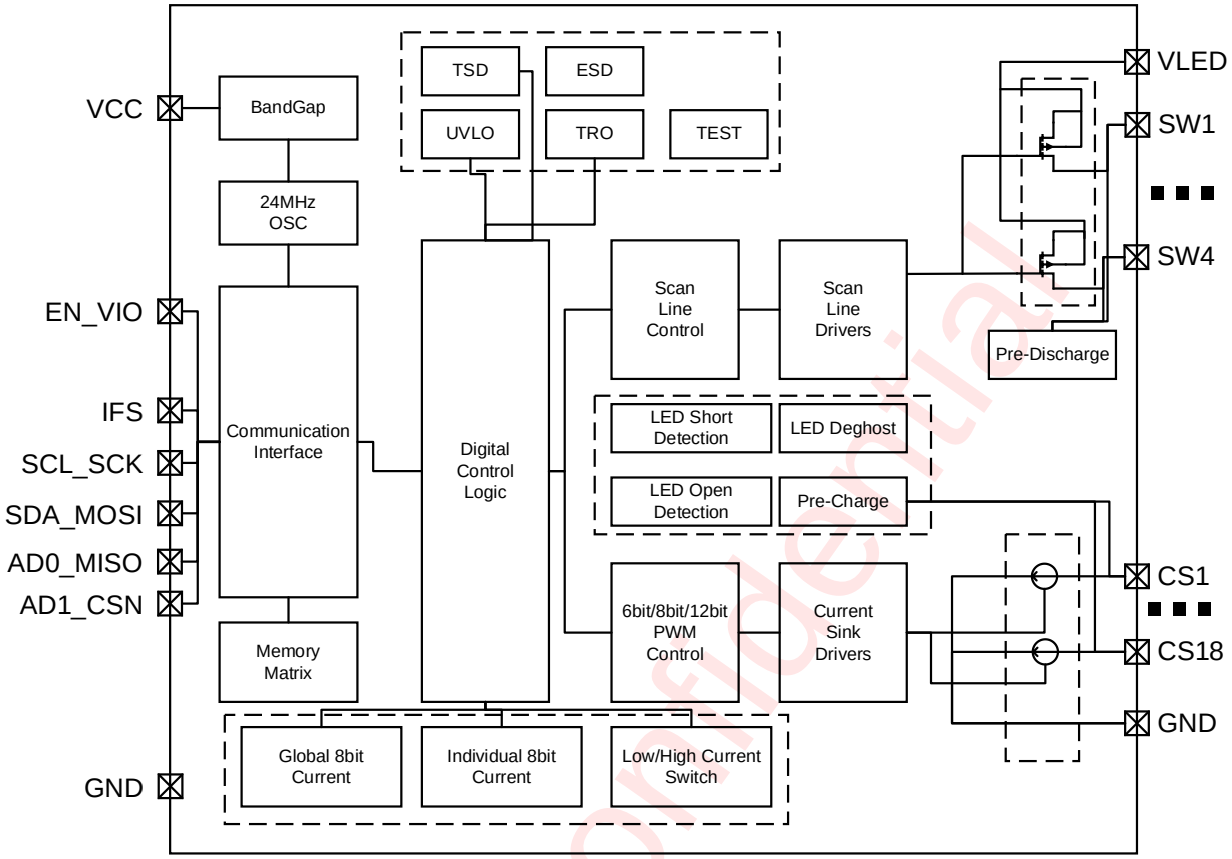


Figure 4 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW25072SQNR	-40℃～105℃	QFN 4X4-32L	N4CL	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC, VLED		-0.3V to 6V
Input voltage range	IFS, SCL_SCK, SDA_MOSI, AD0_MISO, AD1_CSN, EN_VIO	-0.3V to VCC
Junction-to-ambient thermal resistance θ_{JA}		30.71°C/W
Maximum operating junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (Including CDM HBM)(NOTE 2)		
HBM		±4kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM test method: ESDA/JEDEC JS-001-2023*, CDM test method:* ESDA/JEDEC JS -002-2022

Electrical Characteristics

Typical values apply for VCC=3.6V VLED=5V TA=25℃.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltages and Currents						
VIN	VIN supply voltage range		2.7		5.5	V
V_{UVLO}	Under-voltage lockout threshold	VIN rising		2.5		V
		VIN falling		2.3		V
I_Q	Quiescent current	LEDx ON，PWM=1，VCC Current		2.4		mA
I_{SD1}	Shutdown down current	EN_VIO =0V		0.2	1	μA
I_{SD2}	Shutdown down current	EN_VIO =1.2V		1	1.5	μA
I_{out}	Output current of CSy	GCC=0XFF, SL=0XFF		51		mA
$\triangle I_{MAT}$	Between channels	LED_IME=0, LED_CAIE=1, I_{out}=51mA, GCC=0xFF, SL=0xFF	-4		4	%
$\triangle I_{ACC}$	Between device to device	LED_IME=0, LED_CAIE=1, I_{out}=51mA, GCC=0xFF, SL=0xFF	-4		4	%
$\triangle I_{MAT}$	Between channels	LED_IME=0, LED_CAIE=1, IREF_LCAIE=1, I_{out}=24mA, GCC=0x78, SL=0xFF	-3		3	%
$\triangle I_{ACC}$	Between device to device	LED_IME=0, LED_CAIE=1, IREF_LCAIE=1, I_{out}=24mA, GCC=0x78, SL=0xFF	-3		3	%
$\triangle I_{MAT}$	Between channels	LED_IME=1, LED_CAIE=1, IREF_LCAIE=1, I_{out}=6mA, GCC=0X78, SL=0XFF	-3		3	%
$\triangle I_{ACC}$	Between device to device	LED_IME=1, LED_CAIE=1, IREF_LCAIE=1, I_{out}=6mA, GCC=0X78, SL=0XFF	-3		3	%
V_{HR}	Current switch headroom voltage SWx	Isw=918mA,		350		mV
	Current switch headroom voltage SWx	Isw=450mA,		200		mV
	Current sink headroom voltage CSy	LED_IME=0, LED_CAIE=1, Ics=51mA		250	350	mV
	Current sink headroom voltage CSy	LED_IME=0, LED_CAIE=1, IREF_LCAIE=1, Ics=24mA		200		mV
	Current sink headroom voltage CSy	LED_IME=1, LED_CAIE=1, IREF_LCAIE=1, Ics=6mA		200		mV
V_{OD}	LED open detect threshold	VCC=5V, I_{out}>1mA, PWM>6% measured at CSy		0.1		mV
V_{SD}	LED short detect threshold	VCC=5V, I_{out}>1mA, PWM>6% measured at VLED-V_{SWx}		1.4		mV
T_{SD}	Over temperature protection threshold			150		℃
T_{SD_HY}	Over temperature protection hysteresis			20		℃

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
F_{OSC}	OSC frequency		23.04	24	24.96	MHz
LOGIC EN_VIO						
V_{IH}	High level input voltage	VCC=2.5V to 5.0V	1.08			V
V_{IL}	Low level input voltage				0.36	V
I_{IL}	Logic "0" input Current	V_{input}=0V		5		nA
I_{IH}	Logic "1" input Current	V_{input}=VCC		5		nA
LOGIC SDA, SCL,AD0,AD1,IFS						
V_{IH}	High level input voltage	VCC=2.5V to 5.0V	0.7* V_{EN_VIO}			V
V_{IL}	Low level input voltage				0.3* V_{EN_VIO}	V
VOH	Low level output voltage, MISO(AD0)	$I_{pull-up}$=3mA	0.7* V_{EN_VIO}			V
VOL	Low level output voltage, SDA, MISO(AD0)	$I_{pull-up}$=3mA			0.4	V
I_{IL}	Logic "0" input Current	V_{input}=0V		5		nA
I_{IH}	Logic "1" input Current	V_{input}=VCC		5		nA

I²C INTERFACE TIMING REQUIREMENTS

Parameter		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

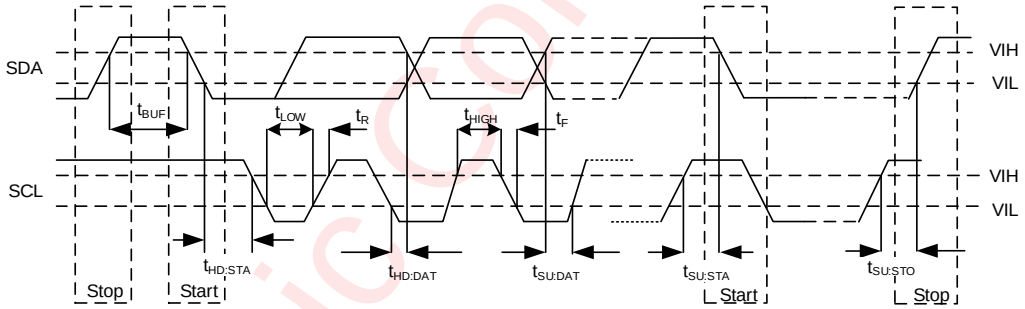


Figure 5 I²C Interface Timing

SPI INTERFACE TIMING REQUIREMENTS

Parameter		Min.	Typ.	Max.	Unit
F_{SCK}	Interface clock frequency	-	-	20	MHz
T_{CSAS}	CS active setup time	30			ns
T_{CSNS}	CS not active setup time	15			ns
T_{CSNH}	CS not active hold time	30			ns
T_{CH}	SCK high time	25			ns
T_{CL}	SCK low time	25			ns
T_{DS}	Data in setup time	20			ns
T_{DH}	Data in hold time	15			ns
T_{DO}	SCK falling edge to MISO data update time			30	ns

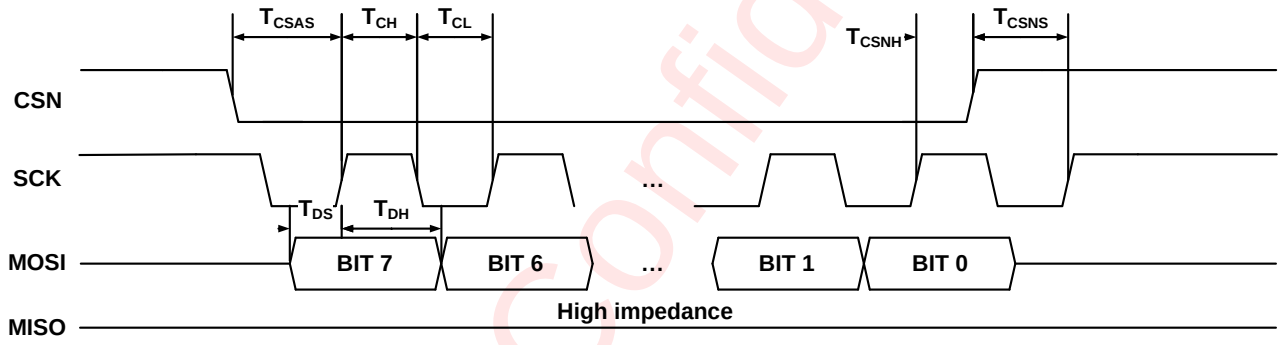


Figure 6 SPI Interface Input Timing

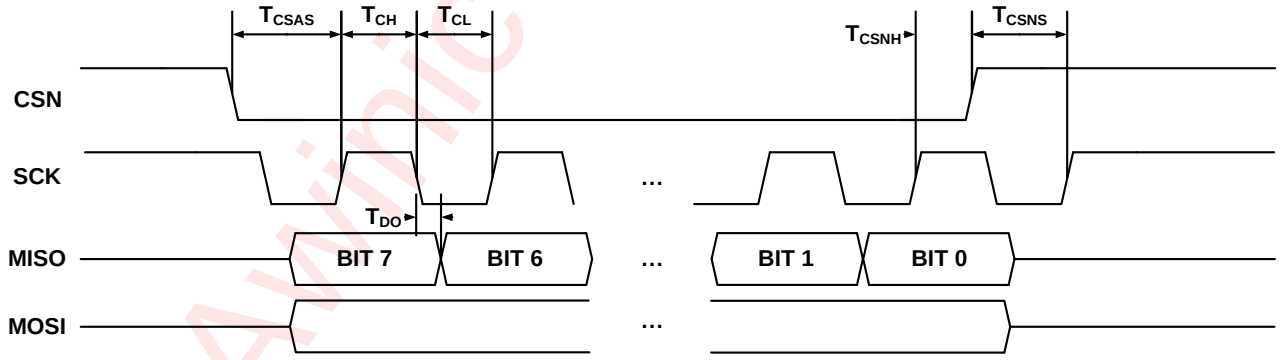


Figure 7 SPI Interface Output Timing

Detailed Functional Description

Overview

The device incorporates a 4-channel switching FET array and 18-channel constant current sink modules. Utilizing a time-multiplexed dynamic scan matrix architecture, a single IC can drive up to 72 monochromatic LED nodes or 24 RGB tricolor pixel units. Device startup timing is showed below.

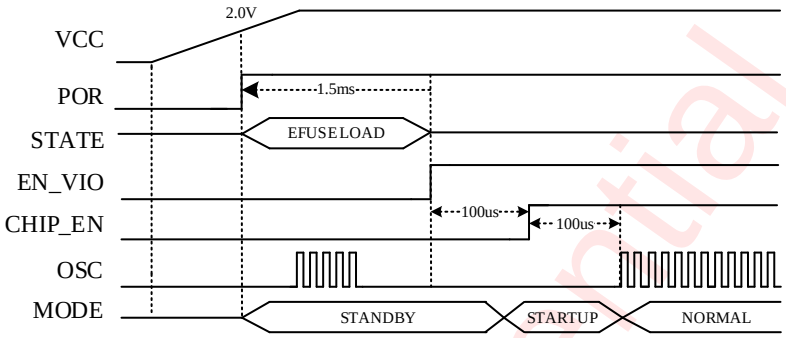


Figure 8 Startup Timing

Dimming

Analog Dimming

Analog dimming of chip is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 8-bits Global Current Control(GCC) without external resistor
- Individual 8-bit CS Current (SL_CSx) setting
- Output current reduce to 1/4 maximum value enable(LED_IME)

When LED_IME is 0, $I_{OUT(PEAK)}$ follow the formula below:

$$I_{OUT(PEAK)} = 51mA * \frac{GCC}{255} * \frac{SL}{255}$$

When LED_IME is 1, $I_{OUT(PEAK)}$ follow the formula below:

$$I_{OUT(PEAK)} = 12.75mA * \frac{GCC}{255} * \frac{SL}{255}$$

For applications of $I_{OUT(PEAK)}$=0mA~12.75mA, LED_IME in register CONFIG(00h) should be set to 1, LED_CAIE and IREF_LCAIE in register MISC_CFG2(DCh) should be set to 1.

For applications of $I_{OUT(PEAK)}$=12.75mA~24mA, LED_IME in register CONFIG(00h) should be set to 0, LED_CAIE and IREF_LCAIE in register MISC_CFG2(DCh) should be set to 1.

For applications of $I_{OUT(PEAK)}$=24mA~51mA, LED_IME in register CONFIG(00h) should be set to 0, LED_CAIE in register MISC_CFG2(DCh) should be set to 1 and IREF_LCAIE in register MISC_CFG2(DCh) should be set to 0.

PWM Dimming

A complete scan cycle can be divided into four parts: DGST (De-ghosting Time), SETUP (Setup Time), PWMGEN (PWM Generation Time), and HOLD (Hold Time).

a) Single Scan Sequence Timing

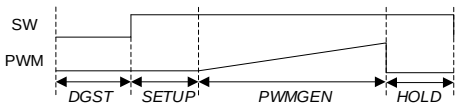


Figure 9 Single Scan Sequence Timing

DGST: During this phase, if the De-ghosting switch is enabled, the pull-down resistor of the SW (switch) and the pull-up resistor on the CS are activated.

SETUP: This is the setup time for the SW (switch).

PWMGEN: The period during which the PWM signal is generated.

HOLD: The time from when the PWM signal resets to zero until the SW transitions to a low level.

To minimize audible noise, the durations of DGST, SETUP, and HOLD can be configured via the registers PHASE_CFG1(1Bh) and PHASE_CFG2(1Ch).

b) Scan Timing of the SW (Switch) Cycle

To reduce audible noise, LEDs 1 to 18 are sequentially divided into 3 groups, with a delay 42ns between groups. This delay enable is configurable via registers PHASE_CFG3(1Dh). The overall timing sequence is illustrated in the diagram below.

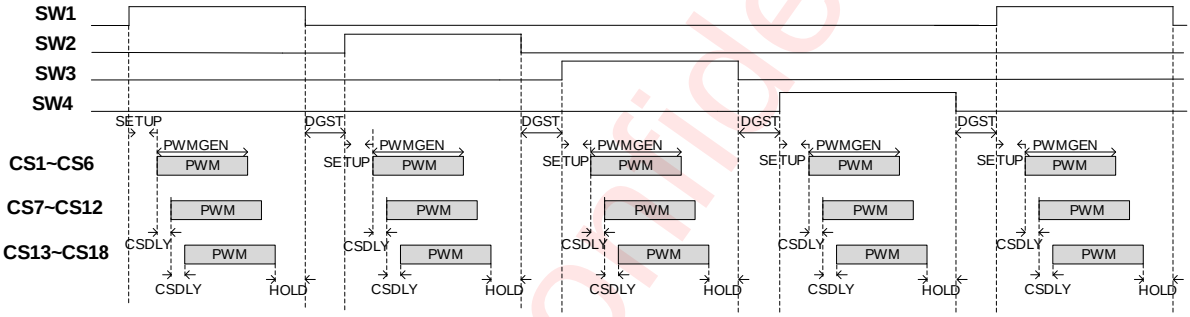


Figure 10 overall timing sequence

Table 1 PWM Timing

symbol	description	duration
T_{DGST}	Duration from SW being pulled low to next SW being pulled high	(DEGHOST_TIME+1)*pwm_clk_time
T_{SETUP}	Duration from SW being pulled high to the start of the CS cycle	(SETUP_TIME+1)*pwm_clk_time
T_{HOLD}	Duration from completion of the last CS group counting cycle to SW being pulled low	(HOLD_TIME)*pwm_clk_time
T_{CSDLY}	Every cs group delay time	42ns

- Every 6 CS signals form a group, with the 18 CS channels divided into 3 groups. The first and last groups have a group delay duration of $2\times T_{CSDLY}$.
- The number of SW instances can be configured via the register CONFIG (00h).
- Pwm_clk_time represents the duration of one full cycle of the pwm_clk signal. Pwm_clk is a clock signal derived from the system clock after being divided down by the PWM_CLK_DIV (PWM_CLK_CFG, 1Eh).

Table 2 PWM Clock period

PWM_CLK_DIV	0	1	2	3	4	5	6	7
Pwm_clk	24MHz	12MHz	6MHz	3MHz	1.5MHz	750kHz	375kHz	187.5kHz

Pwm_clk_time(ns)	41.7	83.3	166.7	333.3	666.7	1333.3	2666.7	5333.3

The formula for calculating the average current of each led throughout the entire scanning cycle is as follows:

$$I_{LED\ (AVG)} = I_{OUT(PEAK)} \times DUTY$$

DUTY is the current duty cycle at the CS end.

$$\text{Duty} = \frac{PWM \times \text{Pwm\_clk\_time}}{T_{DGST} + T_{SETUP} + (2^n \times \text{Pwm\_clk\_time}) + xT_{CSDLY} + T_{HOLD}} \times \frac{1}{N}$$

PWM is the value written into the PWM register. The value of n in $2^n \times \text{Pwm\_clk\_time}$ is determined by the set PWM dimming precision and can be configured as 6/8/12 through PWM_MODE(CONFIG, 00h). Whether Dither is enabled or not does not affect the value of n here. The value of x in xT_{CSDLY} is determined by whether the group delay (PHASE_CFG3, 1Dh) is enabled. When it is not enabled, x = 0; when it is enabled, x = 2, and T_{CSDLY} = 42 ns. In $\frac{1}{N}$, N represents the number of enabled SWs.

PWM Display Data Mapped in Memory

In different PWM modes, the storage addresses of PWM data in the output ports are different.

PWM outputs 8-bit data, with each output occupying 1 addresses.

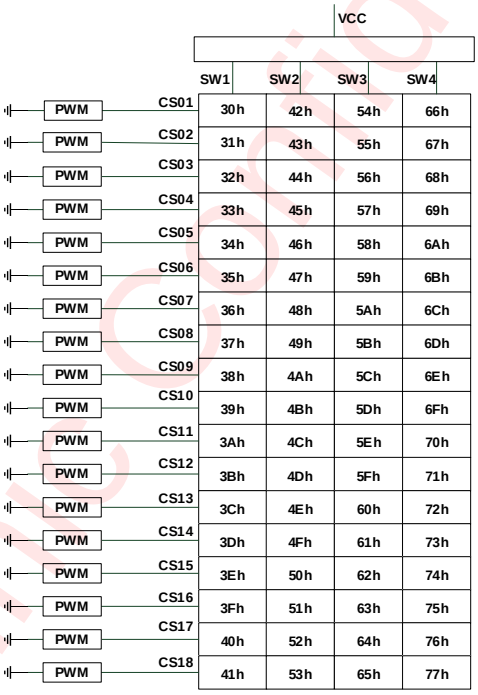


Figure 11 8-bit PWM data storage addresses

PWM outputs 12-bit data, with each output occupying 2 addresses: the lower address stores the low 8 bits, and the higher address stores the high 4 bits.

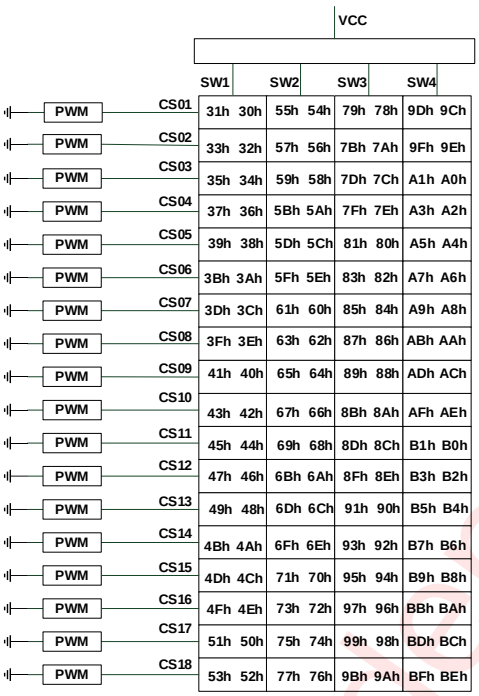


Figure 12 12-bit PWM data storage addresses

LED Matrix Display Timing

Dither Function

Dither is a technique that enhances effective resolution by making small, periodic adjustments to the PWM duty cycle in units of LSBs. In PWM control, the Dither function, through different bit configurations of dither, can achieve higher-precision output with limited hardware resolution. The following is a comparison of different bit dither:

Table 3 Comparison of Dither at Different Bits

Number of dither bits (N)	Equivalent period number (2^N)	Average step length (LSB/2^N)	Maximum resolution gain
2	4	±1/4 LSB	2
4	16	±1/16 LSB	4
6	64	±1/64 LSB	6

PWM FREQUENCY

PWM frequency is configured by bits PWM_CLK_DIV[2:0] of register PWM_CLK_CFG (1Eh). The system clock operates at 24MHz. The specific configurations are as follows:

Table 4 PWM frequency

PWM_CLK_DIV	0	1	2	3	4	5	6	7
pwmclk	24MHz	12MHz	6MHz	3MHz	1.5MHz	750kHz	375kHz	187.5kHz
Carrier frequency /kHz								

6bit+2/6dither	375	187.5	93.75	46.875	23.4375	11.7187	5.8593	2.9296
8bit/8bit+4dither	93.75	46.875	23.437	11.7185	5.8592	2.9296	1.4648	0.7324
12bit	5.85	2.9296	1.4648	0.7324	0.3662	0.1831	0.09155	0.04577

De-ghosting

To prevent the LED ghost effect, the device has integrated pull-down resistors for each SWx(x=1~4) and pull up resistor for each CSx(x=1~18). Mode selection can be configured via the DEGHOST_CFG1 (24h) register.

Table 5 De-ghosting function

Bit	Symbol	Description
1	CS_PULLUP_MODE	0: CS Pull-up only in non-overlap time. 1: CS pull-up in all the time.
0	SW_PULLDOWN_MODE	0: SW Pull-down only in non-overlap time. 1: SW pull-down in all the time.

ON-OFF Mode

The device allows individual on/off control of each LED by writing 1-bit data to the ABM_SWx_CSy registers (x = 1, 2, … ,4) (y = 1, 2, … ,18). Users can configure ONOFF_MODE_EN(1Ah) to enable the ON-OFF mode. When ONOFF_VALUE_SEL(1Ah) is 0, the maximum brightness of each LED dot is determined by ABM_MAX_VALUE (15h); otherwise, the maximum brightness of each LED is determined by PWMx (x=1,2..., 144) Register.

Matrix-On Mode

This device supports a test mode that can quickly detect LED damage. Users can enable all LEDs by configuring the MATRIX_ON_EN(DBh) register, provided that CHIP_EN, GCC, and SLx (x=1,2..., 18) have been pre-configured.

Auto-Breath-Pattern

There is a auto-breath-pattern controller (ABM) in the device. Each LED dot can be configured into ABM by ABM_SWx_CSy register(x = 1, … ,4) (y = 1, … ,18). ABMCFG1~ABMCFG7 (14h~1Ah) are configure registers. When bit ABM_EN in register ABMCFG7 is set to “1”, ABM controller is enabled; when bit ABM_GO in register ABMCFG7 is set to “1”, ABM controller is worked. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode.

AUTONOMOUS BREATHING MODE

When ABM_MODE(1Ah) is set to “1”, the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off-time respectively. Register ABM_MAX_VALUE(15h) and ABM_MIN_VALUE(14h) control the maximum and minimum brightness of the breathing respectively. When bit ABM_LOG_EN(1Ah) is set to “1”, the lighting effects switch to logarithmic mode. In the logarithmic mode, the lighting effect is smoother than the linear mode during T0 and T2, and causes the change in intensity to appear more linear to the human eye.

The actual time of 4 key periods is as follows:

$$Tx_{real} = \frac{\text{ABM\_MAX\_VALUE} - \text{ABM\_MIN\_VALUE}}{256} \times Tx \qquad (x = 0\ or\ 2)$$

$$Tx_{real} = Tx \qquad (x = 1\ or\ 3)$$

The parameter Tx_{real} is the actual time of 4 key periods, The parameter Tx is the register configuration time.

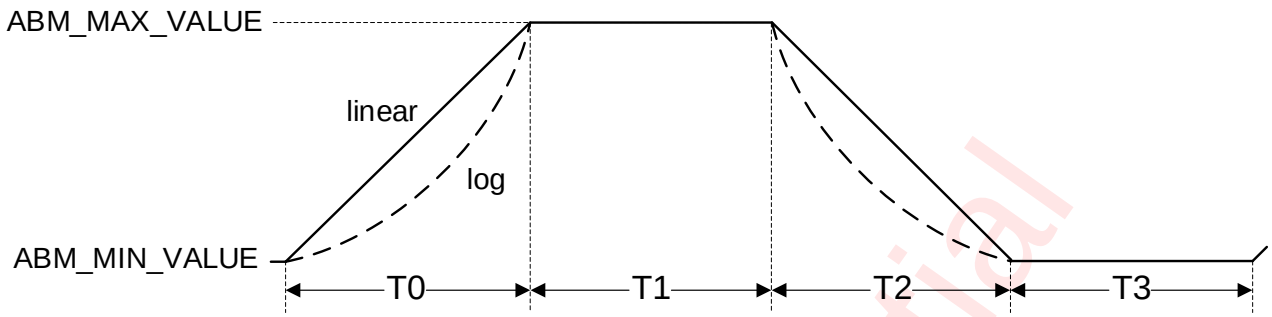


Figure 13 Autonomous Breathing Mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0\T1\T3, which is set by bits ABM_LOOP_START(18h) register. The end point of the loop can only be selected between the end of T0 and the end of T2, which is determined by ABM_LOOP_END(18h) register. The repeat times are determined by the end point defined. If bits ABM_LOOP_END(18h) are not "00", the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If bits ABM_LOOP_END(18h) are "00", the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times are decided by bits ABM_LOOP_TIMES(18h~19h) register. When setting ABM_LOOP_TIMES to "0", the breathing pattern will run unlimited times.

After the breathing pattern is over, the status bit ABM_OVER(D8h) will be set to "1". Once breathing loop start again or pattern controller switches to manual mode by setting ABM_MODE(1Ah) bit to "0", the ABM_OVER(D8h) will also be cleared.

When bit ABM_RUNNING(D8h) is set to "1", breathing pattern is started.

The full process of the autonomous breathing is as follows:

1. Set CHIP_EN,GCC, SL and ABM_MAX_VALUE/ABM_MIN_VALUE parameter.
2. Set C0h~CBh ABM_SWx_CSy register to select the pattern of LEDs.
3. Configure 16h~19h register to control the breath time, start/stop point, and repeat times.
4. Set ABM_EN=1 to enable breathing pattern mode.
5. Set ABM_MODE=1 to select auto breathing mode.
6. Set ABM_LOG_EN to select the breathing in log curve mode or linear mode.
7. Set ABM_GO=1 to start the breath pattern.

MANUAL-CONTROLLED MODE

If bit ABM_MODE is set to "0", manual control mode is selected. In manual control mode, user could set the bit ABM_MANUAL_SWITCH(1Ah) of register ABM_CFG7 to control the output of pattern controller. When ABM_MANUAL_SWITCH is "1", the output of pattern controller is decided by register ABM_MAX_VALUE(15h). When bit SWITCH is set to "0", the output is the decided by register ABM_MIN_VALUE(14h).

If bit ABM_RAMP_EN in register ABM_CFG7 is set to "1", the smooth ramp up/down will be enabled. At the same time, if ABM_MANUAL_SWITCH changes from "0" to "1", the output will be ramp up to ABM_MAX_VALUE smoothly. Similarly, if ABM_MANUAL_SWITCH changes from "1" to "0", the output of the pattern controller will ramp down to ABM_MIN_VALUE smoothly. It's also support the logarithmic mode ramp.

However, if ABM_RAMP_EN is set to "0", the output of the pattern controller will change to ABM_MANUAL_SWITCH or ABM_MIN_VALUE directly with no ramp as the ABM_MANUAL_SWITCH changes.

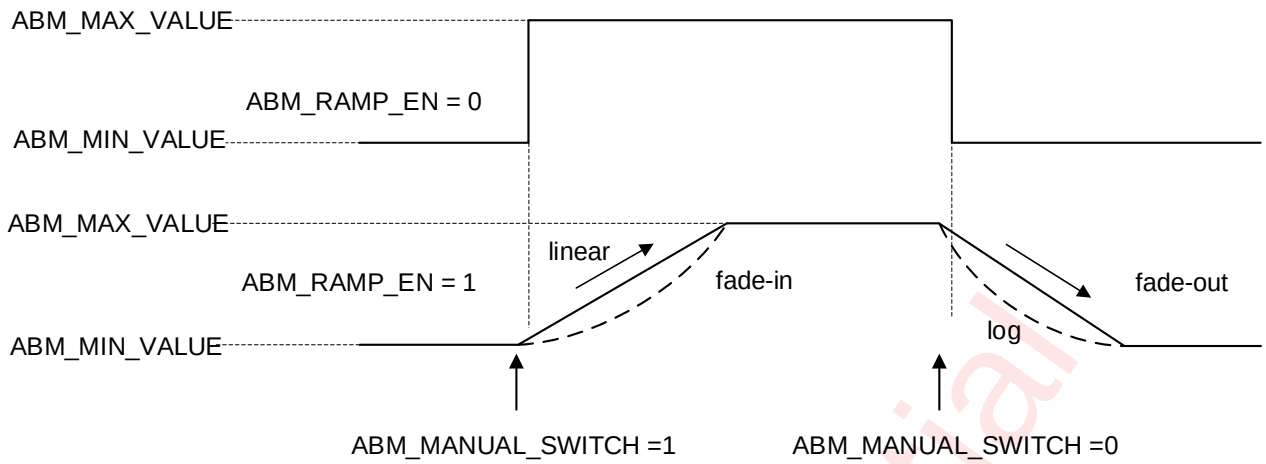


Figure 14 Manual Switch Mode

EMI Reduction

Spread Spectrum

If SSR_EN bit in SSR_CFG1(26h) register is set to "1", spread spectrum function is enabled. By setting the bits SSR_AMP in register SSR_CFG1, various spread spectrum range can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

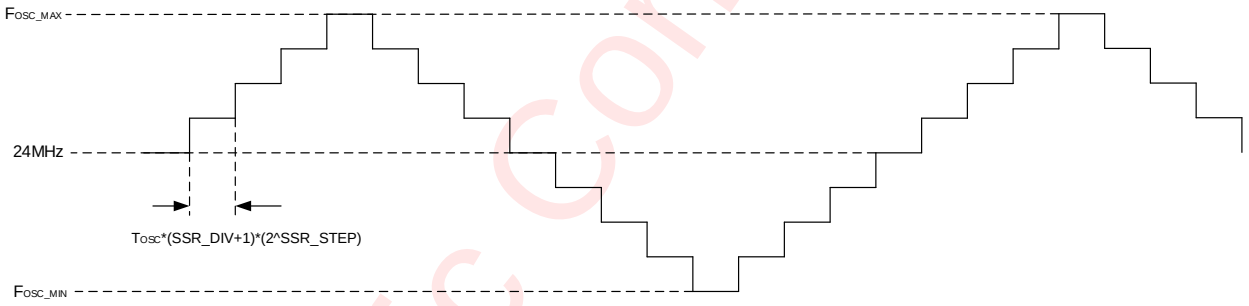


Figure 15 spread spectrum

Table 6 OSC Frequency when SSR is enabled

SSR_AMP(Binary)	F_{OSC_MIN}(MHz)	F_{OSC_MAX}(MHz)
0000	24	24
0001	23.7	24.2
0010	23.5	24.4
0011	23.2	24.7
0100	23	25
0101	22.8	25.1
0110	22.6	25.4
0111	22.4	25.7
1000	22.2	26
1001	22	26.2

1010	21.8	26.5
1011	21.6	26.8
1100	21.4	27.1
1101	21.2	27.4
1110	21.1	27.7
1111	21	28

Slew-Rate

The device supports programmable slew rate control, enabling adjustment of the transition time for turning the LED current sinks (CS1–CS18) on or off, thereby reducing electromagnetic interference (EMI). This control is configured using the LED_SRR and LED_SRF bits in the MISC_CFG2 (DCh) register.

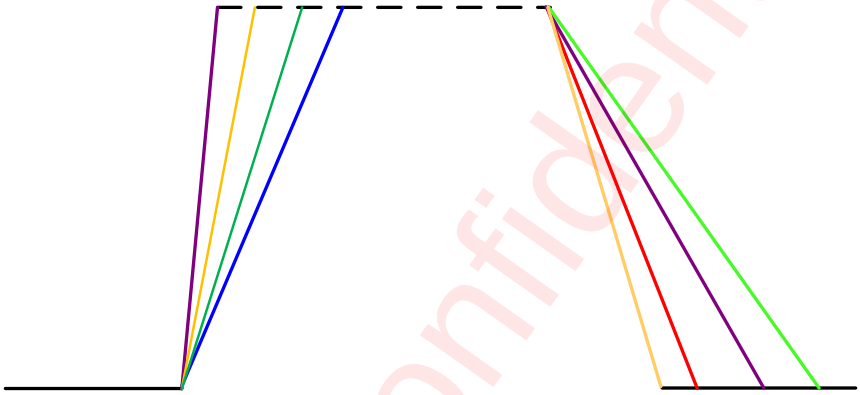


Figure 16 slew rate

Protection Features

Thermal Shutdown (TSD)

The device is equipped with an integrated thermal shutdown protection to prevent overheating-induced damage. This system triggers the LED Thermal Shutdown protocol at a junction temperature of 150°C and automatically restores normal operation when the temperature decreases to 130°C.

This function is enabled by OTP_EN in register MISC_CFG1(DBh); When TSD is happened, the device will enter into LED_THERMAL_SHUTDOWN mode, OTS_FLAG bit in STATUS(D8h) will be set, and this bit will be cleared after write 1.

Thermal Roll-Off (TRO)

The device supports thermal-roll-off. This function will automatically reduce the chip current when the temperature exceeds the user-defined threshold, thereby preventing further temperature escalation and potential chip damage. Upon temperature descent below the threshold, the chip current will be automatically restored to its nominal operational level.

The bits TR_TH[1:0] and bits TR_OF[1:0] of register TR_CFG(29h) are thermal roll off threshold temperature and thermal roll off percentage of I_{OUT} respectively. The threshold temperature can be configured as 140°C, 120°C, 100°C or 90°C. Thermal roll off percentage can be configured as 100%, 75%, 50% or 25%.

When set the bits TR_TH[1:0] to be “00” and set bits TR_OF[1:0] to be “10”, the thermal roll off threshold temperature is “140°C”. Once the temperature is over 140°C, the flag bit TRS_FLG of register STATUS(D8h) is set to “1”, and I_{OUT} will be decreased to its 50%.

Under-Voltage-Lock-Out (UVLO)

The device has an internal comparator that monitors the voltage at VCC. When VCC is below 2.5V, users can choose whether to enter the STANDBY state. When bit UVLO_EN of the register MISC_CFG1 (DBh) is set to “1”, the device monitors the voltage of VCC. If the voltage drops below threshold (2.5V typically), the bit UVS_FLAG of the register STATUS (D8h) will be set to “1”. After write 1, the bit will be clear. If bit UVS_RESET_EN in register MISC_CFG1(DBh) is set, once the event of under voltage occurs, the bit CHIPEN of the register CONFIG (00h) will be cleared to “0”, and then the device will enter into STANDBY mode. If the voltage of VCC rises above 2.6V and then write “1” to bit CHIPEN, the device will enter into active mode again. By default, control bits UVLO_EN, UVS_RESET_EN are all “0”. Both UVLO monitor and protection are disabled.

Power-On Reset (POR)

The device has an internal comparator that monitors the voltage at VCC. When VCC is below 1.6V, reset is active and the device is in the POWERDOWN state.

Open/Short Detection

The device supports LED open/short detection. The threshold for LED open is 0.1V by default and threshold for short detection is VLED-1.4V by default, When performing open-circuit detection, if the voltage at the CS port is less than 0.1V, the LED will be identified as an open circuit; when performing short-circuit detection, if the voltage at the CS port is greater than VLED-1.4V, the LED will be identified as a short circuit. LED open detection and short detection is only performed in specific register configuration scenarios listed below.

1. Soft reset, wait 2ms;
2. Set GCC register, 05h≤ GCC ≤ 80h;
3. Set SLx register to FFh;
4. Set PWM_CLK_DIV in PWM_CLK_CFG(1Eh) to 011b;
5. Set PWM_MODE in CONFIG(00h) to 011b; The configuration of SW_NUM depends on the actual usage;
6. Set CHIP_EN bit to activate chip;
7. Set Dot's PWM value larger than 48h;
8. set bit OPEN_DECT_TH or SHORT_DECT_TH in register OS_CFG(28h) to choose appropriate threshold for open detection or short detection;
9. Set bits OS_SMPLE_SEL to 10b;
10. Set bits OS_DECT_EN to 10b or 11b to activate short detection or open detection;
11. wait 10ms;
12. read bit OS_LED in STATUS(D8h). If the bit is 1, it indicates that one or more LED dots are abnormal.
13. read register CCh~D7h to confirm which specific LED dot has an open or short fault.

	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	CS16	CS17	CS18
SW1	OS_SW1_L						OS_SW1_M						OS_SW1_H					
SW2	OS_SW2_L						OS_SW2_M						OS_SW2_H					
SW3	OS_SW3_L						OS_SW3_M						OS_SW3_H					
SW4	OS_SW4_L						OS_SW4_M						OS_SW4_H					

Figure 17 open/short storage

Device Work Mode

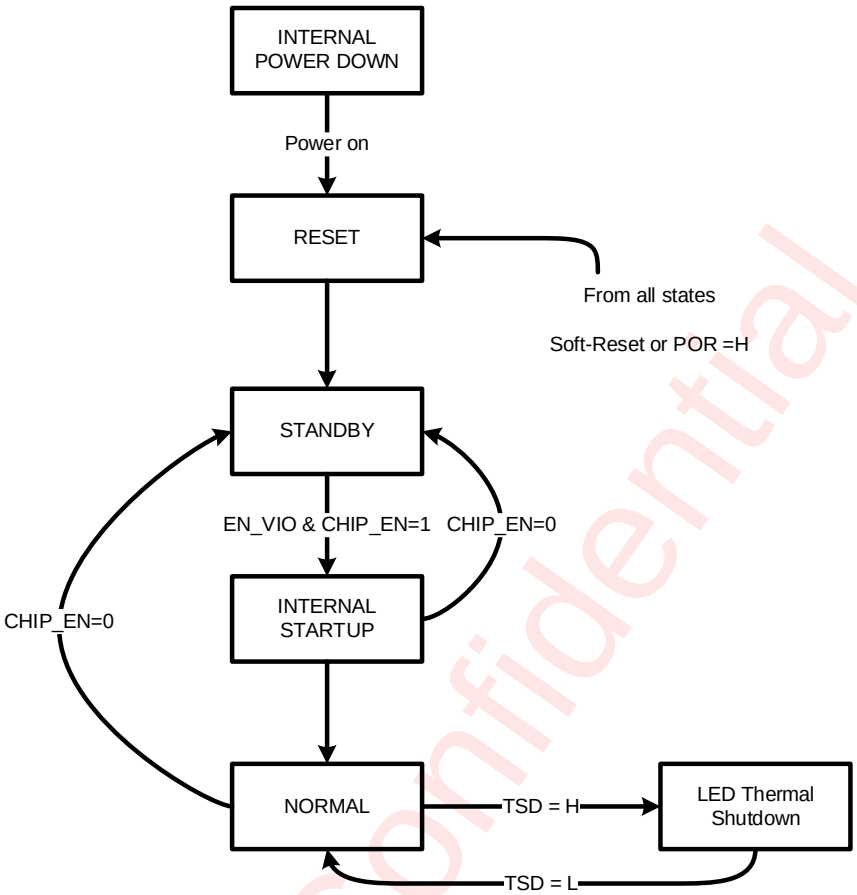


Figure 18 operating mode transition

RESET: In RESET mode, all internal registers are restored to their default states. The system enters RESET mode upon performing the Soft-Reset process or when the internal Power-On Reset (POR) circuit is activated, which occurs during initial chip power-up or when the supply voltage VCC drops below the typical threshold of 1.6V. Following VCC restoration above 2.0V (typ.), the POR function disengages, automatically transitioning the device into STANDBY mode. By default, the CHIP_EN control bit maintains a low logic level after any POR sequence completion.

STANDBY: The device enters STANDBY mode when either the CHIP_EN register bit or the EN_VIO pin is set to LOW while the Reset signal remains inactive, initiating a low-power state where all internal circuitry is deactivated. During this mode, all register settings remain writable provided the EN_VIO pin is subsequently asserted HIGH, enabling configuration updates that become operational immediately upon exiting standby (refer to the Register Details section for specific register behavior and configuration timing requirements). When EN_VIO is pulled low, the CHIP_EN bit will be reset, while the values of other registers remain unchanged, and the communication interface will be inaccessible.

STARTUP: When CHIP_EN bit is written high and EN_VIO pin is high, the internal startup sequence powers up all the needed internal blocks (VREF, bias, oscillator etc.). Startup delay is 100 μs.

NORMAL: During NORMAL mode the user controls the chip using the Control Registers.

LED Thermal Shutdown: In LED Thermal Shutdown mode, LED output circuits will be disabled.

Device Program

The device supports I²C and SPI buses. After power-on, the chip will perform initialization. Users must wait for 1.5 milliseconds and then configure the CHIP_EN bit of the CONFIG (00h) register to enable the chip. Only after the chip is enabled can users configure other registers via the I²C bus. If a global soft reset is required, users must follow the steps below when using different communication protocols.

Soft-Reset Process

When in I²C Mode:

1. Write 0xFF to DAh register
2. wait 1.5ms
3. reconfigure registers to active chip

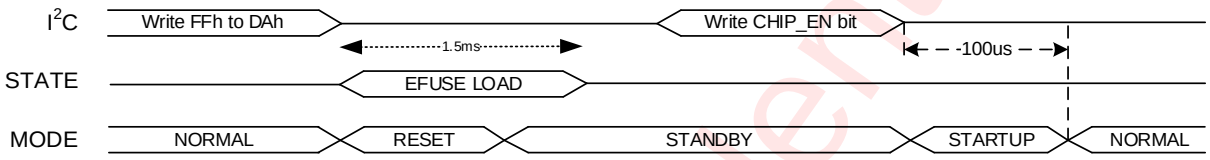


Figure 19 Soft-Reset process in I²C MODE

When in SPI Mode:

1. Write 0xFF06 to DAh register by address automatic increment write shown in Figure26
2. wait 1.5ms
3. reconfigure registers to active chip

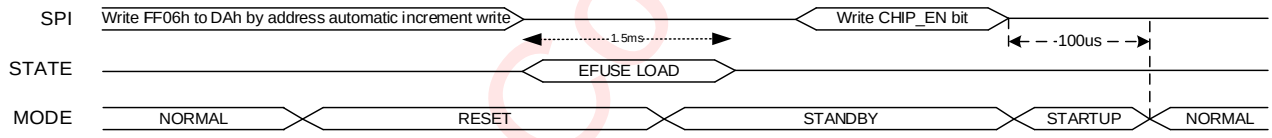


Figure 20 Soft-Reset process in SPI MODE

General I²C Operation

The device supports the I²C serial bus protocol, operating in fast mode at 400 kHz and super-fast mode at 1000 kHz. It functions as a slave device on the I²C bus, with connections established through open-drain SCL and SDA I/O pins. A pull-up resistor within the range of 1 kΩ to 10 kΩ (typically 4.7 kΩ) is recommended for proper operation. The I²C interface supports voltage levels ranging from 1.2 V to 5.0 V.

Device Address

Table 7 I²C Device Address Configuration

AD1 Connection	AD0 Connection	Device Address	
		Independent	Broadcast
GND	GND	0x60	0x40
	VCC	0x61	
	SCL	0x62	
	SDA	0x63	

VCC	GND	0x64	
	VCC	0x65	
	SCL	0x66	
	SDA	0x67	
SCL	GND	0x68	
	VCC	0x69	
	SCL	0x6A	
	SDA	0x6B	
SDA	GND	0x6C	
	VCC	0x6D	
	SCL	0x6E	
	SDA	0x6F	

The I²C device address depends on the status of pins AD0 and AD1. Connecting pin AD0 or AD1 to different signal will change the device address as showed in table above.

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

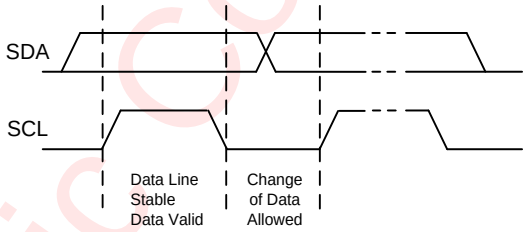


Figure 21 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

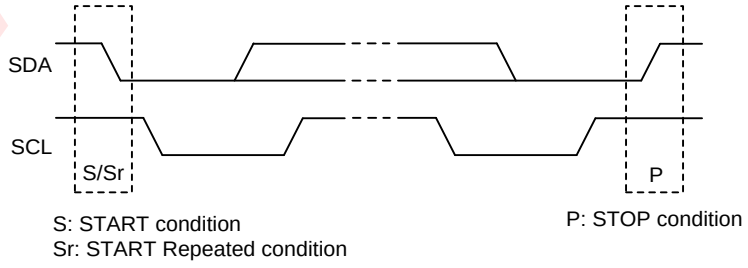


Figure 22 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

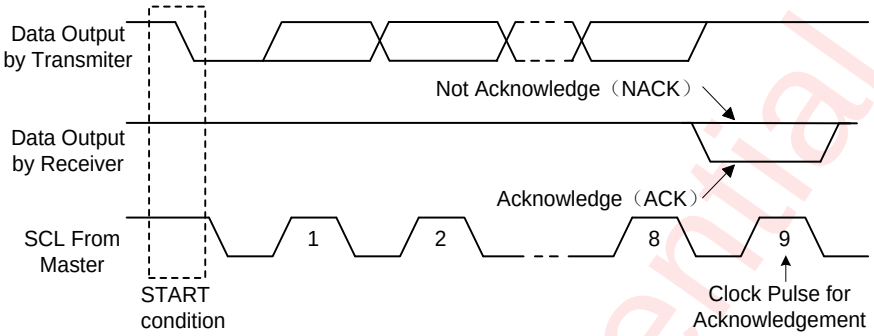


Figure 23 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal
h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)
i) Master generates STOP condition to indicate write cycle end

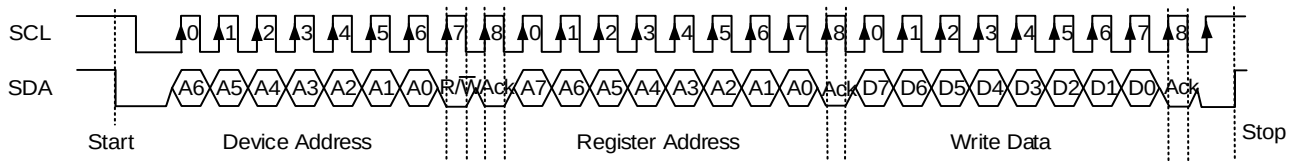


Figure 24 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

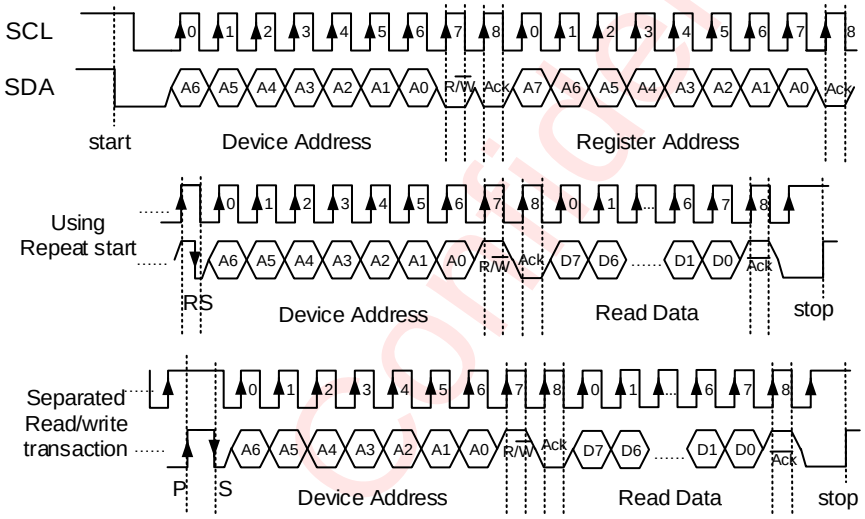


Figure 25 I²C Read Byte Cycle

General SPI Operation

This device supports the SPI bus with CPOL = 1 and CPHA = 1 as shown in the following figure. Data transmission protocol in fast mode up to 20MHz. This device operates as a slave on the SPI bus. SPI master controls write or read register of the device.

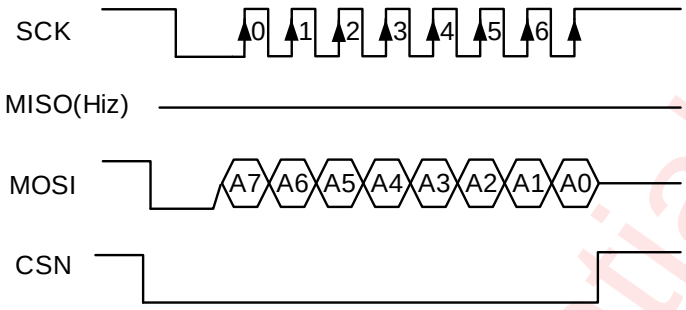


Figure 26 SPI Phase

The SPI data format is 8-bit. The first command byte is composed by 4-bit chip ID, 3-bit page ID and W/R bit, the command byte must be sent first, then is followed by register address and then the register data. the 4-bit chip ID is always 4'b1010, the 3-bit page ID is always 3'b000, If W/R is 0, which will be write operation and master can write data into the register, If W/R is 1, which will be read operation and master can read data from the register.

Table 8 Command Byte

BITS	D7:D4	D3:D1	D0
Value	1010	000	0: Write / 1: Read

Write Cycle

Writing process refers to the master device write data into the slave device. In this process, data is sent from the master device to the slave device in MOSI, MISO will be unchanged.

Typical write:

1. First of all, master sets CSN to low, to enable operation to the device.
2. Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and write command.
3. Then master sends the register address.
4. Then master sends the data to write into register address sent before.
5. Finally master pulls CSN high to finish the operation.

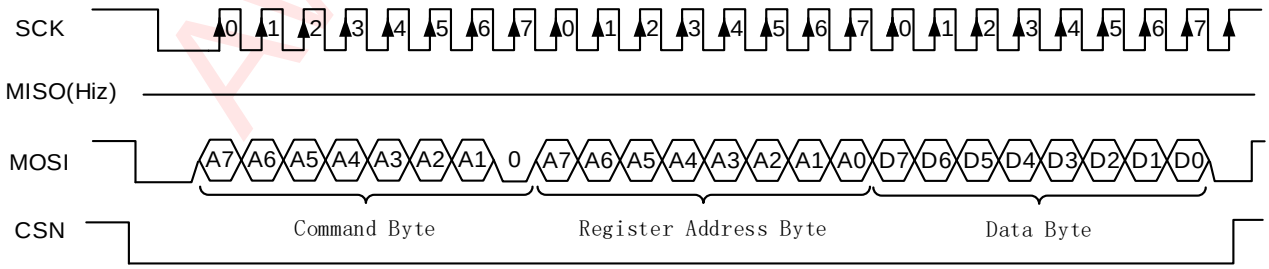


Figure 27 SPI Write cycle (typical)

Automatic address increment write:

1. First of all, master sets CSN to low, to enable operation to the device.
2. Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and write command.
3. Then master sends the register address.

4. During the 8th rising edge of receiving the first data byte, the internal address pointer will increment by one. The next data byte sent to device will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be written to device.
5. Finally master pulls CSN high to finish the operation.

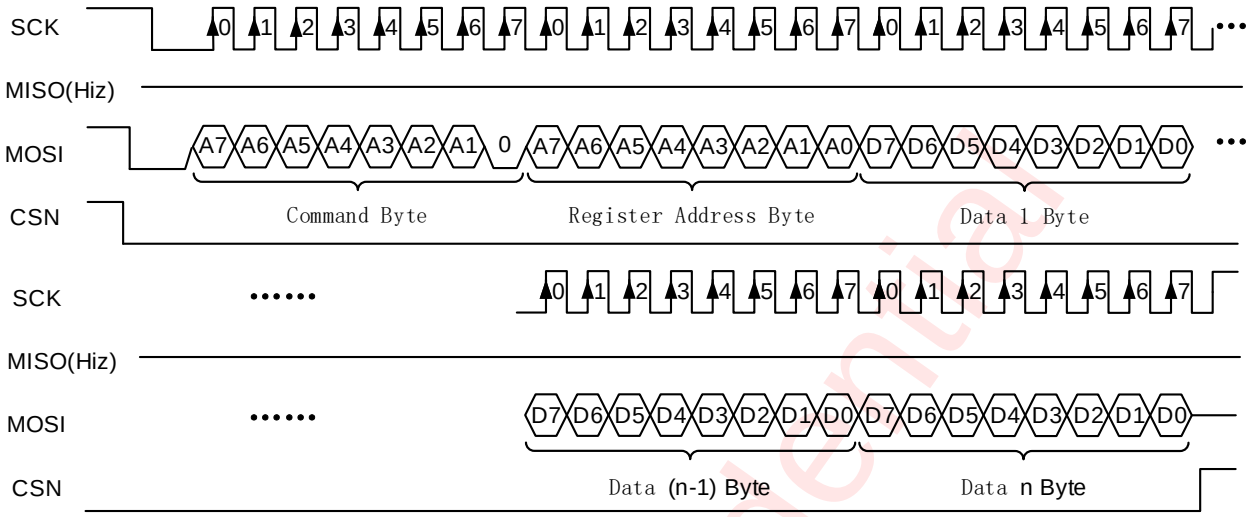


Figure 28 SPI Write cycle (Address-Auto-Increment)

Read Cycle

Reading process refers to the slave device reading data back to the master device. In this process, the read command data and register address will send in MOSI and read data will send back to master in MISO.
Typical read:

1. First of all, master sets CSN to low, to enable operation to the device.
2. Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and read command.
3. Then master sends the register address.
4. Then the device sends the data read out from register address sent before in MISO.
5. Finally master pulls CSN high to finish the operation.

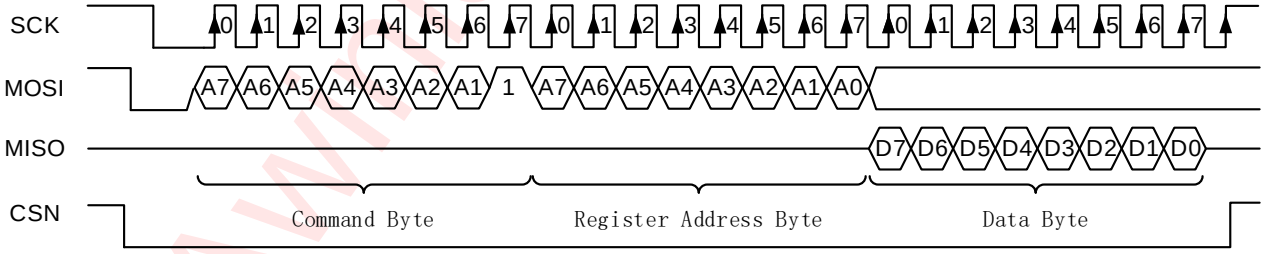


Figure 29 SPI Read cycle (typical)

Automatic address increment read:

1. First of all, master sets CSN to low, to enable operation to the device.
2. Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and read command.
3. Then master sends the register address.
4. During the 8th rising edge of sending the first data byte, the internal address pointer will increment by one. The next data byte sent from chip will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be read from chip.
5. Finally master pulls CSN high to finish the operation.

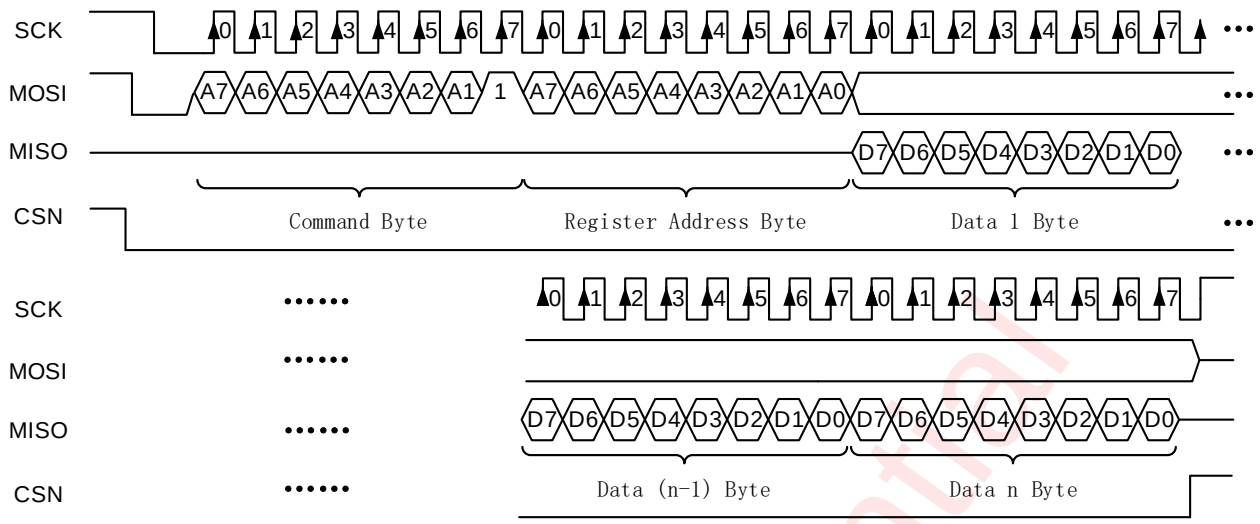


Figure 30 SPI Read cycle (Address-Auto-Increment)

Register Configuration

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	CONFIG	RW	LED_IME		SW_NUM		PWM_MODE			CHIP_EN	0x02
0x01	GCCR	RW	GCC								0x00
0x02 ~ 0x13	SL1~ SL18	RW	SL_CS1~ SL_CS18								0x80
0x14	ABM_CFG1	RW	ABM_MIN_VALUE								0x00
0x15	ABM_CFG2	RW	ABM_MAX_VALUE								0x00
0x16	ABM_CFG3	RW	ABM_T0				ABM_T1				0x00
0x17	ABM_CFG4	RW	ABM_T2				ABM_T3				0x00
0x18	ABM_CFG5	RW	ABM_LOOP_END		ABM_LOOP_START		ABM_LOOP_TIMES_H				0x00
0x19	ABM_CFG6	RW	ABM_LOOP_TIMES_L								0x00
0x1A	ABM_CFG7	RW	ONOFF_MODE_EN	ONOFF_VALUE_SEL	ABM_LOG_EN	ABM_MANUAL_SWITCH	ABM_RAMP_EN	ABM_MODE	ABM_EN	ABM_GO	0x00
0x1B	PHASE_CFG1	RW	SETUP_TIME_LSB		DEGHOST_TIME						0x18
0x1C	PHASE_CFG2	RW	HOLD_TIME				SETUP_TIME_MSB				0x33
0x1D	PHASE_CFG3	RW								CS_GROUP_DELAY	0x00
0x1E	PWM_CLK_CFG	RW						PWM_CLK_DIV			0x00
0x24	DEGHOST_CFG1	RW							CS_PULLUP_MODE	SW_PULLDOWN_MODE	0x00
0x25	DEGHOST_CFG2	RW	CS_PULLUP_SEL				SW_PULLDOWN_SEL				0x00
0x26	SSR_CFG1	RW	SSR_AMP					SSR_STEP		SSR_EN	0x00
0x27	SSR_CFG2	RW	SSR_DIV								0x00
0x28	OS_CFG	RW	OPEN_DECT_TH	SHORT_DECT_TH			OS_SMPLE_SEL		OS_DECT_EN		0x00
0x29	TR_CFG	RW					TR_OF		TR_TH		0x00
0x30 ~ 0xBF	PWMR1~ PWMR144	RW	PWM1~ PWM144								0x00
0xC0	ABM_SW1_L	RW			ABM_SW1_CS6	ABM_SW1_CS5	ABM_SW1_CS4	ABM_SW1_CS3	ABM_SW1_CS2	ABM_SW1_CS1	0x00
0xC1	ABM_SW1_M	RW			ABM_SW1_CS12	ABM_SW1_CS11	ABM_SW1_CS10	ABM_SW1_CS9	ABM_SW1_CS8	ABM_SW1_CS7	0x00
0xC2	ABM_SW1_H	RW			ABM_SW1_CS18	ABM_SW1_CS17	ABM_SW1_CS16	ABM_SW1_CS15	ABM_SW1_CS14	ABM_SW1_CS13	0x00
0xC3	ABM_SW2_L	RW			ABM_SW2_CS6	ABM_SW2_CS5	ABM_SW2_CS4	ABM_SW2_CS3	ABM_SW2_CS2	ABM_SW2_CS1	0x00
0xC4	ABM_SW2_M	RW			ABM_SW2_CS12	ABM_SW2_CS11	ABM_SW2_CS10	ABM_SW2_CS9	ABM_SW2_CS8	ABM_SW2_CS7	0x00
0xC5	ABM_SW2_H	RW			ABM_SW2_CS18	ABM_SW2_CS17	ABM_SW2_CS16	ABM_SW2_CS15	ABM_SW2_CS14	ABM_SW2_CS13	0x00
0xC6	ABM_SW3_L	RW			ABM_SW3_CS6	ABM_SW3_CS5	ABM_SW3_CS4	ABM_SW3_CS3	ABM_SW3_CS2	ABM_SW3_CS1	0x00
0xC7	ABM_SW3_M	RW			ABM_SW3_CS12	ABM_SW3_CS11	ABM_SW3_CS10	ABM_SW3_CS9	ABM_SW3_CS8	ABM_SW3_CS7	0x00
0xC8	ABM_SW3_H	RW			ABM_SW3_CS18	ABM_SW3_CS17	ABM_SW3_CS16	ABM_SW3_CS15	ABM_SW3_CS14	ABM_SW3_CS13	0x00
0xC9	ABM_SW4_L	RW			ABM_SW4_CS6	ABM_SW4_CS5	ABM_SW4_CS4	ABM_SW4_CS3	ABM_SW4_CS2	ABM_SW4_CS1	0x00
0xCA	ABM_SW4_M	RW			ABM_SW4_CS12	ABM_SW4_CS11	ABM_SW4_CS10	ABM_SW4_CS9	ABM_SW4_CS8	ABM_SW4_CS7	0x00
0xCB	ABM_SW4_H	RW			ABM_SW4_CS18	ABM_SW4_CS17	ABM_SW4_CS16	ABM_SW4_CS15	ABM_SW4_CS14	ABM_SW4_CS13	0x00
0xCC	OS_SW1_L	RO			OS_SW1_CS6	OS_SW1_CS5	OS_SW1_CS4	OS_SW1_CS3	OS_SW1_CS2	OS_SW1_CS1	0x00

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0xCD	OS_SW1_M	RO			OS_SW1_CS12	OS_SW1_CS11	OS_SW1_CS10	OS_SW1_CS9	OS_SW1_CS8	OS_SW1_CS7	0x00
0xCE	OS_SW1_H	RO			OS_SW1_CS18	OS_SW1_CS17	OS_SW1_CS16	OS_SW1_CS15	OS_SW1_CS14	OS_SW1_CS13	0x00
0xCF	OS_SW2_L	RO			OS_SW2_CS6	OS_SW2_CS5	OS_SW2_CS4	OS_SW2_CS3	OS_SW2_CS2	OS_SW2_CS1	0x00
0xD0	OS_SW2_M	RO			OS_SW2_CS12	OS_SW2_CS11	OS_SW2_CS10	OS_SW2_CS9	OS_SW2_CS8	OS_SW2_CS7	0x00
0xD1	OS_SW2_H	RO			OS_SW2_CS18	OS_SW2_CS17	OS_SW2_CS16	OS_SW2_CS15	OS_SW2_CS14	OS_SW2_CS13	0x00
0xD2	OS_SW3_L	RO			OS_SW3_CS6	OS_SW3_CS5	OS_SW3_CS4	OS_SW3_CS3	OS_SW3_CS2	OS_SW3_CS1	0x00
0xD3	OS_SW3_M	RO			OS_SW3_CS12	OS_SW3_CS11	OS_SW3_CS10	OS_SW3_CS9	OS_SW3_CS8	OS_SW3_CS7	0x00
0xD4	OS_SW3_H	RO			OS_SW3_CS18	OS_SW3_CS17	OS_SW3_CS16	OS_SW3_CS15	OS_SW3_CS14	OS_SW3_CS13	0x00
0xD5	OS_SW4_L	RO			OS_SW4_CS6	OS_SW4_CS5	OS_SW4_CS4	OS_SW4_CS3	OS_SW4_CS2	OS_SW4_CS1	0x00
0xD6	OS_SW4_M	RO			OS_SW4_CS12	OS_SW4_CS11	OS_SW4_CS10	OS_SW4_CS9	OS_SW4_CS8	OS_SW4_CS7	0x00
0xD7	OS_SW4_H	RO			OS_SW4_CS18	OS_SW4_CS17	OS_SW4_CS16	OS_SW4_CS15	OS_SW4_CS14	OS_SW4_CS13	0x00
0xD8	STATUS	RW	ABM_OVER	ABM_RUNNING			OS_LED	TRS_FLAG	OTS_FLAG	UVS_FLAG	0x00
0xD9	CHIP_ID_R	RO	CHIP_ID								0x1F
0xDA	RESET	WO	SOFT_RESET								0x00
0xDB	MISC_CFG1	RW		MATRIX_ON_EN		UVS_RESET_EN		TRO_EN	OTP_EN	UVLO_EN	0x06
0xDC	MISC_CFG2	RW	LED_CAIE	IREF_LCAIE	LED_SW_MODE_SEL	LED_TR_EN	LED_SRR		LED_SRF		0x3F
0xDD	MISC_CFG3	RW						SDA_SR	MISO_DR		0x01

Register Detailed Description

CONFIG: (Address 00h)

Bit	Symbol	R/W	Description	Default
7	LED_IME	RW	LED output current Iout_max reduce to 1/4 of maximum value. 0: Disable. 1: Enable.	0x0
6	Reserved	RW	Not used	0
5:4	SW_NUM	RW	SW max numbers setting. b00: 1 b01: 2 b10: 3 b11: 4 Note: Cannot changed when LED is working.	0x0
3:1	PWM_MODE	RW	PWM Mode Selection. b000: 6bit + 2Dither b001: 8bit b010: 8bit + 4Dither b011: 12bit Other: 6bit + 6 Dither Note: Cannot changed when LED is working.	0x1
0	CHIP_EN	RW	Chip enable. All registers can STILL be written or read in STANDBY mode. 0: Standby mode. 1: Normal mode.	0x0

GCCR: (Address 01h)

Bit	Symbol	R/W	Description	Default
7:0	GCC	RW	Global Current Setting. Every Step is 0.2mA.	0x00

SLn(n=1~18): (Address 02h~13h)

Bit	Symbol	R/W	Description	Default
7:0	SL_CSn	RW	Current Scaling Control. When LED_IME is 0, I_out = 51mA x (GCC/255) x (SL/255). When LED_IME is 1, I_out = 12.75mA x (GCC/255) x (SL/255).	0x80

ABM_CFG1: (Address 14h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ABM_MIN_VALUE	RW	ABM Pattern lowest pwm value.	0x00

ABM_CFG2: (Address 15h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ABM_MAX_VALUE	RW	When ONOFF_MODE_EN is 1: ONOFF Mode Highest pwm value. When ONOFF_MODE_EN is 0: ABM Pattern Highestest pwm value.	0x00

ABM_CFG3: (Address 16h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	ABM_T0	RW	ABM ramp rise time. b0000 : 0s; b0001 : 0.13s b0010 : 0.26s b0011 : 0.38s b0100 : 0.51s b0101 : 0.77s b0110 : 1.04s b0111 : 1.6s b1000 : 2.1s b1001 : 2.6s b1010 : 3.1s b1011 : 4.2s b1100 : 5.2s b1101 : 6.2s b1110 : 7.3s b1111 : 8.3s	0x00
3:0	ABM_T1	RW	ABM Hold on time Setting. b0000: 0.04s b0001: 0.13s b0010: 0.26s b0011:0.38s b0100:0.51s b0101: 0.77s b0110: 1.04s b0111: 1.6s b1000: 2.1s b1001: 2.6s b1010: 3.1s b1011: 4.2s b1100: 5.2s b1101: 6.2s b1110: 7.3s b1111: 8.3s	0x00

ABM_CFG4: (Address 17h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:4	ABM_T2	RW	ABM Fall time Setting. The fall time refer to the bits ABM_T0 of the register ABM_CFG3	0x00
3:0	ABM_T3	RW	ABM Hold off time Setting. The hold off time refer to the bits ABM_T1 of the register ABM_CFG3	0x00

ABM_CFG5: (Address 18h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	ABM_LOOP_END	RW	ABM end point selection. b00: pattern stop at OFF state. Other: pattern stop as ON state.	0x00
5:4	ABM_LOOP_START	RW	ABM start point selection. b00: pattern start from RISE state. b01: pattern start from ON state. b10: pattern start from OFF state. b11: pattern start from OFF state.	0x00
3:0	ABM_LOOP_TIMES_H	RW	4 MSB of pattern loop times.	0x00

ABM_CFG6: (Address 19h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	ABM_LOOP_TIMES_L	RW	8 LSB of pattern loop times.	0x00

ABM_CFG7: (Address 1Ah)

Bit	Symbol	R/W	Description	Default
7	ONOFF_MODE_EN	RW	when this bit is 1 , write 0xC0~0xCB to control dotx on or off. 0: Disable. 1: Enable.	0x0
6	ONOFF_VALUE_SEL	RW	dot max brightness in on-off Mode. 0: ABM_MAX_VALUE 1: PWMx	0x0
5	ABM_LOG_EN	RW	ABM pwm value LOG enabled. 0: Disable 1: Enable	0x0
4	ABM_MANUAL _SWITCH	RW	Switch on or off at manual mode. 0: OFF 1: ON	0x0
3	ABM_RAMP_EN	RW	pattern ramp enable. 0: Disable 1: Enable	0x0
2	ABM_MODE	RW	0: Manual mode. 1: Auto Breath mode	0x0
1	ABM_EN	RW	ABM Enable. 0: Disable 1: Enable	0x0
0	ABM_GO	RW	ABM Start trigger. Write 1 to start pattern. User should write this bit after ABM_EN, cannot write ABM_GO and ABM_EN at the same time. Note: User should write 0 and write 1 to restart pattern. 0: ABM disable. 1: ABM start.	0x0

PHASE_CFG1: (Address 1Bh)

Bit	Symbol	R/W	Description	Default
7:6	SETUP_TIME_LSB	RW	SW SETUP time setting. T = (42ns x (2^PWM_CLK_DIV)) x ({SETUP_TIME_MSB, SETUP_TIME_LSB} + 1). Note: Cannot changed when LED is working.	0x0
5:0	DEGHOST_TIME	RW	SW De-ghosting time setting. T = (42ns x (2^PWM_CLK_DIV))x (DEGHOST_TIME + 1). Note: Cannot changed when LED is working.	0x18

PHASE_CFG2: (Address 1Ch)

Bit	Symbol	R/W	Description	Default
7:4	HOLD_TIME	RW	SW Hold time setting. T = (42ns x (2^PWM_CLK_DIV)) x HOLD_TIME. If CS_GROUP_DELAY is on, hold time must longer than 100ns. Note: Cannot changed when LED is working.	0x3
3:0	SETUP_TIME_MSB	RW	SW SETUP time setting. T = (42ns x (2^PWM_CLK_DIV)) x ({SETUP_TIME_MSB, SETUP_TIME_LSB} + 1). Note: Cannot changed when LED is working.	0x3

PHASE_CFG3: (Address 1Dh)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0
0	CS_GROUP_DELAY	RW	Every 6 CSs delay 42ns. 0: Disable 1: Enable Note: Cannot changed when LED is working.	0x0

PWM_CLK_CFG: (Address 1Eh)

Bit	Symbol	R/W	Description	Default
7:3	Reserved	RW	Not used	0
2:0	PWM_CLK_DIV	RW	PWM clock frequency setting. f_pwm = 24MHz/(2^PWM_CLK_DIV).	0x0

DEGHOST_CFG1: (Address 24h)

Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1	CS_PULLUP_MODE	RW	CS Pull-up Mode select. 0: only in non-overlap time. 1: all the time. Note: Cannot changed when LED is working.	0x0
0	SW_PULLDOWN_MODE	RW	SW Pull-down Mode select. 0: only in non-overlap time. 1: all the time. Note: Cannot changed when LED is working.	0x0

DEGHOST_CFG2: (Address 25h)

Bit	Symbol	R/W	Description	Default
7:4	CS_PULLUP_SEL	RW	CS pull-up voltage selection. b0000: no pull-up b0001: VLED-1.47V b0010: VLED -1.33V b0011: VLED -1.2V b0100: VLED -1.07V b0101: VLED -0.93V b0110: VLED -0.8V b0111: VLED b1000: no pull-up b1001: VLED -2.94V b1010: VLED -2.66V b1011: VLED -2.4V b1100: VLED -2.14V b1101: VLED -1.86V b1110: VLED -1.6V b1111: VLED	0x0
3:0	SW_PULLDOWN_SEL	RW	SW pull-down voltage selection. b0000: no pull-down b0001: 1.6V b0010: 1.47V b0011: 1.32V b0100: 1.18V b0101: 1.03V b0110: 0.88V b0111: GND b1000: no pull-down b1001: 3.2V b1010: 2.94V b1011: 2.64V b1100: 2.36V b1101: 2.06V b1110: 1.76V b1111: GND	0x0

SSR_CFG1: (Address 26h)

Bit	Symbol	R/W	Description	Default
7:4	SSR_AMP	RW	SSR max amplitude. For example, if set to b0011, then SSR max value is 10011 and min value is 01101, which means OSC max frequency is 24.7MHz and min frequency is 23.2MHz.	0x0
3	Reserved	RW	Not used	0
2:1	SSR_STEP	RW	SSR step. Fssr = sys_freq/[(ssr_div+1)*(2^ssr_step)]	0x0
0	SSR_EN	RW	SSR EN 0:Disable 1: Enable	0x0

SSR_CFG2: (Address 27h)

Bit	Symbol	R/W	Description	Default
7:0	SSR_DIV	RW	SSR divider. Fssr = sys_freq/[(ssr_div+1)*(2^ssr_step)]	0x0

OS_CFG: (Address 28h)

Bit	Symbol	R/W	Description	Default
7	OPEN_DECT_TH	RW	LED Open detection threshold setting. 0: 0.1V 1: 0.2V	0x0

6	SHORT_DECT_TH	RW	LED Short detection threshold setting. 0: VLED-1.4V 1: VLED-0.8V	0x0
5:4	Reserved	RW	Not used	0
3:2	OS_SMPLE_SEL	RW	Open-Short status sample point select. b00: sample at 6% pwm b01: 12.5% b10: 25% b11: 50% Note: When PWM Mode is 6+2/6+6, os_smple_sel MUST be b10; When PWM Mode is 8/8+4, os_smple_sel CANNOT be b11, b10 is recommended; When PWM Mode is 12, os_smple_sel CAN be any value, b10 is recommended.	0x0
1:0	OS_DECT_EN	RW	b00: Disable OS detect; b01: Disable OS detect; b10: Short Detect enable. b11: Open Detect enable. Note: When OS detect is enabled, DEGHOST_CFG2(25h) must be 0 and PWM_CLK_CFG(1Eh) should be larger than 3.	0x0

TR_CFG: (Address 29h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0
3:2	TR_OF	RW	Thermal Protection Current selection. When thermal-error happens, global current will be deduced. b00: 100% b01: 75% b10: 50% b11: 25%	0x0
1:0	TR_TH	RW	Thermal Protection Trigger Temperature selection. b00: 140℃ b01: 120℃ b10: 100℃ b11: 90℃	0x0

PWMR1: (Address 30h)

Bit	Symbol	R/W	Description	Default
7:0	PWM1	RW	When in 6/8bit mode, DOT1 PWM. When 12bit Mode, DOT1 PWM 8 LSB.	0x0

PWMR2: (Address 31h)

Bit	Symbol	R/W	Description	Default
7:0	PWM2	RW	When in 6/8bit mode, DOT2 PWM. When in 12bit mode, DOT1 PWM 4 MSB, only 4 LSB valid.	0x0

...

PWMR71: (Address 76h)

Bit	Symbol	R/W	Description	Default
7:0	PWM71	RW	When in 6/8bit mode, DOT71 PWM. When in 12bit mode, DOT36 PWM 8 LSB.	0x0

PWMR72: (Address 77h)

Bit	Symbol	R/W	Description	Default
7:0	PWM72	RW	When in 6/8bit mode, DOT72 PWM. When in 12bit mode, DOT36 PWM 4 MSB, only 4 LSB valid.	0x0

PWMR73: (Address 78h)

Bit	Symbol	R/W	Description	Default
7:0	PWM73	RW	When in 12bit mode, DOT37 PWM 8 LSB.	0x0

PWMR74: (Address 79h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	PWM74	RW	When in 12bit mode, DOT37 PWM 4 MSB, only 4 LSB valid.	0x0

...

PWMR143: (Address BEh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	PWM143	RW	When in 12bit mode, DOT72 PWM 8 LSB.	0x0

PWMR144: (Address BFh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	PWM144	RW	When in 12bit mode, DOT72 PWM 4 MSB, only 4 LSB valid.	0x0

ABM_SW1_L: (Address C0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RW	Not used	0
5	ABM_SW1_CS6	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW1_CS5	RW		0x0
3	ABM_SW1_CS4	RW		0x0
2	ABM_SW1_CS3	RW		0x0
1	ABM_SW1_CS2	RW		0x0
0	ABM_SW1_CS1	RW		0x0

ABM_SW1_M: (Address C1h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RW	Not used	0
5	ABM_SW1_CS12	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW1_CS11	RW		0x0
3	ABM_SW1_CS10	RW		0x0
2	ABM_SW1_CS9	RW		0x0
1	ABM_SW1_CS8	RW		0x0
0	ABM_SW1_CS7	RW		0x0

ABM_SW1_H: (Address C2h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW1_CS18	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW1_CS17	RW		0x0
3	ABM_SW1_CS16	RW		0x0
2	ABM_SW1_CS15	RW		0x0
1	ABM_SW1_CS14	RW		0x0
0	ABM_SW1_CS13	RW		0x0

ABM_SW2_L: (Address C3h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW2_CS6	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW2_CS5	RW		0x0
3	ABM_SW2_CS4	RW		0x0
2	ABM_SW2_CS3	RW		0x0
1	ABM_SW2_CS2	RW		0x0
0	ABM_SW2_CS1	RW		0x0

ABM_SW2_M: (Address C4h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW2_CS12	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW2_CS11	RW		0x0
3	ABM_SW2_CS10	RW		0x0
2	ABM_SW2_CS9	RW		0x0
1	ABM_SW2_CS8	RW		0x0
0	ABM_SW2_CS7	RW		0x0

ABM_SW2_H: (Address C5h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW2_CS18	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW2_CS17	RW		0x0
3	ABM_SW2_CS16	RW		0x0
2	ABM_SW2_CS15	RW		0x0
1	ABM_SW2_CS14	RW		0x0
0	ABM_SW2_CS13	RW		0x0

ABM_SW3_L: (Address C6h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW3_CS6	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW3_CS5	RW		0x0
3	ABM_SW3_CS4	RW		0x0
2	ABM_SW3_CS3	RW		0x0
1	ABM_SW3_CS2	RW		0x0
0	ABM_SW3_CS1	RW		0x0

ABM_SW3_M: (Address C7h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW3_CS12	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW3_CS11	RW		0x0
3	ABM_SW3_CS10	RW		0x0
2	ABM_SW3_CS9	RW		0x0
1	ABM_SW3_CS8	RW		0x0
0	ABM_SW3_CS7	RW		0x0

ABM_SW3_H: (Address C8h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW3_CS18	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW3_CS17	RW		0x0
3	ABM_SW3_CS16	RW		0x0
2	ABM_SW3_CS15	RW		0x0
1	ABM_SW3_CS14	RW		0x0
0	ABM_SW3_CS13	RW		0x0

ABM_SW4_L: (Address C9h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW4_CS6	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW4_CS5	RW		0x0
3	ABM_SW4_CS4	RW		0x0
2	ABM_SW4_CS3	RW		0x0
1	ABM_SW4_CS2	RW		0x0
0	ABM_SW4_CS1	RW		0x0

ABM_SW4_M: (Address CAh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW4_CS12	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW4_CS11	RW		0x0
3	ABM_SW4_CS10	RW		0x0
2	ABM_SW4_CS9	RW		0x0
1	ABM_SW4_CS8	RW		0x0
0	ABM_SW4_CS7	RW		0x0

ABM_SW4_H: (Address CBh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5	ABM_SW4_CS18	RW	When ONOFF_MODE_EN is 1, dot is turned on or off. 0:Off. 1: On. When ONOFF_MODE_EN is 0, determine whether dot is added to ABM pattern. 0: No. 1: Yes.	0x0
4	ABM_SW4_CS17	RW		0x0
3	ABM_SW4_CS16	RW		0x0
2	ABM_SW4_CS15	RW		0x0
1	ABM_SW4_CS14	RW		0x0
0	ABM_SW4_CS13	RW		0x0

OS_SW1_L: (Address CCh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW1_CS6	RO	Open-Short Status for SW1_CS6. 0: Normal. 1: Open/short.	0x0
4	OS_SW1_CS5	RO	Open-Short Status for SW1_CS5. 0: Normal. 1: Open/short.	0x0
3	OS_SW1_CS4	RO	Open-Short Status for SW1_CS4. 0: Normal. 1: Open/short.	0x0
2	OS_SW1_CS3	RO	Open-Short Status for SW1_CS3. 0: Normal. 1: Open/short.	0x0
1	OS_SW1_CS2	RO	Open-Short Status for SW1_CS2. 0: Normal. 1: Open/short.	0x0
0	OS_SW1_CS1	RO	Open-Short Status for SW1_CS1. 0: Normal. 1: Open/short.	0x0

OS_SW1_M: (Address CDh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW1_CS12	RO	Open-Short Status for SW1_CS12. 0: Normal. 1: Open/short.	0x0
4	OS_SW1_CS11	RO	Open-Short Status for SW1_CS11. 0: Normal. 1: Open/short.	0x0
3	OS_SW1_CS10	RO	Open-Short Status for SW1_CS10. 0: Normal. 1: Open/short.	0x0
2	OS_SW1_CS9	RO	Open-Short Status for SW1_CS9. 0: Normal. 1: Open/short.	0x0
1	OS_SW1_CS8	RO	Open-Short Status for SW1_CS8. 0: Normal. 1: Open/short.	0x0
0	OS_SW1_CS7	RO	Open-Short Status for SW1_CS7. 0: Normal. 1: Open/short.	0x0

OS_SW1_H: (Address CEh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW1_CS18	RO	Open-Short Status for SW1_CS18. 0: Normal. 1: Open/short.	0x0
4	OS_SW1_CS17	RO	Open-Short Status for SW1_CS17. 0: Normal. 1: Open/short.	0x0
3	OS_SW1_CS16	RO	Open-Short Status for SW1_CS16. 0: Normal. 1: Open/short.	0x0
2	OS_SW1_CS15	RO	Open-Short Status for SW1_CS15. 0: Normal. 1: Open/short.	0x0
1	OS_SW1_CS14	RO	Open-Short Status for SW1_CS14. 0: Normal. 1: Open/short.	0x0
0	OS_SW1_CS13	RO	Open-Short Status for SW1_CS13. 0: Normal. 1: Open/short.	0x0

OS_SW2_L: (Address CFh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW2_CS6	RO	Open-Short Status for SW1_CS6. 0: Normal. 1: Open/short.	0x0
4	OS_SW2_CS5	RO	Open-Short Status for SW1_CS5. 0: Normal. 1: Open/short.	0x0
3	OS_SW2_CS4	RO	Open-Short Status for SW1_CS4. 0: Normal. 1: Open/short.	0x0
2	OS_SW2_CS3	RO	Open-Short Status for SW1_CS3. 0: Normal. 1: Open/short.	0x0
1	OS_SW2_CS2	RO	Open-Short Status for SW1_CS2. 0: Normal. 1: Open/short.	0x0
0	OS_SW2_CS1	RO	Open-Short Status for SW1_CS1. 0: Normal. 1: Open/short.	0x0

OS_SW2_M: (Address D0h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW2_CS12	RO	Open-Short Status for SW1_CS12. 0: Normal. 1: Open/short.	0x0
4	OS_SW2_CS11	RO	Open-Short Status for SW1_CS11. 0: Normal. 1: Open/short.	0x0
3	OS_SW2_CS10	RO	Open-Short Status for SW1_CS10. 0: Normal. 1: Open/short.	0x0
2	OS_SW2_CS9	RO	Open-Short Status for SW1_CS9. 0: Normal. 1: Open/short.	0x0
1	OS_SW2_CS8	RO	Open-Short Status for SW1_CS8. 0: Normal. 1: Open/short.	0x0
0	OS_SW2_CS7	RO	Open-Short Status for SW1_CS7. 0: Normal. 1: Open/short.	0x0

OS_SW2_H: (Address D1h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW2_CS18	RO	Open-Short Status for SW1_CS18. 0: Normal. 1: Open/short.	0x0
4	OS_SW2_CS17	RO	Open-Short Status for SW1_CS17. 0: Normal. 1: Open/short.	0x0
3	OS_SW2_CS16	RO	Open-Short Status for SW1_CS16. 0: Normal. 1: Open/short.	0x0
2	OS_SW2_CS15	RO	Open-Short Status for SW1_CS15. 0: Normal. 1: Open/short.	0x0
1	OS_SW2_CS14	RO	Open-Short Status for SW1_CS14. 0: Normal. 1: Open/short.	0x0
0	OS_SW2_CS13	RO	Open-Short Status for SW1_CS13. 0: Normal. 1: Open/short.	0x0

OS_SW3_L: (Address D2h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW3_CS6	RO	Open-Short Status for SW1_CS6. 0: Normal. 1: Open/short.	0x0
4	OS_SW3_CS5	RO	Open-Short Status for SW1_CS5. 0: Normal. 1: Open/short.	0x0
3	OS_SW3_CS4	RO	Open-Short Status for SW1_CS4. 0: Normal. 1: Open/short.	0x0
2	OS_SW3_CS3	RO	Open-Short Status for SW1_CS3. 0: Normal. 1: Open/short.	0x0
1	OS_SW3_CS2	RO	Open-Short Status for SW1_CS2. 0: Normal. 1: Open/short.	0x0
0	OS_SW3_CS1	RO	Open-Short Status for SW1_CS1. 0: Normal. 1: Open/short.	0x0

OS_SW3_M: (Address D3h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW3_CS12	RO	Open-Short Status for SW1_CS12. 0: Normal. 1: Open/short.	0x0
4	OS_SW3_CS11	RO	Open-Short Status for SW1_CS11. 0: Normal. 1: Open/short.	0x0
3	OS_SW3_CS10	RO	Open-Short Status for SW1_CS10. 0: Normal. 1: Open/short.	0x0
2	OS_SW3_CS9	RO	Open-Short Status for SW1_CS9. 0: Normal. 1: Open/short.	0x0
1	OS_SW3_CS8	RO	Open-Short Status for SW1_CS8. 0: Normal. 1: Open/short.	0x0
0	OS_SW3_CS7	RO	Open-Short Status for SW1_CS7. 0: Normal. 1: Open/short.	0x0

OS_SW3_H: (Address D4h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW3_CS18	RO	Open-Short Status for SW1_CS18. 0: Normal. 1: Open/short.	0x0
4	OS_SW3_CS17	RO	Open-Short Status for SW1_CS17. 0: Normal. 1: Open/short.	0x0
3	OS_SW3_CS16	RO	Open-Short Status for SW1_CS16. 0: Normal. 1: Open/short.	0x0
2	OS_SW3_CS15	RO	Open-Short Status for SW1_CS15. 0: Normal. 1: Open/short.	0x0
1	OS_SW3_CS14	RO	Open-Short Status for SW1_CS14. 0: Normal. 1: Open/short.	0x0
0	OS_SW3_CS13	RO	Open-Short Status for SW1_CS13. 0: Normal. 1: Open/short.	0x0

OS_SW4_L: (Address D5h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW4_CS6	RO	Open-Short Status for SW1_CS6. 0: Normal. 1: Open/short.	0x0
4	OS_SW4_CS5	RO	Open-Short Status for SW1_CS5. 0: Normal. 1: Open/short.	0x0
3	OS_SW4_CS4	RO	Open-Short Status for SW1_CS4. 0: Normal. 1: Open/short.	0x0
2	OS_SW4_CS3	RO	Open-Short Status for SW1_CS3. 0: Normal. 1: Open/short.	0x0
1	OS_SW4_CS2	RO	Open-Short Status for SW1_CS2. 0: Normal. 1: Open/short.	0x0
0	OS_SW4_CS1	RO	Open-Short Status for SW1_CS1. 0: Normal. 1: Open/short.	0x0

OS_SW4_M: (Address D6h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW4_CS12	RO	Open-Short Status for SW1_CS12. 0: Normal. 1: Open/short.	0x0
4	OS_SW4_CS11	RO	Open-Short Status for SW1_CS11. 0: Normal. 1: Open/short.	0x0
3	OS_SW4_CS10	RO	Open-Short Status for SW1_CS10. 0: Normal. 1: Open/short.	0x0
2	OS_SW4_CS9	RO	Open-Short Status for SW1_CS9. 0: Normal. 1: Open/short.	0x0
1	OS_SW4_CS8	RO	Open-Short Status for SW1_CS8. 0: Normal. 1: Open/short.	0x0
0	OS_SW4_CS7	RO	Open-Short Status for SW1_CS7. 0: Normal. 1: Open/short.	0x0

OS_SW4_H: (Address D7h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5	OS_SW4_CS18	RO	Open-Short Status for SW1_CS18. 0: Normal. 1: Open/short.	0x0
4	OS_SW4_CS17	RO	Open-Short Status for SW1_CS17. 0: Normal. 1: Open/short.	0x0
3	OS_SW4_CS16	RO	Open-Short Status for SW1_CS16. 0: Normal. 1: Open/short.	0x0
2	OS_SW4_CS15	RO	Open-Short Status for SW1_CS15. 0: Normal. 1: Open/short.	0x0
1	OS_SW4_CS14	RO	Open-Short Status for SW1_CS14. 0: Normal. 1: Open/short.	0x0
0	OS_SW4_CS13	RO	Open-Short Status for SW1_CS13. 0: Normal. 1: Open/short.	0x0

STATUS: (Address D8h)

Bit	Symbol	R/W	Description	Default
7	ABM_OVER	RO	pattern is over or not. 0: Running 1: Over	0x0
6	ABM_RUNNING	RO	pattern is running or not. 1: Running 0: Over	0x0
5:4	Reserved	RW	Not used	0x0
3	OS_LED	RO	If there is a DOT is in open or short status, this bit will be 1.	0x0
2	TRS_FLAG	RW	Thermal Error Flag. Write 1 to Clear.	0x0
1	OTS_FLAG	RW	Over-Temperature Flag. Write 1 to Clear.	0x0
0	UVS_FLAG	RW	Under-Voltage Flag. Write 1 to Clear.	0x0

CHIP_ID_R: (Address D9h)

Bit	Symbol	R/W	Description	Default
7:0	CHIP_ID	RO	CHIP ID	0x1F

RESET: (Address DAh)

Bit	Symbol	R/W	Description	Default
7:0	SOFT_RESET	WO	Write FF to reset chip.	0x0

MISC_CFG1: (Address DBh)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	MATRIX_ON_EN	RW	Write 1 to lighten all dot.	0x0
5	Reserved	RW	Not used	0
4	UVS_RESET_EN	RW	When UVLO happens, chip_en register will be reset.	0x0
3	Reserved	RW	Not used	0
2	TRO_EN	RW	Thermal Roll-off Protection enable.	0x1
1	OTP_EN	RW	Over-Temperature Protection Enable. 0: Disable 1: Enable	0x1
0	UVLO_EN	RW	Under-Voltage Protection Enable. 0: Disable 1: Enable	0x0

MISC_CFG2: (Address DCh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	LED_CAIE	RW	LED current accuracy improve enable. Suggested to be 1.	0x0
6	IREF_LCAIE	RW	IREF low current accuracy improve enable.	0x0
5	LED_SW_MODE_SEL	RW	1: Analog Switch is in constant-current mode. 0 : switch mode.	0x1
4	LED_TR_EN	RW	When set to 1, it enhances the PWM rising edge speed (accelerates the transition time of the PWM signal's rising edge).	0x1
3:2	LED_SRR	RW	LED Rising slew rate. 0 for slowest and 3 for fastest.	0x3
1:0	LED_SRF	RW	LED Falling slew rate. 0 for slowest and 3 for fastest.	0x3

MISC_CFG3: (Address DDh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:3	Reserved	RW	Not used	0
2	SDA_SR	RW	SDA slew rate. 0: 1MHz I^2C 1: 400kHz I^2C	0x0
1:0	MISO_DR	RW	AD0_MISO for SPI drive strength. b00: 25% b01: 50% b10: 75% b11: 100%	0x1

Application Information

The device supports 18x4 matrix LEDs and can support up to 72 LEDs or 24 RGB LEDs.

1. It is recommended to use a combination of 1μF and 0.1μF X5R or X7R capacitors for input capacitance.

2. VLED is used for power supply of LED matrix, which requires $V_F+V_{HRSW}+V_{HRCS}$ corresponding to the maximum LED current used;

3. The communication interface can be configured by IFS. I²C is selected when IFS is low. SPI is selected when IFS is high.;

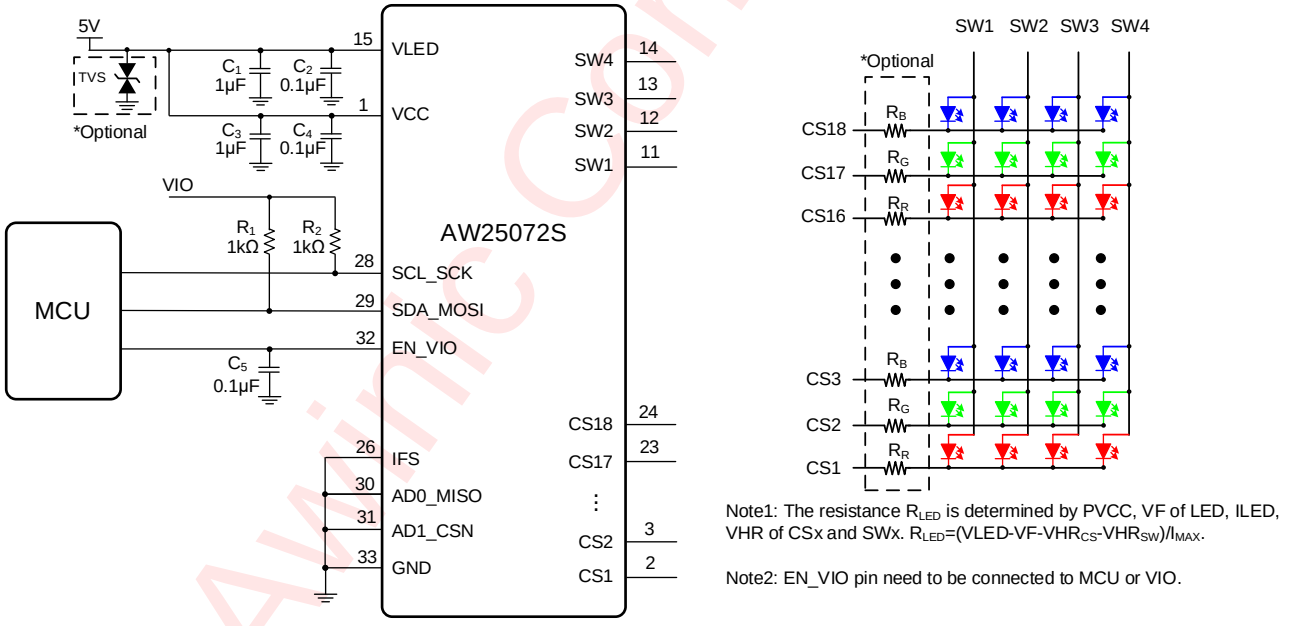
4. When selecting I²C, the I²C address is selected by AD0/AD1;

5. While enabling the chip, EN_VIO also determines the communication logic level. It is recommended to connect EN_VIO to the GPIO or the power supply of MCU to ensure communication level matching. When using SPI, the high-level driving power of MISO comes from EN_VIO, and attention should be paid to the driving capability of EN_VIO at this time;

6. The LED cathode and CSx pin can be directly connected in series with a resistor to alleviate the heat dissipation pressure of the chip when the output power is high. The resistor here has no effect on the output current.

7. It is recommended to reserve TVS positions at the power supply and interfaces that need to be externally connected to the PCB board to prevent possible ESD or surge voltages. When selecting TVS, attention should be paid to the clamp voltage being lower than the absolute maximum ratings.

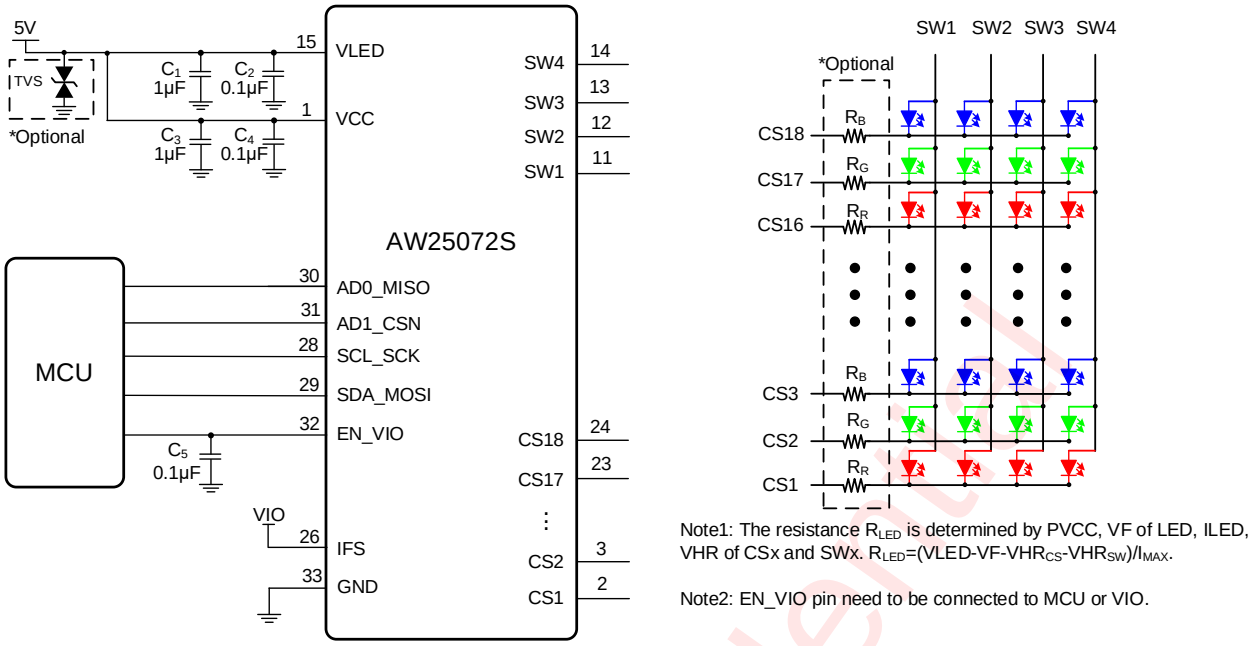
Typical Application



Note1: The resistance R_{LED} is determined by PVCC, VF of LED, ILED, VHR of CSx and SWx. $R_{LED}=(VLED-VF-VHR_{CS}-VHR_{SW})/I_{MAX}$.

Note2: EN_VIO pin need to be connected to MCU or VIO.

Figure 31 Application Circuit through I²C interface



Note1: The resistance R_{LED} is determined by PVCC, VF of LED, ILED, VHR of CSx and SWx. R_{LED}=(VLED-VF-VHR_{CS}-VHR_{SW})/I_{MAX}.

Note2: EN_VIO pin need to be connected to MCU or VIO.

Figure 32 Application Circuit through SPI interface

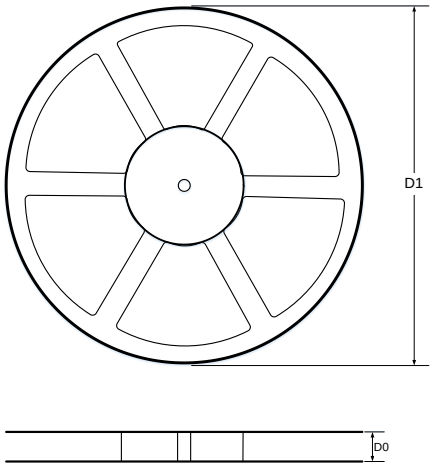
PCB Layout Consideration

1. Power decoupling capacitors (C1, C2, C3, C4) should be placed close to the corresponding pins of the chip, and small-sized high-frequency filtering capacitors are closer to the pins than large-sized low-frequency filtering capacitors;

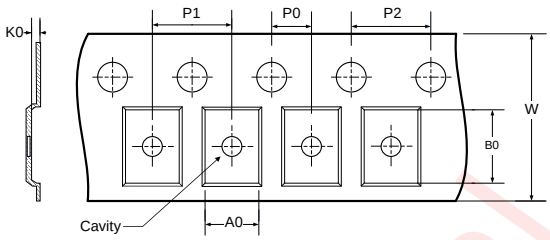
2. SWx wiring should be as thick and short as possible to reduce parasitic inductance, which can effectively suppress the overshoot phenomenon on LED current

Tape And Reel Information

REEL DIMENSIONS

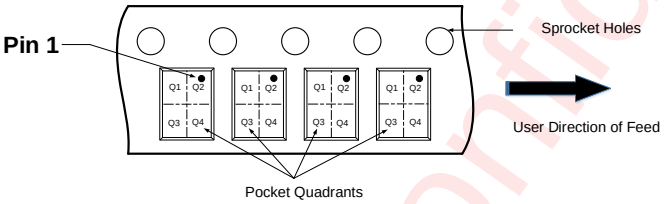


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



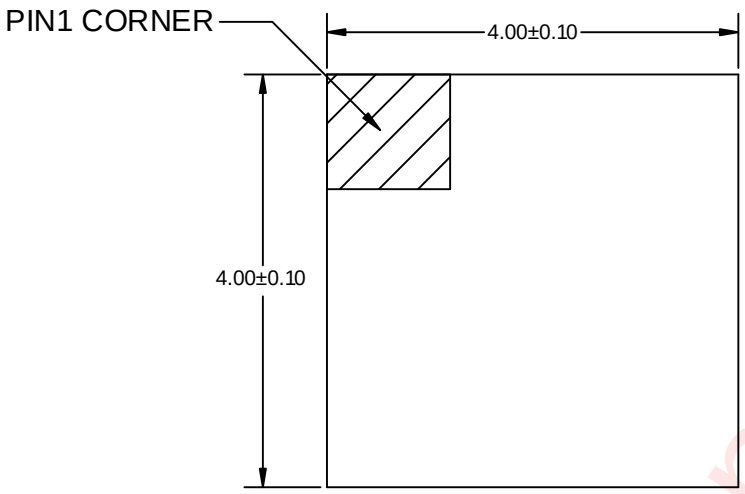
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

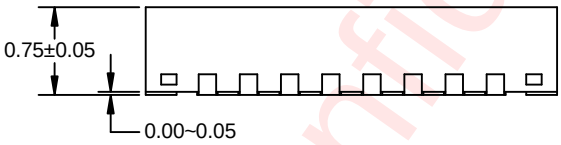
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.0	12.40	4.30	4.30	1.10	2.00	8.00	4.00	12.00	Q2

All dimensions are nominal

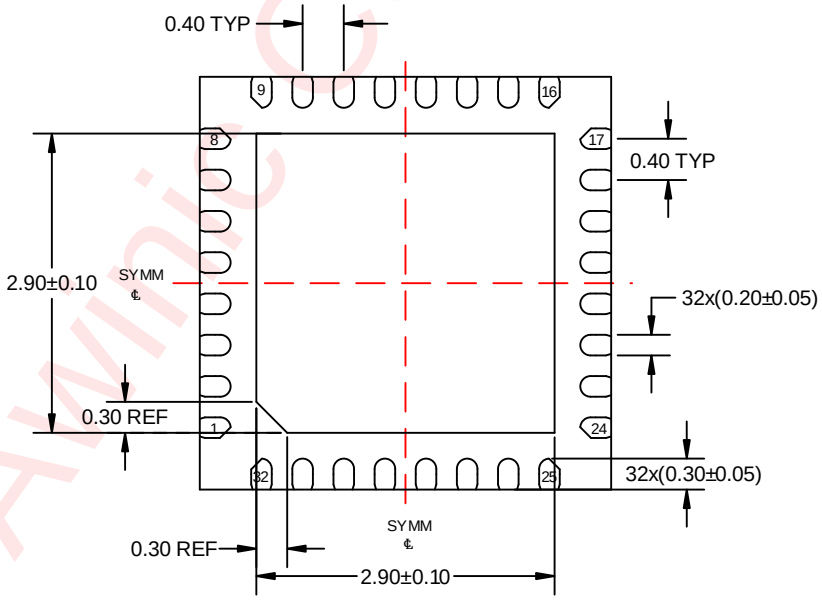
Package Description



TOP VIEW



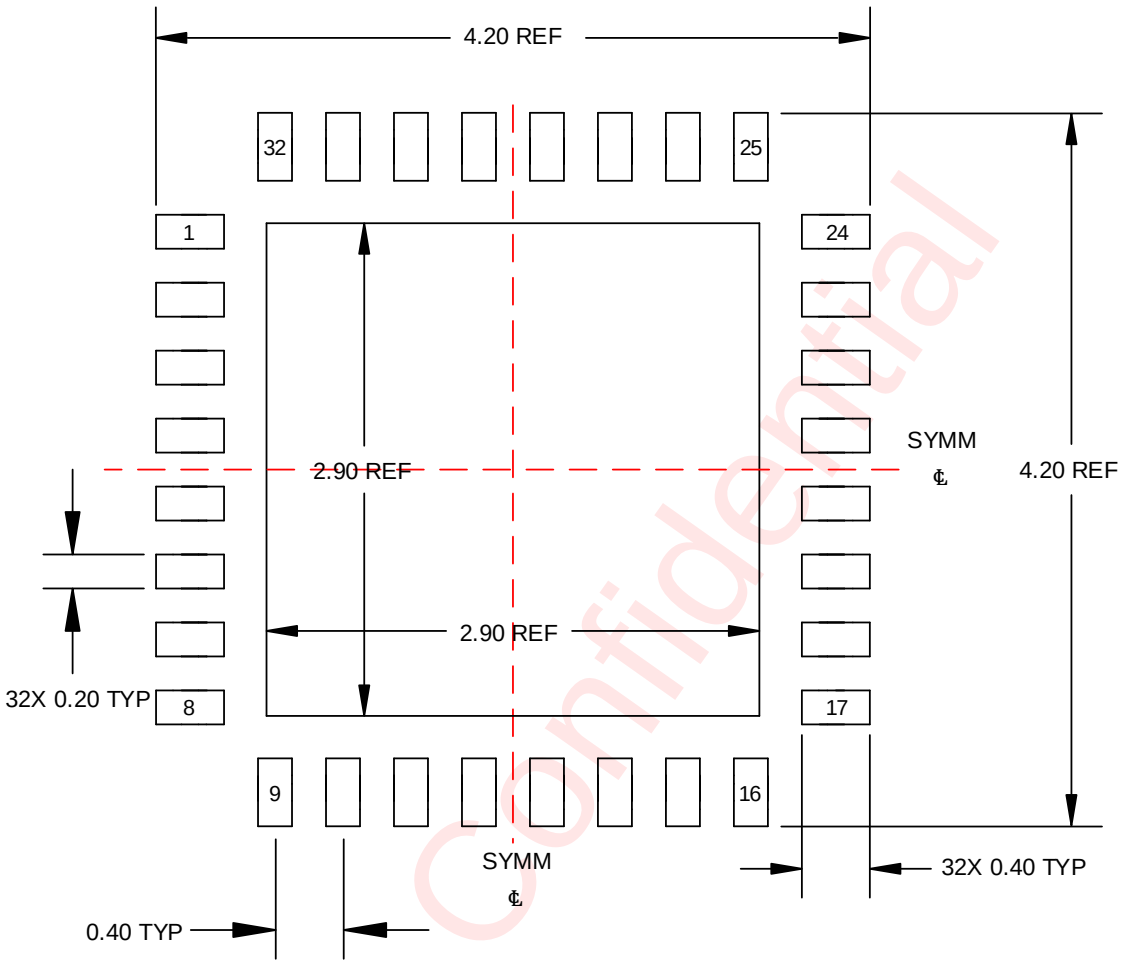
SIDE VIEW

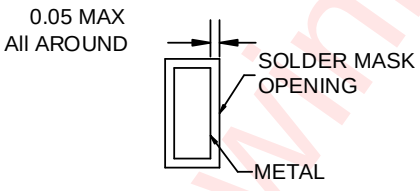


BOTTOM VIEW

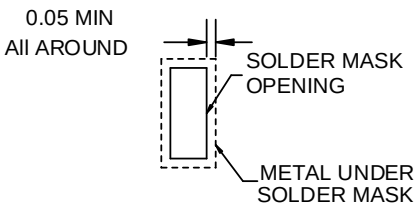
Unit：mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun 2025	Officially released
V1.1	Jun. 2025	Modify device address(P19-20)
V1.2	Jul. 2025	1.Modify spi soft reset process (P19) 2.Modify register list (P26) 3.Modify register detailed description (P29)
V1.3	Aug.2025	1.Modify the minimum value of the EN_VIO VIH parameter (P7) 2.Modify IF0 and IF1 to IFS (P7) 3.Modify register detailed description (P27)
V1.4	Sep.2025	1.Add Auto-Breath-Pattern (P14) 2.Modify register list (P28) 3.Modify register detailed description (P29)
V1.5	Sep.2025	1.Update the formula for AUTONOMOUS BREATHING MODE parameters T0 and T2 (P15)

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

