

## Description

The IDT XA devices are ultra-precision crystal oscillators with 750 to 890fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the XA series crystal oscillators utilize a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XA devices are an excellent choice over the conventional technologies. The XA devices have stabilities as tight as  $\pm 25$ ppm with extremely quick delivery for both standard and custom frequencies.

## Pin Assignments

**NOTE:** To minimize power supply line noise, a 0.01 $\mu$ F bypass capacitor should be placed between  $V_{DD}$  (Pin 6) and GND (Pin 3) on 6-pin devices, or  $V_{DD}$  (Pin 4) and GND (Pin 2) on 4-pin devices.

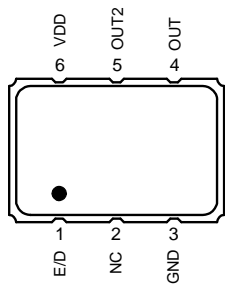


Table 1. 6-pin Package

Pin #	Pin Name	Description
1	E/D	Enable/Disable [a,b]
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output
6	$V_{DD}$	Supply voltage

## Features

- Conforms to AEC-Q200
- Frequency range: 0.750MHz to 1350MHz
- Output types: LVDS, LVPECL, LVCMOS
- Frequency stability:  $\pm 25$ ,  $\pm 50$ , or  $\pm 100$  ppm
- Supply voltage: 2.5V or 3.3V
- Phase jitter (12kHz to 20MHz): 750fs to 890fs typical
- Package options:
  - 3.2 × 2.5 × 1.0 mm
  - 5.0 × 3.2 × 1.2 mm
- Operating temperature: -40°C to +85°C (Grade 3)
  - Frequency stability options:  $\pm 25$ ,  $\pm 50$ , or  $\pm 100$  ppm
- Operating temperature: -40°C to +105°C (Grade 2)
  - Frequency stability options:  $\pm 50$  or  $\pm 100$  ppm

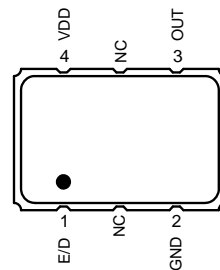


Table 2. 4-pin Package

Pin #	Pin Name	Description
1	E/D	Enable/Disable [a,b]
2	GND	Connect to ground
3	OUT	Output
4	$V_{DD}$	Supply voltage

[a] Pulled high internally.  
 [b] Low = output disabled.

See [Ordering Information](#) for more details.

---

## Contents

Description .....	1
Features .....	1
Pin Assignments .....	1
Absolute Maximum Ratings .....	3
ESD Compliance .....	3
Mechanical Testing .....	3
Solder Reflow Profile .....	3
DC Electrical Characteristics .....	4
AC Electrical Characteristics .....	6
Output Waveforms – LVDS .....	9
Output Waveforms – LVPECL .....	9
Output Waveforms – LVCMOS .....	10
Package Outline Drawings .....	10
Ordering Information .....	11
Revision History .....	12

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings

Item	Rating			
$V_{DD}$	-0.5 to +5.0V			
E/D	-0.5V to $V_{DD} + 0.5V$			
OUT	-0.5V to $V_{DD} + 0.5V$			
Storage Temperature	-55°C to 125°C			
Maximum Junction Temperature	125°C			
Core Current	65mA maximum			
Theta $J_A$	JS6	89.6 °C/W	JX6	94.7 °C/W
Theta $J_B$	5.0 × 3.2 × 1.2 mm	54.3 °C/W	3.2 × 2.5 × 1.0 mm	66.8 °C/W

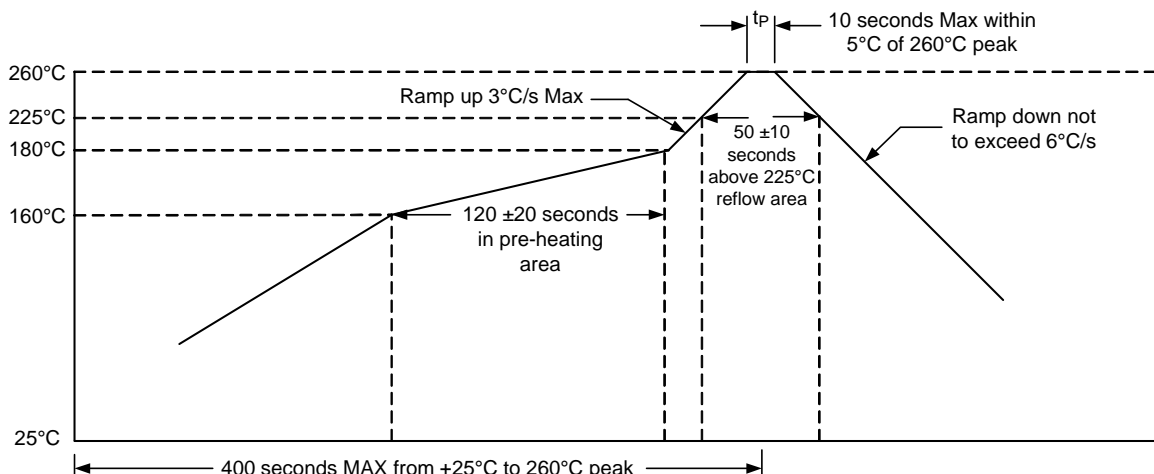
## ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

## Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface—3 times.
Mechanical Vibration	10–55Hz, 1.5mm amplitude, 1 minute sweep; 2 hours each in 3 directions (X, Y, Z).
High Temperature Burn-in	Under power at 125°C for 2000 hours.
Hermetic Seal	He pressure: $4 \pm 1 \text{ kgf/cm}^2$ 2 hour soak.

## Solder Reflow Profile



## DC Electrical Characteristics

Table 4. 3.3V IDD DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
$I_{DD}$	Power Supply Current	LVDS	—	—	—	100	mA
		LVPECL	—	—	—	120	
		LVCMOS	0.75MHz to 20MHz.	—	—	32	
			20+MHz to 50MHz.	—	—	35	
			50+MHz to 130MHz.	—	—	47	
			130+MHz to 200MHz.	—	—	55	
200+MHz to 250MHz.	—	—	60				

Table 5. 2.5V IDD DC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
$I_{DD}$	Power Supply Current	LVDS	0.75MHz to 20MHz.	—	—	26	mA
			20+MHz to 220MHz.	—	—	34	
			220+MHz to 630MHz.	—	—	44	
			630+MHz to 1000MHz.	—	—	65	
		LVPECL	0.75MHz to 20MHz.	—	—	33	
			20+MHz to 220MHz.	—	—	41	
			220+MHz to 630MHz.	—	—	63	
			630+MHz to 1000MHz.	—	—	72	
		LVCMOS	0.75MHz to 20MHz.	—	—	22	
			20+MHz to 50MHz.	—	—	25	
			50+MHz to 100MHz.	—	—	29	
			100+MHz to 130MHz.	—	—	32	
			130+MHz to 160MHz.	—	—	35	
			160+MHz to 180MHz.	—	—	37	

Table 6. LVDS DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C, -40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage	$V_{DD} = 3.3V \pm 5\%$ .	—	—	0.6	V
		$V_{DD} = 2.5V \pm 5\%$ .	—	—	0.4	
$V_{OS}$	Output Offset Voltage	$V_{DD} = 3.3V \pm 5\%$ .	—	—	1.3	
		$V_{DD} = 2.5V \pm 5\%$ .	—	—	1.25	
$V_{IH}$	Enable/Disable Input High Voltage (Output enabled)	—	$70\% V_{DD}$	—	—	
$V_{IL}$	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	$30\% V_{DD}$	

Table 7. LVPECL DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C, -40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage	$V_{DD} = 3.3V \pm 5\%$ .	2.055	—	2.405	V
		$V_{DD} = 2.5V \pm 5\%$ .	—	1.4	—	
$V_{OS}$	Output Offset Voltage	$V_{DD} = 3.3V \pm 5\%$ .	1.305	—	1.65	
		$V_{DD} = 2.5V \pm 5\%$ .	—	0.68	—	
$V_{IH}$	Enable/Disable Input High Voltage (Output enabled)	—	$70\% V_{DD}$	—	—	
$V_{IL}$	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	$30\% V_{DD}$	

Table 8. LVCMOS DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C, -40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage	$V_{DD} = 3.3V \pm 5\%$ .	0.75MHz to 150MHz.	$90\% V_{DD}$	—	—	V
			150+MHz to 250MHz.	$80\% V_{DD}$	—	—	
		$V_{DD} = 2.5V \pm 5\%$ .	0.75MHz to 160MHz.	$90\% V_{DD}$	—	—	
			160+MHz to 180MHz.	$80\% V_{DD}$	—	—	
$V_{OL}$	Output Low Voltage	$V_{DD} = 3.3V \pm 5\%$ .	0.75MHz to 150MHz.	—	—	$10\% V_{DD}$	
			150+MHz to 250MHz.	—	—	$20\% V_{DD}$	
		$V_{DD} = 2.5V \pm 5\%$ .	0.75MHz to 160MHz.	—	—	$10\% V_{DD}$	
			160+MHz to 180MHz.	—	—	$20\% V_{DD}$	
$V_{IH}$	Enable/Disable Input High Voltage (Output enabled)	—	—	$70\% V_{DD}$	—	—	
$V_{IL}$	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	—	$30\% V_{DD}$	

## AC Electrical Characteristics

Table 9. 3.3V AC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.75	—	1350	MHz
		LVPECL.		0.75	—	1350	
		LVCMOS.		0.75	—	250	
	Frequency Stability	Temperature = $-40^\circ C$ to $+85^\circ C$ .		$\pm 25$	—	$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+105^\circ C$ .		$\pm 50$	—	$\pm 100$	ppm
	Aging (1st year)	$T_A = 25^\circ C$ .		—	—	$\pm 3$	ppm
	Aging (10 years)	$T_A = 25^\circ C$ .		—	—	$\pm 10$	ppm
	Output Load	LVDS.	Differential.	—	100	—	$\Omega$
		LVPECL.	$V_{DD} - 2.0V$ .	—	50	—	
		LVCMOS.	To GND.	—	15	—	pF
$T_{ST}$	Start-up Time	Output valid time after $V_{DD}$ meets minimum specified level.		—	—	10	ms
$t_R$	Output Rise Time	LVDS.	20% to 80% $V_{pp}$ .	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	10% to 90% $V_{DD}$ .	—	—	3	ns
$t_F$	Output Fall Time	LVDS.	80% to 20% $V_{pp}$ .	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	90% to 10% $V_{DD}$ .	—	—	3	ns
$O_{DC}$	Output Clock Duty Cycle	LVDS.		45	—	55	%
		LVPECL.		45	—	55	
		LVCMOS.	$F_{OUT} \leq 62.5MHz$ .	45	—	55	
			$F_{OUT} \geq 62.5MHz$ .	40	—	60	
$T_{OE}$	Output Enable/ Disable Time	—		—	—	100	ns
$J_{PER}$	Period Jitter, RMS	LVDS.		—	3	—	ps
		LVPECL.		—	5.8	—	
		LVCMOS.	$F_{OUT} = 125MHz$ .	—	5	—	
$R_J$	Random Jitter	LVDS.		—	1.3	—	ps
		LVPECL.		—	1.29	—	
		LVCMOS.	$F_{OUT} = 125MHz$ .	—	0.6	—	
$D_J$	Deterministic Jitter	LVDS.		—	5.8	—	ps
		LVPECL.		—	9.3	—	
		LVCMOS.	$F_{OUT} = 125MHz$ .	—	10	—	

Table 9. 3.3V AC Electrical Characteristics (Cont.)

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
$T_J$	Total Jitter	LVDS.	—	23.6	—	ps
		LVPECL.	—	27.7	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	19	
$f_{JITTER}$	Phase Jitter (12kHz–20MHz)	LVDS.	—	890	—	fs
		LVPECL.	—	860	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	750	

Table 10. 2.5V AC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units	
F	Output Frequency Range	LVDS.	0.75	—	1000	MHz	
		LVPECL.	0.75	—	1000		
		LVC MOS.	0.75	—	180		
	Frequency Stability	Temperature = $-40^\circ C$ to $+85^\circ C$ .	$\pm 25$	—	$\pm 100$	ppm	
		Temperature = $-40^\circ C$ to $+105^\circ C$ .	$\pm 50$	—	$\pm 100$	ppm	
	Aging (1st year)	$T_A = 25^\circ C$ .	—	—	$\pm 3$	ppm	
	Aging (10 years)	$T_A = 25^\circ C$ .	—	—	$\pm 10$	ppm	
	Output Load	LVDS.	Differential.	—	100	$\Omega$	
		LVPECL.	$V_{DD} - 2.0V$ .	—	50		
		LVC MOS.	To GND.	—	15	$\mu F$	
$T_{ST}$	Start-up Time	Output valid time after $V_{DD}$ meets minimum specified level.	—	—	10	ms	
$t_R$	Output Rise Time	LVDS.	20% to 80% $V_{pp}$ .	—	—	400	ps
		LVPECL.		—	—	400	
		LVC MOS.	10% to 90% $V_{DD}$ .	—	—	3.5	ns
$t_F$	Output Fall Time	LVDS.	80% to 20% $V_{pp}$ .	—	—	400	ps
		LVPECL.		—	—	400	
		LVC MOS.	90% to 10% $V_{DD}$ .	—	—	3	ns
$O_{DC}$	Output Clock Duty Cycle	LVDS.	45	—	55	%	
		LVPECL.	45	—	55		
		LVC MOS.	45	—	55		
$T_{OE}$	Output Enable/ Disable Time	—	—	—	100	ns	

Table 10. 2.5V AC Electrical Characteristics (Cont.)

$V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

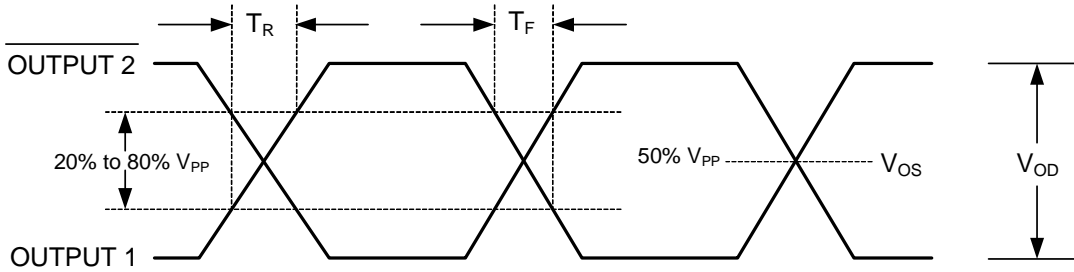
Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
$J_{PER}$	Period Jitter, RMS	LVDS.	—	4	—	ps
		LVPECL.	—	5.12	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	3.3	
$R_J$	Random Jitter	LVDS.	—	1.4	—	ps
		LVPECL.	—	1.36	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	1.3	
$D_J$	Deterministic Jitter	LVDS.	—	9.2	—	ps
		LVPECL.	—	10	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	6.7	
$T_J$	Total Jitter	LVDS.	—	29.2	—	ps
		LVPECL.	—	29.3	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	25.6	
$f_{JITTER}$	Phase Jitter (12kHz–20MHz)	LVDS.	—	1040	—	fs
		LVPECL.	—	1200	—	
		LVC MOS.	$F_{OUT} = 125MHz.$	—	850	

Notes for all AC Electrical Characteristics tables:

<sup>1</sup> All jitter values provided at 156.25MHz, unless noted otherwise.

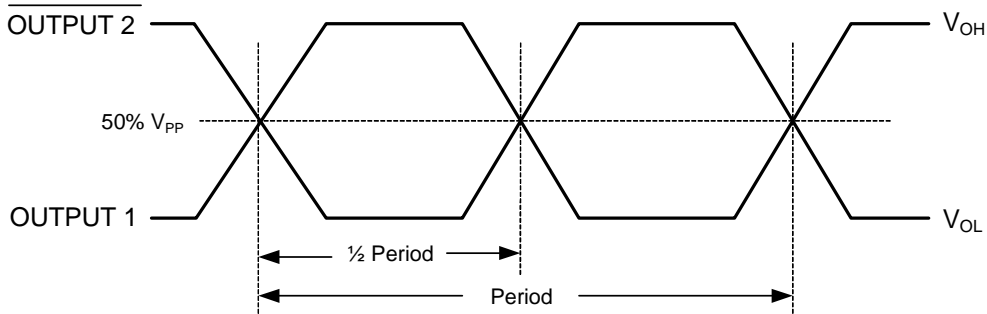
## Output Waveforms – LVDS

### Output Levels/Rise Time/Fall Time Measurements



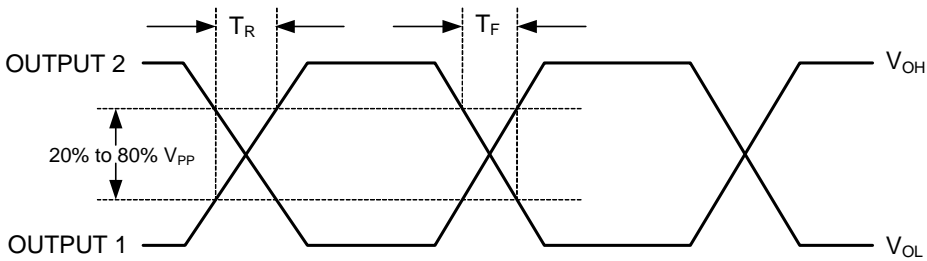
### Oscillator Symmetry

Ideally, Symmetry should be 50/50 for  $\frac{1}{2}$  period – Other expressions are 45/55 or 55/45

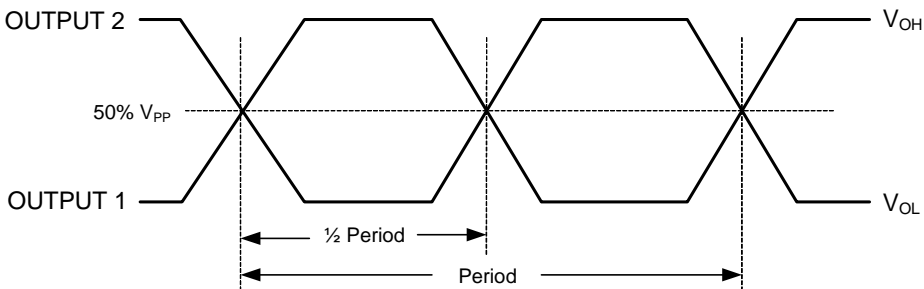


## Output Waveforms – LVPECL

### Rise Time/Fall Time Measurements

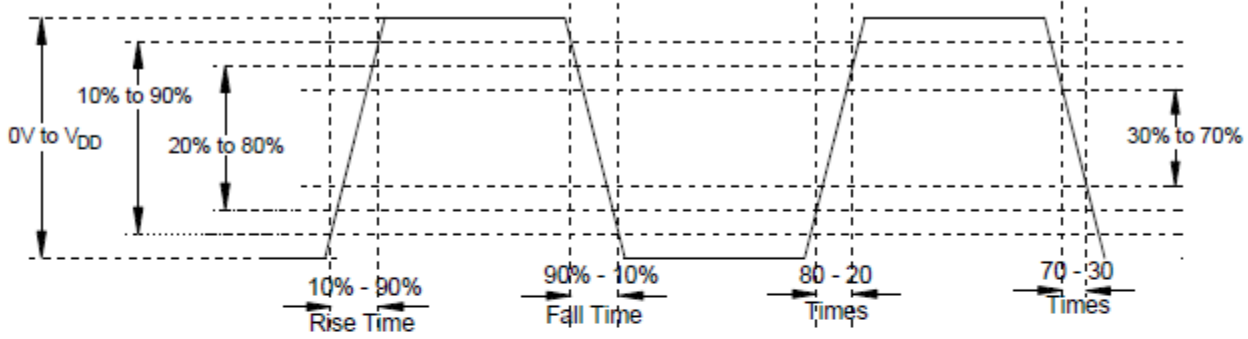


### Oscillator Symmetry

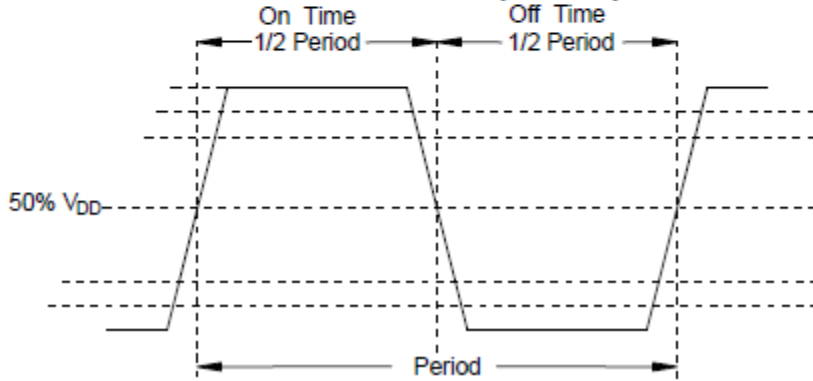


## Output Waveforms – LVCMOS

### Rise Time / Fall Time Measurements



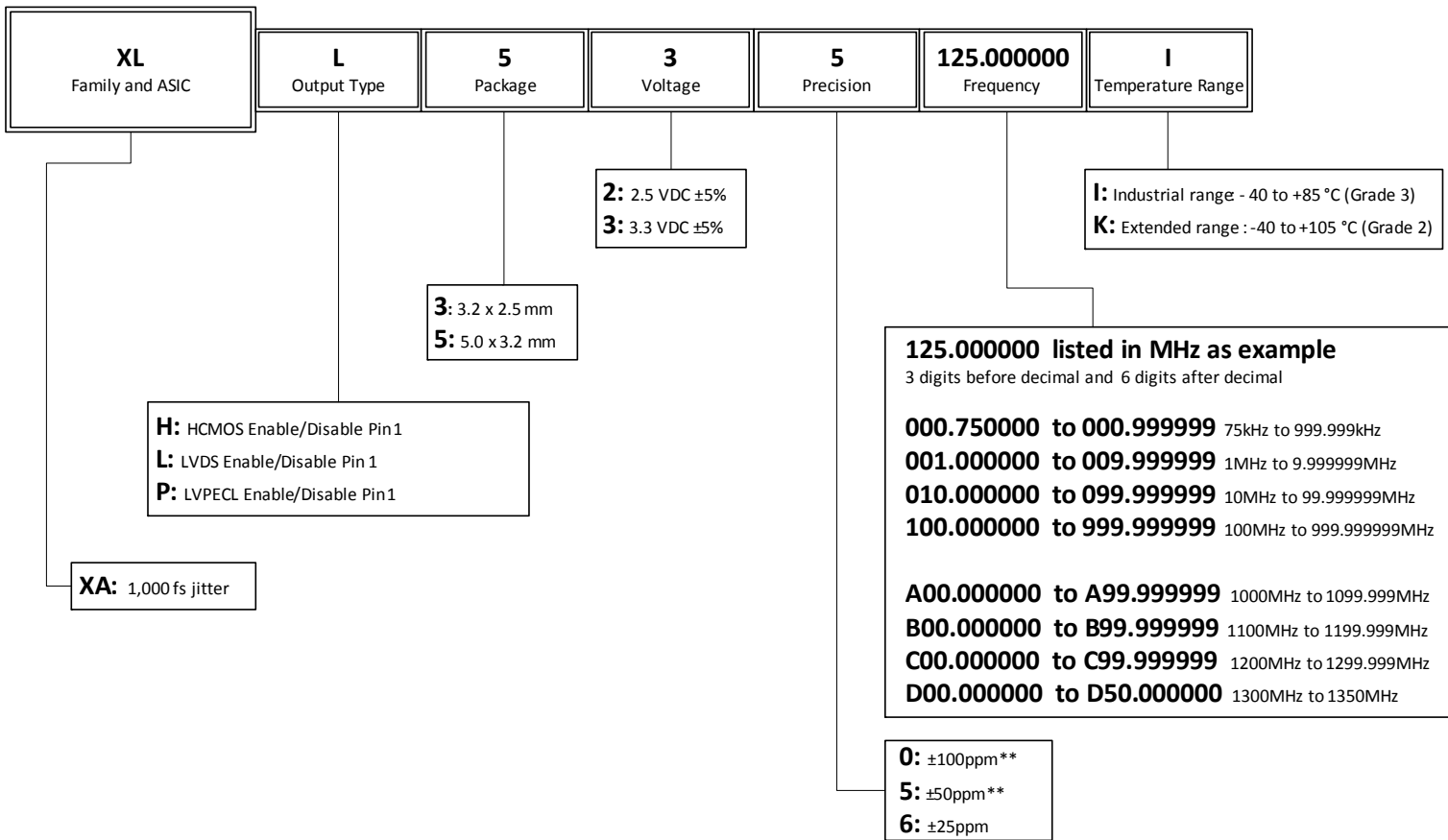
### Oscillator Symmetry



## Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available.

# Ordering Information

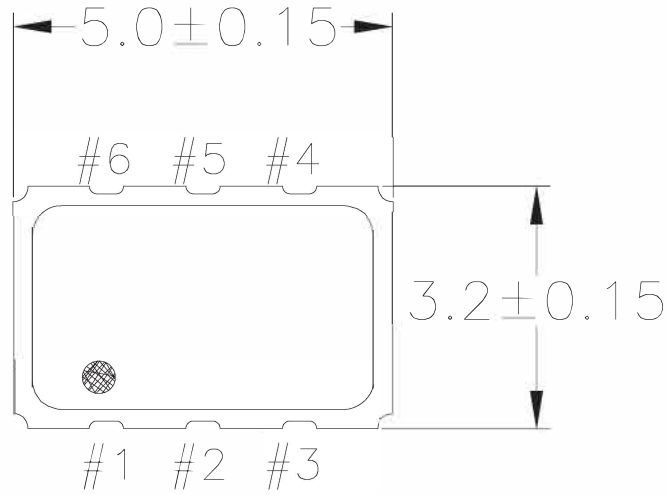


\*\* ±100ppm and ±50ppm for K (-40°C to +105°C) only.

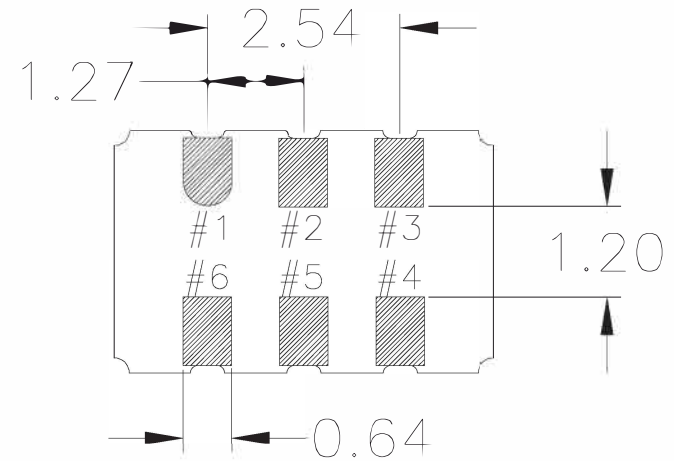
## Revision History

Revision Date	Description of Change
May 24, 2018	Updated LVCMOS Output Clock Duty Cycle, FOUT test condition.
April 27, 2018	Initial release.

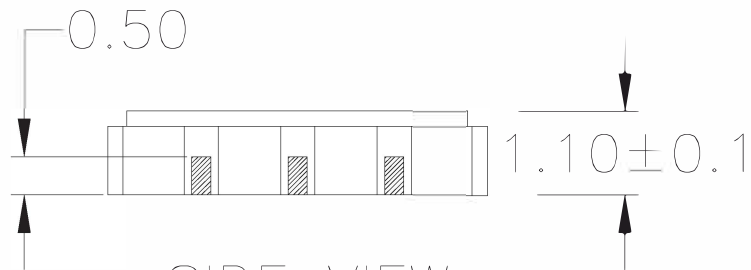
			DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



TOP VIEW




BOTTOM VIEW



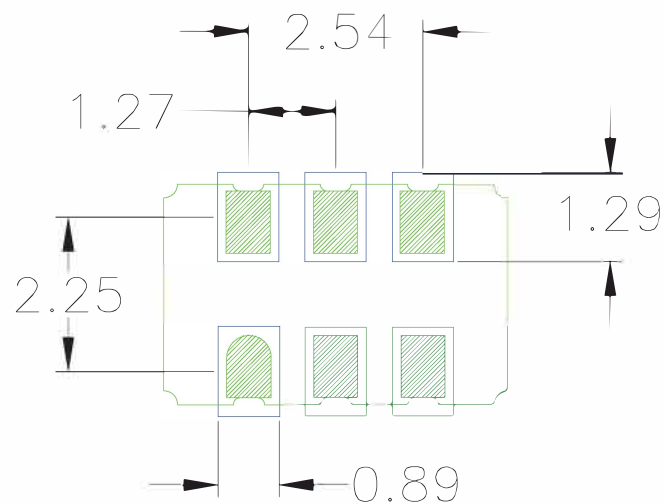
SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		 <b>www.IDT.com</b>	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL	ANGULAR			
XX±	±			
XXX±				
XXXX±				
APPROVALS	DATE	TITLE JS6 PACKAGE OUTLINE		
DRAWN <i>RLC</i>	04/2/12	5.0 x 3.2 mm BODY		
CHECKED		1.1 mm Thick		
		SIZE	DRAWING No.	REV
		C	PSC-4411	03
DO NOT SCALE DRAWING				SHEET 1 OF 2


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



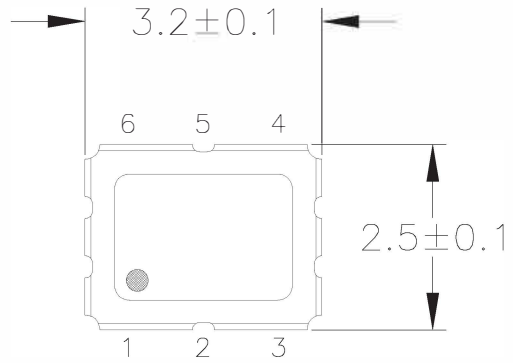
RECOMMENDED LAND PATTERN

NOTES:

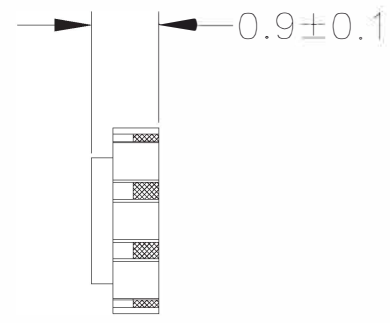
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>www.IDT.com</b> 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>RLC</i>	04/2/12	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
CHECKED		
	SIZE	DRAWING No.
	C	PSC-4411
		REV
		03
DO NOT SCALE DRAWING		SHEET 2 OF 2

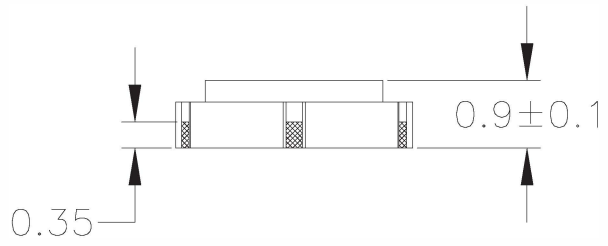
			HOR
00	INITIAL RELEASE	8/11/14	J.HUA
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



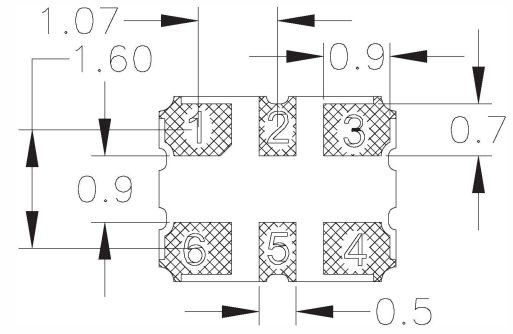
TOP VIEW



END VIEW




SIDE VIEW



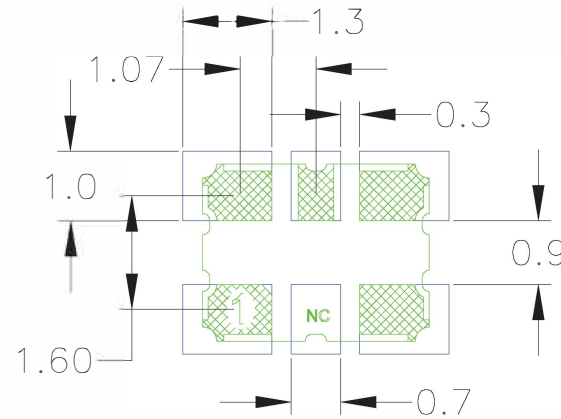
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 <a href="http://www.IDT.com">www.IDT.com</a>
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
TITLE		JX6 PACKAGE OUTLINE
		3.2 x 2.5 mm BODY
		0.9 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4412	01
DO NOT SCALE DRAWING		SHEET 1 OF 2


REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
00	INITIAL RELEASE	8/11/14	J.HUA
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



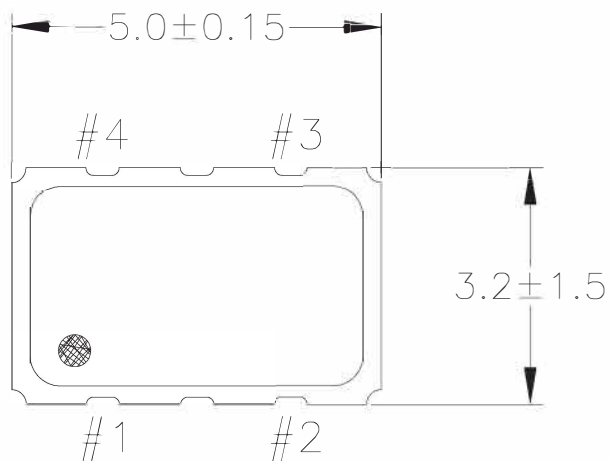
RECOMMENDED LAND PATTERN DIMENSION

NOTES:

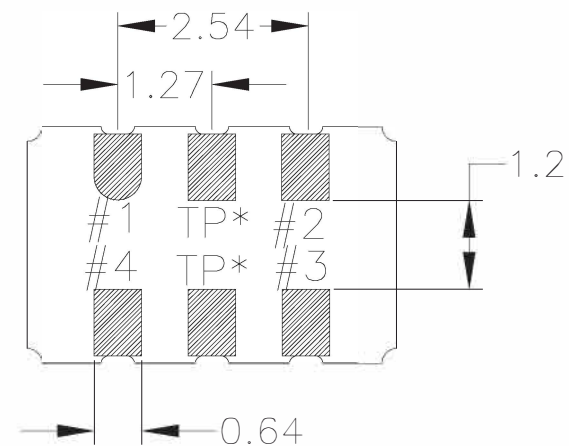
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		<a href="http://www.IDT.com">www.IDT.com</a>
TITLE		JX6 PACKAGE OUTLINE
		3.2 x 2.5 mm BODY
		0.9 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4412	01
DO NOT SCALE DRAWING		SHEET 2 OF 2

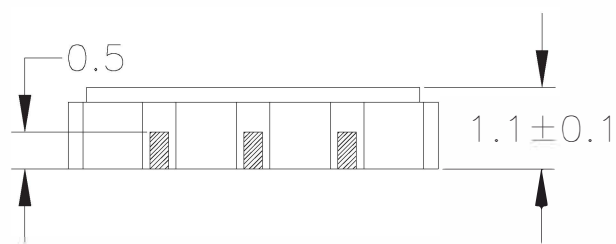
00	INITIAL RELEASE	08/21/12	K. Stahn
01	UPDATED LID TOLERANCES	12/03/12	K. Stahn
02	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



TOP VIEW




BOTTOM VIEW



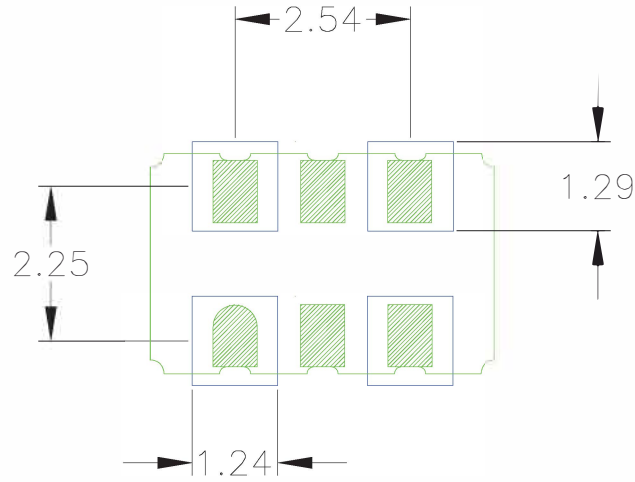
SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8116 FAX: (408) 492-8874 <a href="http://www.IDT.com">www.IDT.com</a>
DECIMAL	ANGULAR	
XX±	±	
XXX±		
APPROVALS	DATE	TITLE
DRAWN <i>JCS</i>	07/16/12	JS4 PACKAGE OUTLINE
CHECKED		5.0 x 3.2 mm BODY
		1.1 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4429	02
DO NOT SCALE DRAWING		SHEET 1 OF 2


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	08/21/12	K. Stahn
01	UPDATED LID TOLERANCES	12/03/12	K. Stahn
02	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



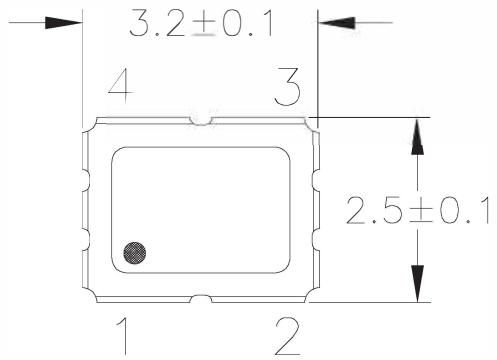
RECOMMENDED LAND PATTERN

NOTES:

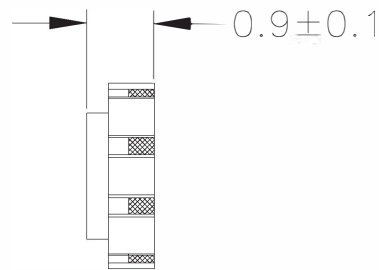
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>IDT™</b> 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8116 FAX: (408) 492-8874 <a href="http://www.IDT.com">www.IDT.com</a>		
DECIMAL	ANGULAR			
XX±	±			
XXX±				
APPROVALS	DATE	TITLE		
DRAWN <i>gcs</i>	07/18/12	JS4 PACKAGE OUTLINE		
CHECKED		5.0 x 3.2 mm BODY 1.1 mm Thick		
		SIZE	DRAWING No.	REV
		C	PSC-4429	02
DO NOT SCALE DRAWING			SHEET 2 OF 2	

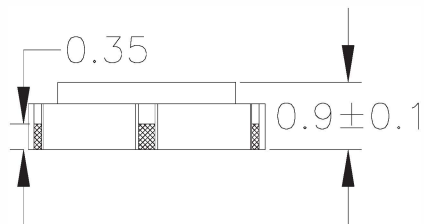
00	INITIAL RELEASE	8/8/14	J.HUA
01	ADD OPTION 1 & 2	4/2/15	J.HUA



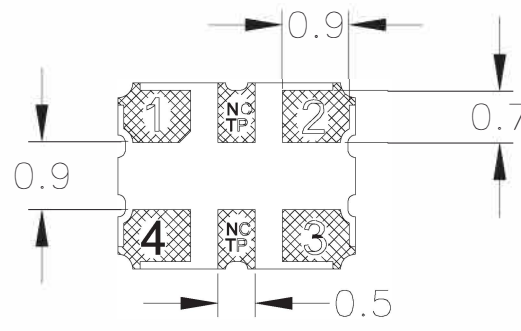
TOP VIEW



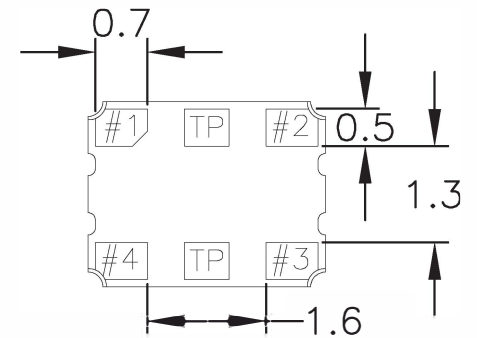
END VIEW



SIDE VIEW




OPTION 1  
BOTTOM VIEW



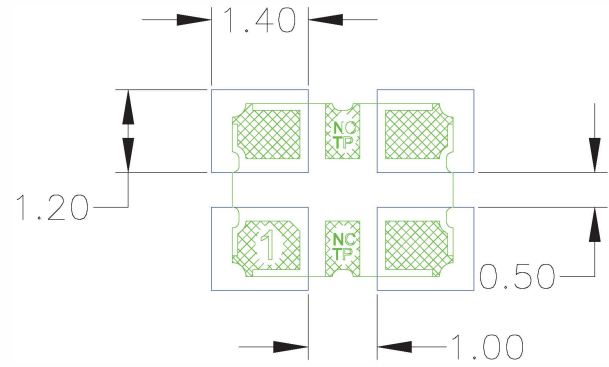
OPTION 2  
BOTTOM VIEW

NOTES:

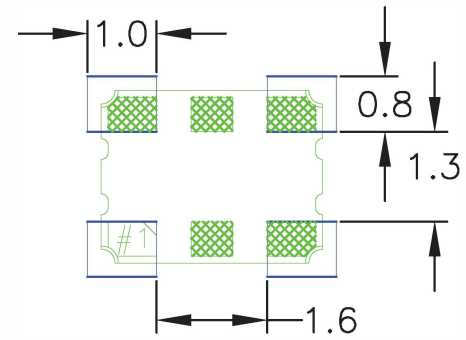
1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		 <b>www.IDT.com</b>	6024 Silver Creek Valley Rd. San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL	ANGULAR			
XX±	±			
XXX±				
XXXX±				
APPROVALS	DATE	TITLE JX4 PACKAGE OUTLINE		
DRAWN <i>BAC</i>	8/8/14	3.2 x 2.5 mm BODY		
CHECKED		0.9 mm Thick		
		SIZE	DRAWING No.	REV
		C	PSC-4489	01
DO NOT SCALE DRAWING			SHEET 1 OF 2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/8/14	J.HUA
01	ADD OPTION 1 & 2	4/2/15	J.HUA



OPTION 1



OPTION 2

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
  3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
    - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
    - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
  6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
  11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.