钍地半导体
Tudi Semiconductor

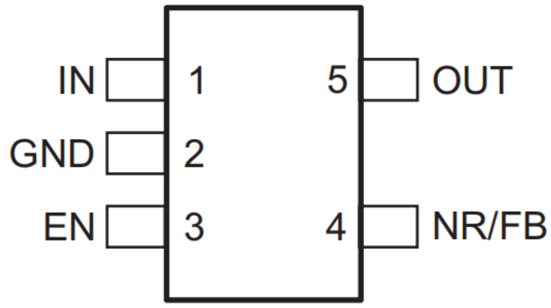
Product Specification

TUDI-TPS71733

Low-noise, high-bandwidth PSRR, low voltage drop, 150 mA linear regulator

Features

- ●Input voltage: 2.5V to 6.5V
- ● Multiple output versions available:
- - Fixed output voltage range:0.9V to 5V
- - Adjustable output voltage range: 0.9V to 6.2V
- ●Ultra-high PSRR:
- - 0dB at 1kHz, 67dB at 100kHz, 45dB at 1MHz
- ●Excellent load and line transient response
- ● Ultra dropout: 170mV (typical) at 150mA
- ●Low noise: 30μVRMS typical (100Hz to 100kHz)
- ●Compact 5-pin SC-70, 2mm×2mm WSON-6 (Wafer Level No-Lead Small Outline Package), and 1.mm×1.5mm WSON-6 packages



DCK Package
SC70-5
(Top View)

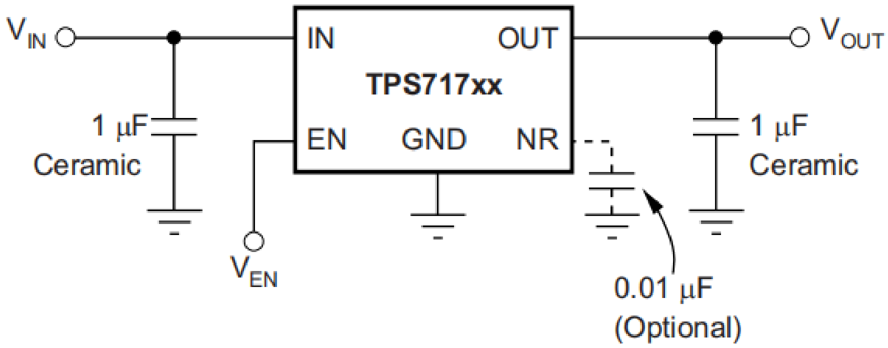
Applications

- ●Camera sensor power
- ●Mobile phone earphones
- ● Palmtop computers (PDA) and smartphones
- ●Wireless LAN, Bluetoot

Description

The TPS717xx series low-dropout (LDO), low-power linear regulators are housed in an ultra-small -pin Small Outline Transistor (SOT) package, featuring a very high power supply rejection ratio (PSRR) while maintaining an ultra-low 45μA ground. This series of regulators utilizes an advanced Bipolar CMOS (BiCMOS) process and Power Metal-Oxide-Semiconductor Field-Effect Transistor (PMOSFET) devices to achieve fast startup, ultra-low noise, excellent transient response, and outstanding PSRR performance. The TPS717xx devices remain stable when used with a 1F ceramic output capacitor, and employ a precise voltage reference and feedback loop to achieve at least 3 % accuracy across all load, line, process, and temperature variations. The device has a rated temperature range of TJ=-40°C to 125°C, and is available in a small SOT (SC70-5) package, 2mm x 2mm WSON-6 package with an exposed thermal pad, and a 1.5mm x 1.5mm WSON-6 package, it ideal for small-sized portable devices (such as wireless handheld devices and PDAs).

针对固定电压版本的典型应用电路



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DCK	DRV	DSE		
EN	3	4	4	I	Driving the enable pin (EN) above $V_{EN(high)}$ turns on the regulator. Driving this pin below $V_{EN(low)}$ puts the regulator into standby mode, thereby disabling the output and reducing operating current.
FB	4	2	3	I	Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation.
GND	2	3	2	—	Ground
IN	1	6	6	I	Input to the device. A 0.1-µF to 1-µF capacitor is recommended for better performance.
N/C	—	5	5	—	Not connected. This pin can be tied to ground to improve thermal dissipation.
NR	4	2	3	—	Fixed voltage versions only. The noise reduction capacitor filters the noise generated by the internal band gap, thus lowering output noise.
OUT	5	1	1	O	This pin is the regulated output voltage. A minimum capacitance of 1 µF is required for stability from this pin to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted), all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	7	V
	V_{FB}	–0.3	3.6	V
	V_{NR}	–0.3	3.6	V
	V_{EN}	–0.3	V_{IN} + 0.3 V(2)	V
	V_{OUT}	–0.3	7	V
Current	I_{OUT}	Internally limited		A
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Operating junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{EN} absolute maximum rating is V_{IN} + 0.3 V or 7 V, whichever is greater.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		6.5	V
V_{OUT}	Output voltage	0.9		5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		V_{IN}	V
C_{OUT}	Output capacitor	1		100	µF
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS717xx			UNIT
		DCK	DRV	DSE	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.2	71.1	190.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	96.5	94.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	74.1	40.5	149.3	
ψ_{JT}	Junction-to-top characterization parameter	0.8	2.7	6.4	
ψ_{JB}	Junction-to-board characterization parameter	73.1	40.9	152.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	10.7	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; I_{OUT} = 0.5 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, C_{NR} = 0.01 µF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8 V. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)				2.5		6.5	V
V_{FB}	Internal reference (TPS71701)				0.790	0.800	0.810	V
V_{OUT}	Output voltage range	(TPS717xx)			0.9		5.0	V
		(TPS71701)			0.9		6.5 – V_{DO}	V
V_{OUT}	Output accuracy	Nominal	T_J = 25°C			±2.5		mV
	Output accuracy (V_{OUT} < 1.0 V)	Over V_{IN}, I_{OUT}, Temp(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V 0 mA ≤ I_{OUT} ≤ 150 mA		–30		+30	mV
	Output accuracy (V_{OUT} ≥ 1.0 V)	Over V_{IN}, I_{OUT}, Temp(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.5 V 0 mA ≤ I_{OUT} ≤ 150 mA		–3.0%		+3.0%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (1)		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 6.5 V, I_{OUT} = 5 mA			125		µV/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA			70		µV/mA
V_{DO}	Dropout voltage(3) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 150 mA			170	300	mV
I_{LIM} (fixed)	Output current limit (fixed output)		V_{OUT} = 0.9 × $V_{OUT(nom)}$		200	325	575	mA
I_{LIM} (adjustable)	Output current limit (TPS71701)		V_{OUT} = 0.9 × $V_{OUT(nom)}$		200	325	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0.1 mA			45	80	µA
			I_{OUT} = 150 mA			100		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, T_J = –40°C to 85°C	2.5 V ≤ V_{IN} < 4.5 V		0.20	1.5	µA
				4.5 V ≤ V_{IN} ≤ 6.5 V		0.90		µA
I_{FB}	Feedback pin current (TPS71701)					0.02	1.0	µA
PSRR	Power-supply rejection ratio		V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 150 mA	f = 100 Hz		70		dB
				f = 1 kHz		70		dB
				f = 10 kHz		67		dB
				f = 100 kHz		67		dB
				f = 1 MHz		45		dB
V_n	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 10 mA	C_{NR} = none		95 × V_{OUT}		$µV_{RMS}$
				C_{NR} = 0.001 µF		25 × V_{OUT}		$µV_{RMS}$
				C_{NR} = 0.01 µF		12.5 × V_{OUT}		$µV_{RMS}$
				C_{NR} = 0.1 µF		11.5 × V_{OUT}		$µV_{RMS}$
t_{STR}	Startup time		V_{OUT} = 90% $V_{OUT(nom)}$, R_L = 19 Ω, C_{OUT} = 1 µF	0.9 V ≤ V_{OUT} ≤ 1.6V, C_{NR} = 0.001 µF		0.700		ms
				1.6 V < V_{OUT} < V_{MAX}, C_{NR} = 0.01 µF		0.160		ms
$V_{EN(high)}$	Enable high (enabled)		V_{IN} ≤ 5.5 V		1.2		6.5(4)	V
			5.5 V < V_{IN} ≤ 6.5 V		1.25		6.5	V
$V_{EN(low)}$	Enable low (shutdown)				0		0.4	V
$I_{EN(high)}$	Enable pin current, enabled		EN = 6.5 V			0.02	1.0	µA
UVLO	Undervoltage lockout		V_{IN} rising		2.41	2.45	2.49	V
	Hysteresis		V_{IN} falling			150		mV
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		°C
T_J	Operating junction temperature				–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.5 V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) V_{DO} is not measured for devices with $V_{OUT(nom)}$ < 2.6 V because the minimum V_{IN} is 2.5 V.
(4) Maximum $V_{EN(high)}$ = V_{IN} + 0.3 or 6.5 V, whichever is smaller.

7 Detailed Description

7.1 Overview

The TPS717xx family of low-dropout (LDO) regulators combines the high performance required by many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection with very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS717xx family of devices an excellent choice for battery-powered applications. All versions have thermal and overcurrent protection.

7.2 Functional Block Diagrams

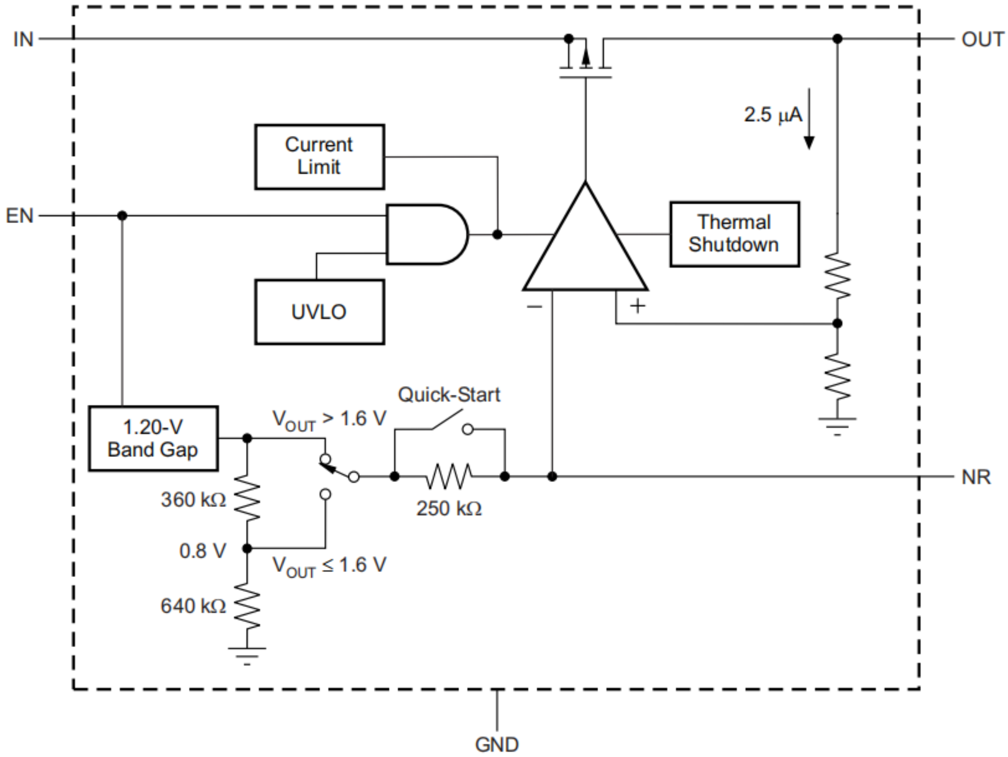


Figure 31. Fixed Voltage Versions

Functional Block Diagrams (continued)

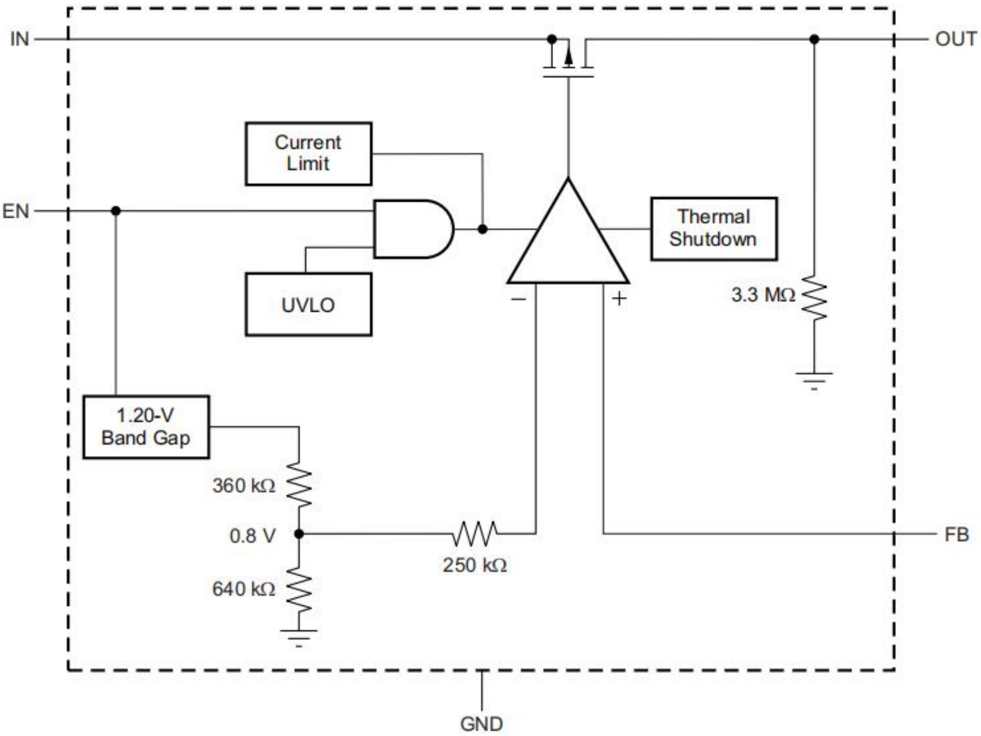


Figure 32. Adjustable Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS717xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS717xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS717xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see Figure 31). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low-leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, apply V_{IN} first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to Figure 29 in *Typical Characteristics*. The quick-start switch is closed for approximately 135 μs. To ensure that C_{NR} is fully charged during the quick-start time, use a 0.01-μF or smaller capacitor.

Feature Description (continued)

For output voltages below 1.6 V, a voltage divider on the band-gap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor (C_{NR}) results in slower start-up times for output voltages below 1.6 V.

Equation 1 approximates the start-up time as a function of C_{NR} for output voltages below 1.6 V:

$$t_{START} = 160\mu s + (540\frac{\mu s}{nF} \times C_{NR} nF)\mu s \quad (1)$$

7.3.4 Undervoltage Lockout (UVLO)

The TPS717xx uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a limited glitch immunity so undershoot transients are typically ignored on the input if these transients are less than 5 μs in duration.

7.3.5 Minimum Load

The TPS717xx is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717xx employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717xx is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS717xx into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

Device Functional Modes (continued)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and V_{IN} > UVLO	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	UVLO < $V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	V_{IN} < UVLO – V_{hys}	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$

8.3 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible in the range of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not place any components in the feedback loop except for the output capacitor and feedback resistors.

Do not exceed the device absolute maximum ratings.

Do not float the enable (EN) pin.

9 Power Supply Recommendations

The TPS717xx is designed to operate from an input voltage between 2.5 V and 6.5 V. The input supply must provide adequate headroom for the device to operate in a normal mode of operation.

Connect a low output impedance power supply directly to the IN pin of the TPS717xx. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor. To increase the overall PSRR of the power solution, use a pi-filter before the input of the LDO or after the FB network of the LDO.

8.1 Application Information

The TPS717xx belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for automotive applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to 125°C.

8.1.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases duration of the transient. The TPS717xx has an ultra-wide loop bandwidth that allows it to respond quickly to load transient events. As with any regulator, the loop bandwidth is finite and the initial transient voltage peak is controlled by the sizing of the output capacitor. Typically, larger output capacitors reduce the peak while also reducing the bandwidth of the LDO, slowing the response time.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF or larger low equivalent series resistance (ESR) capacitor from IN to GND near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS717xx is designed to be stable with ceramic output capacitors of values 1 μF or larger. The X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. The maximum ESR of the output capacitor must be less than 1 Ω.

8.1.3 Dropout Voltage

The TPS717xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DSon} of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 15 through Figure 17 in *Typical Characteristics*.

Application Information (continued)

8.1.4 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS717xx, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5 µA of divider current has the same noise performance as a fixed voltage version.

Equation 2 approximates the total noise referred to the feedback point (FB pin) when C_{NR} = 0.01 µF:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \quad (2)$$

8.2 Typical Applications

8.2.1 Application for Fixed Voltage Versions and Adjustable Voltage Version

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701). **Note that the NR pin is not available on the adjustable version.**

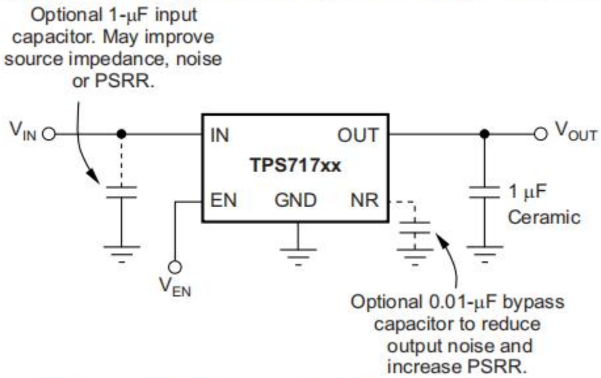


Figure 33. Typical Application Circuit (Fixed Voltage Versions)

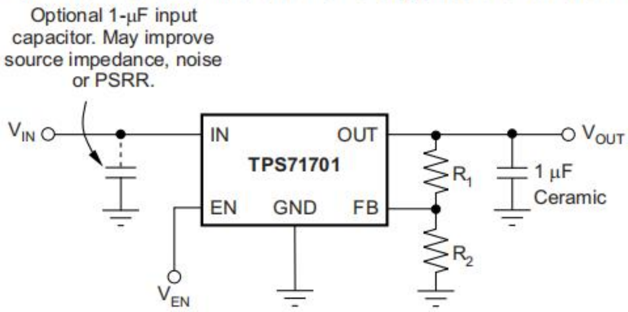


Figure 34. Typical Application Circuit (Adjustable Voltage Version)

8.2.1.1 Design Requirements

Table 2 summarizes the design requirements for Figure 36.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V, ±10%
Output voltage	2.8 V, ±5%
Output current	100 mA typical, 150 mA peak
Output voltage transient deviation	5%
Maximum ambient temperature	85°C

8.2.1.2 Detailed Design Procedure

For the adjustable version (TPS71701), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 3:

$$R_1 = R_2 * (V_{OUT} / V_{REF} - 1) \quad (3)$$

The value of R_2 directly impacts the operation of the device and must be chosen in the range of approximately 160 kΩ to 320 kΩ. Sample resistor values for common output voltages are shown in Table 3.

Table 3. Sample 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1	80.6 kΩ	324 kΩ
1.2	162 kΩ	324 kΩ
1.5	294 kΩ	332 kΩ
1.8	402 kΩ	324 kΩ
2.5	665 kΩ	316 kΩ
3.3	1.02 MΩ	324 kΩ
5	1.74 MΩ	332 kΩ

8.2.1.3 Application Curve

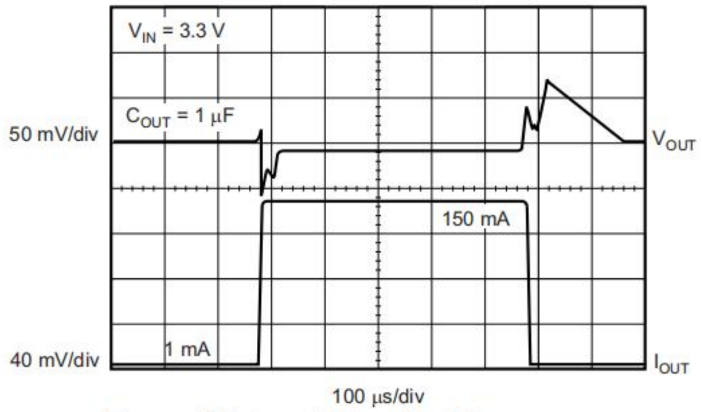


Figure 35. Load Transient Response

8.2.2 Powering a PLL Integrated on an SOC

Figure 36 shows the TPS71701 powering a phase-locked loop (PLL) that is integrated into a system-on-a-chip (SOC).

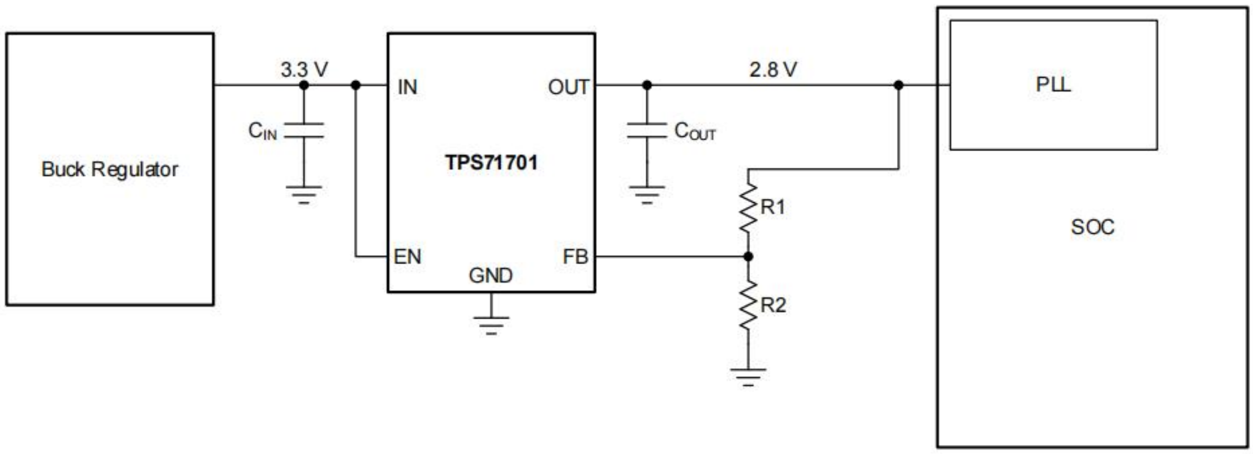


Figure 36. Typical Application Circuit: PLL on an SOC

Use the input and output capacitors to ensure the voltage transient requirements. A 1-µF input and 1-µF output capacitor are selected to maximize the capacitance and minimize capacitor size.

R_2 is chosen to be 158 kΩ for optimal noise and PSRR, and by Equation 4, R_1 is selected to be 402 kΩ. Both R_1 and R_2 must be 1% tolerance resistors to meet the dc accuracy specification over line, load, and temperature.

10 Layout

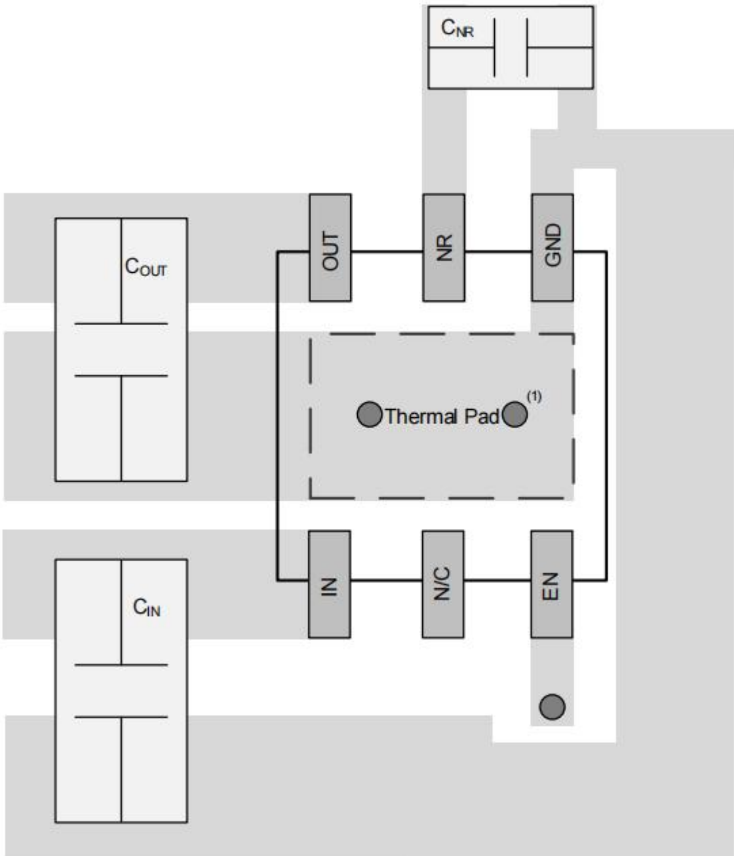
10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to the GND pin as possible, connected by wide, component-side, copper surface area. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and functions similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

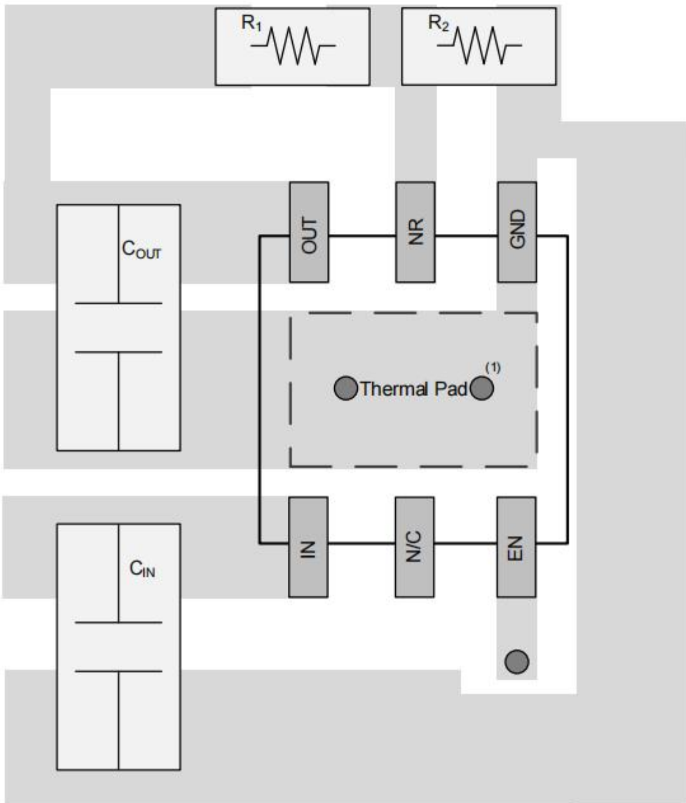
10.2 Layout Example



(1) Circles within thermal pad area indicate vias to other layers on the board, for electrical connections or thermal conduction.

Figure 37. Fixed Voltage Layout

Layout Example (continued)



(1) Circles within thermal pad area indicate vias to other layers on the board, for electrical connections or thermal conduction.

Figure 38. Adjustable Voltage Layout

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 5.

$$\Psi_{JT}:\ T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}:\ T_J = T_B + \Psi_{JB} \bullet P_D$$

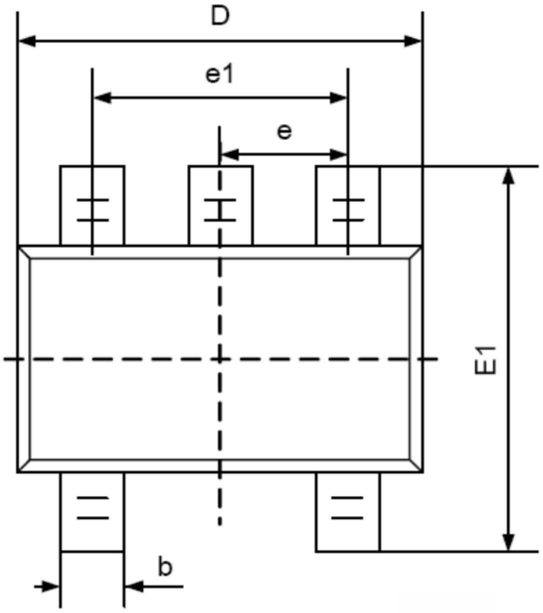
where

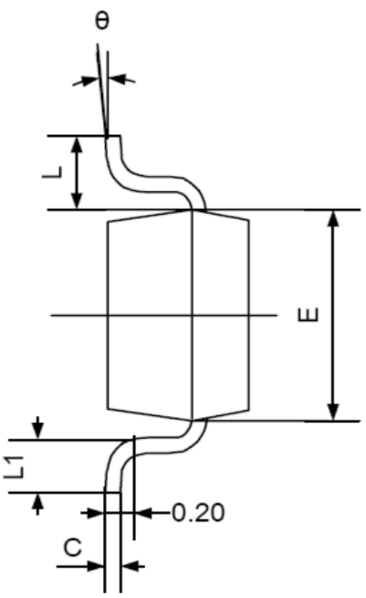
- P_D is the power dissipation shown by Equation 4,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (5)

Order information

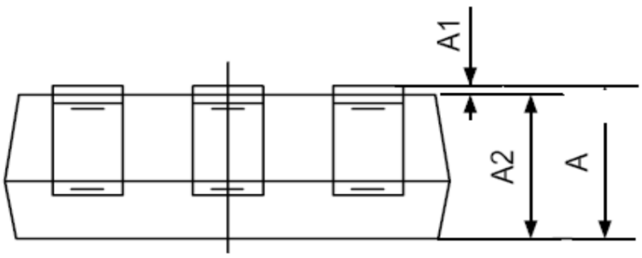
Order Number	Package	Package Quantity	Marking On The park
TPS71733DCKR-TUDI	SC70	Tape,Reel,3000	TPS71733DCKR
TPS71733DCKT-TUDI	SC70	Tape,Reel,3000	TPS71733DCKT

Package SC70-5





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°



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