钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65ALS176

差分总线收发器

网址 www.sztdbdt.com

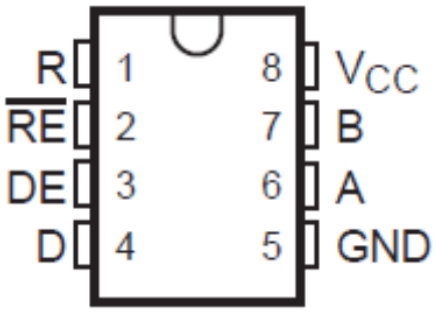
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

特性

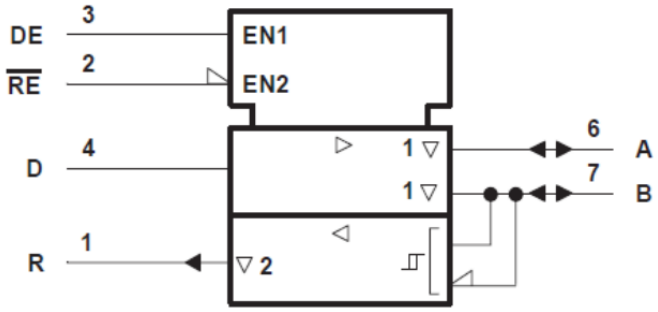
● 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 的要求 1 以及 ITU 建议 V.11 和 X.27
●在高达 35Mbaud 的数据速率下运行
●提供四个偏差限制：
– SN65ALS176：15ns
– SN75ALS176：10ns
– SN75ALS176A：7.5ns
– SN75ALS176B：5ns
●适用于嘈杂环境中长距离总线线路上的多点传输
●低电源电流要求：30mA（最大值）
● 宽正负输入/输出总线电压范围
● 热关断保护
●驱动器正负电流限制
●接收器输入迟滞
●无干扰上电和断电保护
● 接收器开路失效防护设计



D or P Package (Top View)

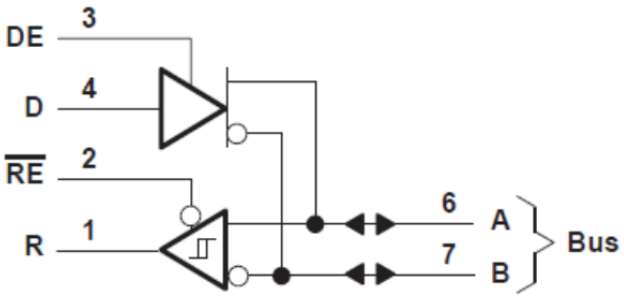
说明

SN65ALS176 和 SN75ALS176 系列差分总线收发器旨 在实现多点总线传输线路上的双向数据通信。这些器件 专为平衡传输线路而设计，符合 TIA/EIA-422-B、TIA/ EIA-485-A 和 ITU 建议 V.11 和 X.27。
SN65ALS176 和 SN75ALS176 系列整合了一个三态差 分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效 和低电平有效使能端，它们可以在外部连接在一起以用 作方向控制。驱动器差分输出端和接收器差分输入端在 内部连接以形成差分输入/输出 (I/O) 总线端口，这些端 口用于在禁用驱动器或 Vcc = 0 时为总线提供最小负载。该端口具有较宽的正负共模电压范围，使得该器件 适用于合用线应用。
SN65ALS176 的额定工作温度范围为 –40 ° C 至 85 ° C。SN75ALS176 系列的额定工作温度范围为 0 ° C 至 70 ° C。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图（正逻辑）

表 4-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	$\overline{RE}$	I	Receiver enable, active low
3	DE	i	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-7	12	V
V_I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 建议运行条件

（除非另有说明）

			最小值	标称值	最大值	单位
V_{CC}	电源电压		4.75	5	5.25	V
V_I 或 V_{IC}	任何总线端子上的输入电压（独立或共模）				12	V
					–7	
V_{IH}	高电平输入电压	D、DE 和 $\overline{RE}$	2			V
V_{IL}	低电平输入电压	D、DE 和 $\overline{RE}$			0.8	V
V_{ID}	差动输入电压(1)				±12	V
I_{OH}	高电平输出电流	驱动器			-60	mA
		接收器			–400	μA
I_{OL}	低电平输出电流	驱动器			60	mA
		接收器			8	
T_A	自然通风工作温度范围	SN65ALS176	–40		85	℃
		SN75ALS176 系列	0		70	

(1) 差分输入/输出总线电压在同相端子 A 和反相端子 B 之间测得。

5.3 Thermal Information

THERMAL METRIC(1)		P (PDIP) 8-Pins	D (SOIC) SN65 Devices 8-Pins	D (SOIC) SN75 Devices 8-Pin	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	62.6	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 图 6-1	½ V_{OD1} or 2(3)			V
		R_L = 54 Ω	See 图 6-1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See 图 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See 图 6-1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
I_O	Output current	Outputs disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I= 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current(5)	V_O = –4 V	SN65ALS176			–250	mA
		V_O = –6 V	SN75ALS176			–250	
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω loadis either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			15	ns
$t_{sk(p)}$	Pulse skew(2)	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			15	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	C_L = 50 pF,	See 图 6-5			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.6 Switching Characteristics - Driver

SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3	3	8	13	ns
		'ALS176A				4	7	11.5	
		'ALS176B				5	8	10	
$t_{sk(p)}$	Pulse skew(2)		R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω	C_L = 50 pF,	See 图 6-3			10	ns
		'ALS176A						7.5	
		'ALS176B						5	
$t_{t(OD)}$	Differential output transition time		R_L = 54 Ω	C_L = 50 pF,	See 图 6-3		8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω	C_L = 50 pF,	See 图 6-5		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.7 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t(R_L = 100 Ω)	V_t(R_L = 54 W)
$\|V_{OD3}\|$	None	V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	None
I_O	$\|Ix_a\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+}– $V_{IT–}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See 图 6-6	I_{OH} = –400 mA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, SeeFigure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
V_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.9 Switching Characteristics - Receiver

SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew(2)	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	R_L = 54 Ω See 图 6-3	C_L = 50 pF,			15	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See 图 6-8		11	18	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See 图 6-8		11	18	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See 图 6-8			50	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See 图 6-8			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH}– t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

5.10 Switching Characteristics - Receiver

SN75ALS176,SN75ALS176A, SN75ALS176B

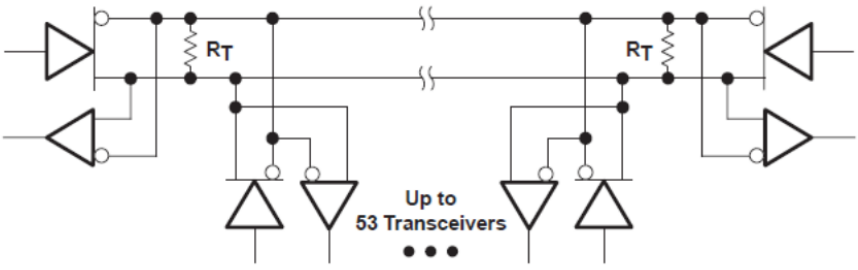
over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
$t_{sk(p)}$	Pulse skew(2)		V_{ID} = –1.5 V to 1.5 V, See 图 6-7	C_L = 15 pF,		0	2	ns
$t_{sk(lim)}$	Pulse skew(3)	'ALS176	R_L = 54 Ω See 图 6-3	C_L = 50 pF,			10	ns
		'ALS176A					7.5	
		'ALS176B					5	
t_{PZH}	Output enable time to high level		C_L = 15 pF,	See 图 6-8		7	14	ns
t_{PZL}	Output enable time to low level		C_L = 15 pF,	See 图 6-8		20	35	ns
t_{PHZ}	Output disable time from high level		C_L = 15 pF,	See 图 6-8		20	35	ns
t_{PLZ}	Output disable time from low level		C_L = 15 pF,	See 图 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

6 Parameter Measurement Information

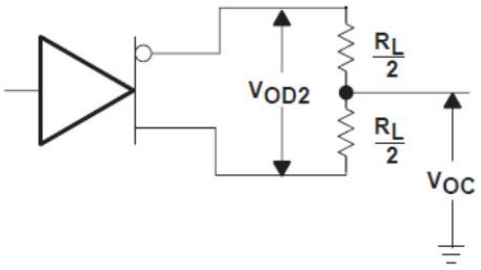


图 6-1. Driver V_{OD2} and V_{OC}

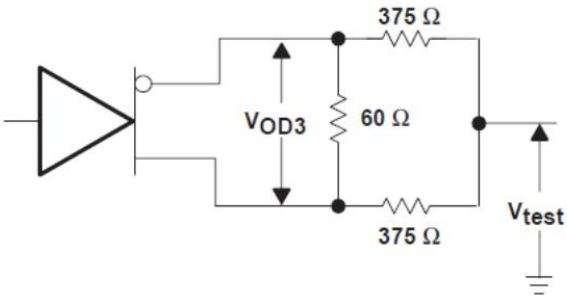
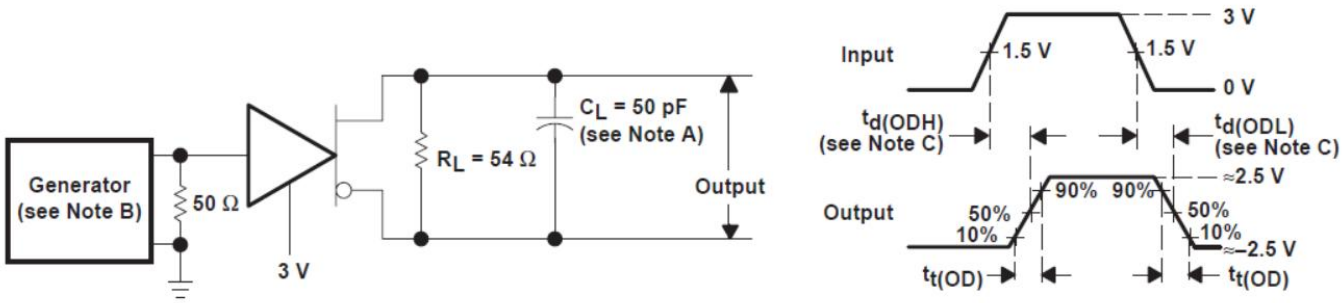


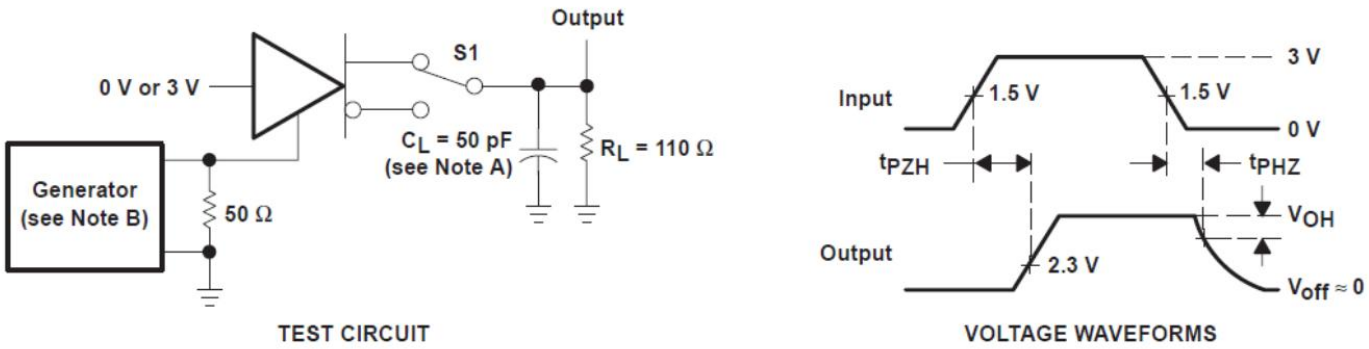
图 6-2. Driver V_{OD3}



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-4. Driver Test Circuit and Voltage Waveforms

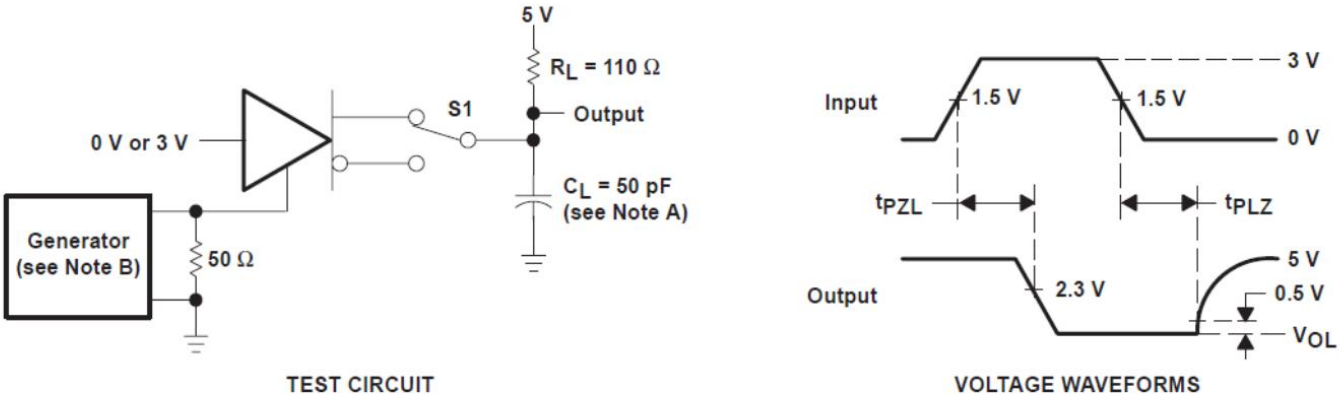


图 6-5. Driver Test Circuit and Voltage Waveforms

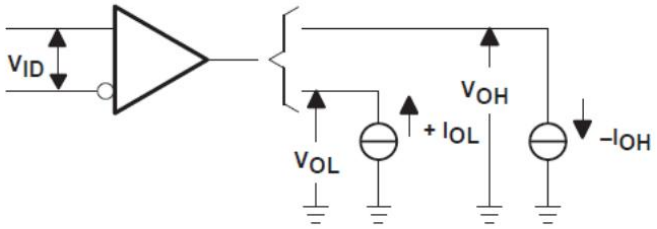
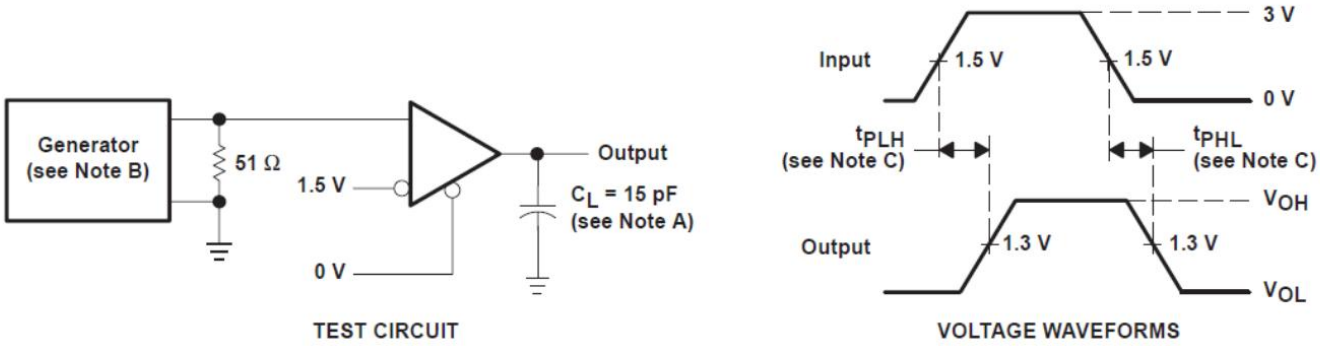


图 6-6. Receiver V_{OH} and V_{OL} Test Circuit

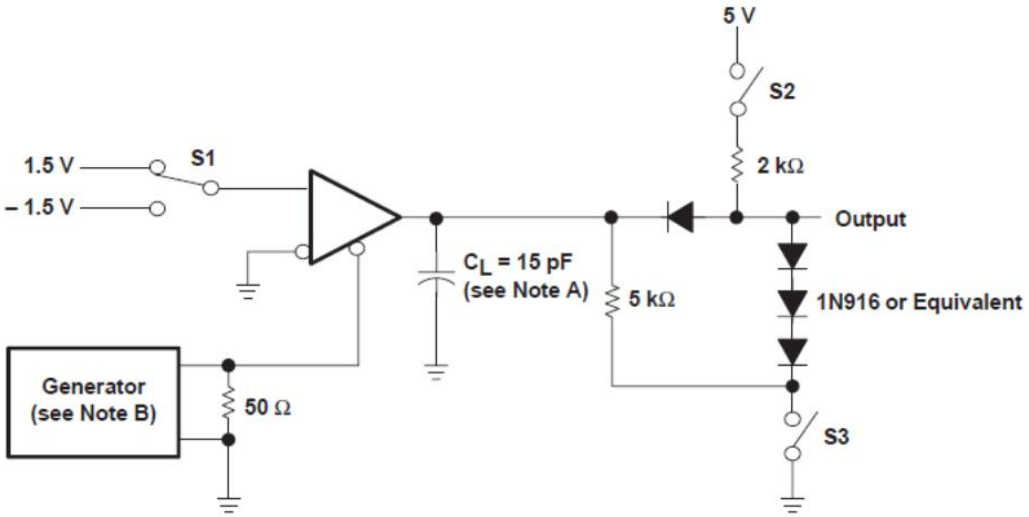


A. C_L includes probe and jig capacitance.

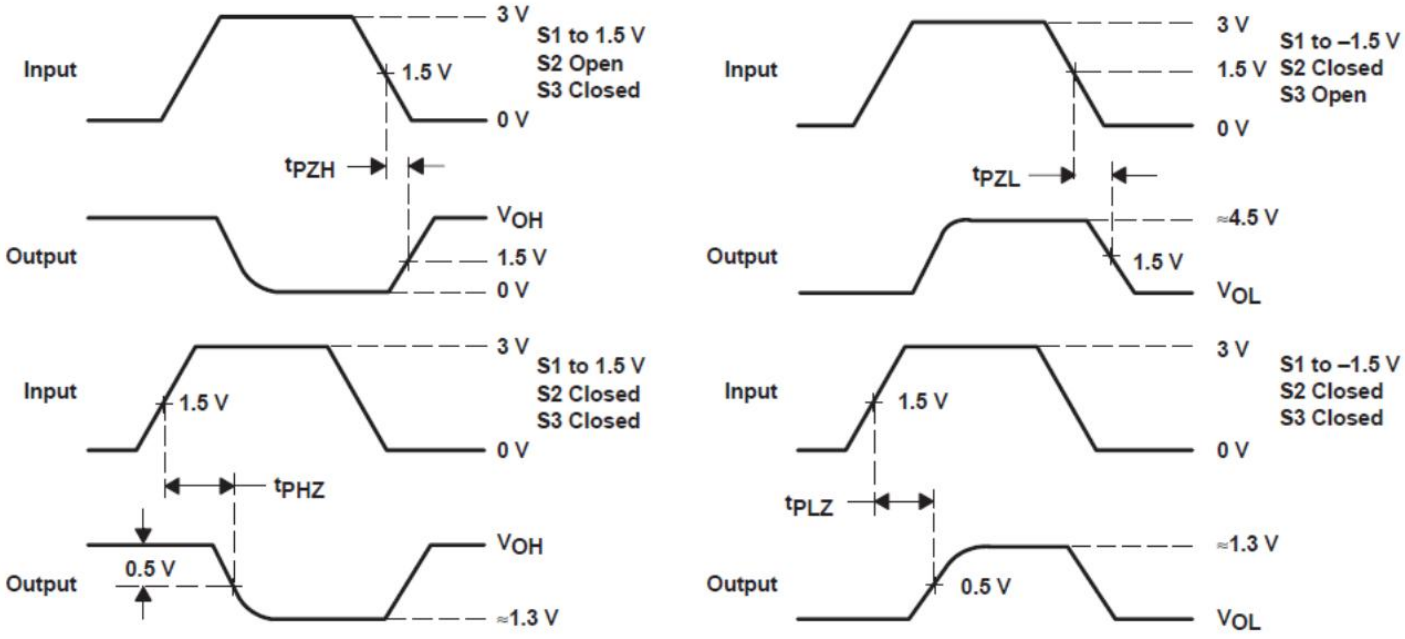
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

C. $t_{pd} = t_{PLH}$ or t_{PHL}.

图 6-7. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, Z_O = 50 Ω.

图 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

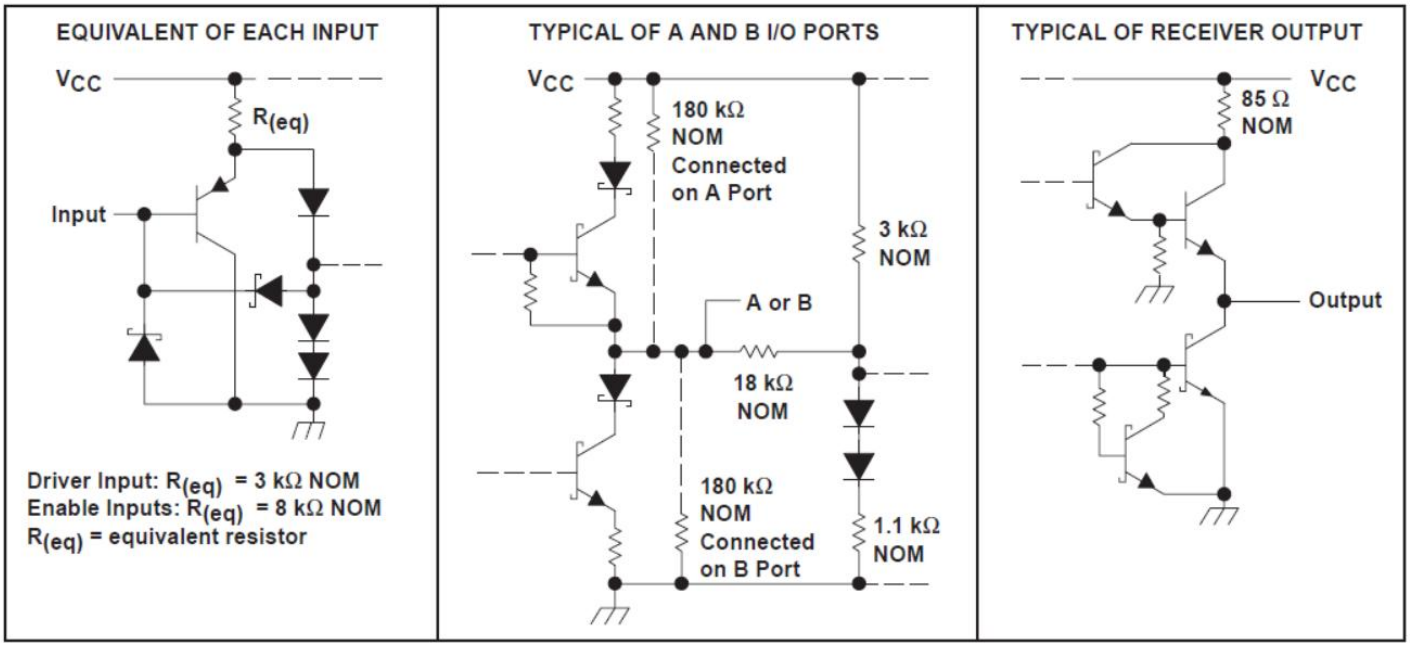


图 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Receiver(1)

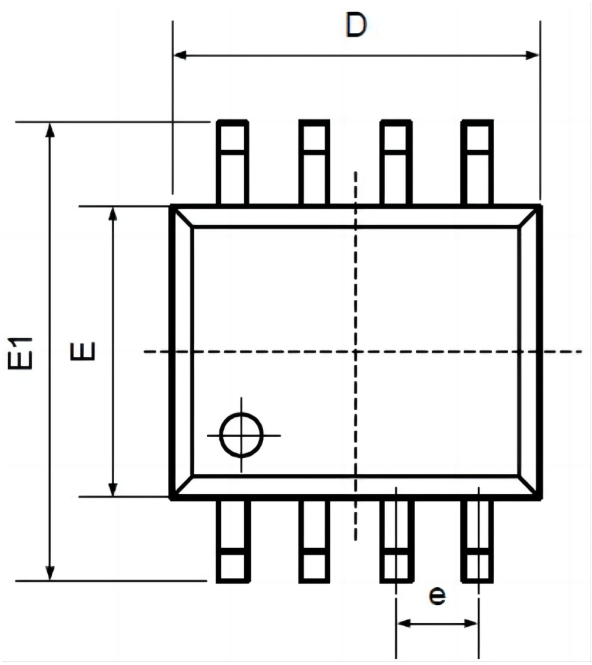
DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

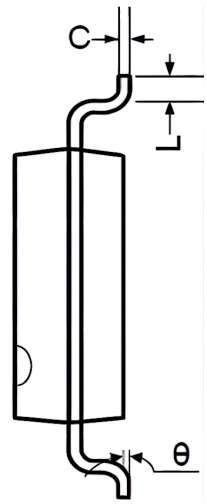
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

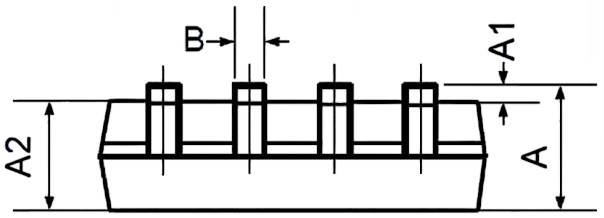
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65ALS176ADR-TUDI	SOP8	Tape,Reel,2500	SN65ALS176ADR
SN65ALS176DR-TUDI	SOP8	Tape,Reel,2500	SN65ALS176DR

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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