AW9539-Q1 16-Bit I²C and SMBus I/O Expander with Interrupt Output and Configuration Registers

Features

- Full automotive qualification AEC-Q100 Grade1
- 16-bit I/O expander
- I²C bus and SMBus compatible
- Open-drain active-low interrupt output
- 400kHz I²C interface
- 1.65V~5.5V power supply
- Configurable slave address with 2 address pins
- Polarity inversion register
- Low standby current consumption of 0.7μA (typical at 3.3V V_{CC})
- No glitch on power-up
- 5.5V tolerant I/O ports
- Noise filter on SCL/SDA inputs
- Latched outputs with high-current drive capability for directly driving LEDs
- Each I/O can be configured as an input or an output independently, default input
- Operation temperature range: -40°C~125°C
- Package: TSSOP-24L

Applications

Automotive Infotainment
Advanced Drive Assistance Systems (ADAS)
Automotive Body Electronics
HEV, EV, and Power train
Industrial, Factory, and Building Automation
Test & Measurement
EPOS

General Description

AW9539TSR-Q1 is a 16-bit I/O expander that can be controlled through the I²C bus. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface.

The AW9539TSR-Q1 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low operation) registers. At power on, all the 16 I/O ports are configured as inputs. The system master can configure each I/O as an input or an output independently by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output register. The Polarity Inversion register can invert the polarity of the Input Port register.

The AW9539TSR-Q1 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The AW9539TSR-Q1 has a hardware RSTN pin that can be used to reset the device to its default state.

Two hardware pins (A0, A1) vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus. All I/O pins are 5.5V tolerant.

Typical Application Circuit

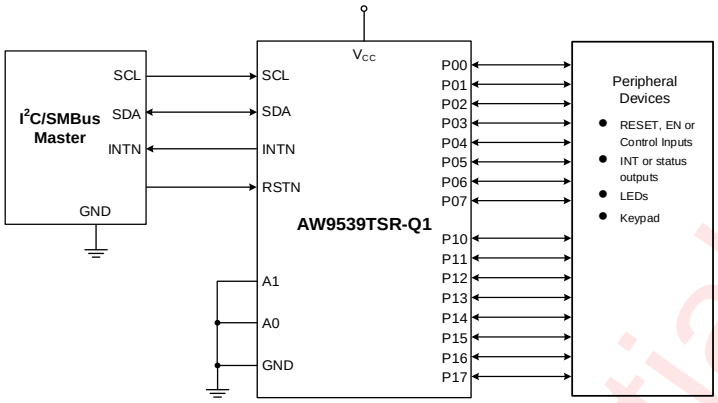
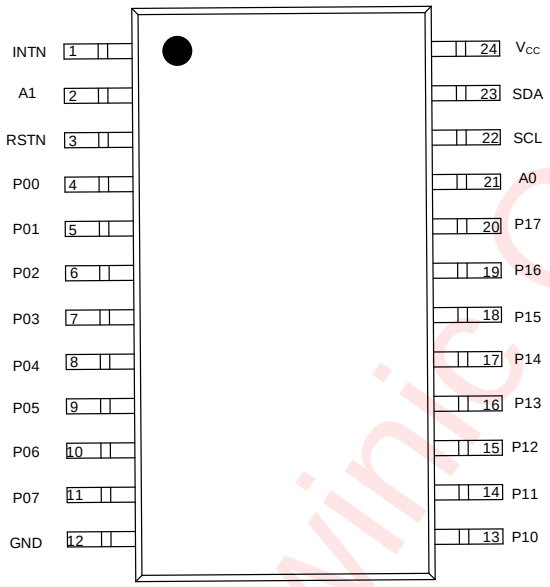


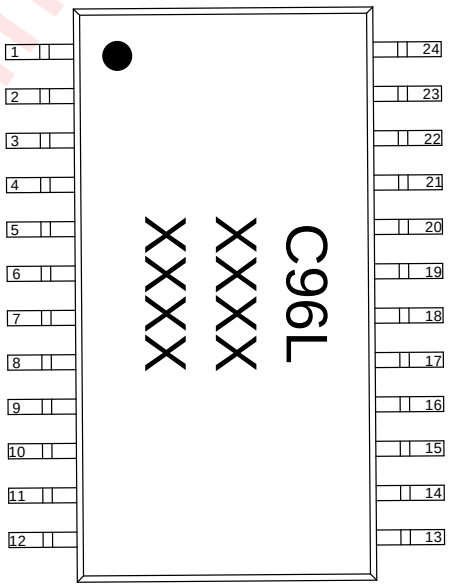
Figure 1 AW9539TSR-Q1 Simplified Application Circuit

Pin Configuration And Top Mark

AW9539TSR-Q1
（Top View）



AW9539TSR-Q1 Marking
（Top View）



C96L- AW9539TSR-Q1
XXXX/XXXX－Production Tracing Code

Figure 2 Pin Configuration and Marking

Pin Definition

Name	NAME	Description
INTN	1	Interrupt output. Connect to V_{CC} through an external pull-up resistor
A1	2	Address input 1. Connect directly to V_{CC} or ground
RSTN	3	Active-low reset input. Connect to V_{CC} through a pull-up resistor if no active connection is used

Name	NAME	Description
P00	4	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01	5	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02	6	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03	7	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04	8	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05	9	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06	10	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07	11	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
GND	12	Ground
P10	13	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
P11	14	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12	15	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13	16	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14	17	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15	18	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16	19	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17	20	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
A0	21	Address input 0. Connect directly to V_{CC} or ground
SCL	22	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	23	Serial data bus. Connect to V_{CC} through a pull-up resistor
V_{CC}	24	Supply voltage

Functional Block Diagram

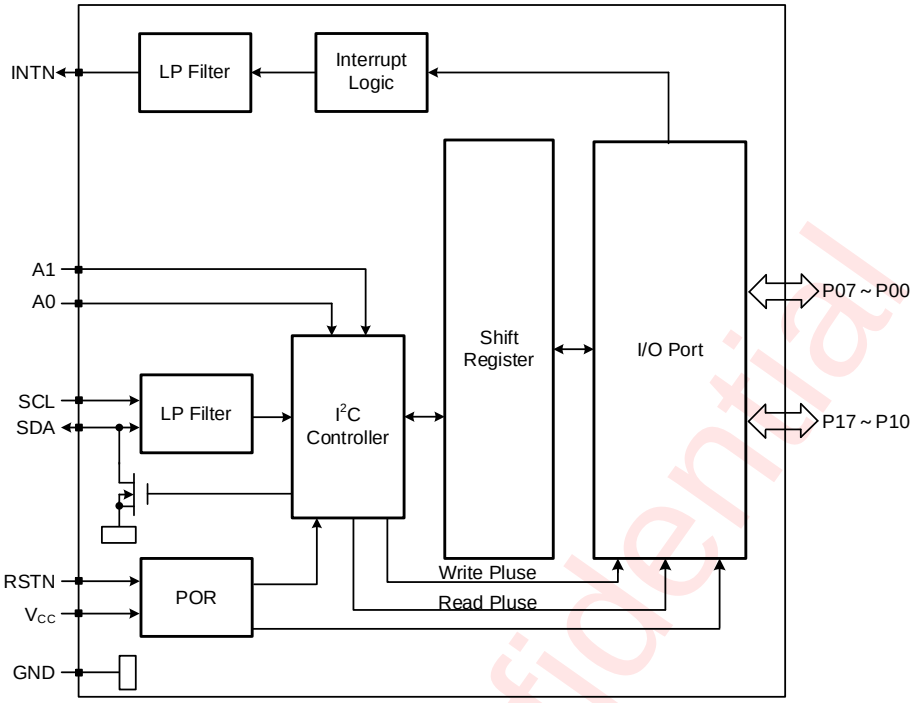


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9539TSR-Q1	-40°C~125°C	TSSOP-24L	C96L	MSL1	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

Parameters		Range
Supply voltage, V_{CC}		-0.5V to 6V
Input voltage, V_I		-0.5V to 6V
Output voltage, V_O		-0.5V to 6V
Continuous output low current, I_{OL}	V_O=0 to V_{CC}	50mA
Continuous output high current, I_{OH}	V_O=0 to V_{CC}	-50mA
Continuous current through GND, I_{CC}		-200mA
Continuous current through V_{CC}, I_{CC}		160mA
Operating free-air temperature range T_A		-40°C to 125°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

Parameters	Range
Maximum operating junction temperature T_{JMAX}	150°C
ESD(Including CDM HBM)(NOTE2)	
HBM	±4kV
CDM	±1.5kV
Latch-Up	
Test condition: AEC_Q100-004-Rev-C	+IT: 300mA -IT: -300mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method of AW9539TSR-Q1: AEC-Q100-002-RevE, the CDM test method of AW9539TSR-Q1: AEC-Q100-011-RevD.

Recommended Operating Conditions

Symbol	Parameters		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		1.65		5.5	V
V_{IH}	High-level input voltage	SCL, SDA, RSTN	0.7×V_{CC}		V_{CC}	V
		A1-A0, P07-P00, P17-P10	0.7×V_{CC}		5.5	V
V_{IL}	Low-level input voltage	SCL, SDA, RSTN	-0.5		0.3×V_{CC}	V
		A1-A0, P07-P00, P17-P10	-0.5		0.3×V_{CC}	V
I_{OH}	High-level output current	P07-P00, P17-P10			-10	mA
I_{OL}	Low-level output current	P07-P00, P17-P10			25	mA
		INTN, SDA			6	mA
T_A	Operating free-air temperature		-40		125	°C

Electrical Characteristics

V_{CC}=1.65V to 5.5V, T_A=25°C for typical values (unless otherwise noted).

Parameters		Test Condition	V_{CC}	Min	Typ.	Max	Unit
V_{CC}	Supply voltage			1.65		5.5	V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I=V_{CC} or GND, I_O= 0	1.65V to 5.5V		1.3	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I=V_{CC} or GND, I_O= 0	1.65V to 5.5V	0.75	1.1		V
V_{OH}	P-port high-level output voltage(NOTE3)	I_{OH}=-8mA	1.65V	1.2			V
			2.3V	1.8			V
			3V	2.6			V
			4.75V	4.1			V
		I_{OH}=-10mA	1.65V	1			V
			2.3V	1.7			V
			3V	2.5			V
			4.75V	4			V
I_{OL}	P port low-level output current(NOTE4)	V_{OL}=0.5V	1.65V to 5.5V	8			mA
		V_{OL}=0.7V	1.65V to 5.5V	10			mA
	SDA low-level output current	V_{OL}=0.4V	1.65V to 5.5V	10			mA
	INTN low-level output current	V_{OL}=0.4V	1.65V to 5.5V	3			mA
I_I	SCL, SDA,RSTN input leakage current	V_I=V_{CC} or GND	1.65V to 5.5V			±1	μA
	A1-A0 input leakage current		1.65V to 5.5V			±1	μA
I_{IH}	P port input high leakage current	V_I=V_{CC}	1.65V to 5.5V			1	μA
I_{IL}	P port input low leakage current	V_I=GND	1.65V to 5.5V			-1	μA
I_{CC}	Operating mode	V_I=V_{CC}, I_O= 0, I/O=inputs, f_{SCL}=400kHz, no load	5.5V		21	40	μA
			3.6V		12	30	μA
			3.3V		10.5	25	μA
			2.7V		8.5	19	μA
			1.95V		5.5	11	μA
			1.65V		4.5	10	μA
	Standby mode	V_I=V_{CC}, I_O=0, I/O=inputs, f_{SCL}=0kHz, no load	5.5V		1.2	2.5	μA
			3.6V		0.8	1.7	μA
			3.3V		0.7	1.5	μA
			2.7V		0.55	1.2	μA
			1.95V		0.35	0.9	μA
			1.65V		0.3	0.8	μA

Parameters		Test Condition	V_{CC}	Min	Typ.	Max	Unit
ΔI_{CC}	additional quiescent supply current	SCL, SDA, RSTN, A1~A0; one input at V_{CC}-0.6V, other inputs at V_{CC}	1.65V to 5.5V		0.2	5	μA
		P port; one input at V_{CC}-0.6V, other inputs at V_{CC}	1.65V to 5.5V		0.2	5	μA
C_i	SCL input capacitance	V_I=V_{CC} or GND	1.65V to 5.5V		4		pF
C_{io}	SDA input-output pin capacitance	V_{IO}=V_{CC} or GND	1.65V to 5.5V		5		pF
	P port input-output pin capacitance				9		pF

NOTE3: The total current sourced by all I/Os must be limited to 160mA (80mA for P07-P00 and 80mA for P17-P10).

NOTE4: Each I/O must be externally limited to a maximum of 25mA, and each octal (P07-P00 and P17-P10) must be limited to a maximum current of 100mA, for a device total of 200mA.

I²C Interface Timing Requirements

Parameters			Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
f_{SCL}	Interface clock frequency		0	100	-	400	kHz
$t_{HD:STA}$	(Repeat-start) START condition hold time		4		0.6	-	μs
t_{LOW}	Low level width of SCL		4.7		1.3	-	μs
t_{HIGH}	High level width of SCL		4		0.6	-	μs
$t_{SU:STA}$	(Repeat-start) START condition setup time		4.7		0.6	-	μs
$t_{HD:DAT}$	Data hold time		0		0	-	μs
$t_{SU:DAT}$	Data setup time		0.25		0.1	-	μs
t_R	Rising time of SDA and SCL			1000	20	300	ns
t_F	Falling time of SDA and SCL			300	20	300	ns
$t_{SU:STO}$	STOP condition setup time		4		0.6	-	μs
t_{BUF}	Time between start and stop condition		4.7		1.3	-	μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{VD:DAT}$	Valid-data time	SCL low to SDA output valid		3.45		0.9	μs
$t_{VD:ACK}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		3.45		0.9	μs
C_b	Capacitive load for each bus line			400		400	pF

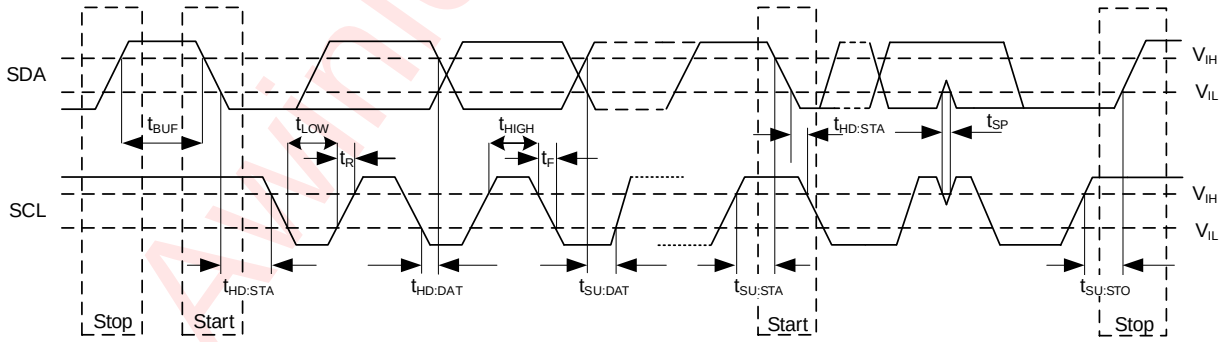


Figure 4 Definition of Timing on The I²C-bus

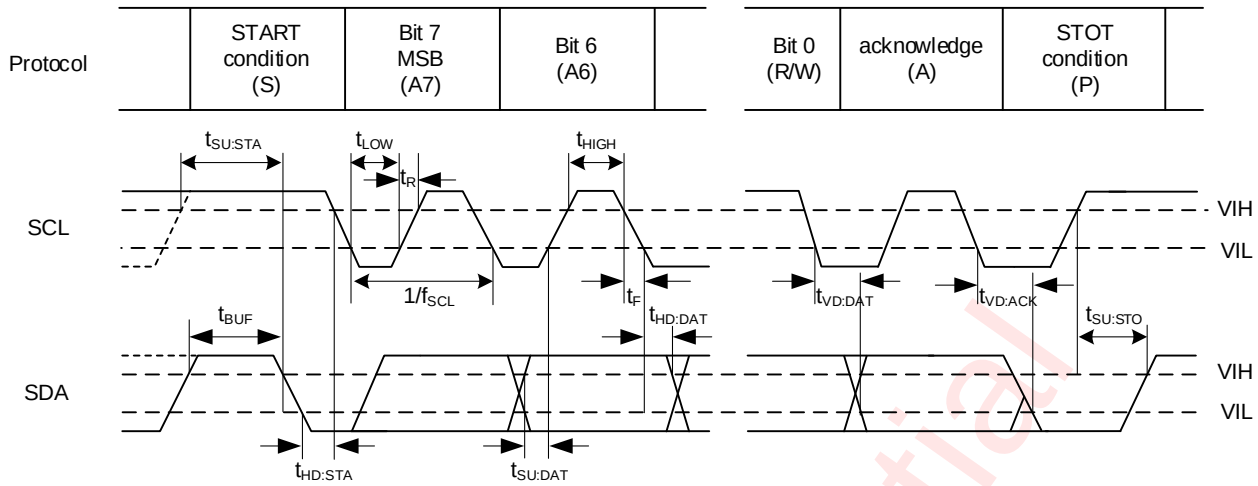


Figure 5 I²C-bus Timing Diagram

Timing Requirements

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_w	Reset pulse width		180		ns
t_{REC}	Reset recovery time		180		ns
t_{RESET}	time to Reset		400		ns

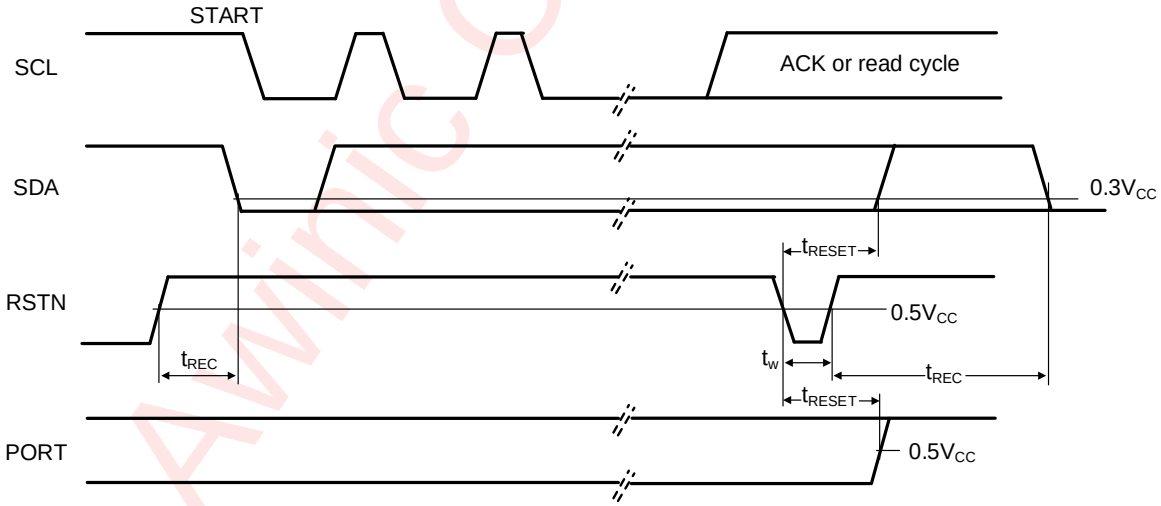


Figure 6 RSTN Timing Diagram

Switching Characteristics

Symbol	Parameter	From (Input)	To (Output)	Min.	Max.	Unit
t_{iv}	Interrupt valid time	P port	INTN		1	μs
t_{ir}	Interrupt reset delay time	SCL	INTN		1	μs
t_{pv}	Output data valid time	SCL	P port		400	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	300		ns

Typical Characteristics

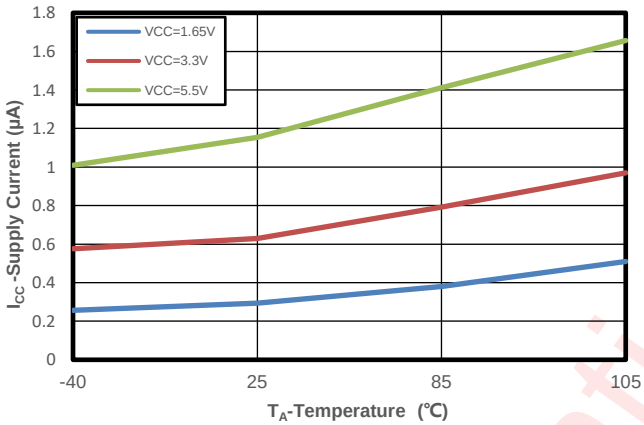


Figure 7 AW9539 Standby Supply Current (P port=V_{CC} or GND) VS Temperature for Different Supply Voltage (V_{CC})

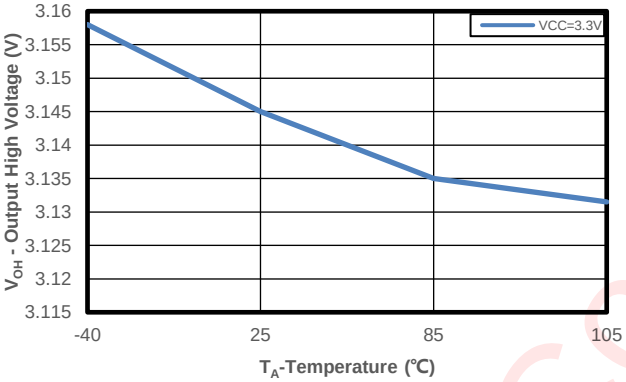


Figure 8 AW9539 GPIO Output High Voltage VS Temperature

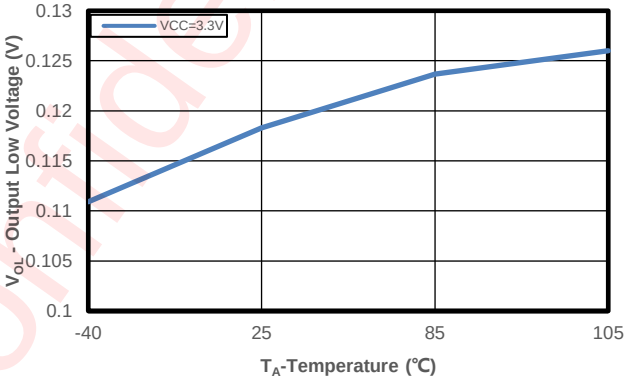


Figure 9 AW9539 GPIO Output Low Voltage VS Temperature

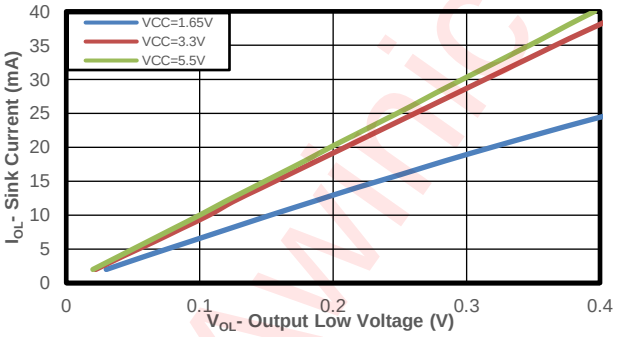


Figure 10 AW9539 P Port Output Low Voltage VS Current for Different V_{CC}

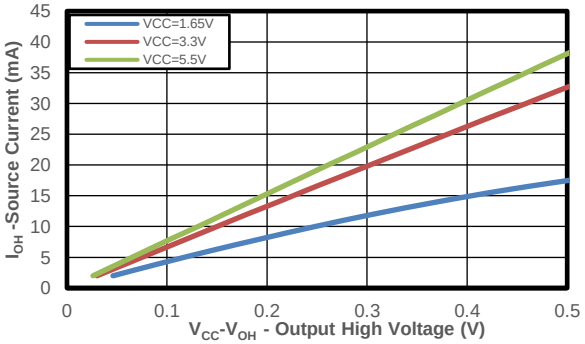


Figure 11 AW9539 P Port Output High Voltage VS Current for Different V_{CC}

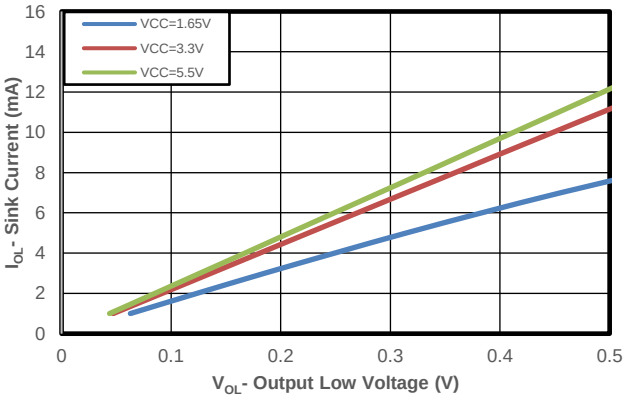


Figure 12 AW9539 INTN Pin Output Low Voltage VS INTN Current for Different V_{CC}

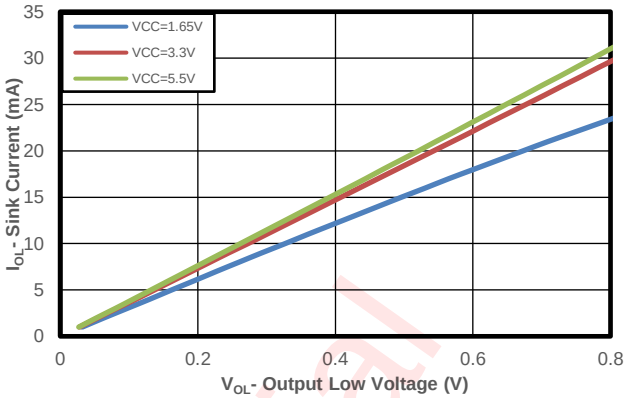


Figure 13 AW9539 SDA Pin Output Low Voltage VS SDA Current for Different V_{CC}

Detailed Functional Description

AW9539TSR-Q1 is a 16-bit I/O expander that can be controlled through the I²C bus. Each I/O port can be configured as output or input independently. After power-on, all channels are configured as inputs.

The system controller can reset the AW9539TSR-Q1 in the event of a time-out or other improper operation by asserting a low in the RSTN input. The power-on reset puts the registers in their default state and initializes the I²C-SMBus state machine. Asserting RSTN causes the same reset-initialization to occur without depowering the part.

When configured as inputs, any port state change are indicated by the INTN. The INTN output can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. The INTN can be cleared by reading Input State register through I²C or the port is changed to the original setting. When configured as input, the polarity of the Input Port register can be inverted with the Polarity Inversion register.

Device Address

The AW9539TSR-Q1 features 2 hardware address pins (A0 and A1) to allow the user to program the device's I²C address by pulling each pin to either V_{CC} or GND to signify the bit value in the address. This allows up to 4 AW9539TSR-Q1 devices to be on the same bus without address conflicts. The voltage on the pins must not change while the device is powered up in order to prevent possible I²C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V_{CC} or GND and cannot be left floating.

The permitted I²C addresses are 0x74(7-bit) through 0x77(7-bit). The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

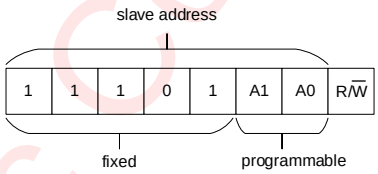


Figure 14 AW9539TSR-Q1 Device Address

Power On Reset

When power (from 0V) is applied to V_{CC}, an internal power-on reset circuit holds the AW9539TSR-Q1 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the AW9539TSR-Q1 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

When power has been applied to V_{CC} above V_{PORR}, and the POR has taken place. After last for about 100ns, the device is in a functioning mode. It is ready to monitor the changes on the input ports. After last for about 250ns, the I²C interface is accessible, the device is ready to accept any incoming I²C requests.

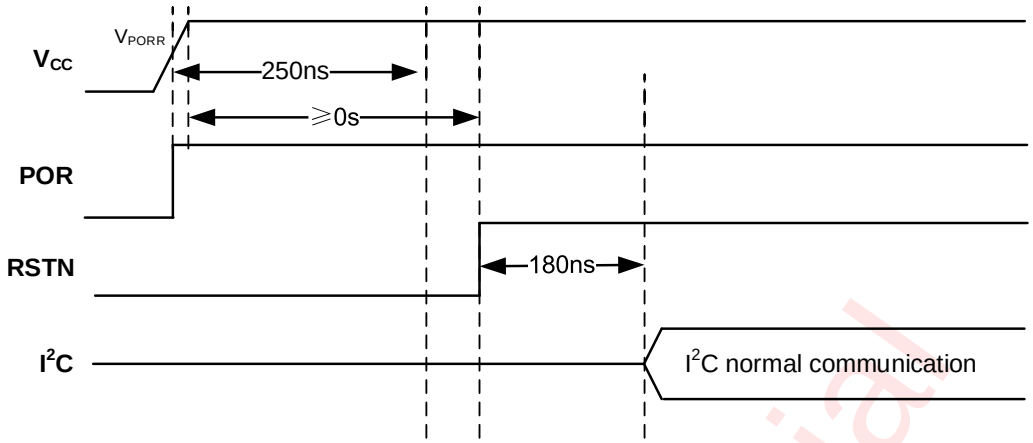


Figure 15 Power On Timing 1

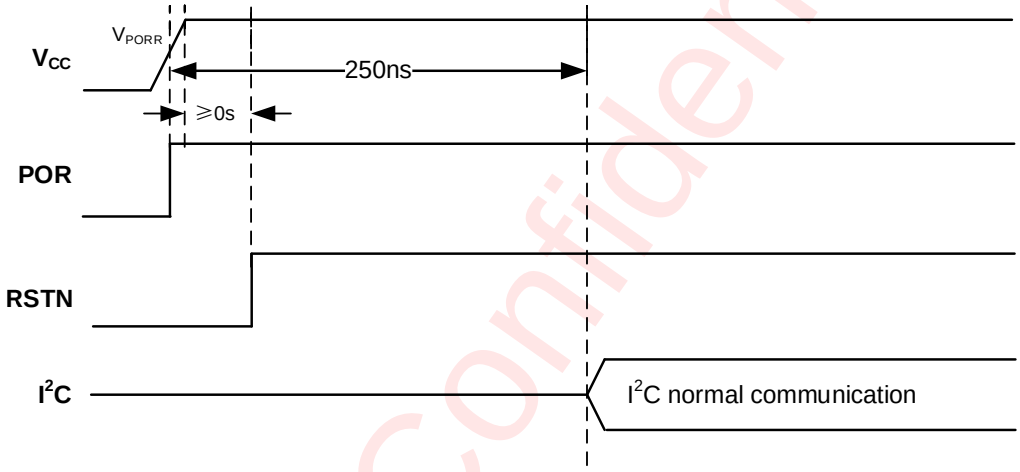


Figure 16 Power On Timing 2

Feature Description

I/O Port

When I/O is configured as an input on AW9539TSR-Q1, FETs Q1 and Q2 are off, creating a high-impedance input without the pull-up resistor. The input voltage of AW9539TSR-Q1 may be raised above V_{CC} to a maximum of 5.5V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation. Figure 17 shows the simplified schematic of I/Os.

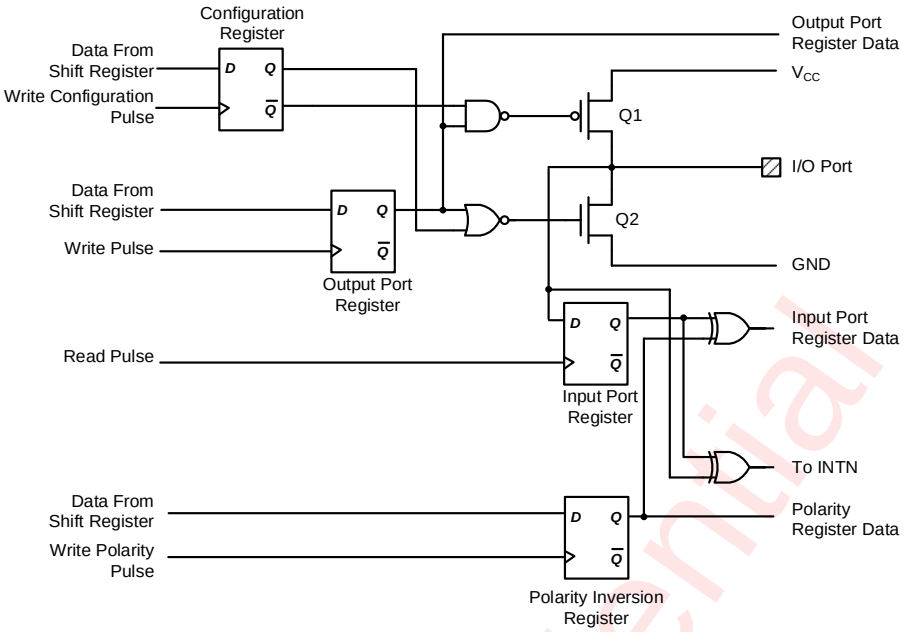


Figure 17 Simplified Schematic of I/Os

Interrupt Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal INTN is valid. The interrupt is reset when data on the port changes back to the original value or when data is read form the port that generated the interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or vice versa. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the INTN is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as INTN.

Reading from or writing to another device does not affect the interrupt circuit, and a port configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. INTN has an open-drain structure and requires a pull-up resistor to V_{CC} (typically 10kΩ in value).

Writing To The Port Registers

Data is transmitted to the AW9539TSR-Q1 by sending the device address and setting the least significant bit to a logic 0. The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the AW9539TSR-Q1 are configured to operate as four register pairs. The four pairs are Input Port, Output Port, Polarity Inversion, and Configuration registers. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte is sent to Output Port 1 (0x03), then the next byte will be stored in Output Port 0 (0x02). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

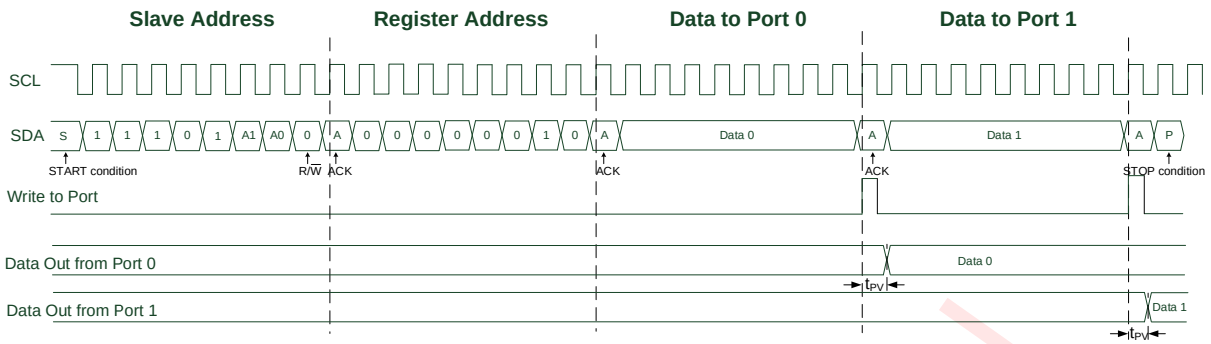
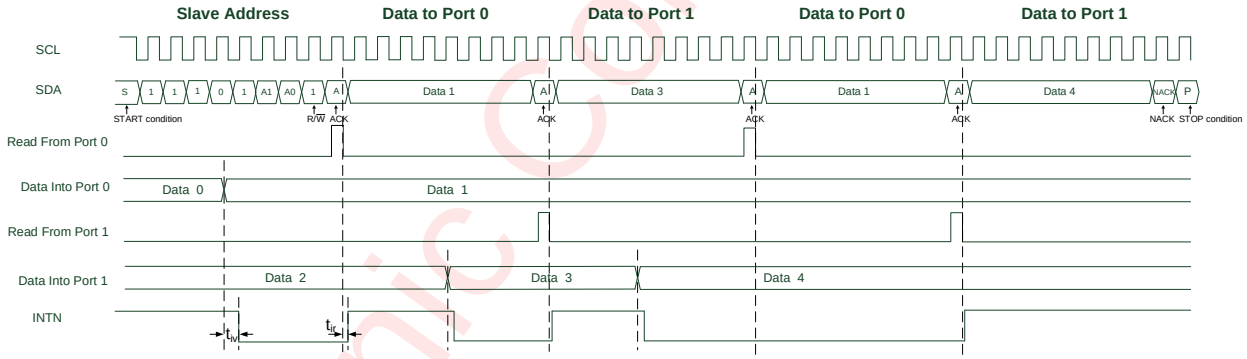


Figure 18 Write to Output Port Registers

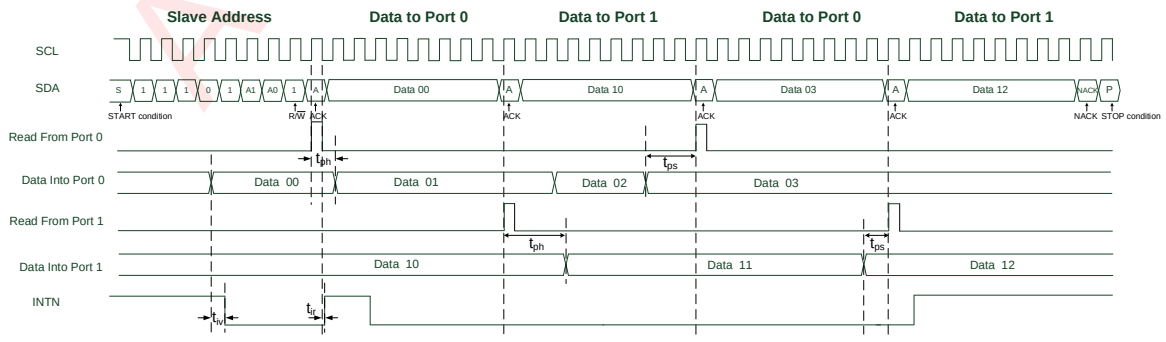
Reading The Port Registers

Reading from a slave is very similar to writing, but requires some additional steps. In order to read data from the AW9539TSR-Q1, the bus master must first send the AW9539TSR-Q1 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the AW9539TSR-Q1 (see Figure 19 and Figure 20). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1 (0x01), then the next byte read would be Input Port 0 (0x00). There is no limitation on the number of data bytes received in one read transmission, but the final byte received, the bus master must not acknowledge the data.



- Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 19 Read Input Port Register, Scenario 1



- Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 20 Read Input Port Register, Scenario 2

General I²C Operation

AW9539TSR-Q1 supports the serial I²C-bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. The size of the pull-up resistor is determined by the amount of capacitance on the I²C lines. The I²C interface supports 1.8V pull-up voltage values. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 8-bit and register data is 8-bit, and the data transmission is in big-endian mode. Data transfer may be initiated only when the bus is not busy.

Data Validation

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

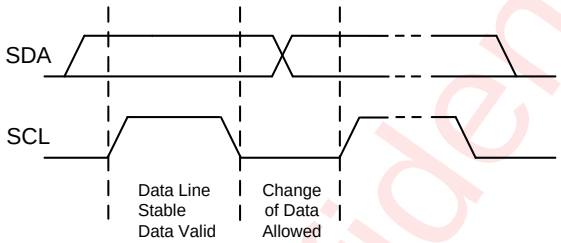


Figure 21 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

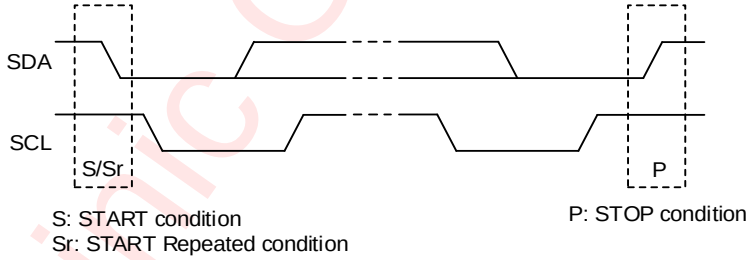


Figure 22 I²C Start/Stop Condition Timing

Acknowledge(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

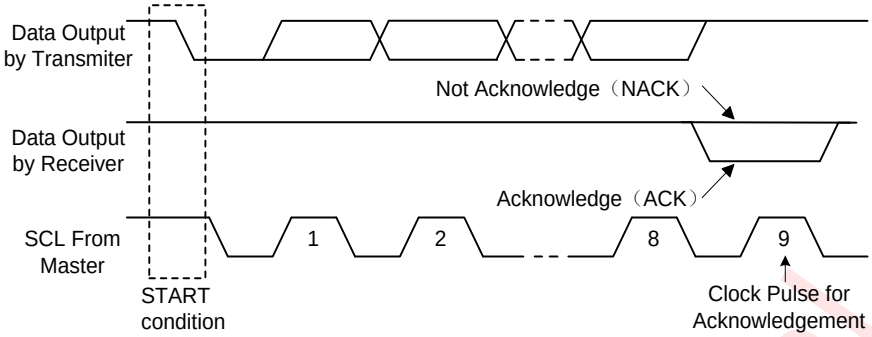


Figure 23 I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends data byte to be written to the addressed register.

g) Slave sends acknowledge signal.

h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g).

i) Master generates STOP condition to indicate write cycle end.

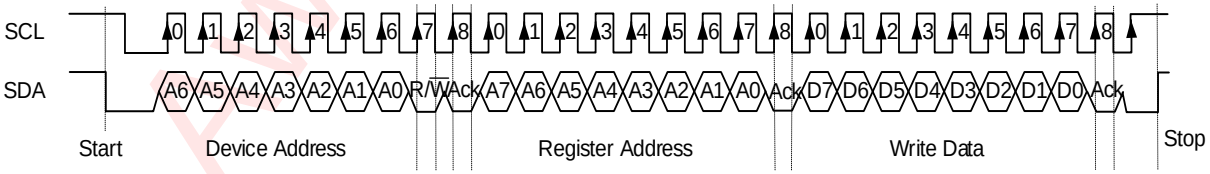


Figure 24 I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. In particular, if the AW9539TSR-Q1 send the first byte, then next bytes will be sent to the master device reflecting the information in the other register in the pair.

k) If the master device generates STOP condition, the read cycle is ended.

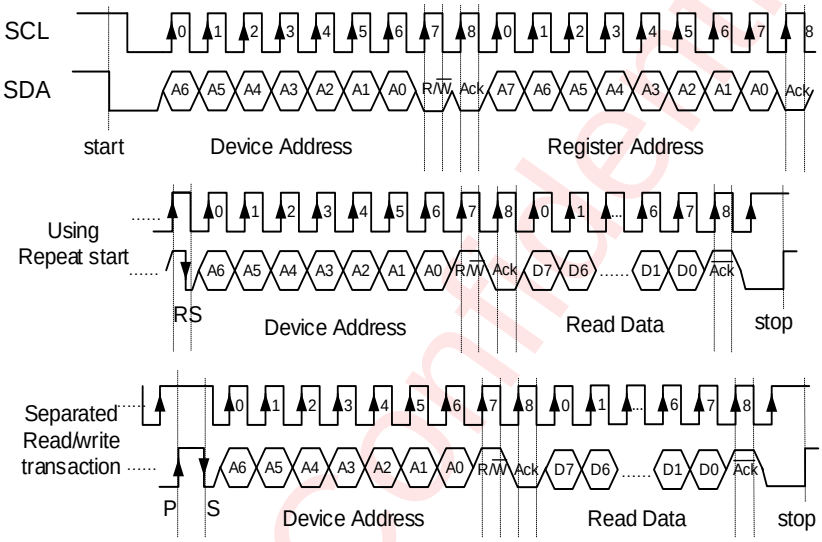


Figure 25 I²C Read Byte Cycle

Register Configuration

Register List

ADDR	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	R	Input Port 0								xxh
0x01	R	Input Port 1								xxh
0x02	W/R	Output Port 0								FFh
0x03	W/R	Output Port 1								FFh
0x04	W/R	Polarity Inversion Port 0								00h
0x05	W/R	Polarity Inversion Port 1								00h
0x06	W/R	Configuration Port 0								FFh
0x07	W/R	Configuration Port 1								FFh

Register Detailed Description

Input Port Registers (Address 00h/01h)

Bit	Register	R/W	Description	Default
7:0	Input Port 0	R	P07~P00 input state 0: low level 1: high level	xxh
7:0	Input Port 1	R	P17~P10 input state 0: low level 1: high level	xxh

The Input Port registers reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, x, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next.

Output Port Registers (Address 02h/03h)

Bit	Register	R/W	Description	Default
7:0	Output Port 0	W/R	P07~P00 output state 0: low level 1: high level	FFh
7:0	Output Port 1	W/R	P17~P10 output state 0: low level 1: high level	FFh

The Output Port registers show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Polarity Inversion Registers (Address 04h/05h)

Bit	Register	R/W	Description	Default
7:0	Polarity Inversion Port 0	W/R	P07~P00 input state invert enable 0: disable 1: enable	00h
7:0	Polarity Inversion Port 1	W/R	P17~P10 input state invert enable 0: disable 1: enable	00h

The Polarity Inversion registers allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in these registers is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Configuration Registers (Address 06h/07h)

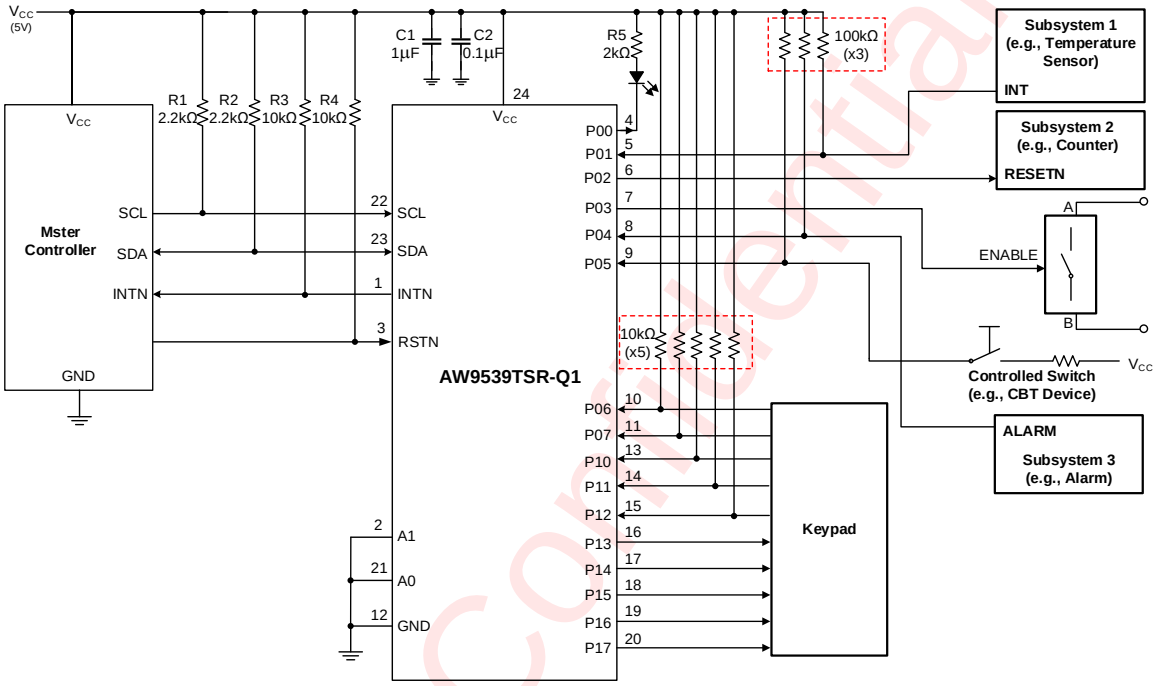
Bit	Register	R/W	Description	Default
7:0	Configuration Port 0	W/R	P07~P00 input/output direction 0: output 1: input	FFh
7:0	Configuration Port 1	W/R	P17~P10 input/output direction 0: output 1: input	FFh

The Configuration registers configure the directions of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Application Information

Applications of the AW9539TSR-Q1 has this device connected as a slave to an I²C master (processor), and the I²C bus may contain any number of other slave devices. The AW9539TSR-Q1 is typically be in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

IO Expanders such as the AW9539TSR-Q1 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons. Figure 26 show an application in which the AW9539TSR-Q1 can be used to control multiple subsystems, and even read inputs from buttons.



(1) In this application schematic, P00, P02, P03 and P13~P17 are configured as outputs.
(2) P01, P04~P07 and P10~P12 are configured as inputs.
(3) Device address is configured as 1110100 for this example.
(4) Pin numbers shown are for TSSOP packages.

Figure 26 AW9539TSR-Q1 Application Circuit

Minimizing I_{CC} When I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 26. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2V less than V_{CC}. The ΔI_{CC} parameter in the Electrical Characteristics table shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to VCC when the LED is off to minimize current consumption.

Figure 27 shows a high-value resistor in parallel with the LED. Figure 28 shows V_{CC} less than the LED supply voltage by at least 1.2V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

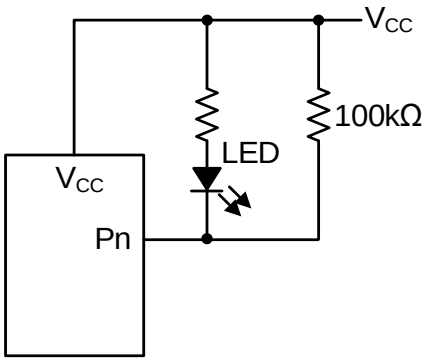


Figure 27 High-Value Resistor in Parallel With LED

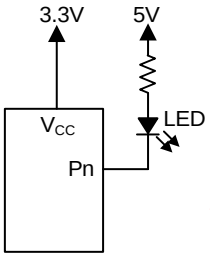


Figure 28 Device Supplied by Lower Voltage

Pull-up Resistor Calculation

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I²C bus. The minimum pull-up resistance is a function of pull-up reference voltage (V_{CC}), V_{OL}(max), and I_{OL} as shown in Equation 1.

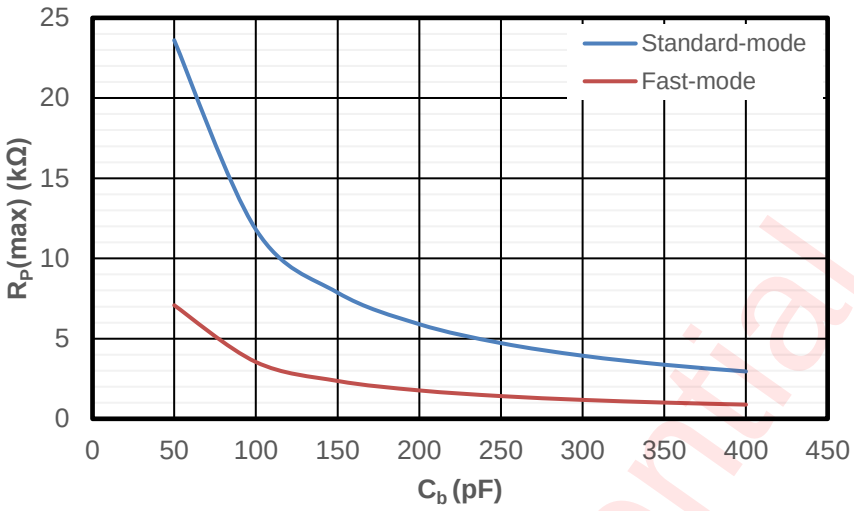
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300ns for fast-mode operation, f_{SCL} =400kHz) and bus capacitance, C_b as shown in Equation 2.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the AW9539TSR-Q1, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections and traces, and the capacitance of additional slaves on the bus.

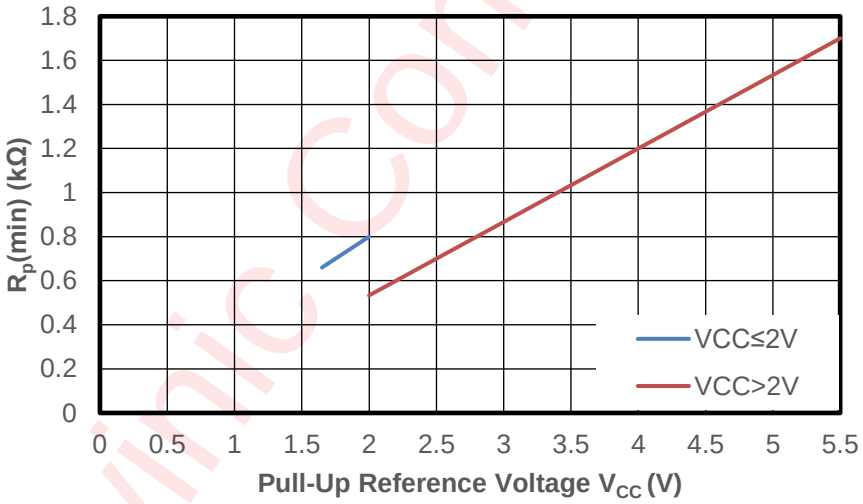
Application Curves



Standard-mode (f_{SCL}=100kHz, t_r=1μs)

Fast-mode (f_{SCL}=400kHz, t_r=300ns)

Figure 29 Maximum Pull-Up Resistance (R_p(max)) vs Bus Capacitance (C_b)



V_{OL}=0.2*V_{CC}, I_{OL}=2mA when V_{CC}≤2V

V_{OL}=0.4V, I_{OL}=3mA when V_{CC}>2V

Figure 30 Minimum Pull-up Resistance (R_p(min)) vs Pull-up Reference Voltage (V_{CC})

Power Supply Recommendations

In the event of a glitch (data output or input or even power) or data corruption, the AW9539TSR-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 31 and Figure 32.

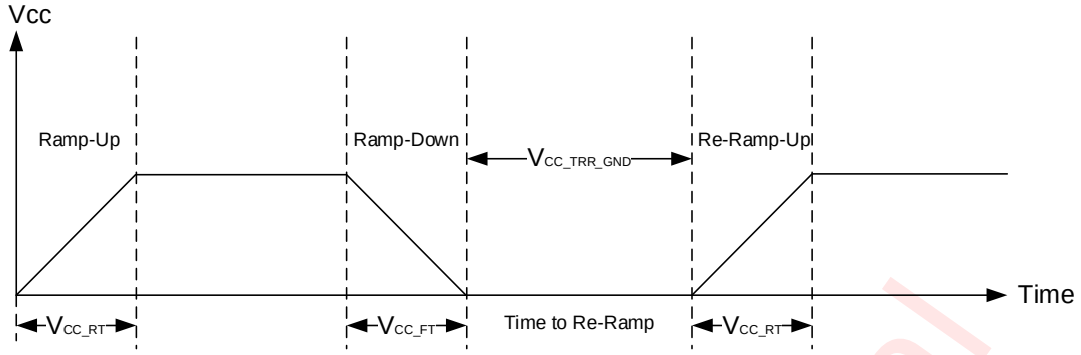


Figure 31 V_{CC} is Lowered Below 0.2V or 0V and Then Ramped Up to V_{CC}

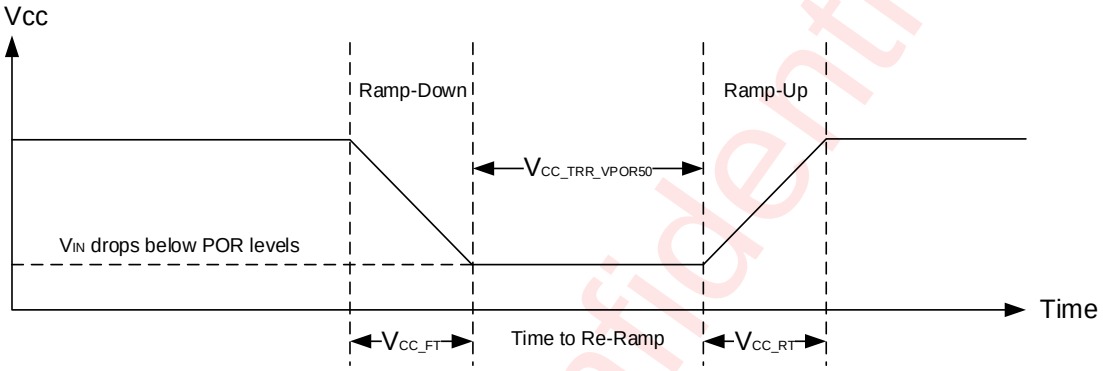


Figure 32 V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 2 specifies the performance of the power-on reset feature for AW9539TSR-Q1 for both types of power-on reset.

Table 2 Recommended Supply Sequencing and Ramp Rates

Parameter			Min.	Typ.	Max.	Unit
V_{CC_FT}	Fall rate of V_{CC}	See Figure 31	0.1		2000	ms
V_{CC_RT}	Rise rate of V_{CC}	See Figure 31	0.1		2000	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops below 0.2V or to GND)	See Figure 31	1			μs
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR(MIN)}$ – 50mV)	See Figure 32	1			μs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW}=1μs	See Figure 33			1.2	V
V_{CC_MV}	The minimum voltage that V_{CC} can glitch down to without causing a reset (V_{CC_GH} must also not be violated)	See Figure 33	1.5			V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH}=0.5×V_{CC} (For V_{CC}>3V)	See Figure 33			10	μs

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 33 and Table 2 provide more information on how to measure these specifications.

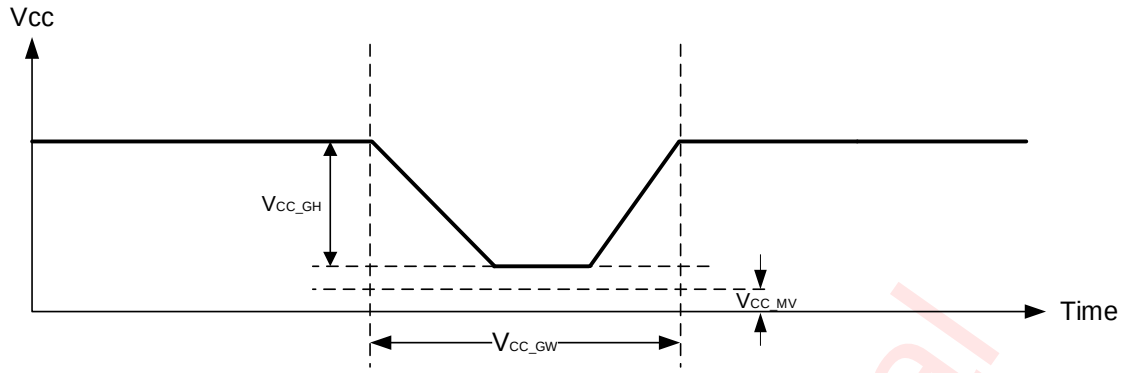


Figure 33 Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0V. Figure 34 and Table 2 provide more details on this specification.

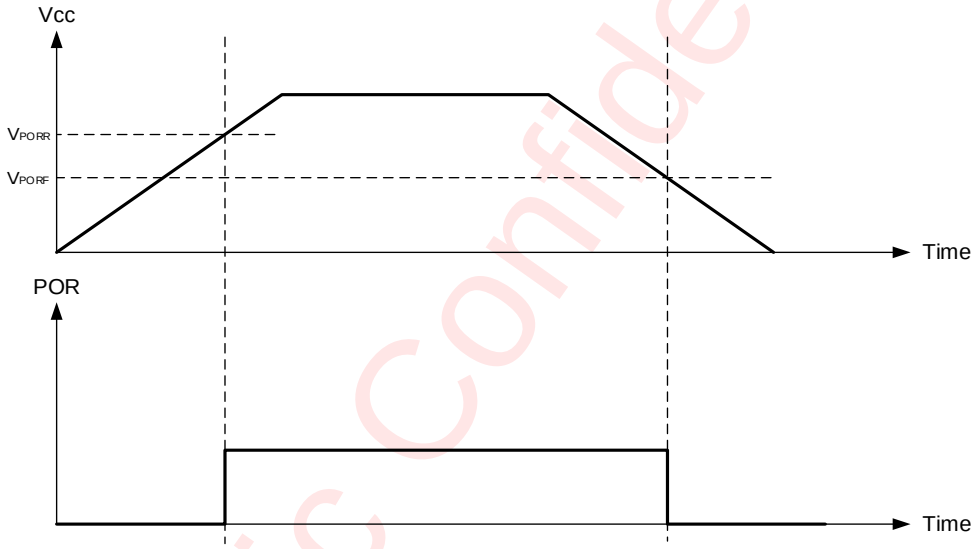


Figure 34 V_{POR}

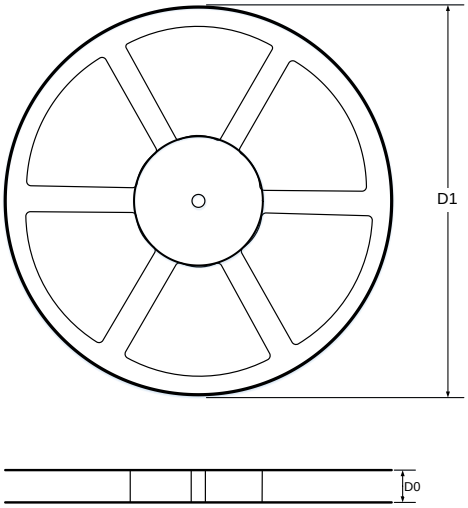
PCB Layout Consideration

AW9539TSR-Q1 is a 16-bit I/O expander that can be controlled through the I^2C bus. To obtain the good thermal performance, PCB layout should be considered carefully. Here are some guidelines:

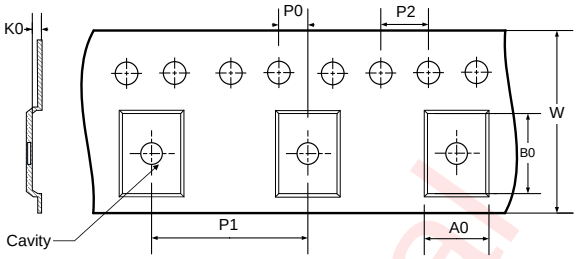
1. The C1, C2 should be placed as close to the chip as possible.
2. The GND pad must be well connected to the ground of the PCB, and add as many thermal vias as possible near the GND on the PCB for the heat conductivity of the device and PCB.

Tape And Reel Information

REEL DIMENSIONS

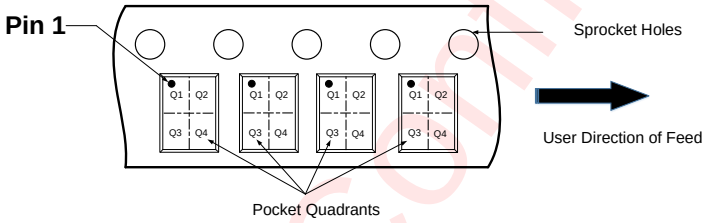


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



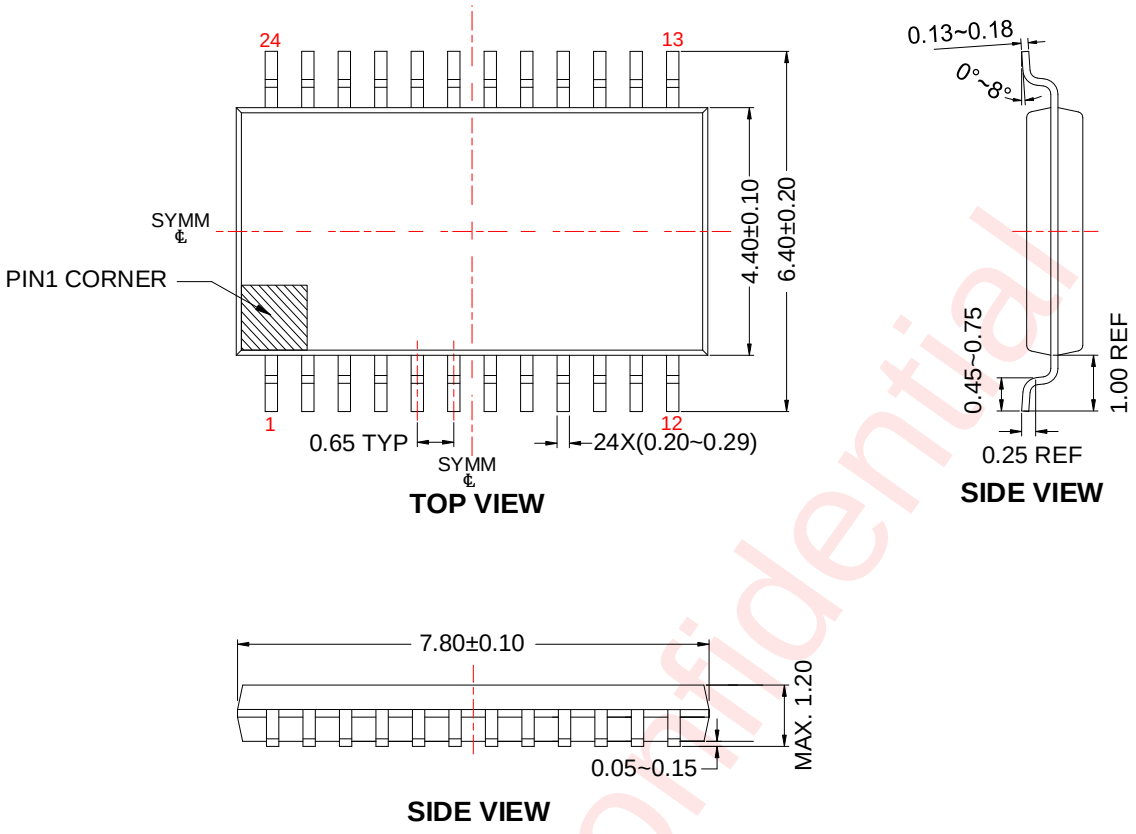
Note: The above picture is for reference only. Please refer the value in the table below for actual size.

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.0	16.4	6.95	8.3	1.6	2.0	8.0	4.0	16.0	Q1

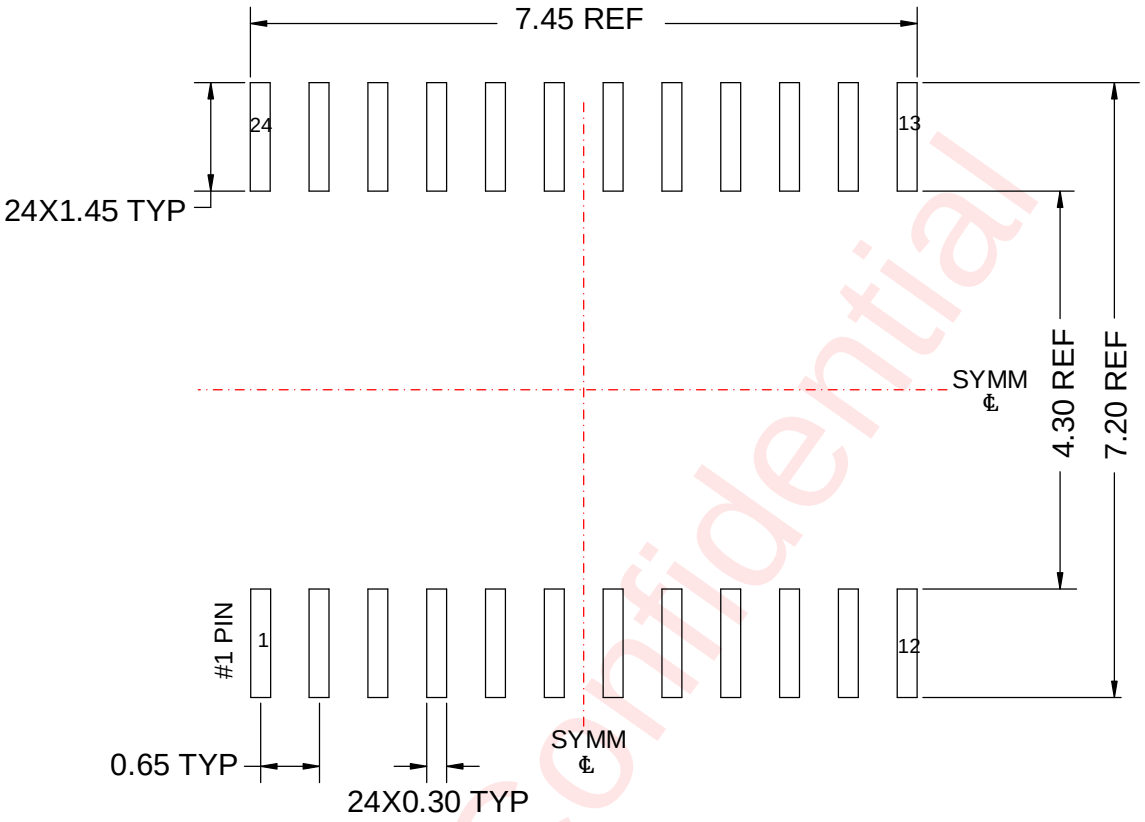
All dimensions are nominal

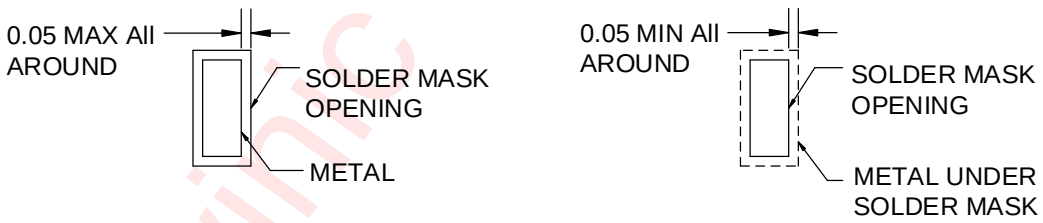
Package Description



Unit:mm

Land Pattern Data





NON SOLDER MASK DEFINED　　SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2024	Officially released
V1.1	May. 2025	Update Test Condition of the Standby mode

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