3.4 W I²S Input mono Digital Smart K Audio Amplifier

FEATURES

- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 9µV**
- **THD+N: 0.016%**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- Three gain settings: -3dB,0dB,+3dB
- I²S interface：
  - I2S Philips
  - Supports 2 slots
  - Input Sample Rates from 32kHz to 48kHz
  - Data Width: 32 Bits
  - Left/right selection and mono mixing
- PDM interface：
  - Input Sample Rates: 3M/6M/12M
  - Left/right selection
- Simplified interface for audio and control settings
- Power Supplies：
  - VDDP：2.5V-5.5V
  - VDDD: 1.65V~1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- WLCSP 1.34mmX1.48mmX0.6mm-9B package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

AW88082 is an I²S/PDM input digital audio amplifier. It receives audio and control settings via an I²S/PDM digital interface. The power-down to operating mode transition is triggered when a clock signal is detected on the bit clock input (BCK). Two devices can be combined to build a stereo application.

Due to its 9µV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 3.4W output power into an 4Ω speaker at 10% THD+N.

AW88082 features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface.

AW88082 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

AW88082 is available in a WLCSP 1.34mmX 1.48mmX0.6mm-9B package.

PIN CONFIGURATION AND TOP MARK

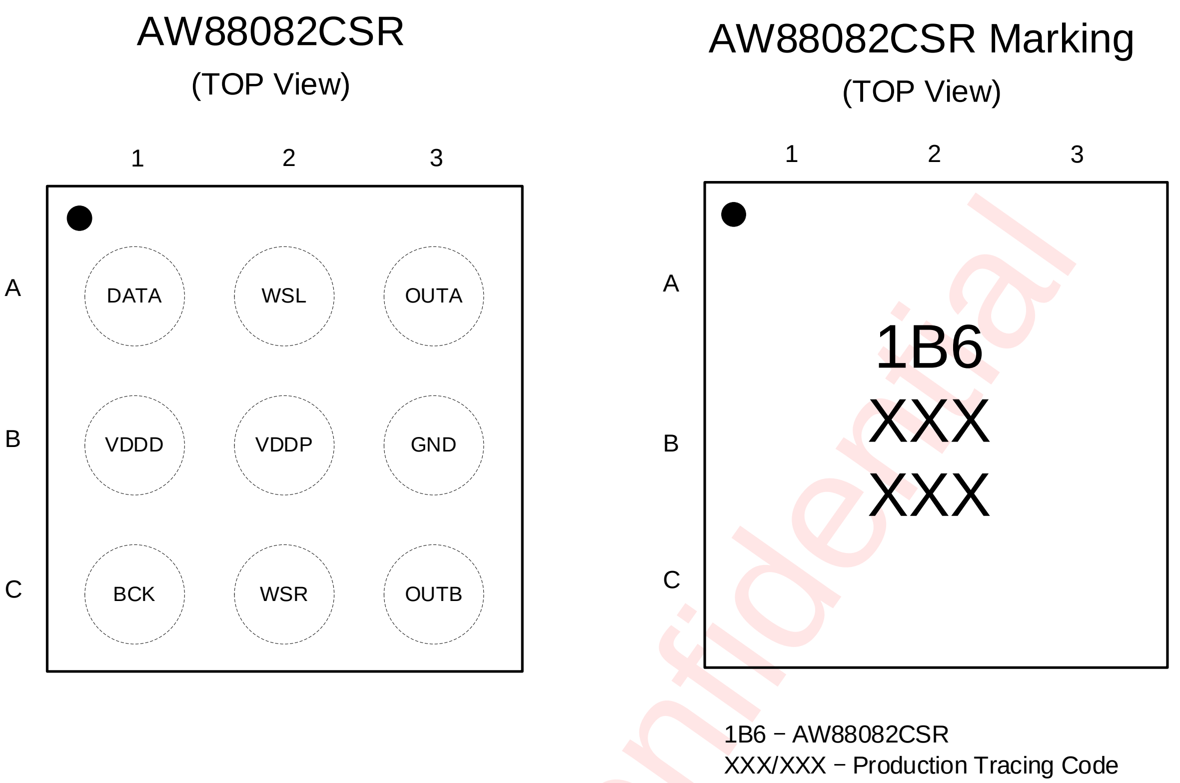

Figure 1 AW88082 pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
A1	DATA	Input data
A2	WSL	I2S word select input/PDM channel select
A3	OUTA	Non-inverting Class-D output
B1	VDDD	Digital power supply
B2	VDDP	Battery power supply
B3	GND	Power ground
C1	BCK	I2S/PDM bit clock input
C2	WSR	I2S word select input
C3	OUTB	Inverting Class-D output

FUNCTIONAL BLOCK DIAGRAM

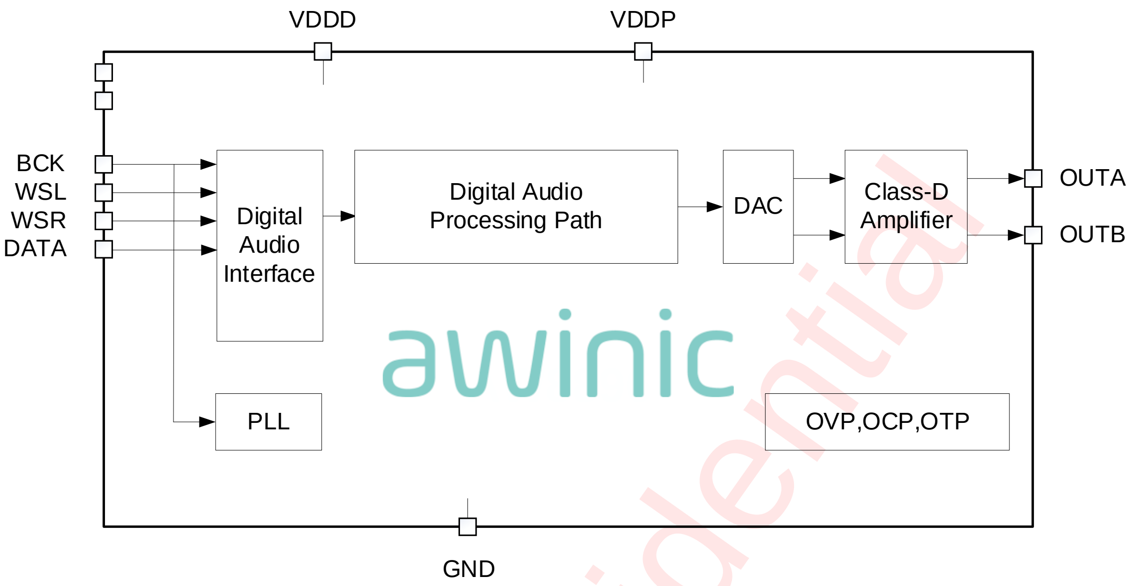

Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

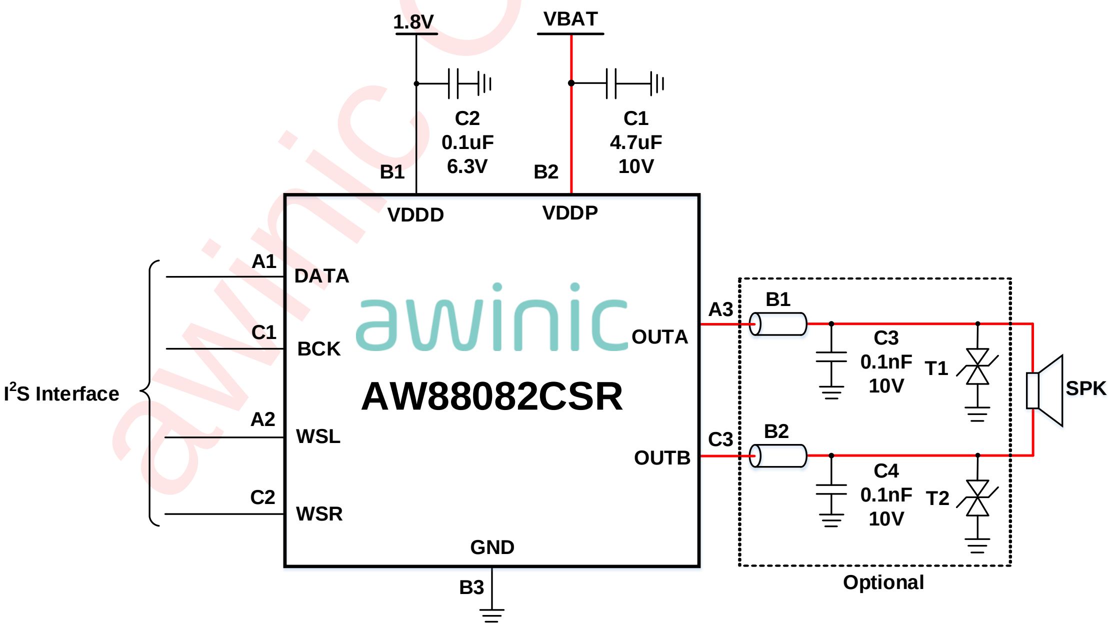

Figure 3 AW88082 Application Circuit

Note: Traces carry high current are marked in red in the above figure

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ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88082CSR	-40℃ ~ 85℃	WLCSP 1.34mmX1.48mmX 0.60mm-9B	1B6	MSL1	RoHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage V_{VDDP}	-0.3V to 6V
Digital Supply Voltage V_{VDDD}	-0.3V to 2V
OUTA/OUTB pin voltage	-0.3 to V_{VDDP} (Note 2)
Minimum load resistance R_L	4Ω
Package Thermal Resistance θ_{JA}	118.93°C/W
Package Thermal Resistance θ_{JT}	7.9°C/W
Package Thermal Resistance θ_{JB}	9.07°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 3,4)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1500V
Latch-up	
Test Condition：JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT：200mA -IT：-200mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*OUITA/OUTB pin can handle 6.5V transients for less than 5ns*

Note 3：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

Note 4：*Test method: JEDEC EIA/JESD22-C101F*

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition：T_A=25°C，VDDP=3.6V，VDDD=1.8V , R_L=4Ω+33μH，f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VDDP}	Battery supply voltage	On pin VDDP	2.5		5.5	V
V_{VDDD}	Digital supply voltage	On pin VDDD	1.65	1.8	1.95	V
I_{VDDP}	Battery supply current	Operating mode,fs=48k		2.25		mA
		Operating mode,fs=32k		1.98		mA
		Standby mode		1.6		μA
		Power down mode, VDDD=0V		1.4	2.3	μA
I_{VDDD}	Digital supply current	Operating mode,fs=48k		2.28		mA
		Operating mode,fs=32k		1.49		mA
		Power down mode		1.5		μA
Class-D						
Po	RMS Output Power	THD+N=1%, R_L=4Ω, VDDP=3.6V, fi=100Hz		1.4		W
		THD+N=1%, R_L=4Ω, VDDP=5V, fi=100Hz		2.74		W
		THD+N=1%, R_L=8Ω, VDDP=3.6V, fi=100Hz		0.76		W
		THD+N=1%, R_L=8Ω, VDDP=5V, fi=100Hz		1.47		W
		THD+N=10%, R_L=4Ω, VDDP=3.6V, fi=100Hz		1.73		W
		THD+N=10%, R_L=4Ω, VDDP=5V, fi=100Hz		3.4		W
		THD+N=10%, R_L=8Ω, VDDP=3.6V, fi=100Hz		0.93		W
		THD+N=10%, R_L=8Ω, VDDP=5V, fi=100Hz		1.82		W
V_{OS}	Output offset voltage	I^2S signal input 0	-10	0	10	mV
F_{PWM}	PWM Switching frequency	Typical Sample Rate: 48kHz		384		kHz
η	Total efficiency	Po=1.3W		91.8		%
THD+N	Total harmonic distortion plus noise	Po=0.1W		0.016		%

Symbol	Description	Test Conditions		Min	Typ.	Max	Units
V_N	Output noise	A-weighting			9		μV
SNR	Signal-to-noise ratio	VDDP=5V, Po=2.3W, A-weighting			109		dB
PSRR	Power supply rejection ratio	$V_{p\text{-}p\_sin}$=200mV	217Hz		84		dB
			1kHz		81		dB
Digital Logical Interface							
V_{IL}	Logic input low level	BCK, WSL,WSR, DATA Pin				0.3 x V_{VDDD}	V
V_{IH}	Logic input high level			0.7 x V_{VDDD}		V_{VDDD}	V
Protection							
T_{SD}	Over temperature protection threshold				150		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
UVP	Under-voltage protection voltage				2.4		V
	Under-voltage protection hysteresis voltage				120		mV

[1] R_L = load resistance + load inductance.

DIGITAL AUDIO INTERFACE TIMING

I2S

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WSL/WSR	32	-	48	kHz
f_{bck}	Bit clock frequency, on pin BCK		64fs		Hz
t_{su}	WSL,WSR, DATA Setup time to BCK	10			ns
t_h	WSL,WSR, DATA hold time to BCK	10			ns

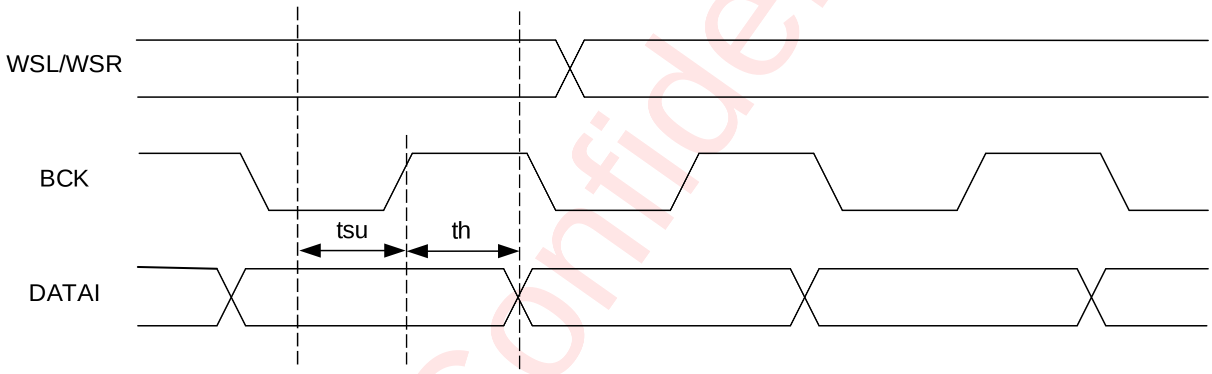


Figure 4 I2S Digital Audio Interface Timing

PDM

Parameter Name		Condition	Min	Typ.	Max	Units
f_{bck}	clock frequency, on pin BCK		3	-	12	MHz
δ_{bck}	clock duty cycle		40		60	%
t_{su}	DATA Setup time to BCK	after clock HIGH	10	-	-	ns
		after clock LOW	10	-	-	ns
t_h	DATA hold time to BCK	after clock HIGH	10	-	-	ns
		after clock LOW	10	-	-	ns

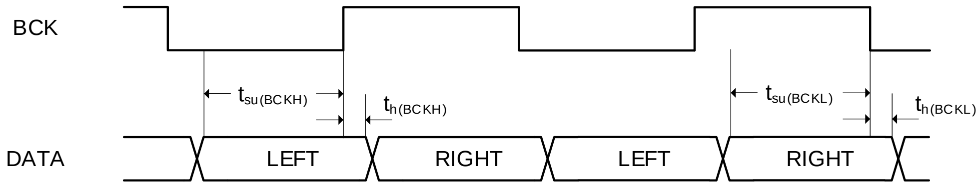
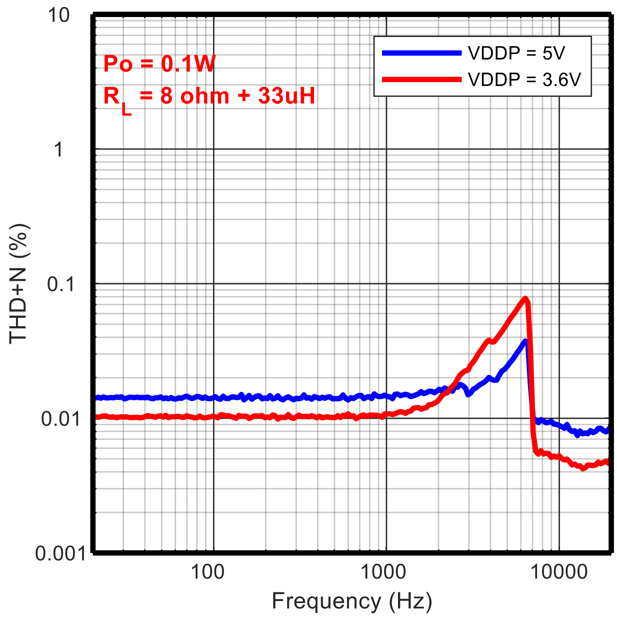


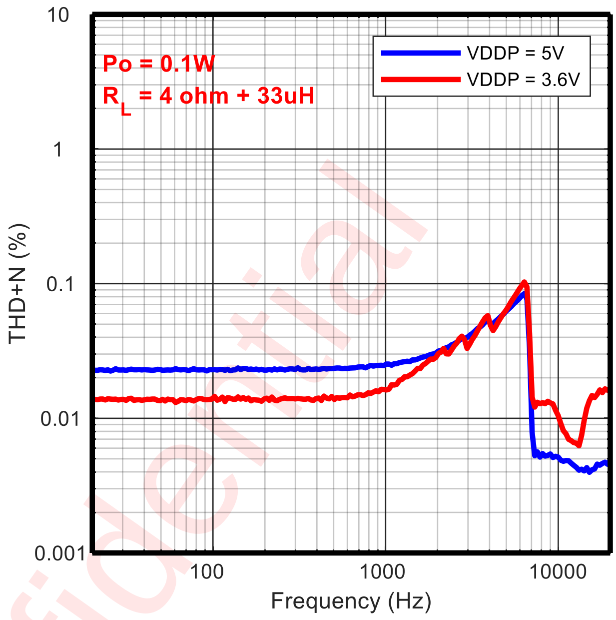
Figure 5 PDM Digital Audio Interface Timing

TYPICAL CHARACTERISTIC CURVES

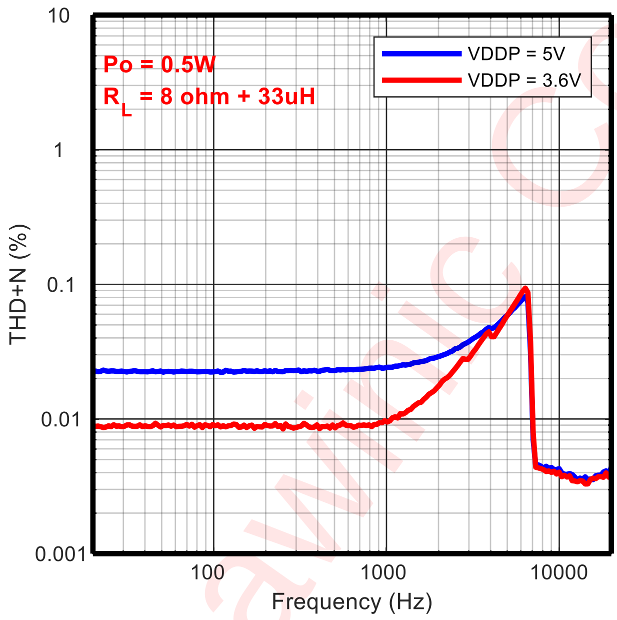
THD+N VS. FREQUENCY



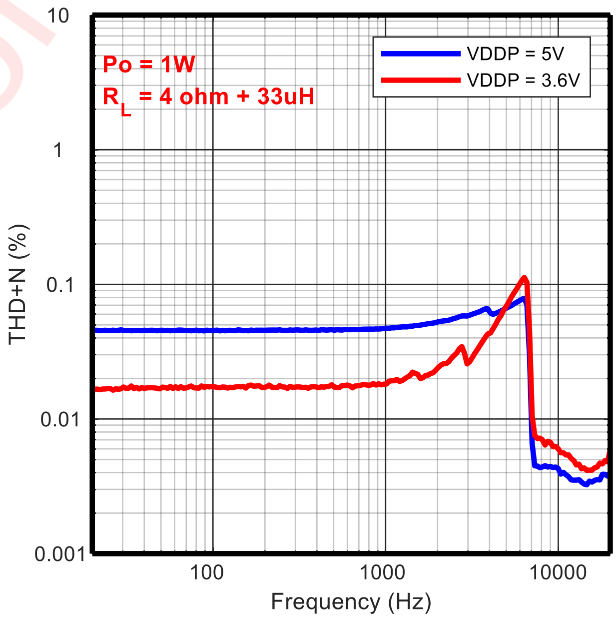
THD+N VS. FREQUENCY

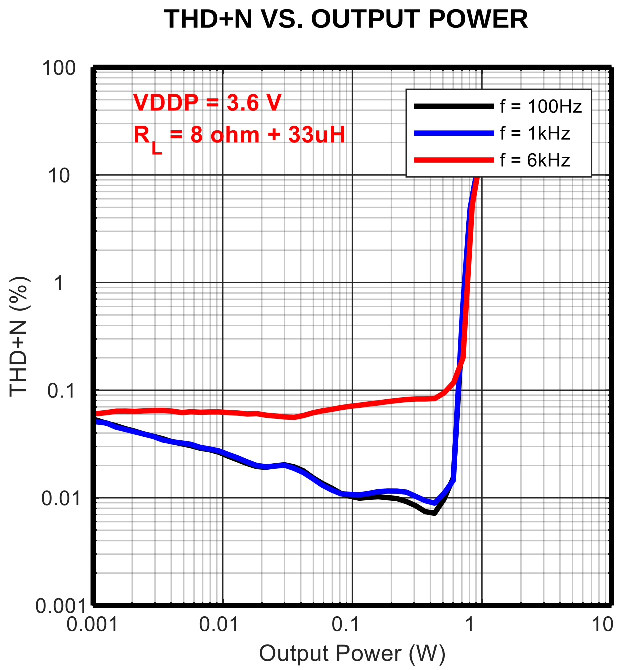


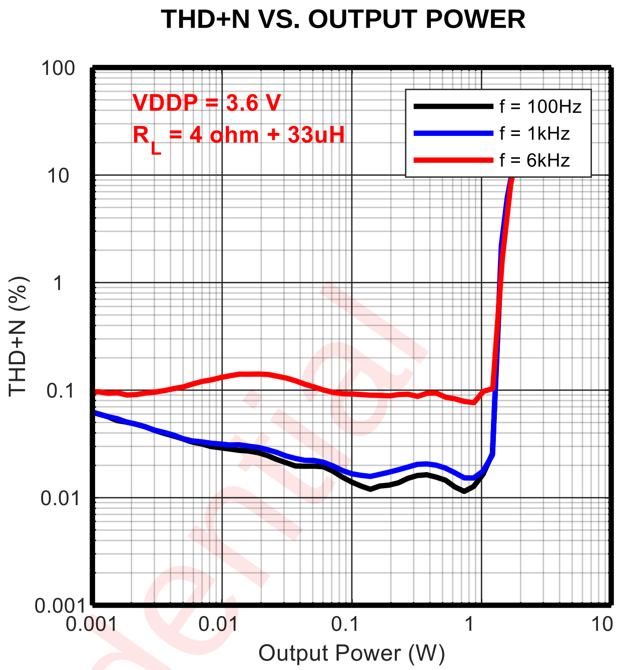
THD+N VS. FREQUENCY

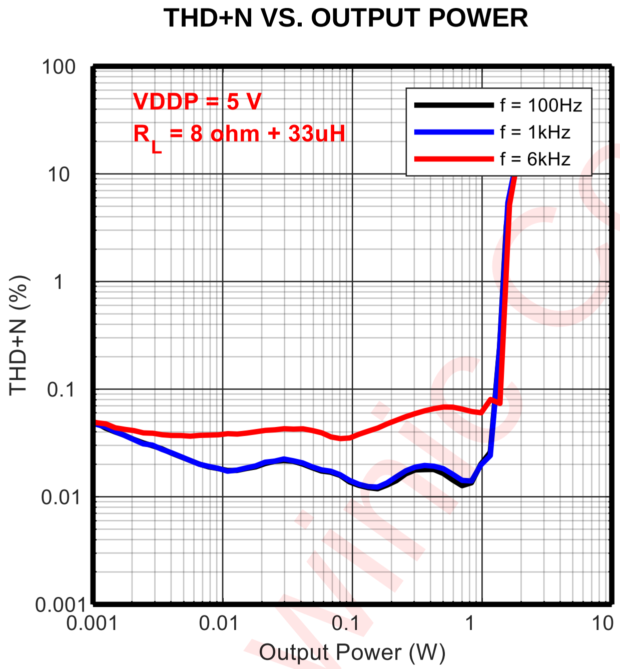


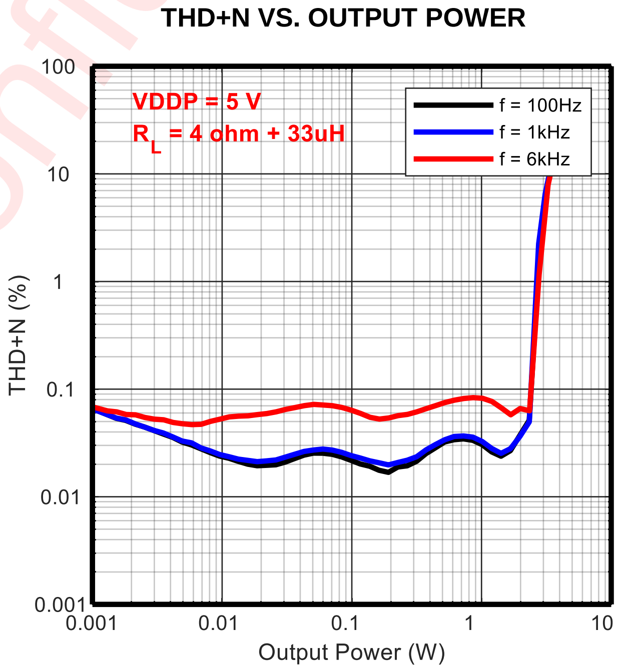
THD+N VS. FREQUENCY

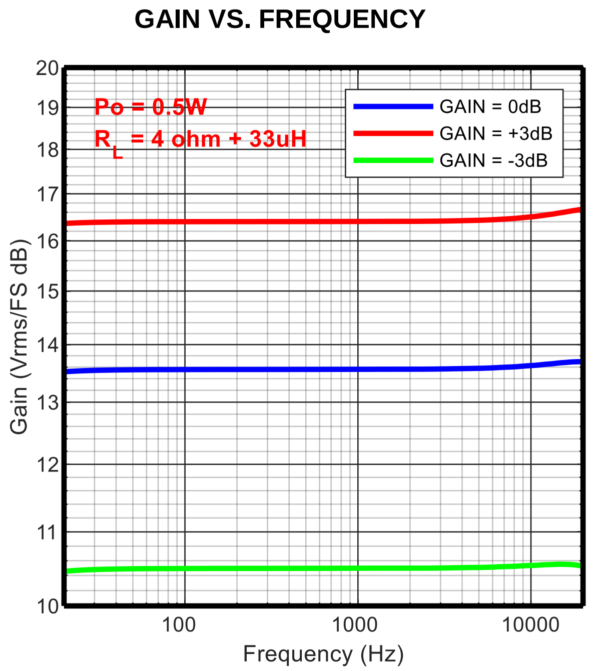


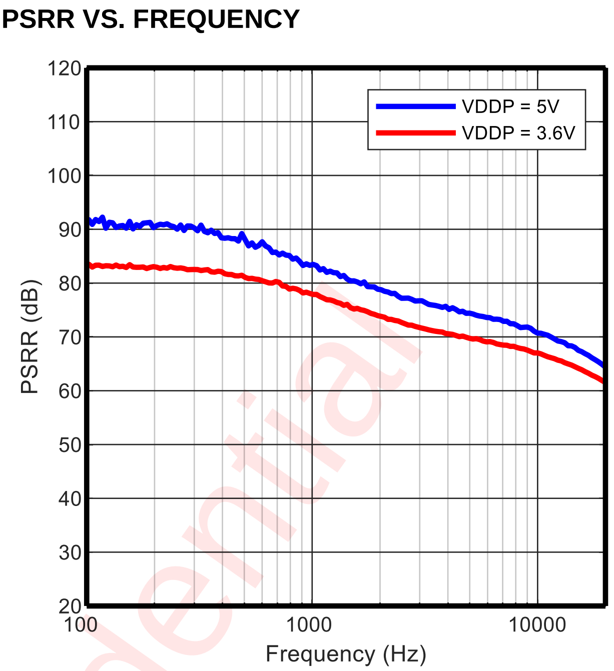

THD+N VS. OUTPUT POWER
VDDP = 3.6 V
R_L = 8 ohm + 33uH
f = 100Hz
f = 1kHz
f = 6kHz
THD+N (%)
Output Power (W)

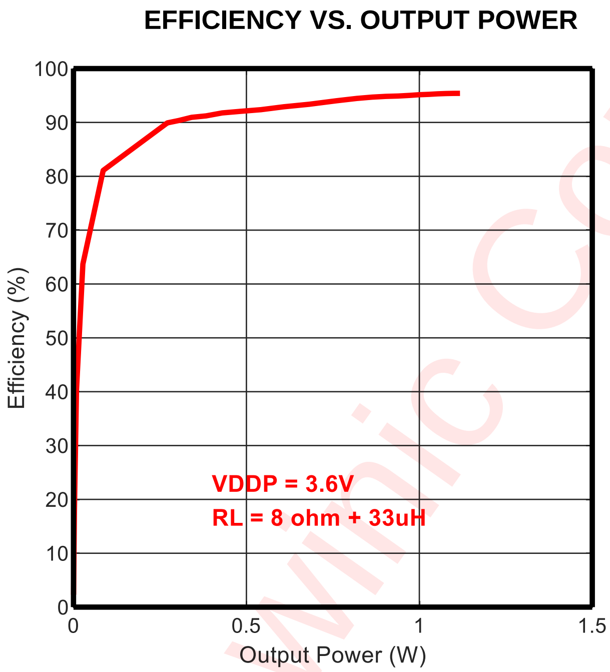

THD+N VS. OUTPUT POWER
VDDP = 3.6 V
R_L = 4 ohm + 33uH
f = 100Hz
f = 1kHz
f = 6kHz
THD+N (%)
Output Power (W)

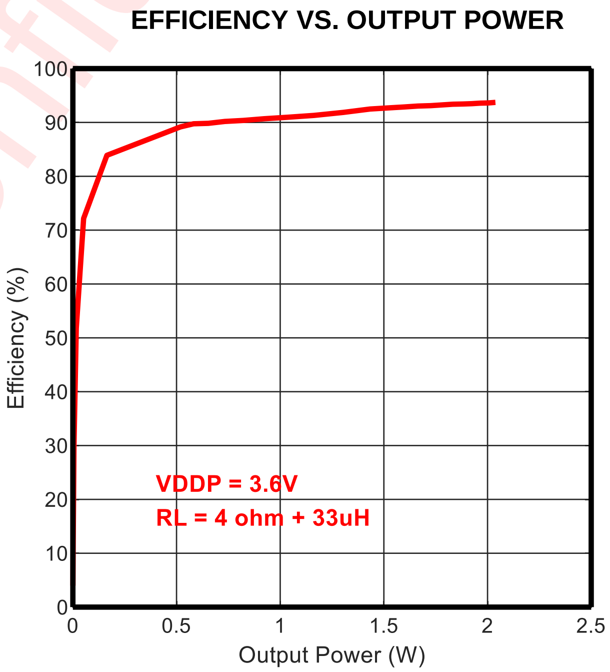

THD+N VS. OUTPUT POWER
VDDP = 5 V
R_L = 8 ohm + 33uH
f = 100Hz
f = 1kHz
f = 6kHz
THD+N (%)
Output Power (W)

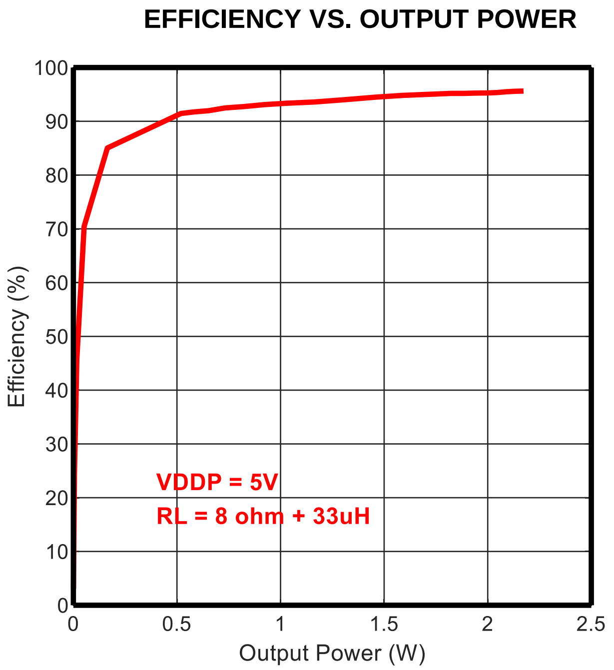

THD+N VS. OUTPUT POWER
VDDP = 5 V
R_L = 4 ohm + 33uH
f = 100Hz
f = 1kHz
f = 6kHz
THD+N (%)
Output Power (W)

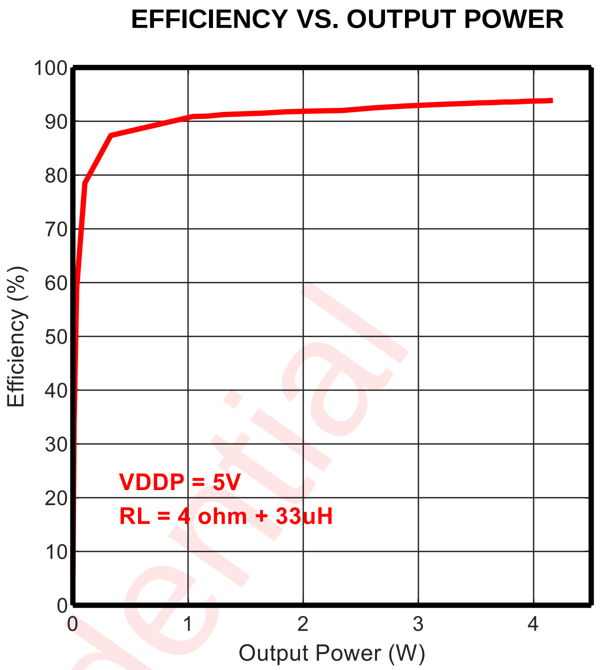

GAIN VS. FREQUENCY
Po = 0.5W
RL = 4 ohm + 33uH
GAIN = 0dB
GAIN = +3dB
GAIN = -3dB
Gain (Vrms/FS dB)
Frequency (Hz)


PSRR VS. FREQUENCY
VDDP = 5V
VDDP = 3.6V
PSRR (dB)
Frequency (Hz)


EFFICIENCY VS. OUTPUT POWER
VDDP = 3.6V
RL = 8 ohm + 33uH
Efficiency (%)
Output Power (W)


EFFICIENCY VS. OUTPUT POWER
VDDP = 3.6V
RL = 4 ohm + 33uH
Efficiency (%)
Output Power (W)


EFFICIENCY VS. OUTPUT POWER
Efficiency (%)
Output Power (W)
VDDP = 5V
RL = 8 ohm + 33uH
100
90
80
70
60
50
40
30
20
10
0
0
0.5
1
1.5
2
2.5


EFFICIENCY VS. OUTPUT POWER
Efficiency (%)
Output Power (W)
VDDP = 5V
RL = 4 ohm + 33uH
100
90
80
70
60
50
40
30
20
10
0
0
1
2
3
4

DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDDP and VDDD supply voltage. When the VDDP supply voltage raises from 0V to 2.1V, or VDDD supply voltage raises from 0V to 1.1V. The internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 3 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	$V_{VDDP} < 2.1V$ $V_{VDDD} < 1.1V$	Power supply is not ready, chipset is power down.
Stand-By	$V_{VDDP} > 2.5V$ $V_{VDDD} > 1.65V$ BCK=0Hz	Power supply is ready, most parts of the device are power down for low power consumption except BCK detect module
Operating	Normal BCK	Amplifier is fully operating

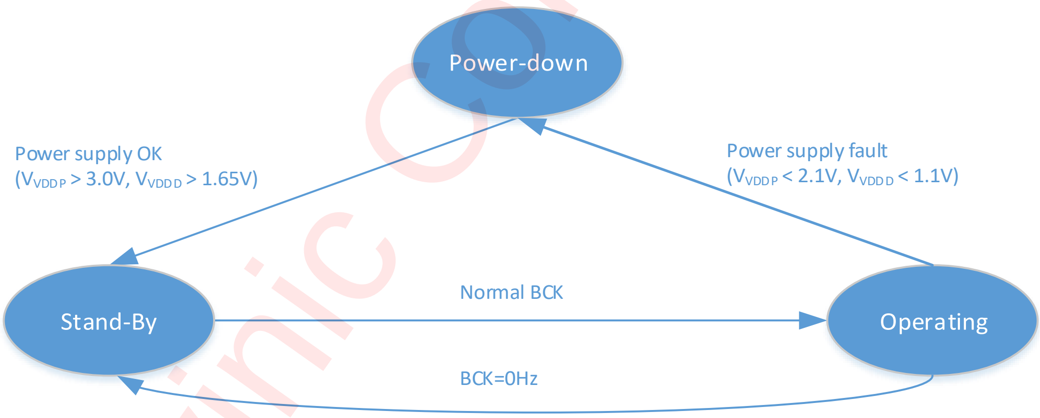


Figure 6 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- $V_{VDDD} < 1.1$ V
- $V_{VDDP} < 2.1$ V

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

$V_{VDDD} > 1.65$ V and $V_{VDDP} > 2.5$ V

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode BCK detect module is working, other modules are still powered down. Customer can set device to mode when the device is no needed to work by close BCK clock.

OPERATING MODE

The device is fully operational in this mode. Amplifier loop will start to work. Applying the BCK clock will case the device switch from STAND-BY mode to OPERATING mode (provide the WS signal is switch on).

SOFTWARE RESET

Writing 0x9A pattern more than 32 times via DATA port (BCK/DATA) will reset the device internal circuits and all configuration registers.

MODE SELECTION

AW88082 support I2S/PDM interface protocol. The default configuration is I2S. Customer can switch to PDM by send PDM pattern.
The way of selecting channel in PDM and I2S mode is different.

I2S

The left or right channel is selected by applying the word select signal to, respectively, the WSL or the WSR terminal. The word select terminal not connected should be connected to VDDD or to PCB ground.
When the word select signal is connected to both terminals, AW88082 amplifies the sum of both channels divided by two.

Table 2 I2S Mode Selection

Mode	Channel	VDDP/VDDD	Frequency on BCK	Frequency on WSL	Frequency on WSR	OUTA/OUTB
Power-Down	-	None	don't care	don't care	don't care	floating
Stand-By	-	3.6V/1.8V (standard)	0Hz	don't care	don't care	floating
Operating	left		2.048 MHz to 3.072 MHz	32 kHz to 48 kHz	0Hz	switching
	right		2.048 MHz to 3.072 MHz	0Hz	32 kHz to 48 kHz	switching
	(left+right)/2		2.048 MHz to 3.072 MHz	32 kHz to 48 kHz	32 kHz to 48 kHz	switching

PDM

The left or right channel is selected by applying VDDD/GND to the WSL terminal.

Table 3 PDM Mode Selection

Mode	Channel	VDDP/VDDD	Frequency on BCK	WSL	WSR	OUTA/OUTB
Power-Down	-	None	don't care	don't care	don't care	floating
Stand-By	-	3.6V/1.8V (standard)	0Hz	don't care	don't care	floating
Operating	left		3.072 MHz to 12.288 MHz	GND	don't care	switching
	right		3.072 MHz to 12.288 MHz	DVDD	don't care	switching

DIGITAL AUDIO INTERFACE

I2S INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 3 dedicated pins:

- BCK
- WS
- DATA

AW88082 supports the Philips I2S standard with a BCK frequency 64 times sampling rate(64fs). The bit length can be from 8 bits to 32 bits. Supported I2S sample rates are listed in Table 4 while Figure 7 illustrates the I2S data transfer format.

The word clock WS is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 32 kHz, 44.1 kHz, 48 kHz.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length.

The word select and bit clock signals of the I^2S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel.

Table 4 Support I2S sample rates

Interface format(MSB first)	Data width	BCK frequency
Standard I2S	8bits to 32bits	64fs

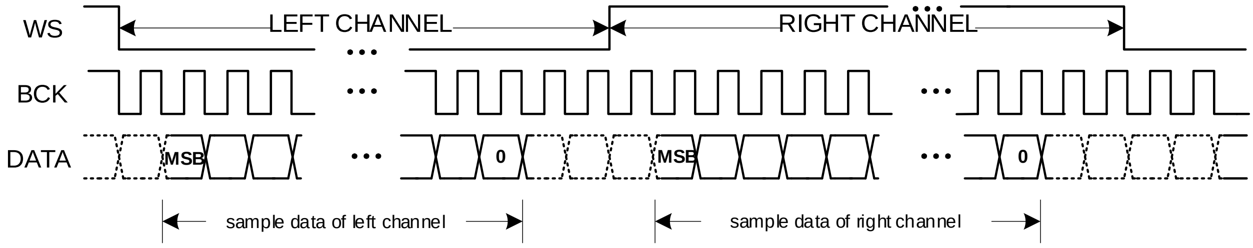


Figure 7 I²S Timing for Standard I²S Mode

- When WS=0 indicating the left channel data, and WS=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

PDM INTERFACE

AW88082 supports the digital stereo PDM stream illustrated in Figure 8. The BCK frequency support 3M/6M/12M.

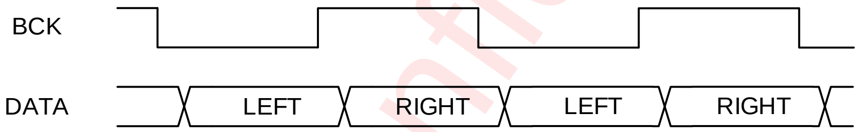


Figure 8 Digital stereo PDM Timing

Table 5 shows the pin control configuration for left and right selection.

Table 5 PDM Left/right selection

WSL pin state	WSR pin state	Description
GND	don't care	left content amplified
VDDD	don't care	right content amplified

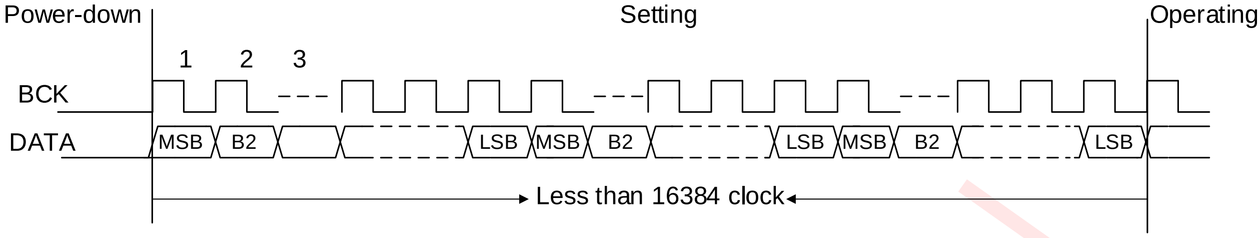
CONTROL SETTINGS

If the device can operate effectively with the default settings, the control settings does not need to be changed.

CONTROL SETTING PATTERN RECOGNITION

AW88082 can detect control settings via the DATA interface(BCK/DATA). Control settings are selected by transmitting control patterns on the DATA input during the power-up sequence (the first 16384-bit clock cycles). When PDM mode switching pattern (0x93/0x95/0x96) is detected, the timer will stop.

Figure 9 illustrates the control setting sequence. After receiving 128 consecutive control pattern 0xAA, AW88082 activates the appropriate control setting (see the third column of Table 6) and switch to operating mode. Control settings remain unchanged in all modes unless control pattern 0x9A is received or the VDDD supply voltage is removed.



LSB = Least Significant Bit; MSB = Most Significant Bit; B2 = Second Most Significant Bit;

NOTE:WS works properly according to the I2S protocol.

Figure 9 Power-up/power-down timing (with control settings)

Table 6 Control settings

Pattern	Related bytes[1]	Control settings
0x87	0xC3/E1/F0/78/3C/1E/F	HAGC enable
0x8B	0xC5/E2/71/B8/5C/2E/17	slope low (EMC)
0x8D	0xC6/63/B1/D8/6C/36/1B	gain = −3 dB (VDDP = 2.5 V);
0x8E	0x47/A3/D1/E8/74/3A/1D	gain = +3 dB (VDDP = 5.0 V);
0x93	0xC9/E4/72/39/9C/4E/27	switch to PDM-3M mode
0x95	0xCA/65/B2/59/AC/56/2B	switch to PDM-6M mode
0x96	0x4B/A5/D2/69/B4/5A/2D	switch to PDM-12M mode
0x9A	0x4D/A6/53/A9/D4/6A/35	reset settings to default[2]

[1] The related bytes are the pattern list from the first column phase shifted by 1,2, 3, 4, 5, 6 and 7 bits.

[2] Reset pattern needs to be written more than 32 times, others need to be written more than 16 times.

HAGC ENABLE

The audio power amplifier with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain.

PWM SLOPE SELECTION

The rise and fall times of the PWM output edges can be set to one of two values, as detailed in Table 7. The default setting is 'slope normal' (3.6 ns with VDDP = 3.6 V). 'Slope low' is selected via control setting 0x8B (see Table 6). This function is implemented to reduce Electro Magnetic Interference (EMI).

Table 7 Slope rise and fall times

Setting	Description
slope low	6ns at VDDP = 3.6 V
slope normal; default setting	3.6ns at VDDP = 3.6 V

GAIN SELECTION

Signal conversion from digital audio in to PWM modulated audio out is independent of supply voltages VDDP and VDDD. At the default gain setting (0 dB), the audio output signal level is just below the clipping point at a supply voltage of 3.6 V at -6 dBFS (peak) input.

AW88082 supports two further gain settings to support full output power at VDDP = 2.5 V and VDDP = 5.0 V. The gain settings can be selected via silence patterns 0x8D and 0x8E.

Table 8 details the corresponding peak output voltage level at -6 dBFS for the three gain settings.

All parameters are guaranteed for VDDP = 3.6 V; VDDD = 1.8 V; RL = 4Ω+33μH[1], fi = 1kHz, fs = 48kHz, Tamb = 25 °C, default settings; unless otherwise specified

Table 8 Output voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OM}	peak output voltage	at −6 dBFS (peak) digital input				
		gain = −3 dB, VDDP = 2.5 V, R_L = 4 Ω		2.4		V
		gain = 0 dB, VDDP = 3.6 V, R_L = 4 Ω; default		3.4		V
		gain = +3 dB, VDDP = 5.0 V, R_L = 8 Ω		4.7		V

[1] R_L = load resistance + load inductance.

PDM MODE

PDM mode is activated when the PDM switching silence pattern (at least 16 consecutive 0x93/95/96 bytes) is applied on the DATA input.

RESET

Writing 0x9A pattern more than 32 times via DATA port (BCK/DATA) will reset the device internal circuits and all configuration registers.

POWER-UP/POWER-DOWN SEQUENCE

AW88082 power-up/power-down sequence is shown in Figure 10. External power supplies VDDP and VDDD should be within their operating limits before AW88082 switches to Operating mode. AW88082 would be switched to power-down mode when the power supplies are disconnected or turned off.

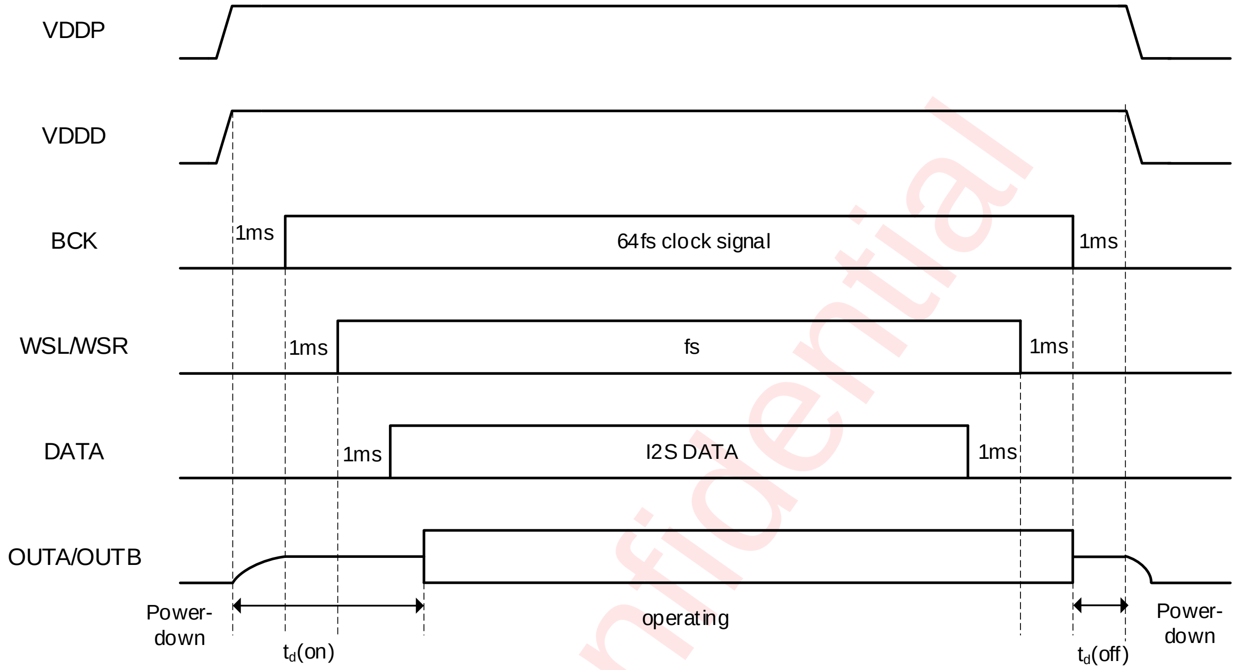


Figure 10 Power-up/power-down timing (without control settings)

All parameters are guaranteed for VDDP = 3.6 V; VDDD = 1.8 V; RL = 4Ω+33μH[1], fi = 1kHz, fs = 48kHz, Tamb = 25 °C, default settings; unless otherwise specified

Table 9 Power-up/power-down timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_d(on)	turn-on delay time	-			6	ms
t_d(off)	turn-off delay time	-			7	μs

[1] R_L = load resistance + load inductance.

[2] all results are Inversely proportional to fs.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- HDCC
- Hardware AGC

The signal processing flow in the DAP (Digital Audio Processor) is illustrated in the following figure.

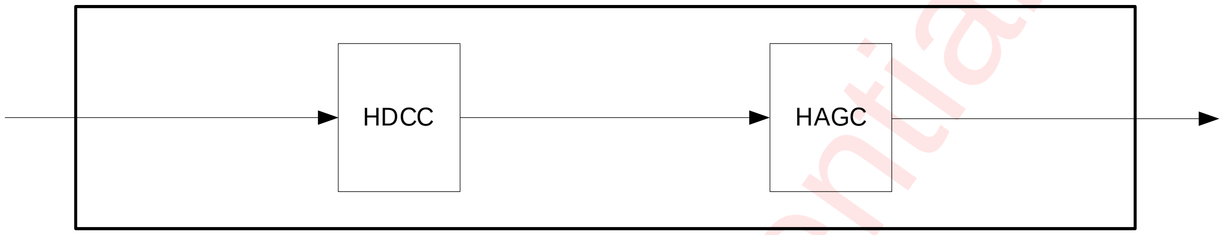


Figure 11 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker, such as in the 5V power supply, as for 4Ω speaker, the maximum undistorted power is about 3.4W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the hardware AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The circuit of device has integrated the over voltage protection control loop. When the voltage of VDDP is above the threshold, the device will stop working, until the voltage of VDDP going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when OUTA/OUTB is short to VDDP/GND or OUTA is short to OUTB, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

APPLICATION INFORMATION

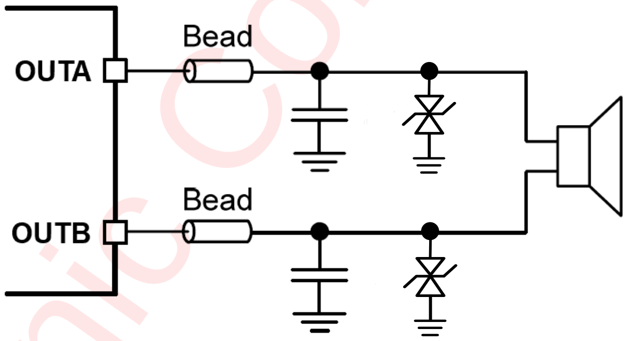
EXTERNAL COMPONENTS

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 4.7μF low equivalent-series-resistance (ESR) ceramic capacitor is recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 4.7μF ceramic capacitor, place a 10μF capacitor on the VDDP supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

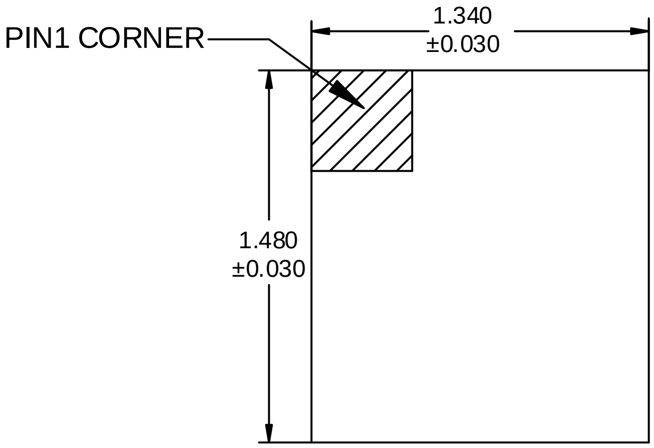
If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 10V. The output(OUTA/OUTB) can reserve ESD devices, used to improve ESD protection capabilities.



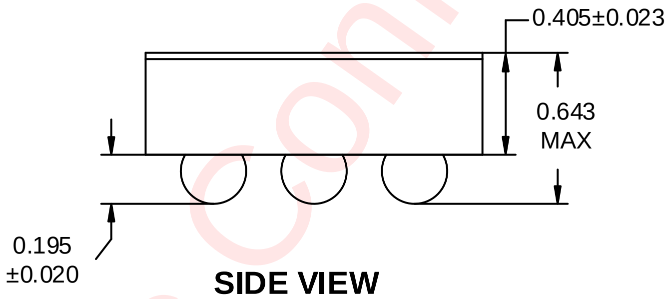
LAYOUT CONSIDERATION

In order to obtain excellent performance of the PA, the below PCB layout guidelines should be followed:
All the filter capacitors should be placed close to the corresponding pins of the PA, including VDDP, VDDD.
The beads and capacitor should be placed close to the OUTA and OUTB pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 1.2mm.
The via numbers determine the current capability.

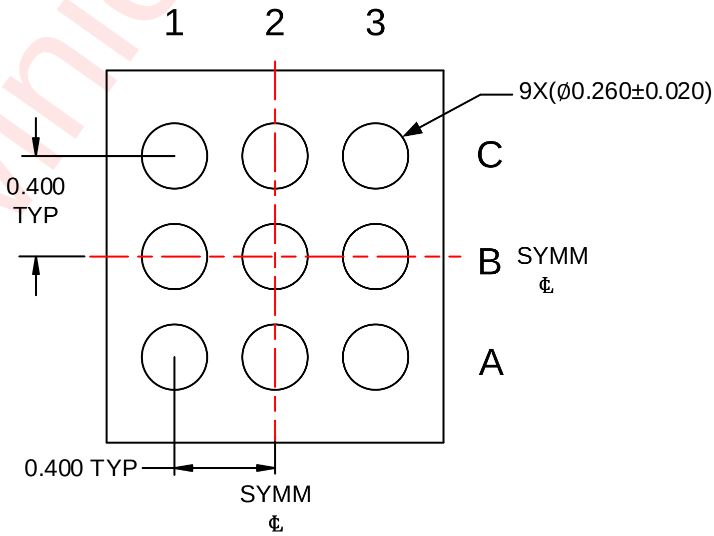
PACKAGE DESCRIPTION



TOP VIEW



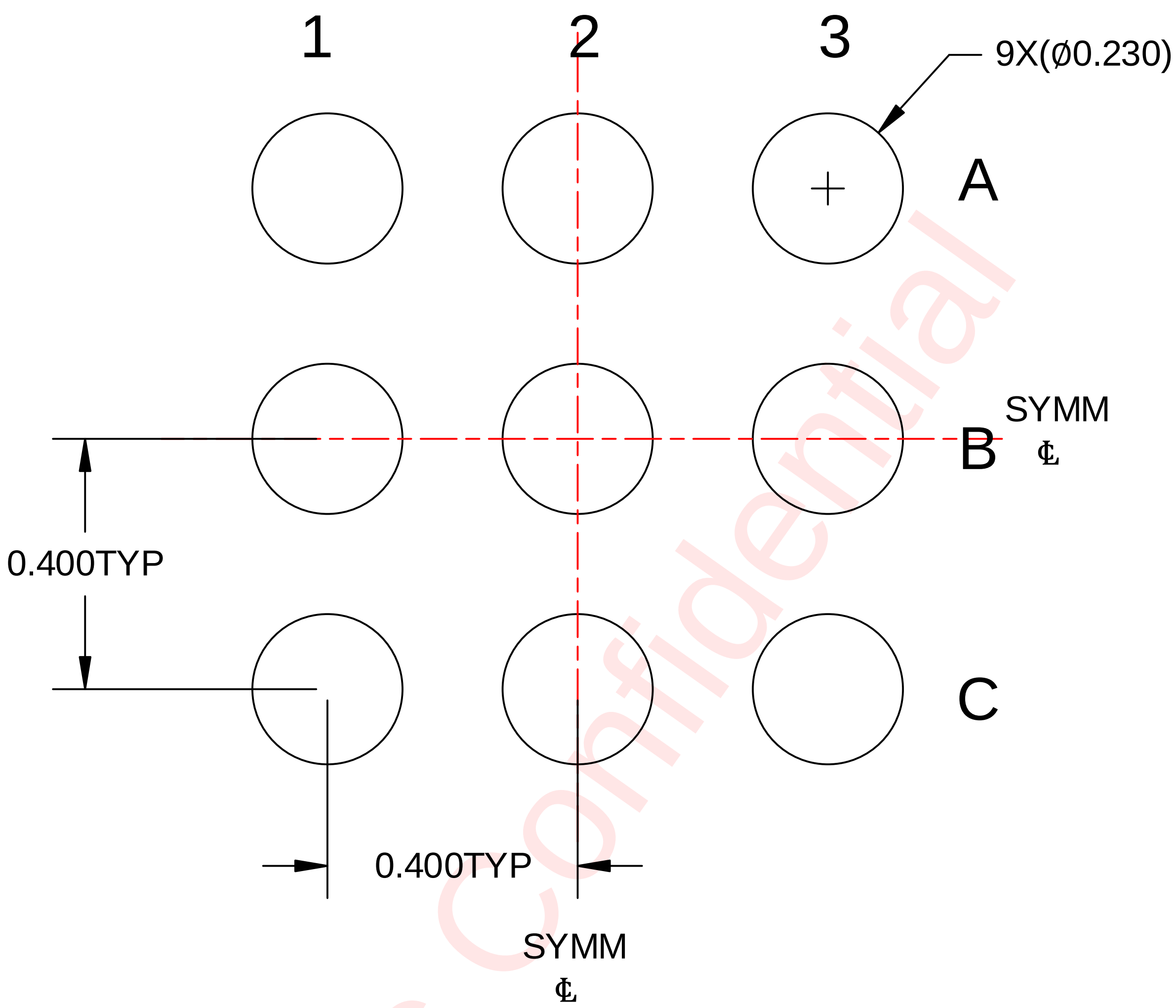
SIDE VIEW

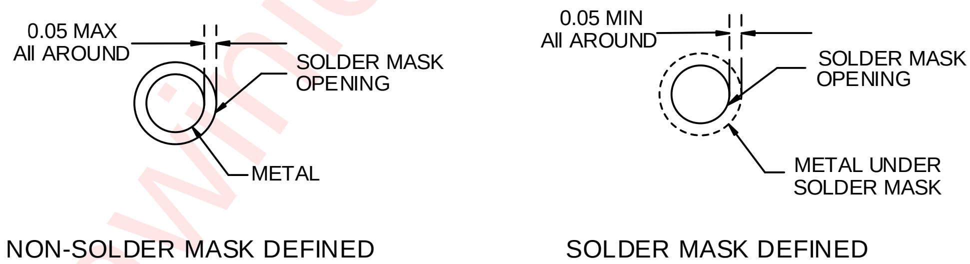


BOTTOM VIEW

Unit: mm

LAND PATTERN DATA

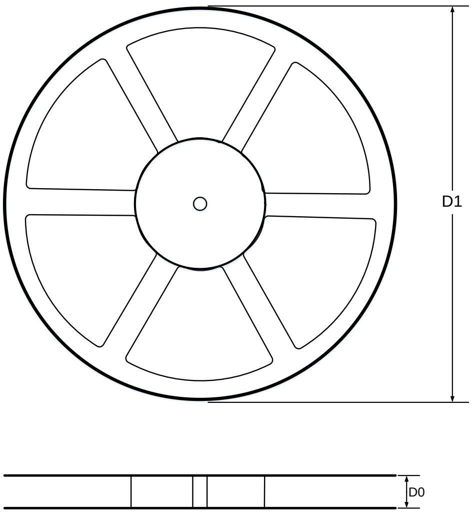




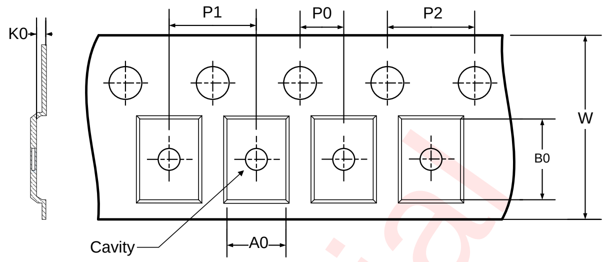
Unit: mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

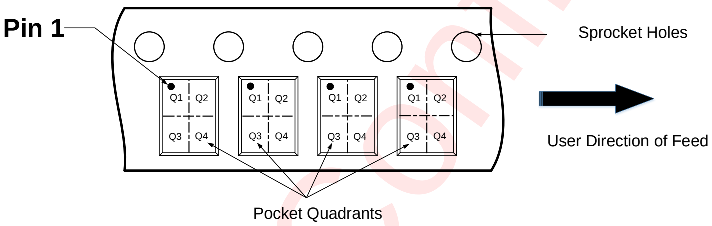


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.48	1.7	0.74	2	4	4	8	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Sep. 2023	Officially Released
V1.1	Feb.2024	1. Changed PIN definition , A3:OUTA;C3:OUTB; 2. Changed the description of PDM Mode Selection.

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