36V Low Power Quad Differential Comparators

Features

- Supply Operation From 2.5 V to 36 V
  ±1.25V to ±18V
- Response time: 1.3 μs(typ) at V_{CC} = 5 V
- Low Current Consumption:109 μA/ch
- Low Input Bias Current:130 pA
- Low Input Offset Voltage: ±0.6 mV(typ)
- Input Common-mode Voltage Range Includes Ground
- Internal Differential Input Voltage Range Equal to the Supply Voltage
- TTL, DTL, ECL, MOS, CMOS compatible Outputs
- Open drain output
- Wide Temperature Range: -40 °C to 125 °C
- High ESD Tolerance: 6 kV HBM, 2 kV CDM

Applications

- Peak and Zero-crossing Detectors
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- High-speed Line or Digital Line Receivers
- High Speed Sampling Circuits

General Description

The AWS72901 consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Quiescent current is independent of the supply voltage. The device is the most cost-effective solutions for applications where low offset voltage, high supply voltage capability, low supply current, and space saving are the primary specifications in circuit design for portable consumer products.

The AWS72901 is available in green small-size SOP - 14L package.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS72901	SOP - 14L	3.9mm × 8.65mm

Typical Application Circuit

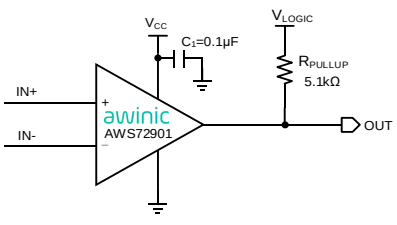
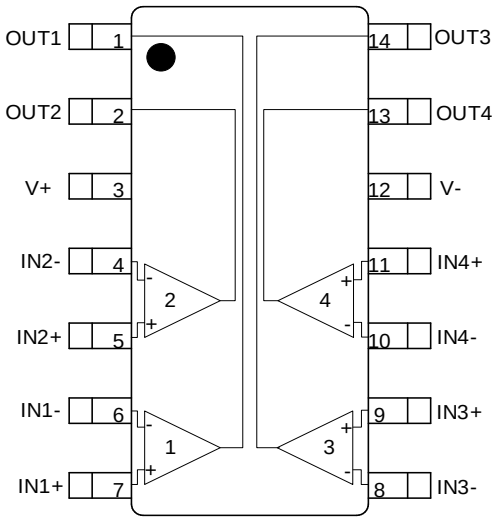


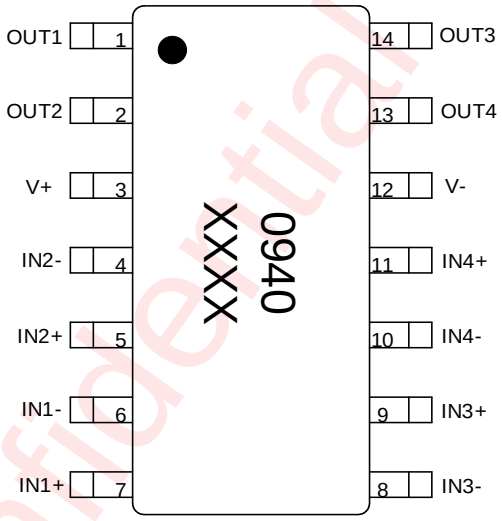
Figure 1 Typical Application of AWS72901

Pin Configuration And Top Mark

AWS72901SPR
(Top view)



AWS72901SPR
(Top view)



0940 - AWS72901SPR
XXXX - Production Tracing Code

Figure 2 Pin Configuration

Pin Definition

PIN		DESCRIPTION
NAME	SOP - 14L	
OUT1	1	Channel 1 output
OUT2	2	Channel 2 output
V+	3	Positive (high) supply
IN2-	4	Channel 2 inverting input
IN2+	5	Channel 2 noninverting input
IN1-	6	Channel 1 inverting input
IN1+	7	Channel 1 noninverting input
IN3-	8	Channel 3 inverting input
IN3+	9	Channel 3 noninverting input
IN4-	10	Channel 4 inverting input
IN4+	11	Channel 4 noninverting input
V-	12	Negative (low) supply or ground (for single-supply operation)
OUT4	13	Channel 4 output
OUT3	14	Channel 3 output

Functional Block Diagram

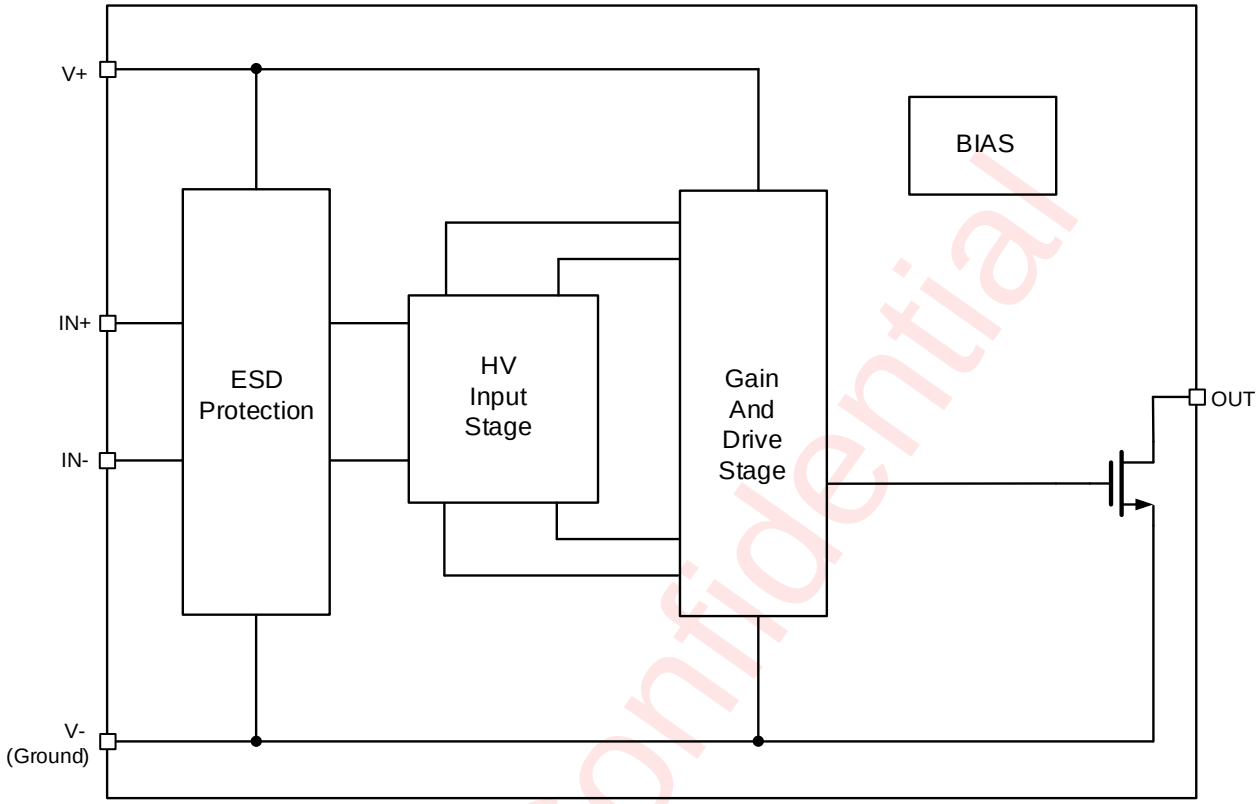


Figure 3 Functional Block Diagram

Typical Application Circuits

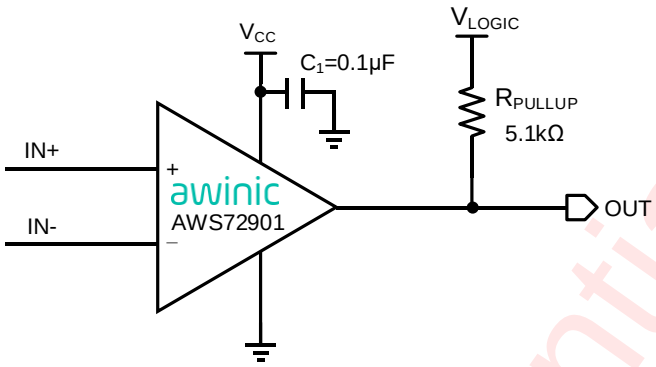


Figure 4 AWS72901 Application Circuit

- ***Notice for typical application circuits:***

1. Bypass capacitors C_1 is used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces. If negative supply is connected to GND, then negative supply to GND can be disconnected to bypass ceramic.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS72901SPR	-40 °C ~ 125 °C	SOP - 14L	0940	MSL3	RoHS+HF	2500 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS	RANGE
Supply voltage, V_S = (V+) - (V-)	42 V
Input Voltage	(V-) - 0.3 V to (V+) + 0.3 V
Output Current: OUT	±20 mA
Output short-circuit (NOTE 2)	Infinite
Operating free-air temperature range T_A	-40 °C to 125 °C
Maximum operating junction temperature T_{JMAX}	150 °C
Storage temperature T_{STG}	-65 °C to 150 °C
Lead temperature (soldering 10 seconds)	260 °C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2:A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 3)	±6	kV
CDM (NOTE 4)	±2	kV
Latch-Up (NOTE 5)	±150	mA

NOTE3: *The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023*

NOTE4: Test method: ESDA/JEDEC JS-002-2022

NOTE5: Test method: JESD78F

Thermal Information

THERMAL METRICS		AWS72901	UNIT
		SOP	
SYMBOL	PARAMETER	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

Electrical Characteristics

Electrical characteristics at V_{CC} = 5 V, T_A = 25 °C, V_{CM} = V_{CC}/2,(unless otherwise specified).

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage			2.5		36	V
V_{OS}	Input offset voltage	V_{CC} = 2.5 V to 36 V		-3	±0.6	3	mV
		-40 °C ~ 125 °C		-6		6	mV
I_{OS}	Input offset current				45		pA
I_B	Input bias current				130		pA
I_{Diff}	Input Differential Current				10		nA
C_{IN}	Input Capacitance	Differential(1)			2		pF
		Common Mode			3.5		pF
V_{CM}	Common-mode Input Voltage Range	25 °C		0		V_{CC} - 1.5	V
		-40 °C ~ 125 °C		0		V_{CC} - 2	V
A_{VD}	Large-signal Differential Voltage Amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4V, R_L ≥ 15 kΩ to V_{CC}		100	500		V/mV
I_{OH}	High-level Output Current	V_{CC} = V_{OH} = 5 V, V_{ID} = 1 V			3.7	200	nA
		V_{CC} = V_{OH} = 36 V, V_{ID} = 1 V, -40 °C ~ 125 °C			75	7000	nA
V_{OL}	Low-Level Output Voltage	I_{OL} = 4 mA, V_{ID} = −1 V			220	400	mV
I_{OL}	Low-Level Output Current	V_{OL} = 1.5 V, V_{ID} = −1 V		10	24		mA
I_Q	Quiescent Current per Comparator	V_{CC} = 5 V			107	150	μA
		V_{CC} = 36 V			109	150	μA
t_{RT}	Response Time	R_L connected to 5 V through 5.1 kΩ, C_L= 15 pF	100-mV input step with 5-mV overdrive		1.3		μs
			TTL-level input step		0.16		μs

(1) The values are guaranteed by design.

Typical Characteristics

At T_A = 25 °C, V_{CC} = 5 V, V_{CM} = 0 V, R_L = Open, unless otherwise noted.

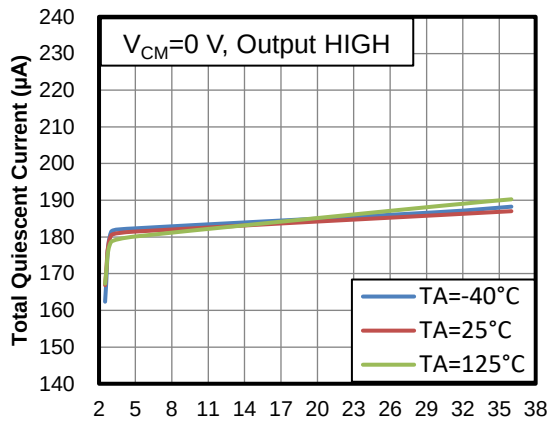


Figure 5 I_Q vs. V_{CC}

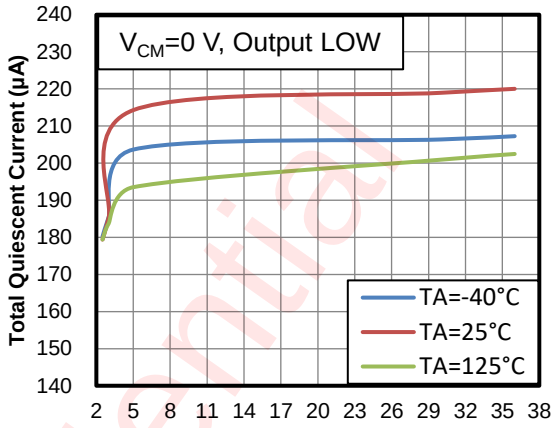


Figure 6 I_Q vs. V_{CC}

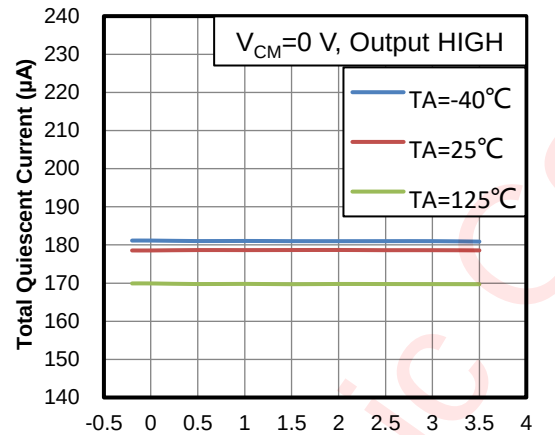


Figure 7 I_Q vs. V_{CM} at V_{CC}=5V

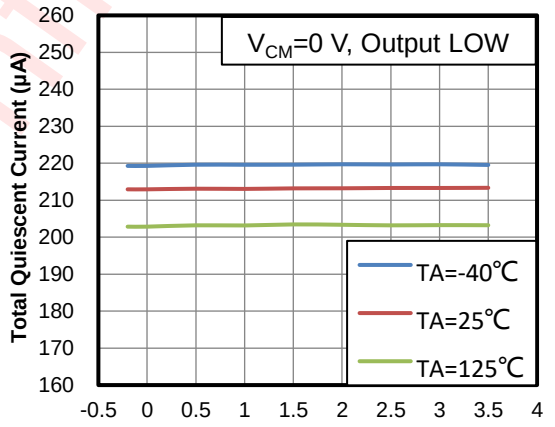


Figure 8 I_Q vs. V_{CM} at V_{CC}=5V

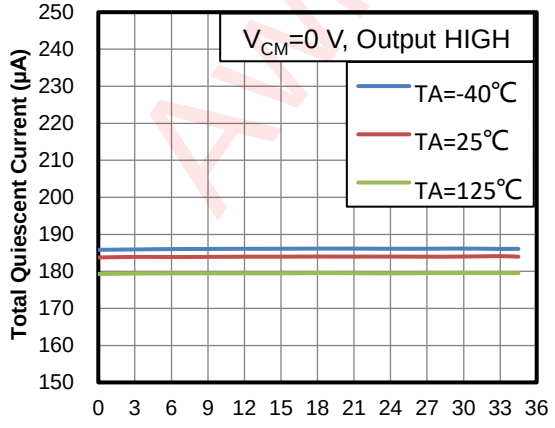


Figure 9 I_Q vs. V_{CM} at V_{CC}=36V

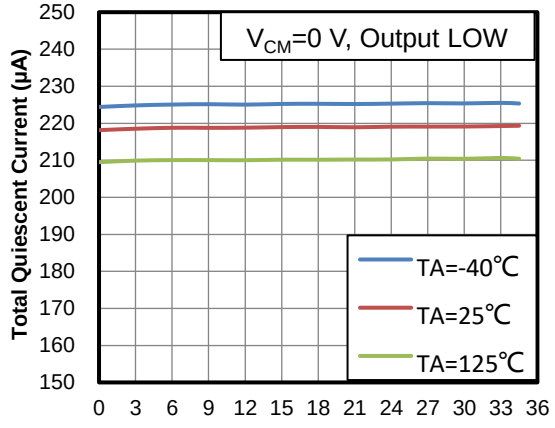


Figure 10 I_Q vs. V_{CM} at V_{CC}=36V

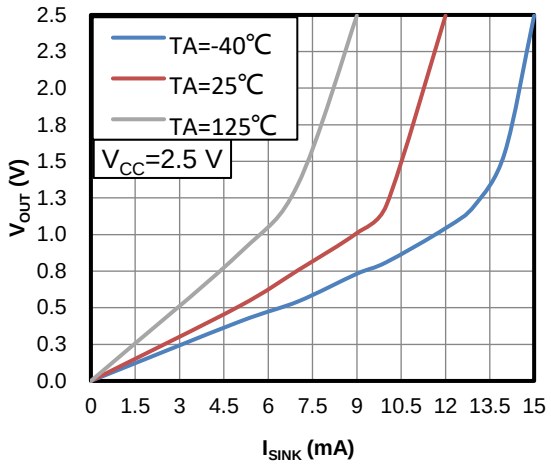


Figure 11 V_{OUT} vs. I_{SINK}

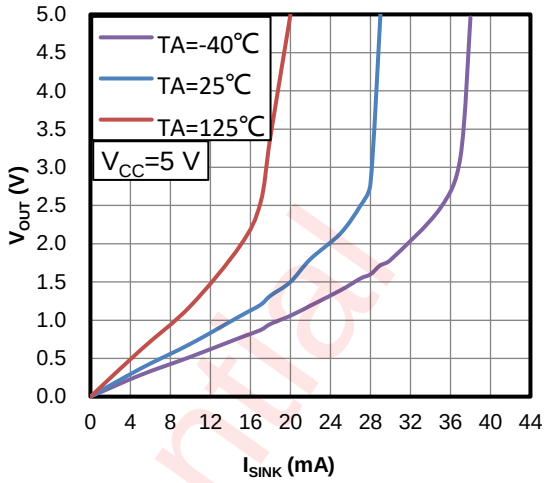


Figure 12 V_{OUT} vs. I_{SINK}

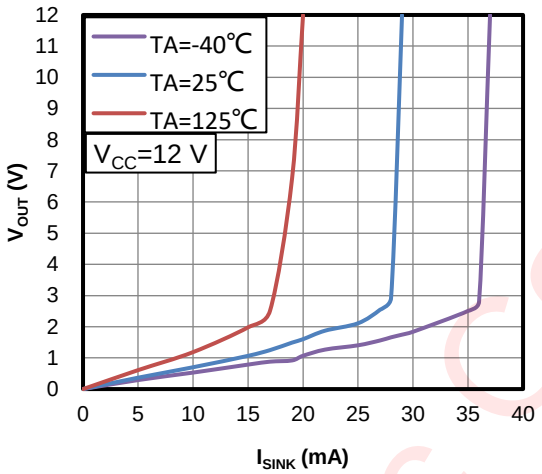


Figure 13 V_{OUT} vs. I_{SINK}

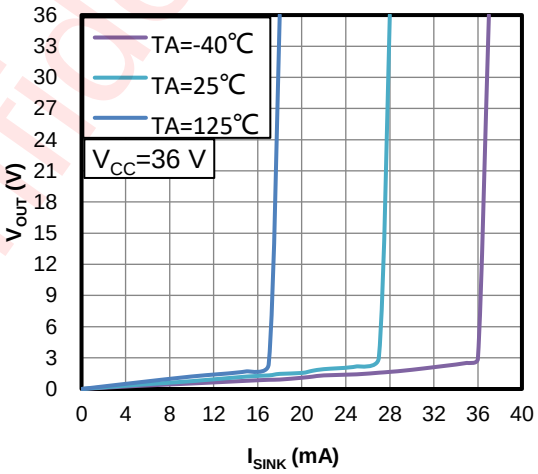


Figure 14 V_{OUT} vs. I_{SINK}

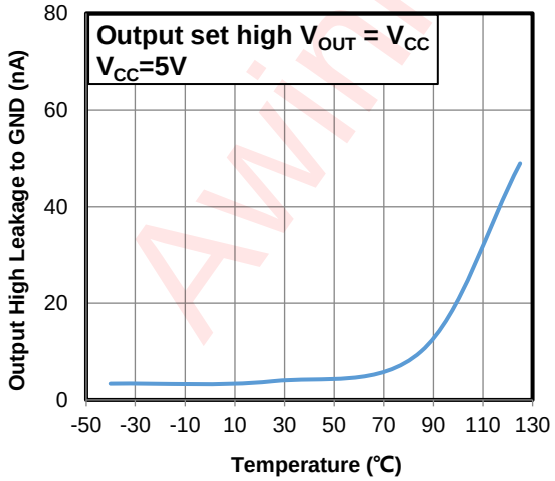


Figure 15 I_{OH} vs. Temperature

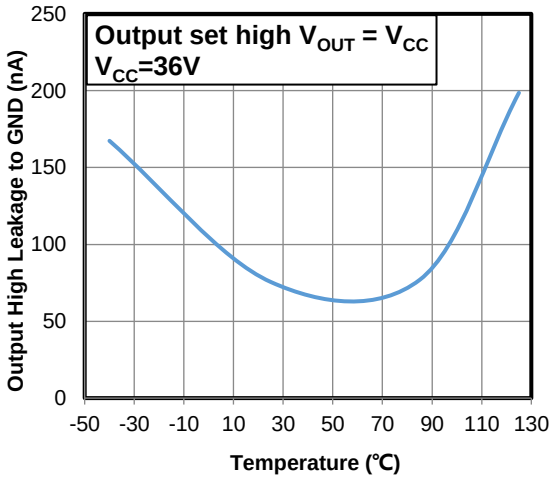


Figure 16 I_{OH} vs. Temperature

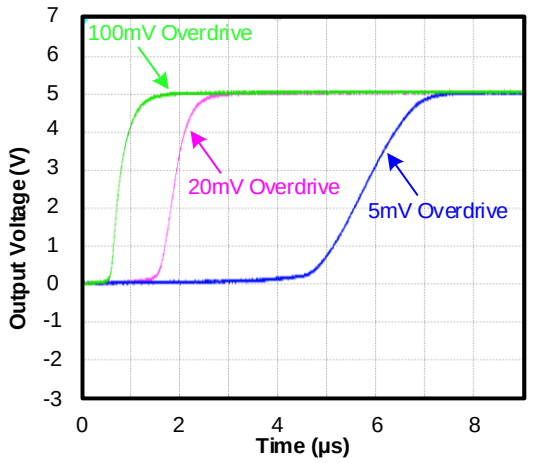


Figure 17 Response Time for Various Input Overdrives: Positive Transition

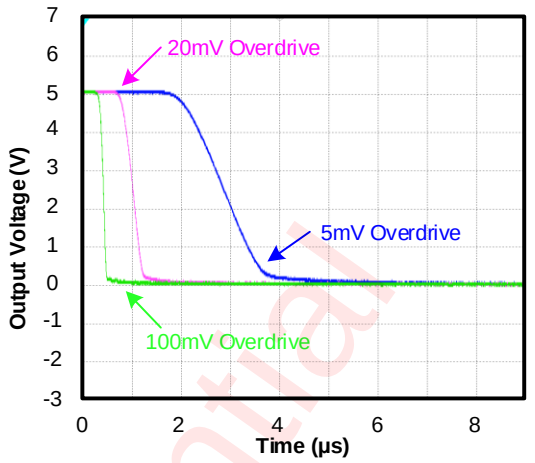


Figure 18 Response Time for Various Input Overdrives: Negative Transition

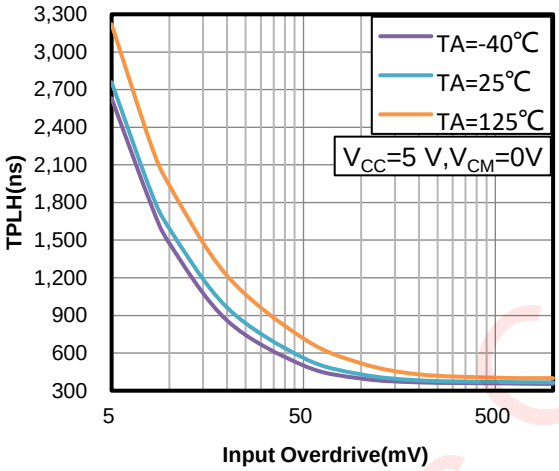


Figure 19 TPLH vs. Input Overdrive

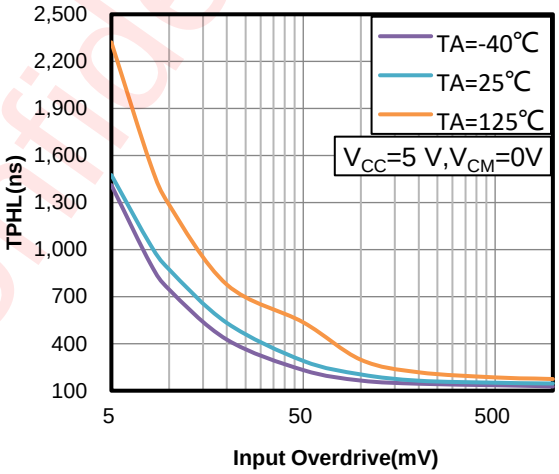


Figure 20 TPHL vs. Input Overdrive

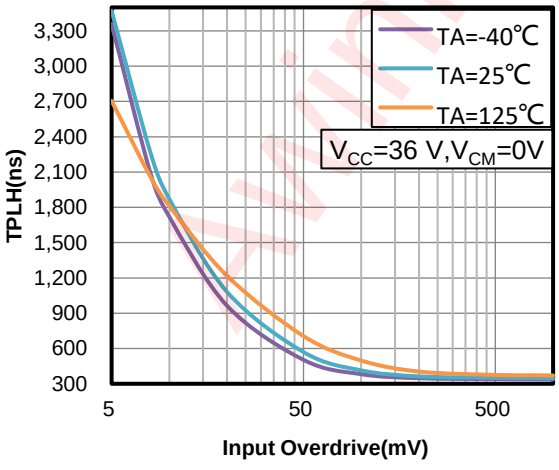


Figure 19 TPLH vs. Input Overdrive

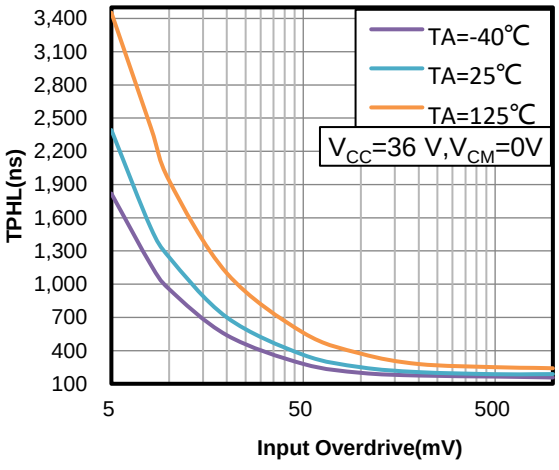


Figure 20 TPHL vs. Input Overdrive

Detailed Functional Description

These four comparators have the ability to operate up to absolute maximum of 36 V on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range, low I_Q and fast response of the devices.

The open-drain output allows the user to configure the output's logic high voltage (V_{OH}) and can be used to enable the comparator to be used in AND functionality.

Voltage Comparison

The device operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

Application Information

The device is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes this comparator optimal for level shifting to a higher or lower voltage.

Typical Application

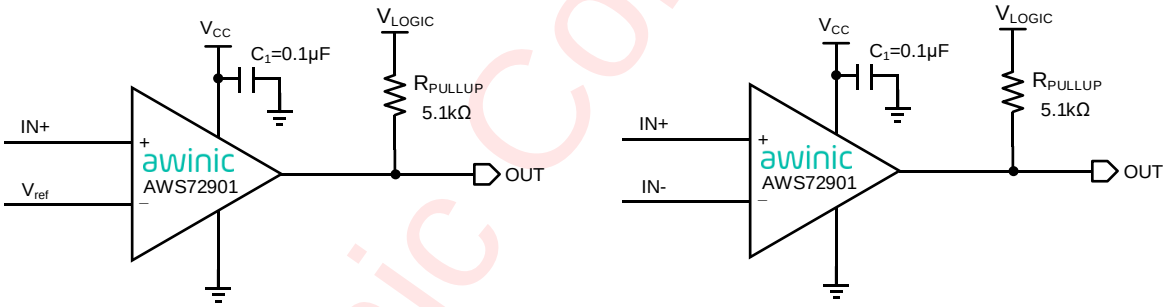


Figure 21 Single-Ended and Differential Comparator Configurations

Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0 V to V_{CC} - 2.0 V. This limits the input voltage range to as high as V_{CC} - 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common mode input voltage. Rail-to-rail input voltage range and low voltage single-supply operation make these devices ideal for portable equipment.

Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should

be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive.

Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current.

Response Time

Response time is a function of input over drive. The rise and falls times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent drain-source resistance (R_{DS}).

PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1 μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.
2. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
3. Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V+ or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.
4. Solder the device directly to the PCB rather than using a socket.
5. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

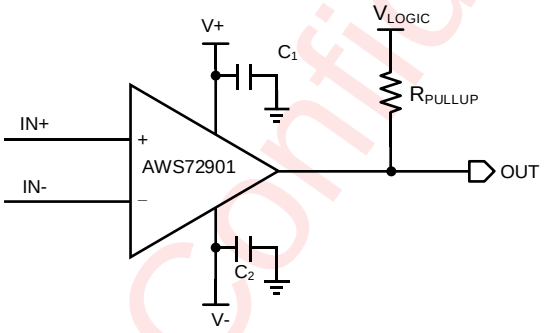


Figure 22 AWS72901 Schematic Example

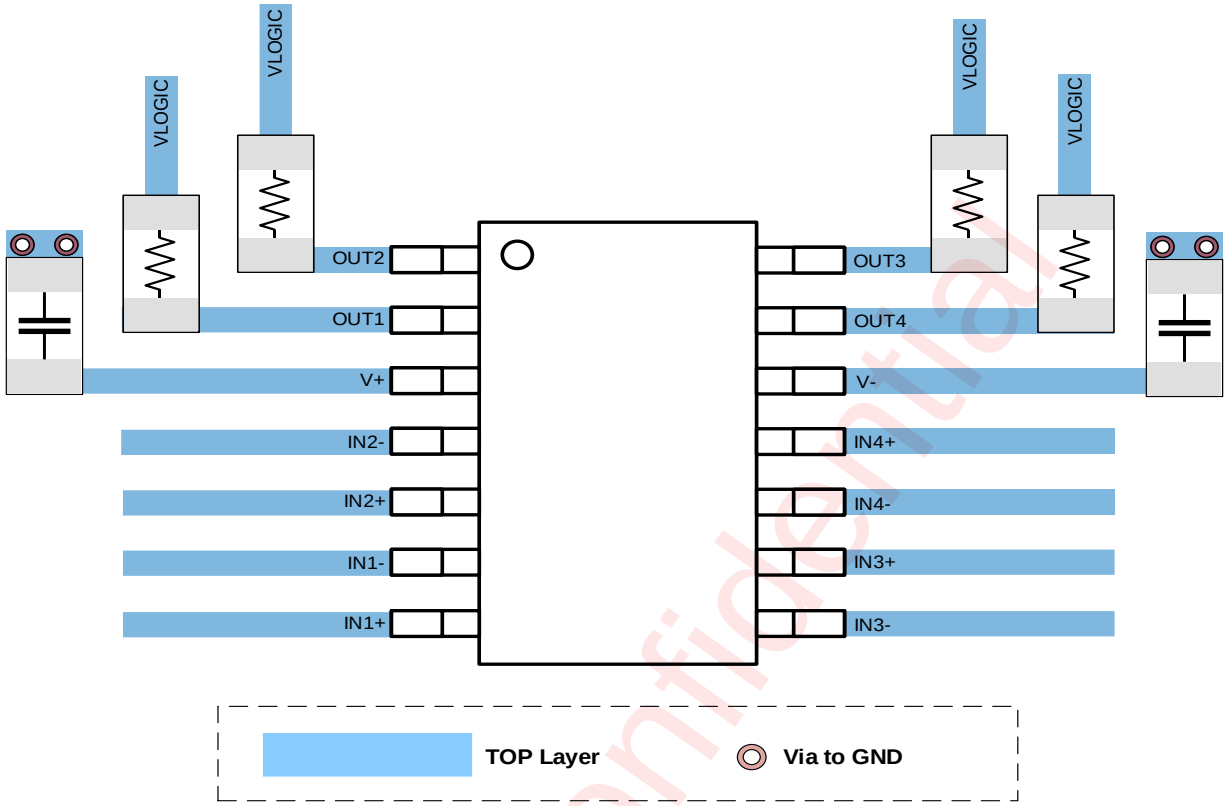


Figure 23 AWS72901 Layout Example

PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impendence node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting Configuration，connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 24. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

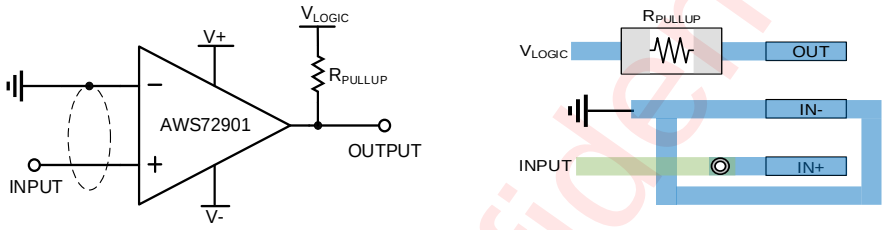


Figure 24　Non-inverting Comparator Application Schematic and Layout Example

Similarly, for inverting Configuration, connect the IN- to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 25. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS72901.

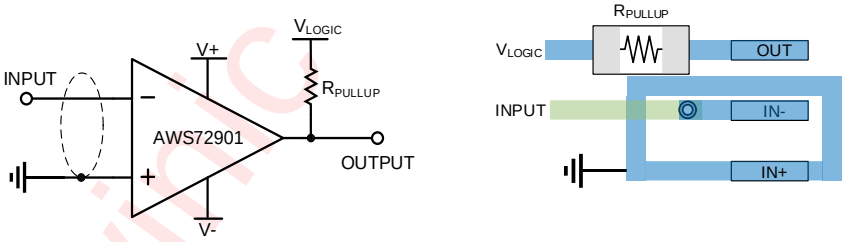
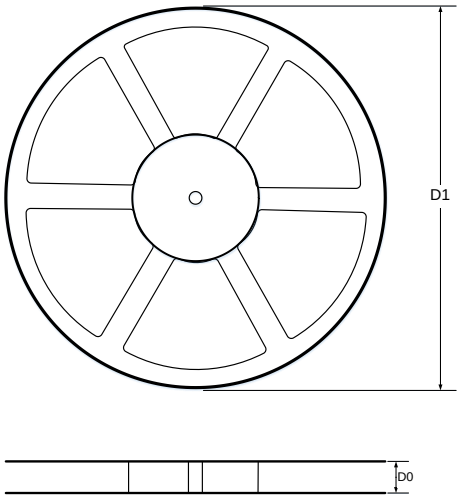


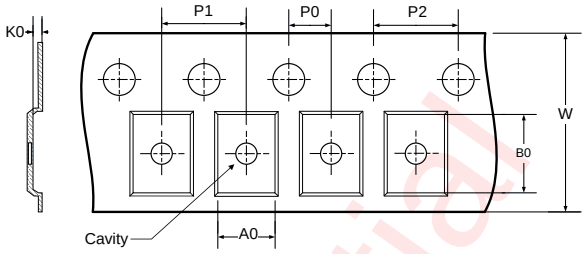
Figure 25　Inverting Comparator Application Schematic and Layout Example

Tape And Reel Information

REEL DIMENSIONS

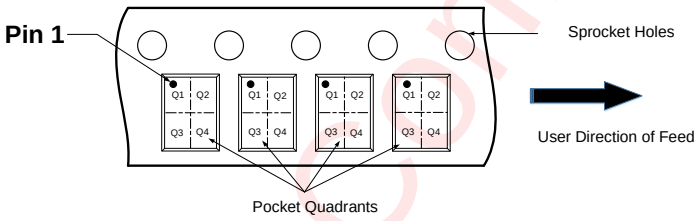


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



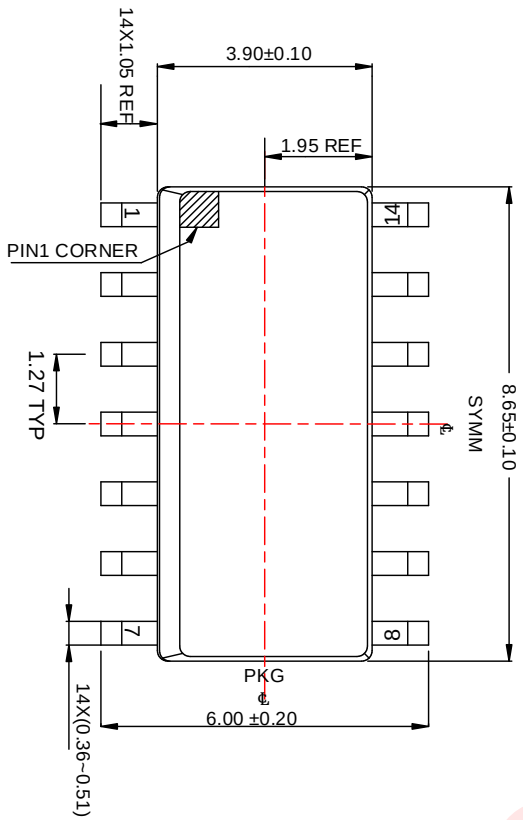
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

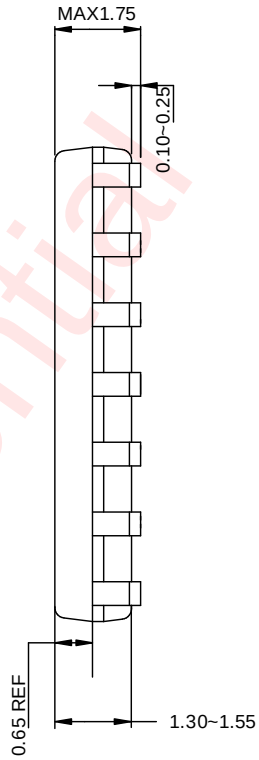
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	16.40	6.50	9.30	2.00	2.00	8.00	4.00	16.00	Q1

All dimensions are nominal

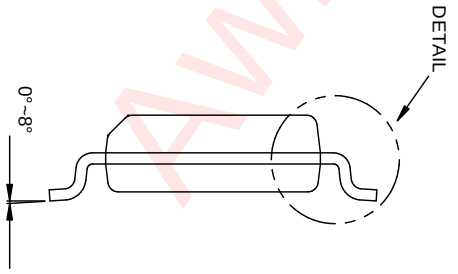
Package Description



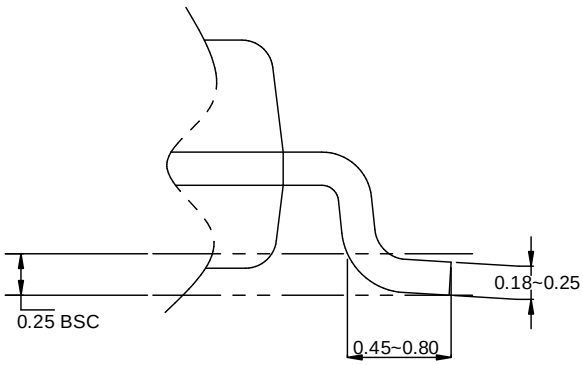
TOP VIEW



SIDE VIEW



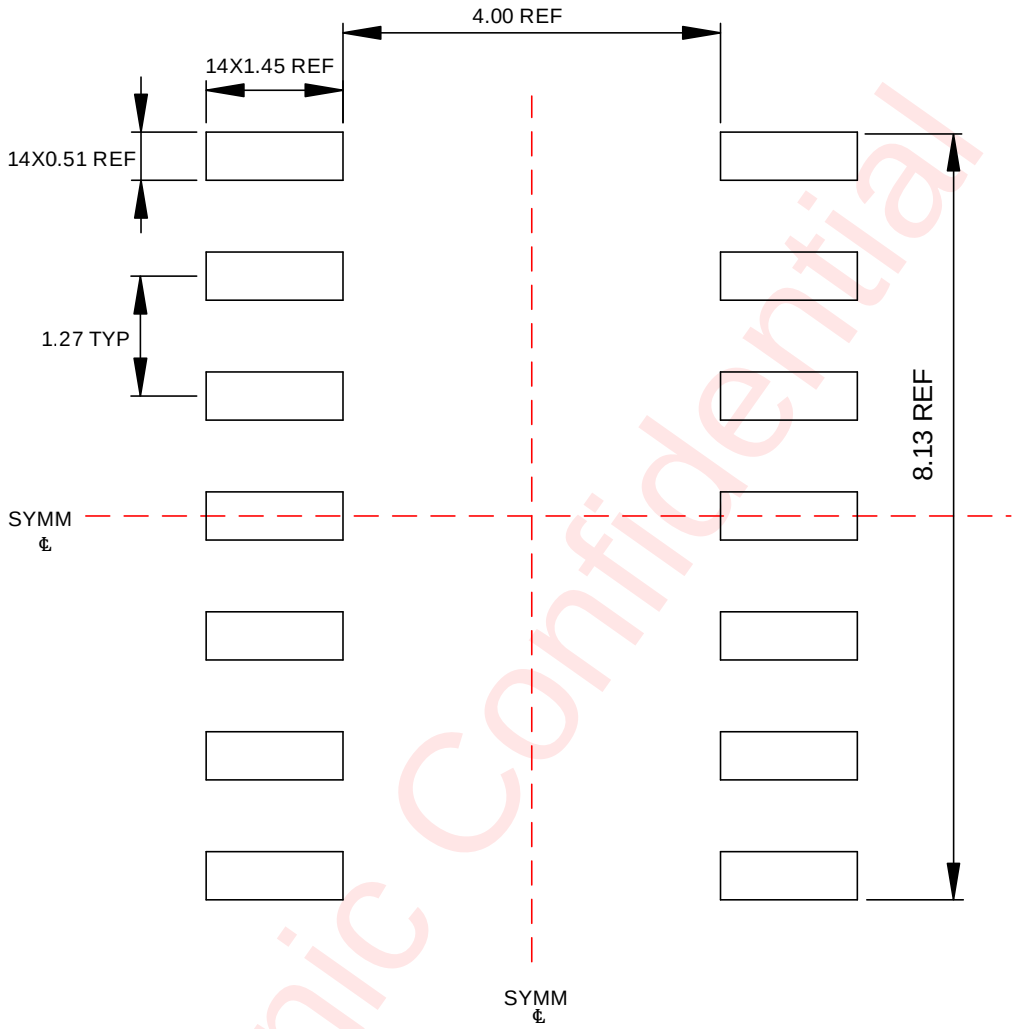
SIDE VIEW

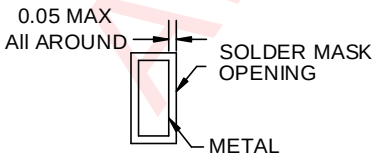


DETAIL

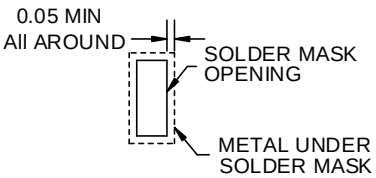
UNIT:mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Mar. 2025	Official released

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