



钜地半导体  
Tudi Semiconductor

## Product Specification

24LC02BT-I/ST-TUDI

2K I<sup>2</sup>C™ Serial EEPROM

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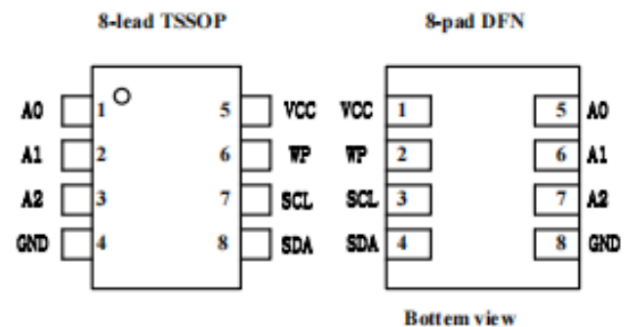
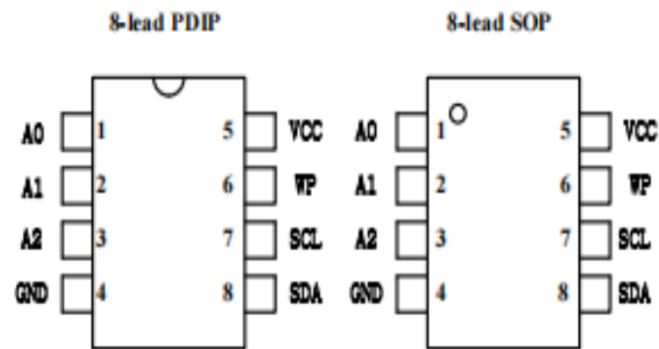
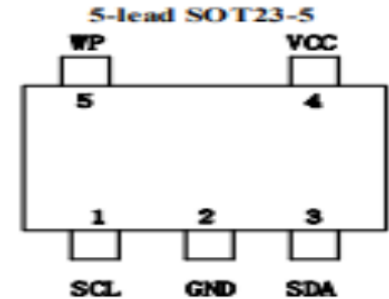
## Device Selection Table

| Part Number | Vcc Range | Max. Clock Frequency   | Temp. Ranges |
|-------------|-----------|------------------------|--------------|
| 24AA02      | 1.8-5.5   | 400 kHz <sup>(1)</sup> | I            |
| 24LC02      | 2.5-5.5   | 400 kHz                | I, E         |

## Features:

- Schmitt Trigger inputs for Noise Suppression
- Output Slope Control to eliminate Ground Bounce
- Self-Timed Erase/Write Cycle
- Hardware Write-Protect
- More than 1 Million Erase/Write Cycles
- Data Retention > 200 Years
- Factory Programming Available
- Packages include 8-lead PDIP, SOIC, TSSOP, MSOP, and SOT-23-5
- Pb-Free and RoHS Compliant

24AA02/24LC02B (24XX02\*) is a 2 Kbit Electrically Erasable PROM. The 24XX02 also has a page write capability for up to 8 bytes of data. The 24XX02 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP, 2x3 DFN, 2x3 TDFN and MSOP packages and is also available in the 5-lead SOT-23 packages



Bottom view



## Pin Descriptions

| Pin Name | Type | Functions          |
|----------|------|--------------------|
| A0-A2    | I    | Address Inputs     |
| SDA      | I/O  | Serial Data        |
| SCL      | I    | Serial Clock Input |
| WP       | I    | Write Protect      |
| GND      | P    | Ground             |
| Vcc      | P    | Power Supply       |

Table 1

## Block Diagram

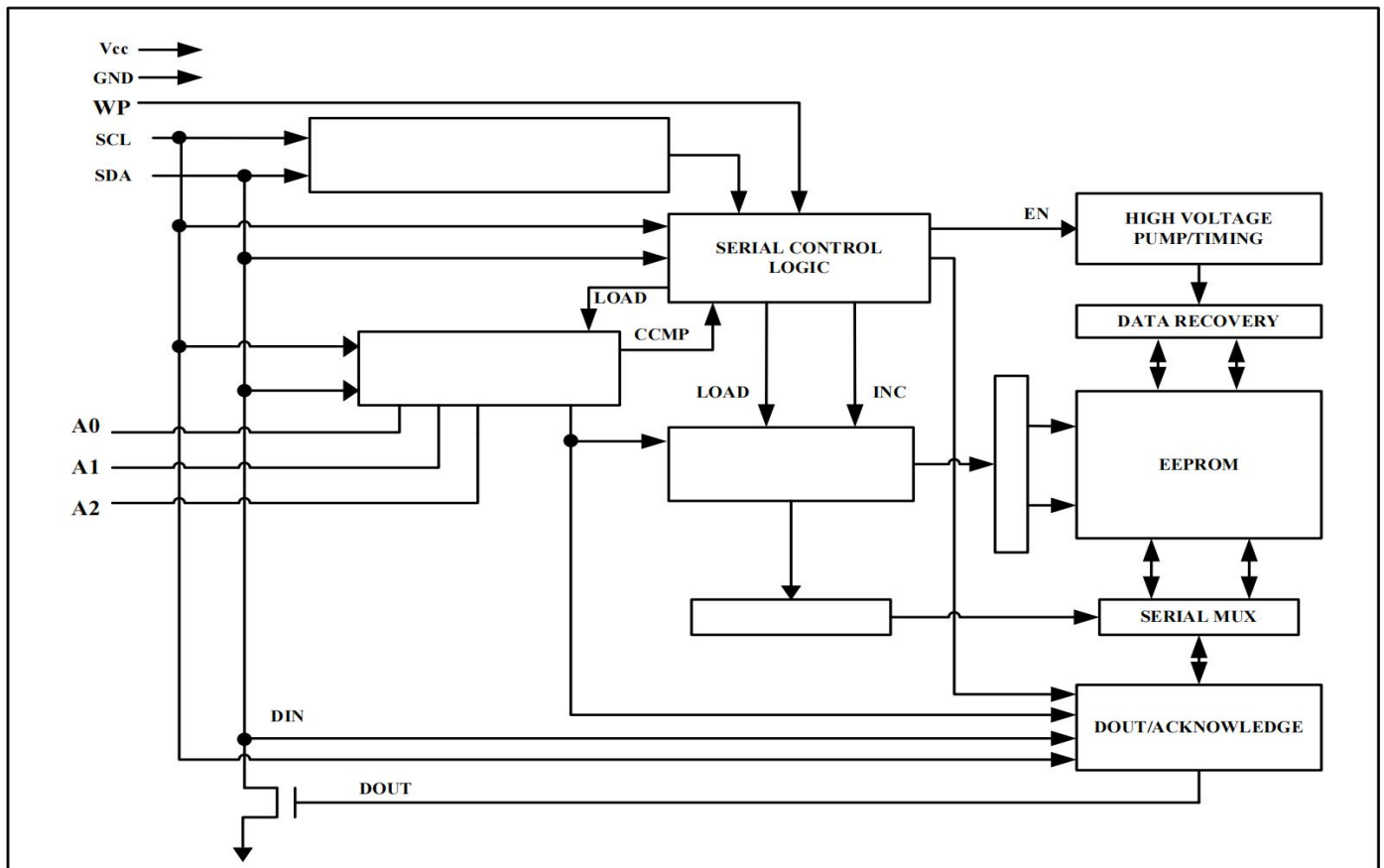


Figure 1

**DEVICE/PAGE ADDRESSES (A2, A1 and A0):** The A2, A1 and A0 pins are device address inputs that are hardwired for the 24LC02B/24AA02 /04/08/16. Eight 2K/4K/8K/16K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

**SERIAL DATA (SDA):** The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.



**WRITE PROTECT (WP):** The 24LC02B/24AA02 /04/08/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **Table 2**.

| WP Pin Status | 24LC02 24AA02 B/04B/08B/16B  |
|---------------|------------------------------|
| At VCC        | Full Array                   |
| At GND        | Normal Read/Write Operations |

Table 2

## Functional Description

### 1. Memory Organization

**24LC02B/24AA02, 2K SERIAL EEPROM:** Internally organized with 16 pages of 16 bytes each, the 2K requires an 8-bit data word address for random word addressing.

**24LC04B/24AA04, 4K SERIAL EEPROM:** Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

**24LC08B/24AA08, 8K SERIAL EEPROM:** Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

**24LC16B/24AA16, 16K SERIAL EEPROM:** Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

### 2. Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

**STANDBY MODE:** The 24LC02B/24AA02 /04/08/16 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

**MEMORY RESET:** After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:



1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Figure 2. Data Validity

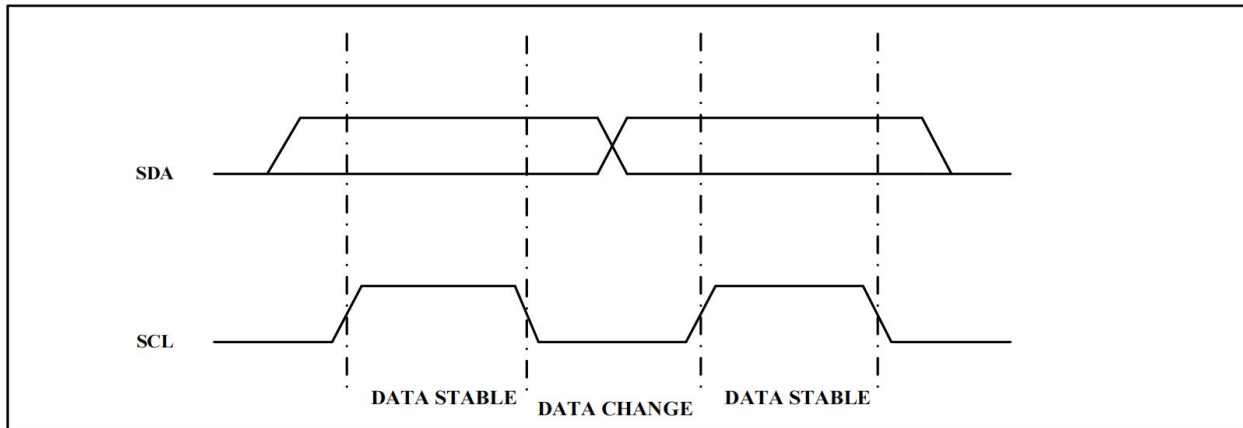


Figure 3. Start and Stop Definition

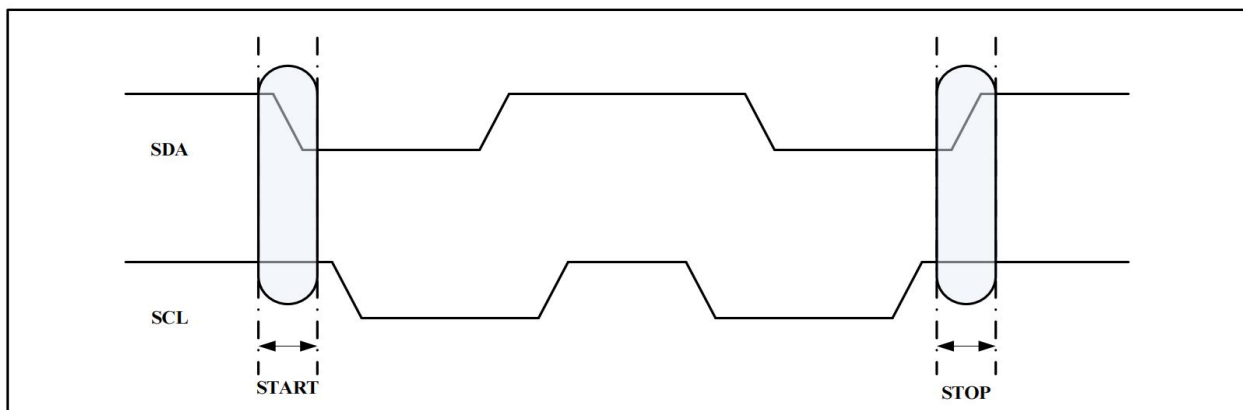
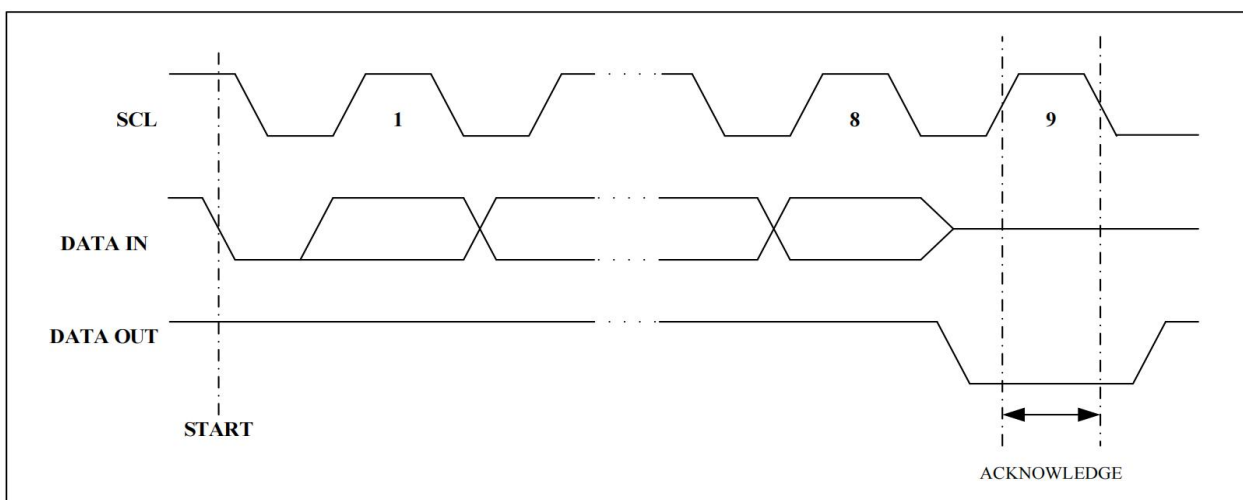


Figure 4. Output Acknowledge





### 3. Device Addressing

The 2K/4K/8K/16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hardwired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hardwired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

### 4. Write Operations

**BYTE WRITE:** A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).

**PAGE WRITE:** The 2K EEPROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) or fifteen (4K, 8K, 16K) more data



words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 7**).

The data word address lower three (2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

**ACKNOWLEDGE POLLING:** Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

## 5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

### CURRENT ADDRESS READ:

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

### RANDOM READ:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**).

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the



microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

Figure 5. Device Address

|     | MSB |   |   |   |    |    |    | LSB |
|-----|-----|---|---|---|----|----|----|-----|
| 2K  | 1   | 0 | 1 | 0 | 0  | 0  | 0  | R/W |
| 4K  | 1   | 0 | 1 | 0 | 0  | 0  | P0 | R/W |
| 8K  | 1   | 0 | 1 | 0 | 0  | P1 | P0 | R/W |
| 16K | 1   | 0 | 1 | 0 | P2 | P1 | P0 | R/W |

Figure 6. Byte Write

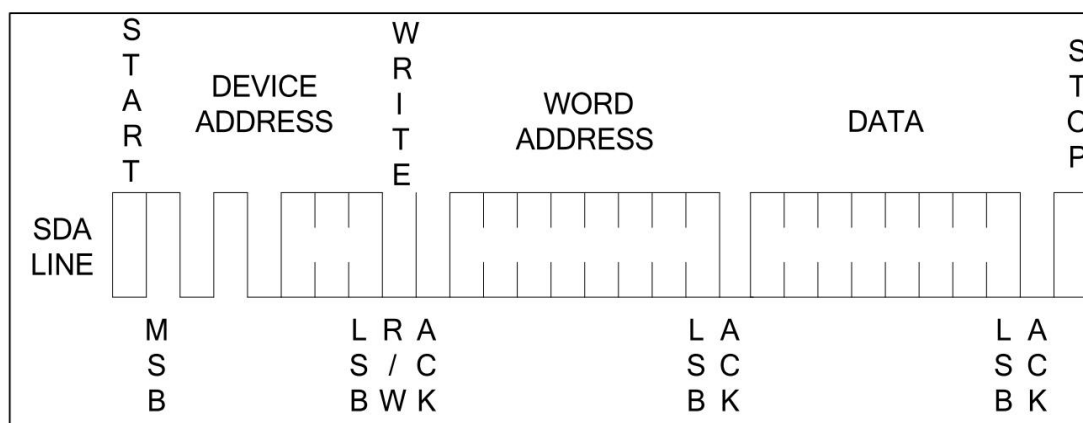


Figure 7. Page Write

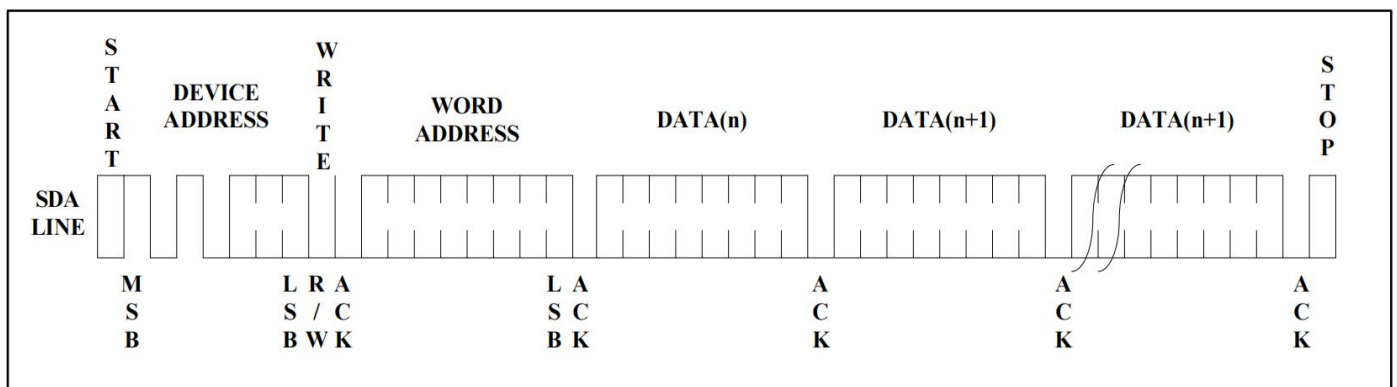




Figure 8. Current Address Read

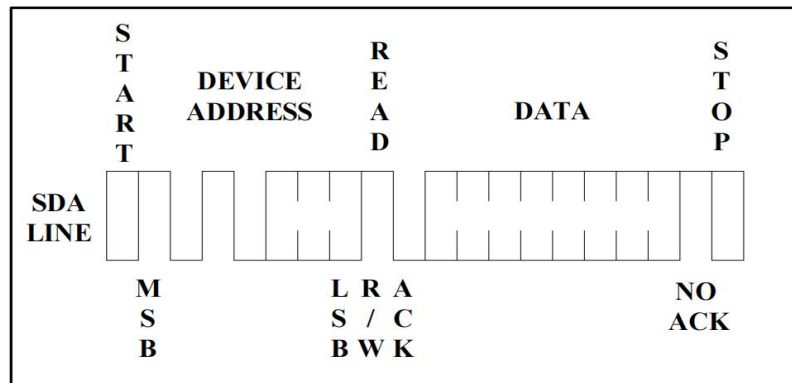


Figure 9. Random Read

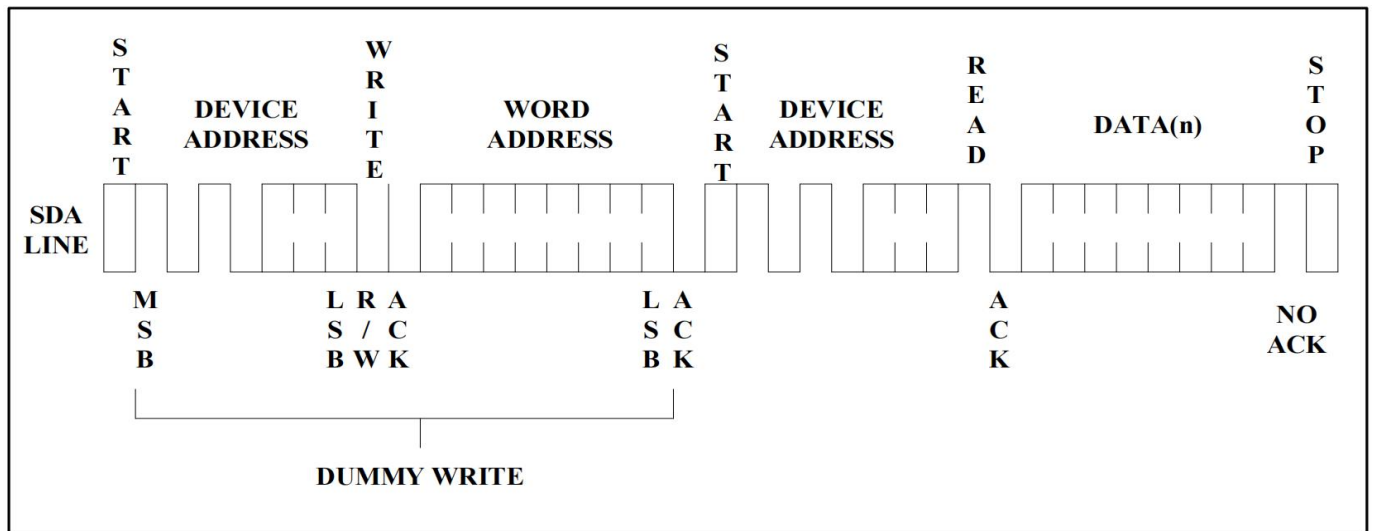
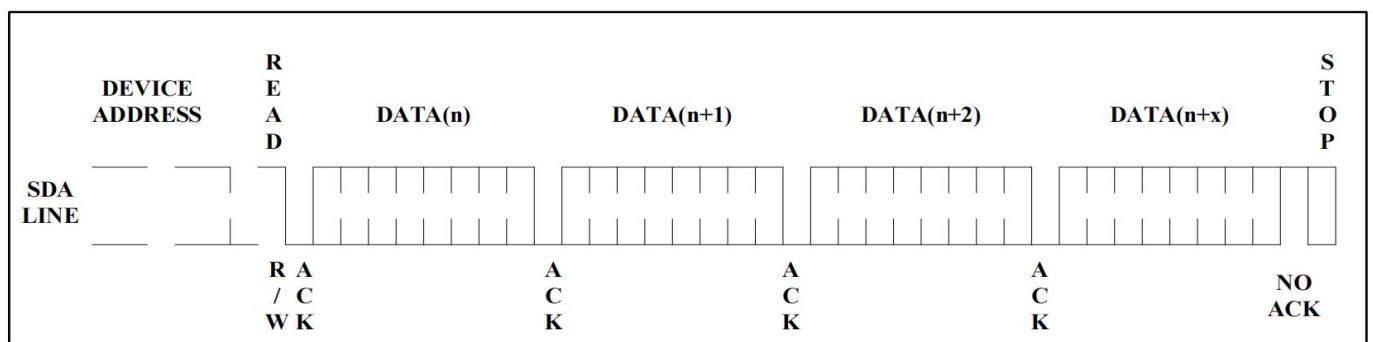


Figure 10. Sequential Read





## Electrical Characteristics

Absolute Maximum Stress Ratings :

- DC Supply Voltage .....-0.3V to +6.5V
- Input / Output Voltage .....GND-0.3V to VCC+0.3V
- Operating Ambient Temperature ..... -40°C to +85°C
- Storage Temperature ..... -65°C to +150°C
- Electrostatic pulse (Human Body model) ..... 8000V

Comments :

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC = +1.7V to +5.5V (unless otherwise noted)

| Parameter                 | Symbol           | Min                  | Typ  | Max                  | Unit | Condition                                            |
|---------------------------|------------------|----------------------|------|----------------------|------|------------------------------------------------------|
| Supply Voltage            | V <sub>CC1</sub> | 1.7                  | -    | 5.5                  | V    | -                                                    |
| Supply Voltage            | V <sub>CC2</sub> | 2.5                  | -    | 5.5                  | V    | -                                                    |
| Supply Current VCC=5.0V   | I <sub>CC1</sub> | -                    | 0.14 | 0.3                  | mA   | READ at 400KHZ                                       |
| Supply Current VCC=5.0V   | I <sub>CC2</sub> | -                    | 0.28 | 0.5                  | mA   | WRITE at 400KHZ                                      |
| Supply Current VCC=5.0V   | I <sub>SB1</sub> | -                    | 0.03 | 0.5                  | μA   | V <sub>IN</sub> =V <sub>CC</sub> or V <sub>SS</sub>  |
| Input Leakage Current     | I <sub>L1</sub>  | -                    | 0.10 | 1.0                  | μA   | V <sub>IN</sub> =V <sub>CC</sub> or V <sub>SS</sub>  |
| Output Leakage Current    | I <sub>LO</sub>  | -                    | 0.05 | 1.0                  | μA   | V <sub>OUT</sub> =V <sub>CC</sub> or V <sub>SS</sub> |
| Input Low Level           | V <sub>IL1</sub> | -0.3                 | -    | V <sub>CC</sub> ×0.3 | V    | V <sub>CC</sub> =1.7V to 5.5V                        |
| Input High Level          | V <sub>IH1</sub> | V <sub>CC</sub> ×0.7 | -    | V <sub>CC</sub> +0.3 | V    | V <sub>CC</sub> =1.7V to 5.5V                        |
| Output Low Level VCC=1.7V | V <sub>OL1</sub> | -                    | -    | 0.2                  | V    | I <sub>OL</sub> =0.15mA                              |
| Output Low Level VCC=5.0V | V <sub>OL2</sub> | -                    | -    | 0.4                  | V    | I <sub>OL</sub> =3.0mA                               |

Table 5

### Pin Capacitance

Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.7V

| Parameter                       | Symbol           | Min | Typ | Max | Unit | Condition           |
|---------------------------------|------------------|-----|-----|-----|------|---------------------|
| Input/Output Capacitance(SDA)   | C <sub>I/O</sub> | -   | -   | 8   | pF   | V <sub>IO</sub> =0V |
| Input Capacitance(A0,A1,A2,SCL) | C <sub>IN</sub>  | -   | -   | 6   | pF   | V <sub>IN</sub> =0V |

Table 6



Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.7\text{V}$  to  $+5.5\text{V}$ ,  $CL = 1$  TTL Gate and  $100\text{ pF}$  (unless otherwise noted)

| Parameter                                                     | Symbol       | $1.7\text{V} \leq V_{CC} < 2.5\text{V}$ |     |      | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |     |      | Units         |
|---------------------------------------------------------------|--------------|-----------------------------------------|-----|------|-----------------------------------------|-----|------|---------------|
|                                                               |              | Min                                     | Typ | Max  | Min                                     | Typ | Max  |               |
| Clock Frequency, SCL                                          | $f_{SCL}$    | -                                       | -   | 400  | -                                       | -   | 1000 | KHZ           |
| Clock Pulse Width Low                                         | $t_{LOW}$    | 0.6                                     | -   | -    | 0.6                                     | -   | -    | $\mu\text{s}$ |
| Clock Pulse Width High                                        | $t_{HIGH}$   | 0.4                                     | -   | -    | 0.4                                     | -   | -    | $\mu\text{s}$ |
| Noise Suppression Time                                        | $t_I$        | -                                       | -   | 50   | -                                       | -   | 50   | ns            |
| Clock Low to Data Out Valid                                   | $t_{AA}$     | 0.1                                     | -   | 0.55 | 0.1                                     | -   | 0.55 | $\mu\text{s}$ |
| Time the bus must be free before a new transmission can start | $t_{BUF}$    | 0.5                                     | -   | -    | 0.5                                     | -   | -    | $\mu\text{s}$ |
| Start Hold Time                                               | $t_{HD:STA}$ | 0.25                                    | -   | -    | 0.25                                    | -   | -    | $\mu\text{s}$ |
| Start Setup Time                                              | $t_{SU:DAT}$ | 0.25                                    | -   | -    | 0.25                                    | -   | -    | $\mu\text{s}$ |
| Data In Hold Time                                             | $t_{HD:DAT}$ | 0                                       | -   | -    | 0                                       | -   | -    | $\mu\text{s}$ |
| Data in Setup Time                                            | $t_{SU:DAT}$ | 100                                     | -   | -    | 100                                     | -   | -    | ns            |
| Input Rise Time(1)                                            | $t_R$        | -                                       | -   | 0.3  | -                                       | -   | 0.3  | $\mu\text{s}$ |
| Input Fall Time(1)                                            | $t_F$        | -                                       | -   | 0.3  | -                                       | -   | 0.3  | $\mu\text{s}$ |
| Stop Setup Time                                               | $t_{Su:STO}$ | 0.25                                    | -   | -    | 0.25                                    | -   | -    | $\mu\text{s}$ |
| Data Out Hold Time                                            | $t_{DH}$     | 50                                      | -   | -    | 50                                      | -   | -    | ns            |
| Write Cycle Time                                              | $t_{WR}$     | -                                       | 1.9 | 3    | -                                       | 1.9 | 3    | ms            |
| 5.0V, $25^{\circ}\text{C}$ , Byte Mode(1)                     | Endurance    | 1M                                      | -   | -    | -                                       | -   | -    | Write Cycle   |

Table 7

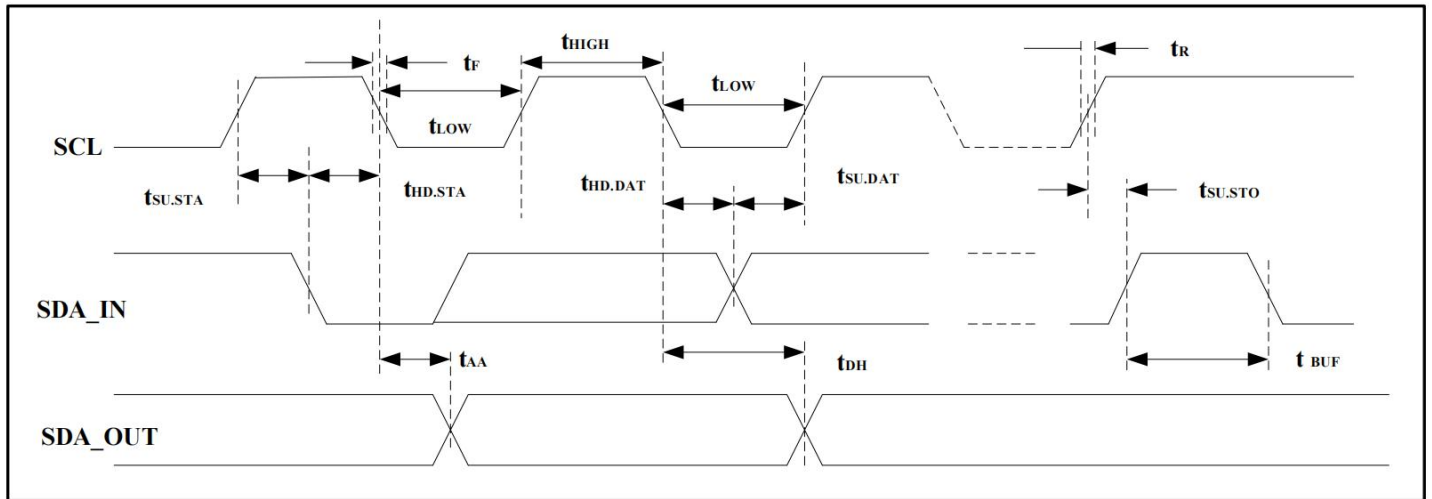
Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:  
 $R_L$  (connects to  $V_{CC}$ ):  $1.3\text{ k}\Omega$   
 Input pulse voltages:  $0.3 V_{CC}$  to  $0.7 V_{CC}$   
 Input rise and fall time:  $50\text{ ns}$   
 Input and output timing reference voltages:  $0.5 V_{CC}$   
 The value of  $R_L$  should be concerned according to the actual loading on the user's system.



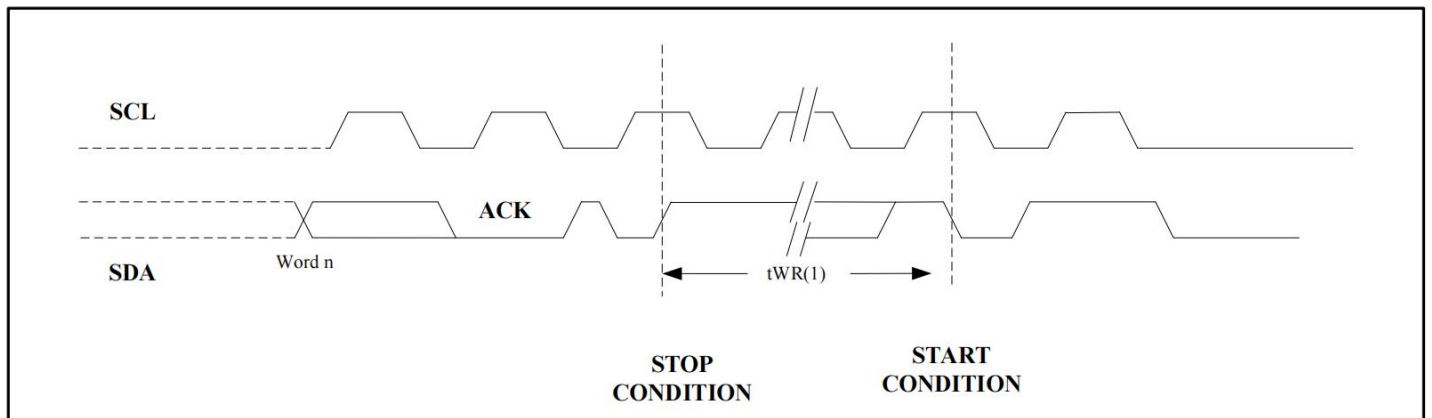
## Bus Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O



## Write Cycle Timing

Figure 12. SCL: Serial Clock, SDA: Serial Data I/O



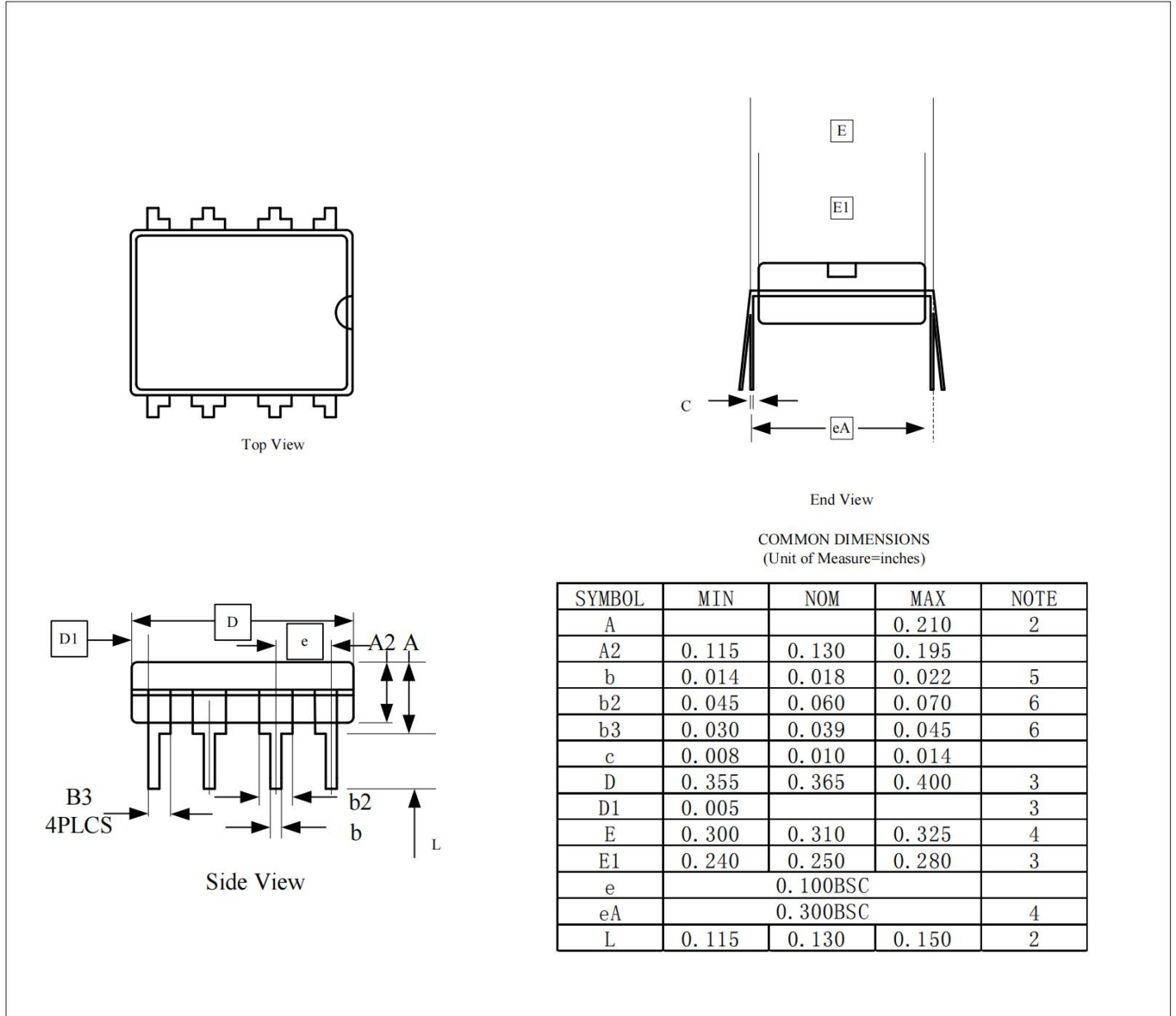
### Notes:

The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



## Package Information

### PDIP Outline Dimensions

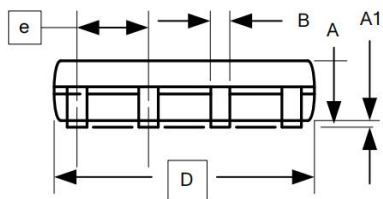
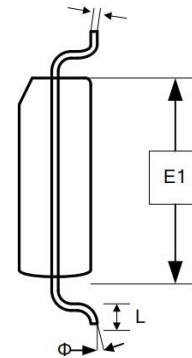
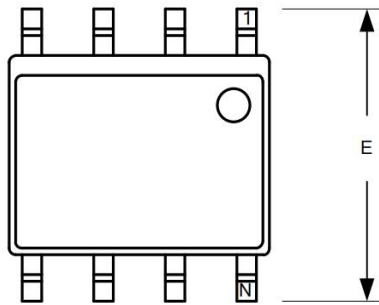


#### Notes:

1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).



SOP



COMMON DIMENSIONS  
(Unit of Measure=mm)

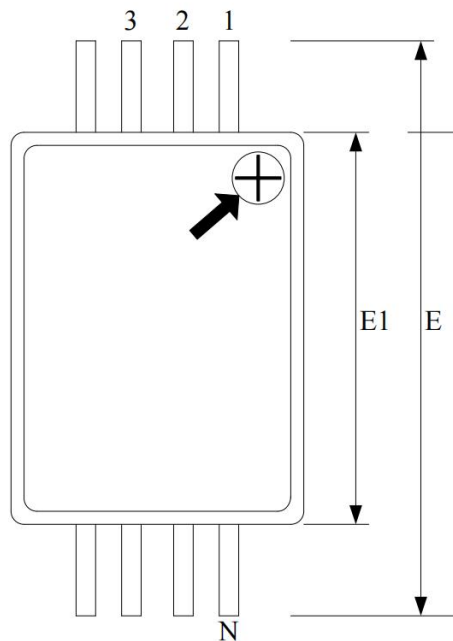
| SYMBOL | MIN     | NOM | MAX  | NOTE |
|--------|---------|-----|------|------|
| A      | 1.35    | —   | 1.75 |      |
| A1     | 0.10    | —   | 0.25 |      |
| b      | 0.31    | —   | 0.51 |      |
| C      | 0.17    | —   | 0.25 |      |
| D      | 4.80    | —   | 5.00 |      |
| E1     | 3.81    | —   | 3.99 |      |
| E      | 5.79    | —   | 6.20 |      |
| e      | 1.27BSC |     |      |      |
| L      | 0.40    | —   | 1.27 |      |
| Φ      | 0"      | —   | 8"   |      |

Notes:

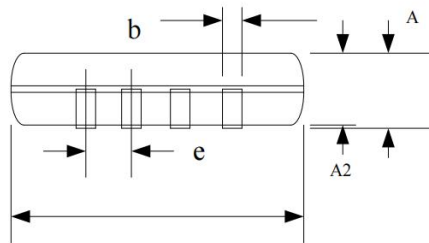
These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.



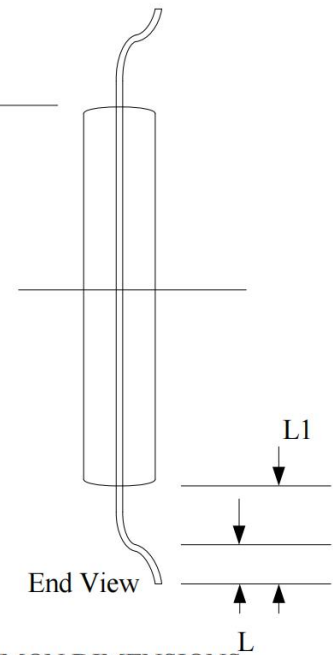
TSSOP



Top View



Side View



End View

COMMON DIMENSIONS

Unit of Measure=mm

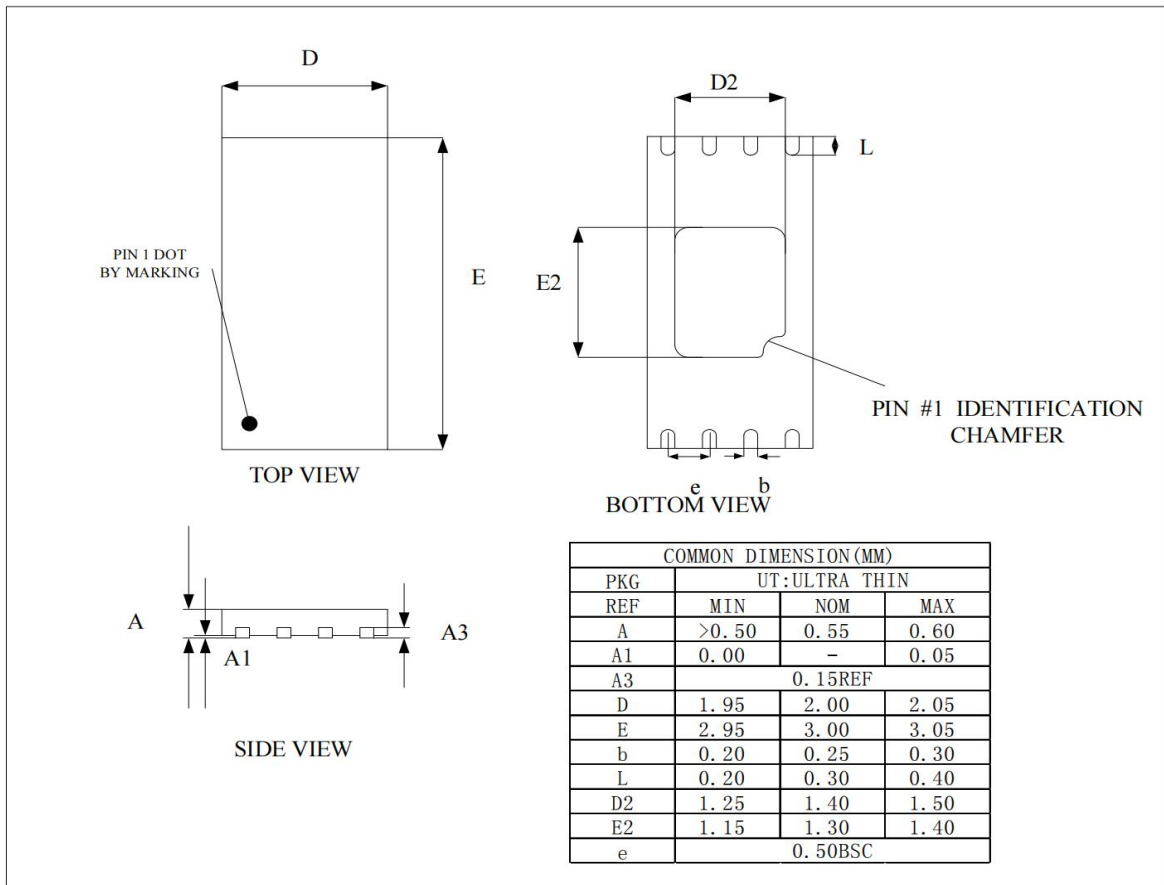
| SYMBOL | MIN     | NOM  | MAX  | NOTE |
|--------|---------|------|------|------|
| D      | 2.90    | 3.00 | 3.10 | 2, 5 |
| E      | 6.40BSC |      |      |      |
| E1     | 4.30    | 4.40 | 4.50 | 3, 5 |
| A      | —       | —    | 1.20 |      |
| A2     | 0.80    | 1.00 | 1.05 |      |
| b      | 0.19    | —    | 0.30 | 4    |
| e      | 0.65BSC |      |      |      |
| L      | 0.45    | 0.60 | 0.75 |      |
| L1     | 1.00REF |      |      |      |

Notes:

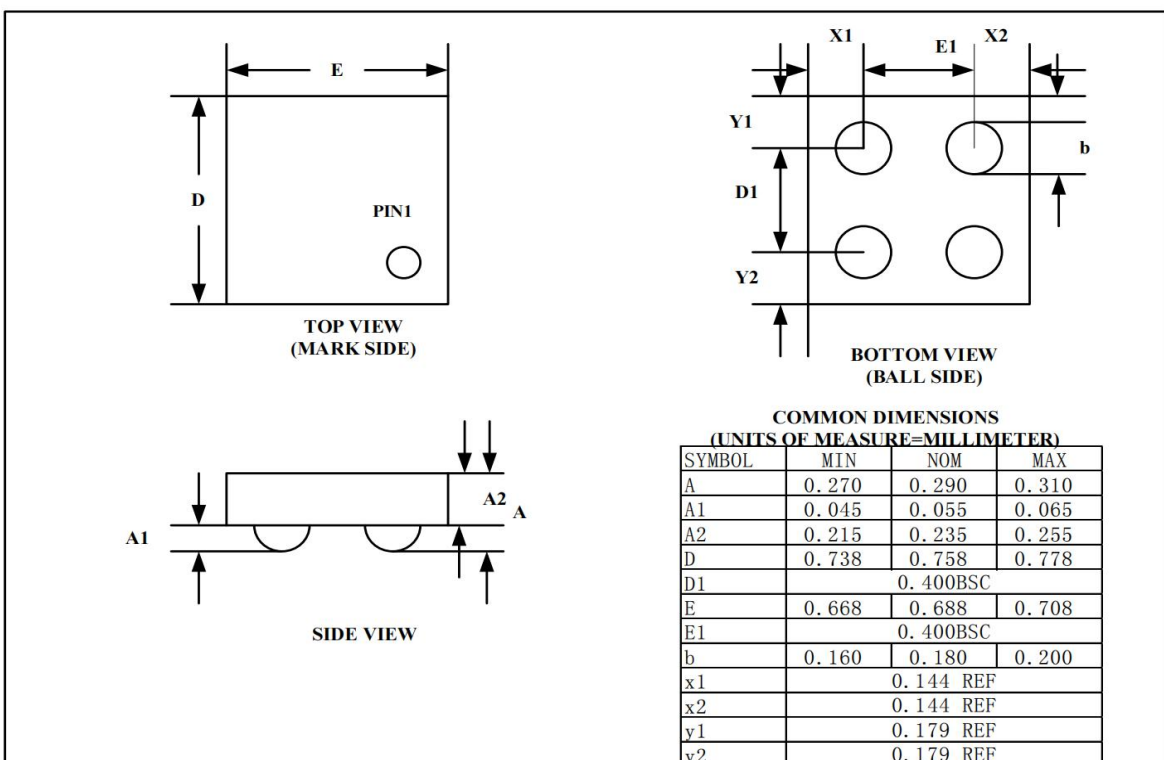
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.



UDFN

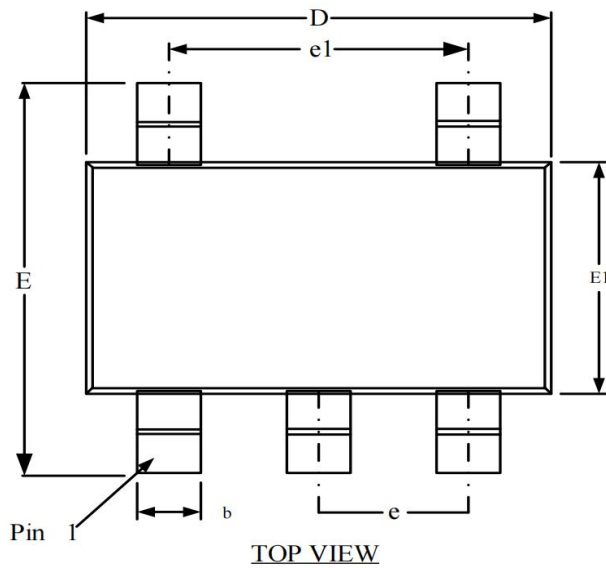


WLCSP

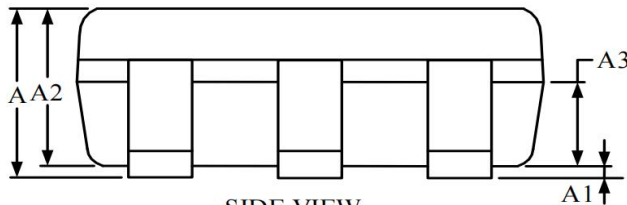




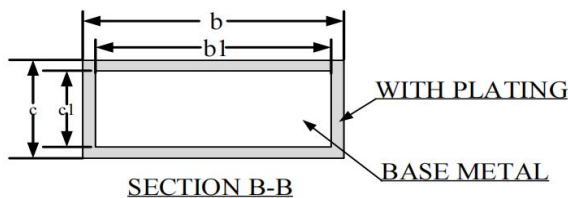
SOT23-5



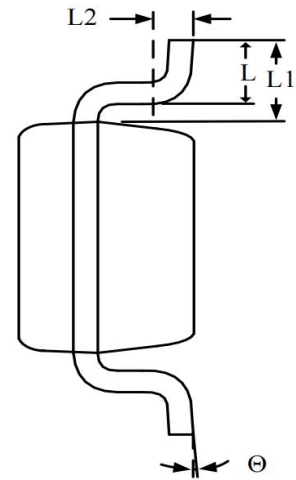
TOP VIEW



SIDE VIEW



SECTION B-B



SIDE VIEW

COMMON DIMENSIONS  
(UNITS OF MEASURE = MILLIMETER)

| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      | —        | —    | 1.35 |
| A1     | 0.04     | —    | 0.15 |
| A2     | 1.00     | 1.10 | 1.20 |
| A3     | 0.55     | 0.65 | 0.75 |
| b      | 0.38     | —    | 0.48 |
| b1     | 0.37     | 0.40 | 0.43 |
| c      | 0.11     | —    | 0.21 |
| c1     | 0.10     | 0.13 | 0.16 |
| D      | 2.72     | 2.92 | 3.12 |
| E      | 2.60     | 2.80 | 3.00 |
| E1     | 1.40     | 1.60 | 1.80 |
| e      | 0.95BSC  |      |      |
| e1     | 1.90BSC  |      |      |
| L      | 0.30     | —    | 0.60 |
| L1     | 0.575REF |      |      |
| L2     | 0.258BSC |      |      |
| Θ      | 0°       | —    | 8°   |

## Ordering information

| Order Number       | Package | Package Quantity | Marking<br>On The park |
|--------------------|---------|------------------|------------------------|
| 24LC02BT-I/ST-TUDI | TSSOP8  | Tape,Reel,2500   | 24LC02B                |



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