



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65HVD230/SN65HVD232

3.3V CAN bus transceiver

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**semiconductor device
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- Design
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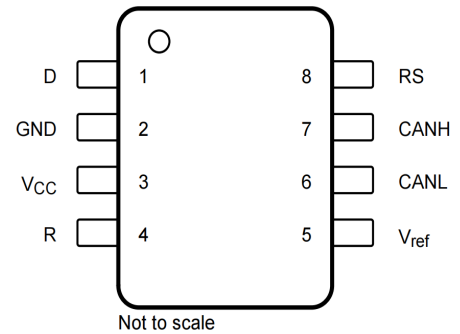


Features

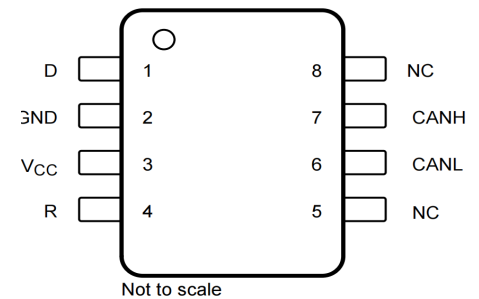
- Powered by a 3.3V single supply
- Complies with ISO 11898-2 standard
- Low-power alternative to PCA82C250 package
- Bus pin electrostatic discharge (ESD) protection exceeds $\pm 16\text{kV}$ human body model (HBM)
- High input impedance, allowing up to 120 nodes to be connected on a single bus
- Adjustable driver transition time, capable of improving radiation performance
 - SN65VD230 and SN65HVD231
- SN65HVD230: Low-current standby mode
 - $370\ \mu$ (typical)
- SN65HVD231: Ultra-low-current sleep mode
 - 40nA (typical)
- Designed for data rates to $1\text{Mbps}^{(1)}$
- Thermal shutdown protection
- Open-circuit fault-safe design
- Glitch-free power-up and power-down protection for hotswap applications

Applications

- Industrial automation, control, sensors and drivesystems
- Motor and robot control
- Building and temperature control (HVAC)
- Telecommunications and base station control and status
- Controller Area Network (CAN) bus standards, such as CANopen, DeviceNet and CAN Kingdom



SN65HVD230D (Marked as VP230)
Top View



SN65HVD232D (Marked as VP232)
Top View



Description

The SN65HVD230, SN65HVD231, and SN65HVD23 controller area network (CAN) transceivers comply with the ISO 11898-2 high-speed CAN physical layer standard (transceiver) specification. These devices are designed for applications with data rates up to 1Mbps and include many protection features to provide robustness for the device and the CAN network. The SN65HVD23x ceivers are designed to be used with 3.3V μ Ps, MCUs, and DSPs from Texas Instruments (TI) that have CAN controllers or equivalent protocol controllers. devices are intended for use in applications that use the CAN serial communication physical layer according to the ISO 11898 standard.

These devices can operate in extremely harsh environments and feature characteristics such as short-circuit protection, ground fault and overvoltage protection overheat protection, and a wide common-mode operating range.

CAN transceivers are CAN physical layer devices used to connect single-ended host CAN protocol controllers to differential CAN buses industrial, building automation, and automotive applications.

These devices operate on the bus within a common-mode voltage range of -2V to 7V and can withstand ± 25 common-mode transient voltages.

SN65HVD230 and SN65HVD231 provide three different operating modes via the RS pin (pin 8 high-speed mode, slew-rate control mode, and low-power mode. Grounding the RS pin selects the high-speed operating mode, which allows the transmitter output transistors to on and off as fast as possible with no restrictions on the rise and fall slew rates. Additionally, the rise and fall slew rates can be adjusted by connecting a resistor in series between RS pin and ground. The slew rate will be proportional to the output current of the pin. When theresistance is $10k\Omega$, the device's slew rate is approximately $15V/\mu s$; when the resistance is $100k\Omega$, the device's slew rate is approximately $2V/\mu s$. For more information please refer to the application information.If a logic high level is applied to the RS pin, the SN65HVD230 enters a low-current standby mode (listen-only). In this mode, the driver is turned off, while the receiver remains operational.

Compared to normal mode, this mode has lower power consumption while still allowing the CAN to monitor bus activity to determine whether the transceiver should return to normal mode or slew-rate control mode. When the device needs to send a message to the bus or receives a bus while in standby mode that requires it to be ready to send again, the host controller (MCU, DSP) will restore the device to transmit mode (high-speed mode or slewrate control mode).

The difference between the SN65HVD230 and SN65HVD231 is that when a logic high level is applied to RS pin, both the driver and receiver in the SN65HVD231 are turned off. In this sleep mode, the device will be unable to communicate with the. The device will remain in sleep mode until it is reactivated by applying a logic low level to the RS pin.



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V _{CC}	3	Supply	Transceiver 3.3V supply voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
V _{ref}	5	O	SN65HVD230 and SN65HVD231: V _{CC} / 2 reference output pin
NC		NC	SN65HVD232: No Connect
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
R _S	8	I	SN65HVD230 and SN65HVD231: Mode select pin: strong pull down to GND = high speed mode, strong pull up to V _{CC} = low power mode, 10k Ω to 100k Ω pull down to GND = slope control mode
NC		I	SN65HVD232: No Connect

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply voltage, V _{CC}	-0.3	6	V
Voltage at any bus terminal (CANH or CANL)	-4	16	V
Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 24)	-25	25	V
Digital Input and Output voltage, V _I (D or R)	-0.5	V _{CC} + 0.5	V
Receiver output current, I _O	-11	11	mA
Continuous total power dissipation	See Thermal Information		
Storage temperature, T _{stg}	-40	85	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.



8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	CANH, CANL and GND	±16000	V
		All pins	±4000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (common mode) V_{IC}		-2 ⁽¹⁾		7	V
Voltage at any bus terminal (separately) V_I		-2.5		7.5	V
High-level input voltage, V_{IH}	D, R	2			V
Low-level input voltage, V_{IL}	D, R			0.8	V
Differential input voltage, V_{ID} (see Figure 22)		-6		6	V
Input voltage, $V_{(RS)}$		0		V_{CC}	V
Input voltage for standby or sleep, $V_{(RS)}$		0.75 V_{CC}		V_{CC}	V
Wave-shaping resistance, R_s		0		100	kΩ
High-level output current, I_{OH}	Driver	-40			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			10		
Operating free-air temperature, T_A		-40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65HVD230	SN65HVD231	SN65HVD232	UNIT
		D			
		8 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	76.8	101.5	101.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	33.4	43.3	43.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	15.3	42.2	42.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.4	4.8	4.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	14.9	41.8	41.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.



8.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	Bus output voltage	Dominant	V _I = 0 V, See Figure 18 and Figure 20	CANH	2.45			V _{CC}	V
				CANL	0.5		1.25		
V _{OL}		Recessive	V _I = 3 V, See Figure 18 and Figure 20	CANH		2.3			
				CANL		2.3			
V _{OD(D)}	Differential output voltage	Dominant	V _I = 0 V, See Figure 18		1.5	2	3	V	
V _I = 0 V, See Figure 19			1.2	2	3				
V _{OD(R)}		Recessive	V _I = 3 V, See Figure 18		-120	0	12	mV	
			V _I = 3 V, No load		-0.5	-0.2	0.05	V	
I _{IH}	High-level input current		V _I = 2 V		-30			μA	
I _{IL}	Low-level input current		V _I = 0.8 V		-30			μA	
I _{OS}	Short-circuit output current		V _{CANH} = -2 V		-250		250	mA	
			V _{CANL} = 7 V		-250		250		
C _o	Output capacitance		See receiver						
I _{CC}	Supply current	Standby	SN65HVD230	V _(RS) = V _{CC}		370		600	μA
		Sleep	SN65HVD231	V _(RS) = V _{CC} , D at V _{CC}		0.04		1	
		All devices	Dominant	V _I = 0 V, No load	Dominant	10		17	mA
			Recessive	V _I = V _{CC} , No load	Recessive	10		17	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.6 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	See Table 1			750	900	mV
V _{IT-}	Negative-going input threshold voltage			500	650	mV	
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT-})				100		
V _{OH}	High-level output voltage	–6 V ≤ V _{ID} ≤ 500 mV, I _O = –8 mA, See Figure 22		2.4			V
V _{OL}	Low-level output voltage	900 mV ≤ V _{ID} ≤ 6 V, I _O = 8 mA, See Figure 22				0.4	
I _I	Bus input current	V _{IH} = 7 V	Other input at 0 V, D = 3 V		100	250	μA
		V _{IH} = 7 V, V _{CC} = 0 V			100	350	
		V _{IH} = -2 V			–200	–30	μA
		V _{IH} = -2 V, V _{CC} = 0 V			–100	–20	
C _I	CANH, CANL input capacitance	Pin-to-ground, V _I = 0.4 sin(4E6πt) + 0.5 V V _(D) = 3 V,		32			pF
C _{Diff}	Differential input capacitance	Pin-to-pin, V _I = 0.4 sin(4E6πt) + 0.5 V V _(D) = 3 V,		16			pF
R _{Diff}	Differential input resistance	Pin-to-pin, V _(D) = 3 V		40	70	100	kΩ
R _I	CANH, CANL input resistance			20	35	50	kΩ
I _{CC}	Supply current	See driver					

(1) All typical values are at 25°C and with a 3.3-V supply.



8.7 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SN65HVD230 AND SN65HVD231							
t _{PLH}	Propagation delay time, low-to-high-level output	V _(RS) = 0 V		35	85	ns	
		R _S with 10 kΩ to ground		70	125		
		R _S with 100 kΩ to ground		500	870		
t _{PHL}	Propagation delay time, high-to-low-level output	V _(RS) = 0 V		70	120	ns	
		R _S with 10 kΩ to ground		130	180		
		R _S with 100 kΩ to ground		870	1200		
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	V _(RS) = 0 V		35		ns	
		R _S with 10 kΩ to ground		60			
		R _S with 100 kΩ to ground		370			
t _r	Differential output signal rise time	C _L = 50 pF, See Figure 21		25	50	100	ns
t _f	Differential output signal fall time			40	55	80	ns
t _r	Differential output signal rise time			80	120	160	ns
t _f	Differential output signal fall time			80	125	150	ns
t _r	Differential output signal rise time			600	800	1200	ns
t _f	Differential output signal fall time			600	825	1000	ns
SN65HVD232							
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 50 pF, See Figure 21		35	85	ns	
t _{PHL}	Propagation delay time, high-to-low-level output			70	120		
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			35			
t _r	Differential output signal rise time			25	50		100
t _f	Differential output signal fall time			40	55		80

8.8 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 23		35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)				10	ns
t_r	Output signal rise time	See Figure 23		1.5		ns
t_f	Output signal fall time			1.5		ns

8.9 Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$V_{(RS)} = 0\text{ V}$, See Figure 26		70	115	ns
		R_S with 10 k Ω to ground, See Figure 26		105	175	
		R_S with 100 k Ω to ground, See Figure 26		535	920	
$t_{(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$V_{(RS)} = 0\text{ V}$, See Figure 26		100	135	ns
		R_S with 10 k Ω to ground, See Figure 26		155	185	
		R_S with 100 k Ω to ground, See Figure 26		830	990	



8.10 Device Control-Pin Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$t_{(WAKE)}$	SN65HVD230 wake-up time from standby mode with R_S	See Figure 25		0.55	1.5	μs
	SN65HVD231 wake-up time from sleep mode with R_S			3	5	μs
V_{ref}	Reference output voltage	$-5 \mu A < I_{(Vref)} < 5 \mu A$	$0.45 V_{CC}$		$0.55 V_{CC}$	V
		$-50 \mu A < I_{(Vref)} < 50 \mu A$	$0.4 V_{CC}$		$0.6 V_{CC}$	
$I_{(RS)}$	Input current for high-speed	$V_{(RS)} < 1 V$	-450		0	μA

(1) All typical values are at 25°C and with a 3.3-V supply.



9 Parameter Measurement Information

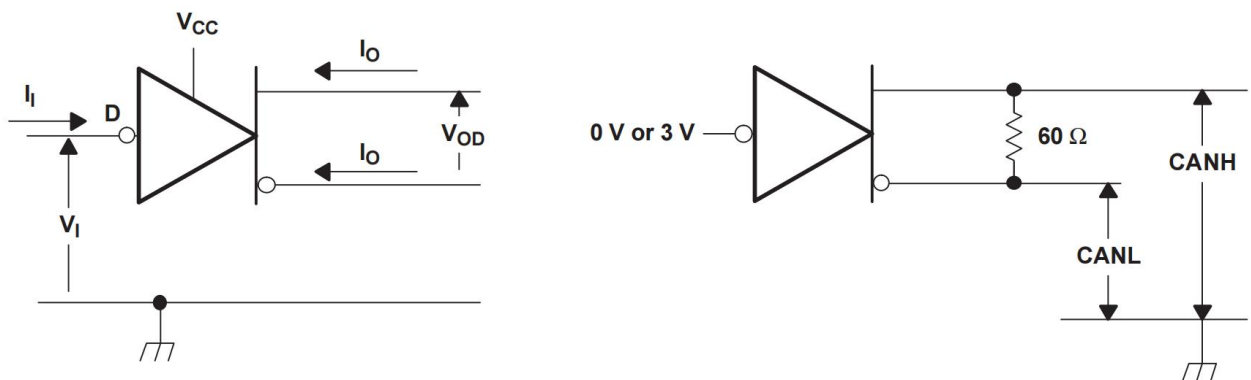


Figure 18. Driver Voltage and Current Definitions

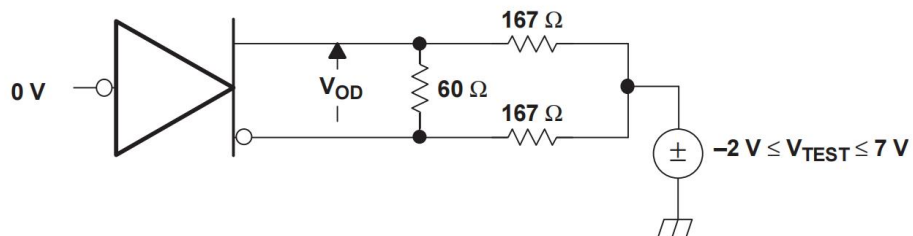


Figure 19. Driver V_{OD}

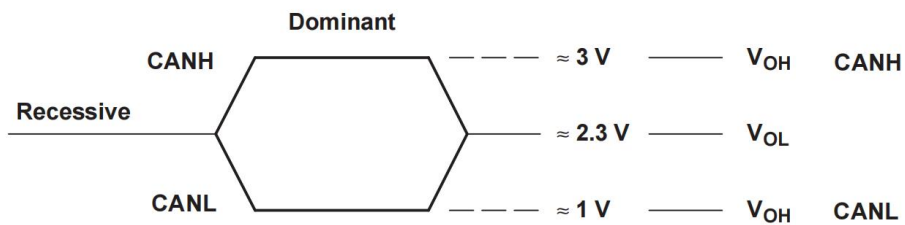
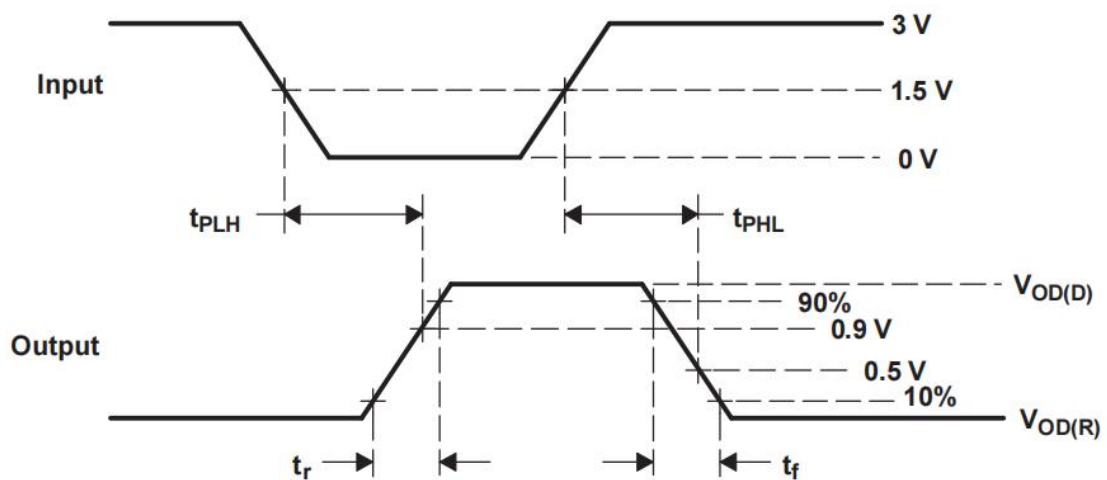
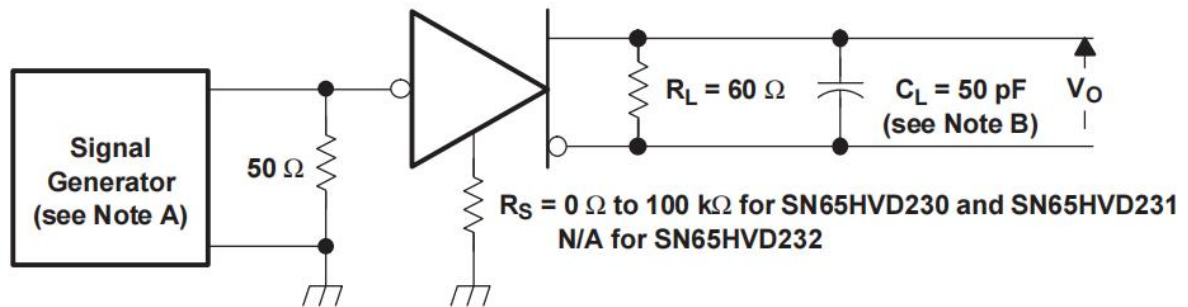


Figure 20. Driver Output Voltage Definitions



Parameter Measurement Information (continued)



- A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 500\ \text{kHz}$, 50% duty cycle, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$, $Z_o = 50\ \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 21. Driver Test Circuit and Voltage Waveforms

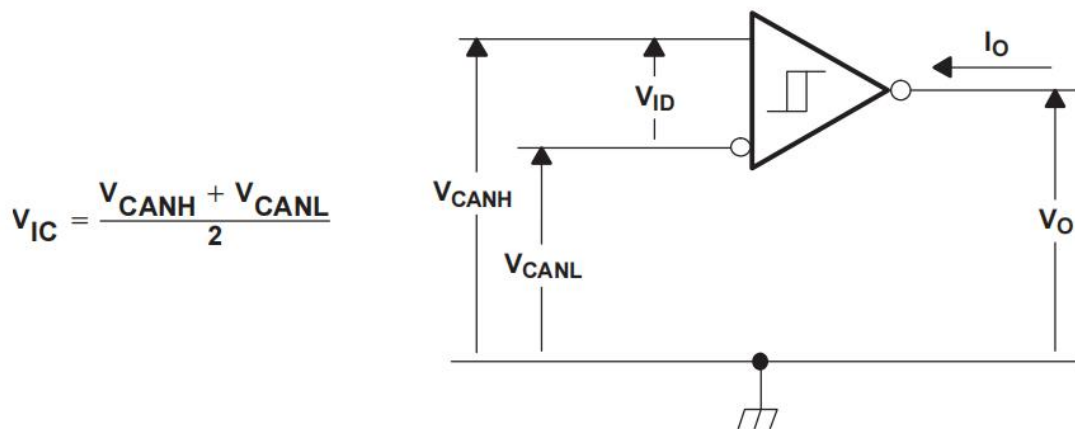
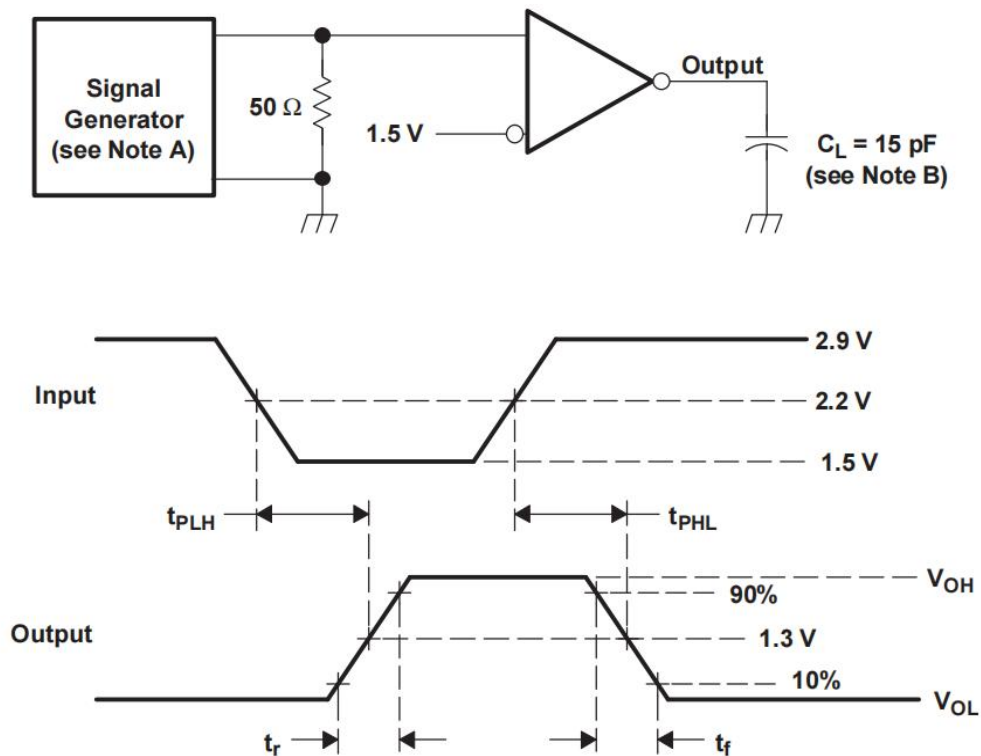


Figure 22. Receiver Voltage and Current Definitions



Parameter Measurement Information (continued)



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 500 \text{ kHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_o = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 23. Receiver Test Circuit and Voltage Waveforms

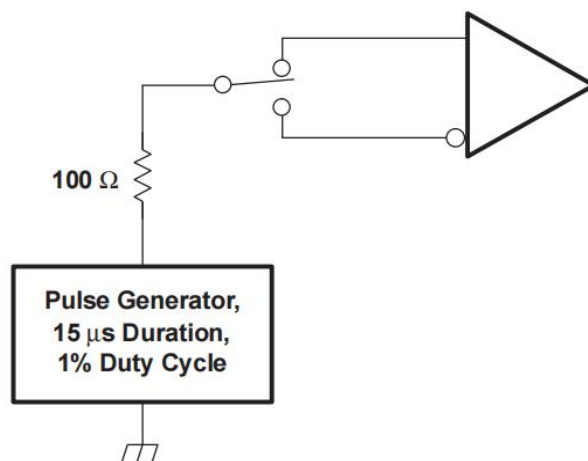


Figure 24. Overvoltage Protection



Parameter Measurement Information (continued)

Table 1. Receiver Characteristics Over Common Mode With $V_{(RS)} = 1.2 \text{ V}$

V_{IC}	V_{ID}	V_{CANH}	V_{CANL}	R OUTPUT	
-2 V	900 mV	-1.55 V	-2.45 V	L	V_{OL}
7 V	900 mV	8.45 V	6.55 V	L	
1 V	6 V	4 V	-2 V	L	
4 V	6 V	7 V	1 V	L	
-2 V	500 mV	-1.75 V	-2.25 V	H	V_{OH}
7 V	500 mV	7.25 V	6.75 V	H	
1 V	-6 V	-2 V	4 V	H	
4 V	-6 V	1 V	7 V	H	
X	X	Open	Open	H	

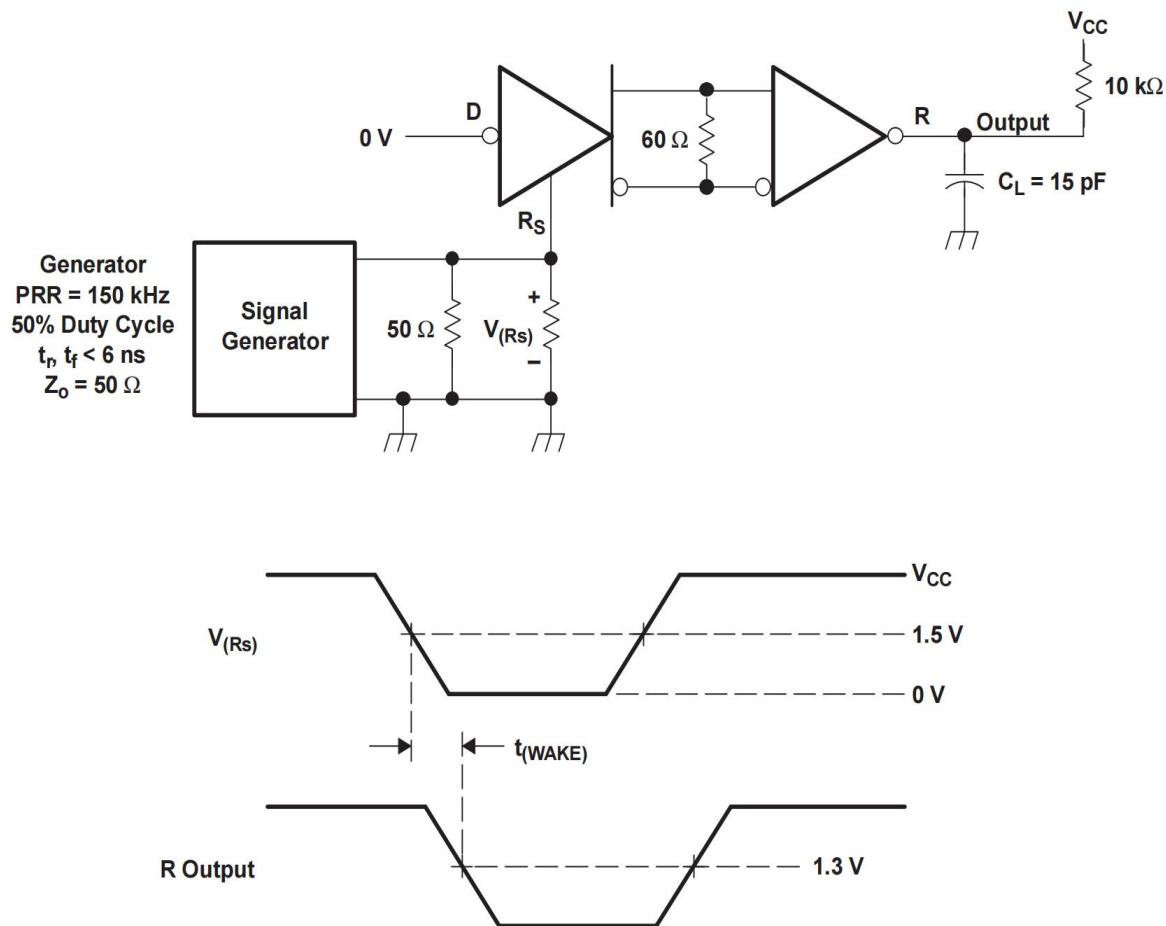
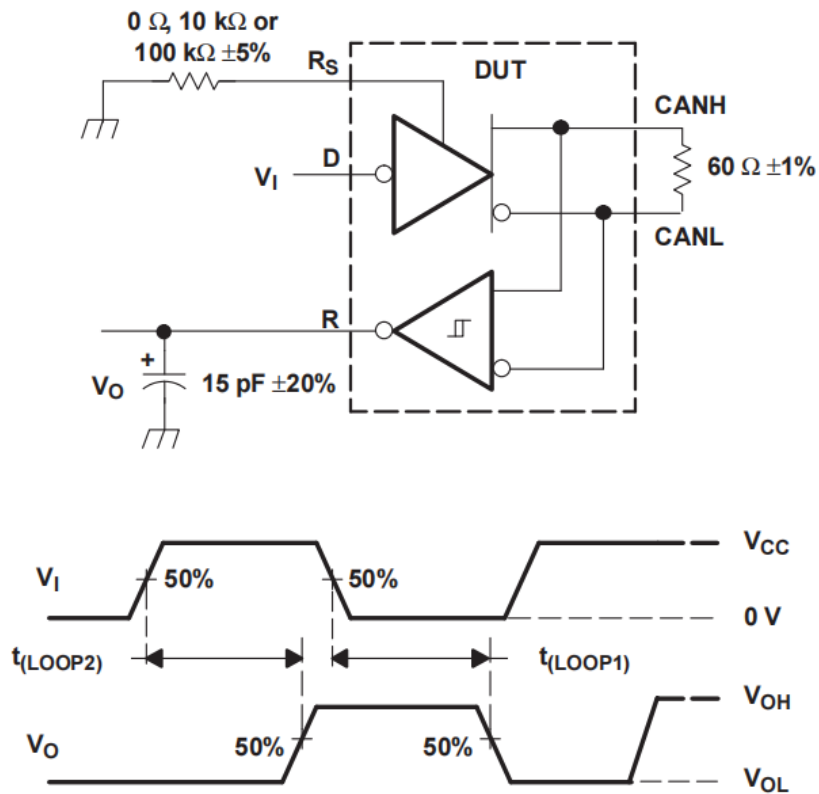


Figure 25. $t_{(WAKE)}$ Test Circuit and Voltage Waveforms



- A. All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 26. t_{LOOP} Test Circuit and Voltage Waveforms

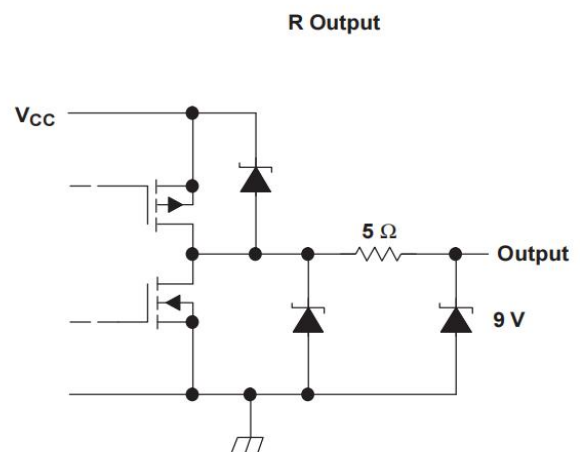
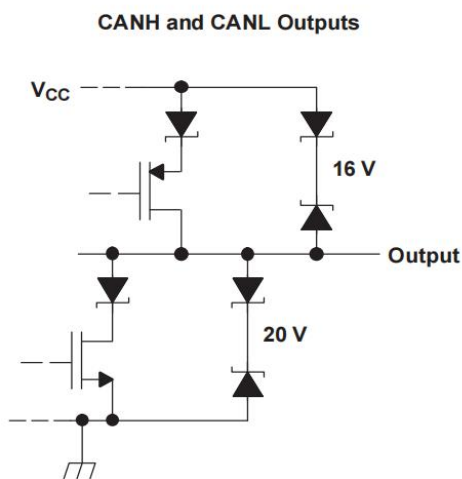
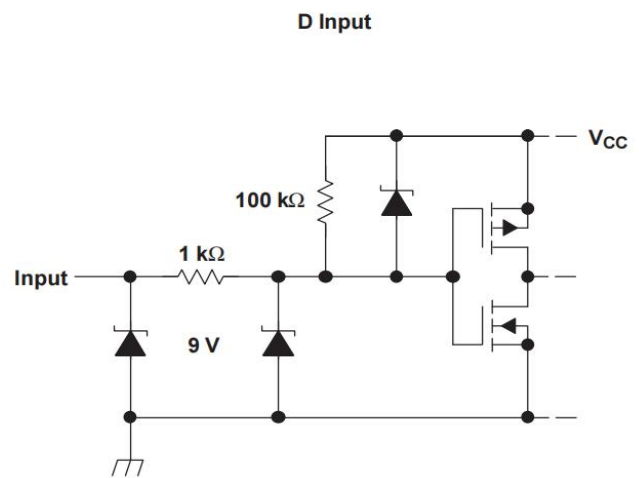
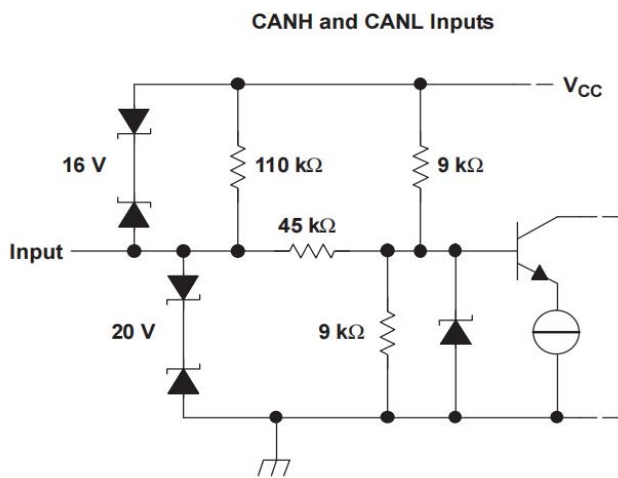


Figure 27. Equivalent Input and Output Schematic Diagrams



10 Detailed Description

10.1 Overview

ISO 11898 family of standards are the international standard for high speed serial communication using the controller area network (CAN) bus protocol and physical layers (transceivers). It supports multimaster operation, real time control, programmable data rates up to 1 Mbps, and powerful redundant error checking procedures that provide reliable data transmission. It is suited for networking *intelligent* devices as well as sensors and actuators within the rugged electrical environment of a machine chassis or factory floor. The SN65HVD23x family of 3.3 V CAN transceivers implement the lowest layers of the ISO/OSI reference model, the ISO11898-2 standard. This is the interface with the physical signaling output of the CAN controller of the Texas Instruments μ Ps, MCUs and DSPs, such as TMS320Lx240x 3.3 V DSPs, as illustrated in Figure 28.

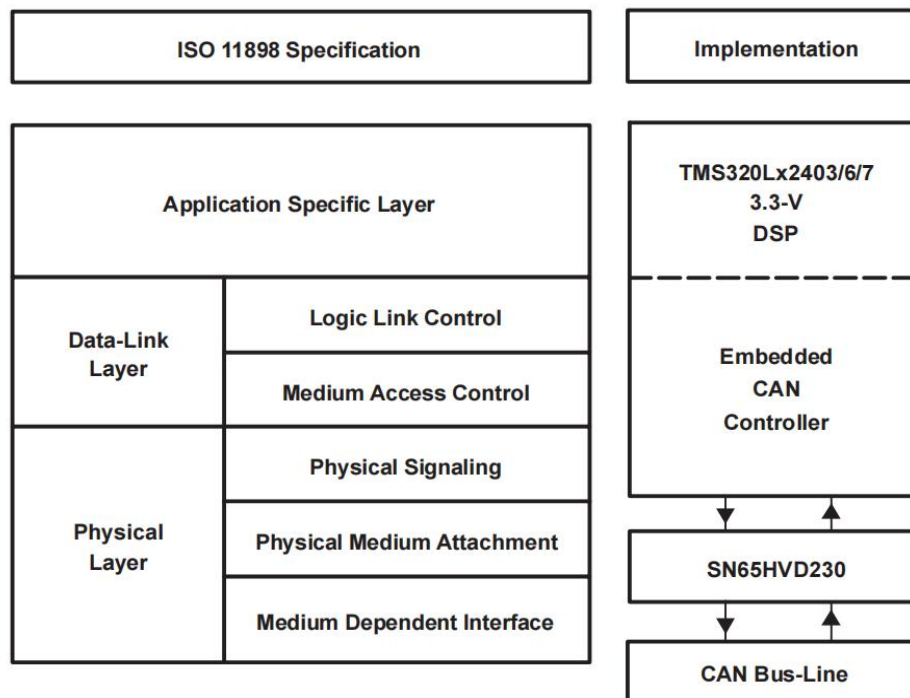


Figure 28. Layered ISO 11898 Standard Architecture

10.2 Functional Block Diagram

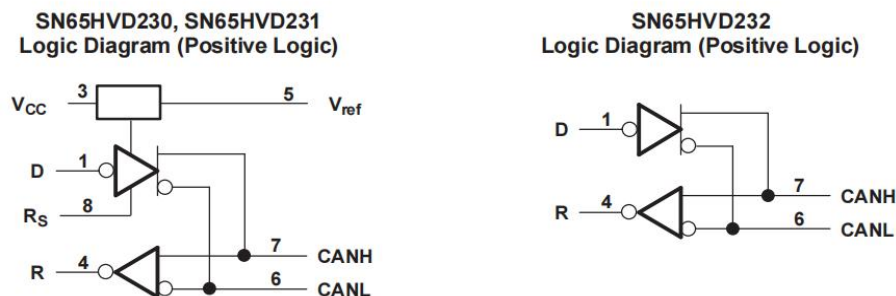


Figure 29. Logic Diagram (Positive Logic)



10.3 Feature Description

The SN65HVD230/231/232 are pin-compatible (but not functionally identical) with one another and, depending upon the application, may be used with identical circuit boards.

These transceivers feature single 3.3 V supply operation and standard compatibility with signaling rates up to 1 Mbps, ± 16 kV HBM ESD protection on the bus pins, thermal shutdown protection, bus fault protection, and open-circuit receiver failsafe. The fail-safe design of the receiver assures a logic high at the receiver output if the bus wires become open circuited.

The bus pins are also maintained in a high-impedance state during low V_{CC} conditions to ensure glitch-free power-up and power-down bus protection for hot-plugging applications. This high-impedance condition also means that an unpowered node does not disturb the bus. Transceivers without this feature usually have a very low output impedance. This results in a high current demand when the transceiver is unpowered, a condition that could affect the entire bus.

10.3.1 V_{ref} Voltage Reference

The V_{ref} pin (pin 5) on the SN65HVD230 and SN65HVD231 is available as a $V_{CC}/2$ voltage reference. This pin can be connected to the common mode point of a split termination to help further stabilize the common mode voltage of the bus. If the V_{ref} pin is not used it may be left floating.

10.3.2 Thermal Shutdown

If a high ambient temperature or excessive output currents result in thermal shutdown, the driver will be disabled and the bus pins become high impedance. During thermal shutdown the D pin to bus transmission path is blocked and the CAN bus pins are high impedance and biased to a recessive level. Once the thermal shutdown condition is cleared and the junction temperature drops below the thermal shutdown temperature the driver will be reactivated and resume normal operation. During a thermal shutdown the receiver to R pin path remains operational.

10.4 Device Functional Modes

The R_S pin (Pin 8) of the SN65HVD230 and SN65HVD231 provides three different modes of operation: high-speed mode, slope-control mode, and low-power mode.

10.4.1 High-Speed Mode

The high-speed mode can be selected by applying a logic low to the R_S pin (pin 8). The high-speed mode of operation is commonly employed in industrial applications. High-speed allows the output to switch as fast as possible with no internal limitation on the output rise and fall slopes. If the high speed transitions are a concern for emissions performance slope control mode can be used.

If both high speed mode and the low-power standby mode is to be used in the application, direct connection to a μP , MCU or DSP general purpose output pin can be used to switch between a logic-low level (< 1.2 V) for high speed operation, and the logic-high level ($> 0.75 V_{CC}$) for standby. Figure 30 shows a typical DSP connection, and Figure 31 shows the HVD230 driver output signal in high-speed mode on the CAN bus.

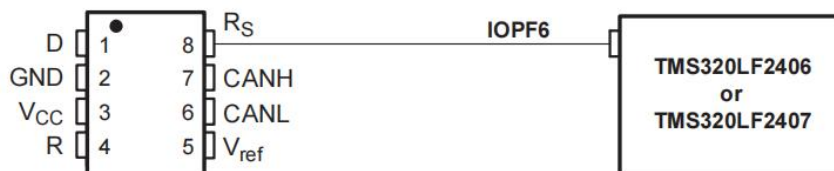


Figure 30. R_S (Pin 8) Connection to a TMS320LF2406/07 for High Speed/Standby Operation



10.4.2 Slope Control Mode

Electromagnetic compatibility is essential in many applications while still making use of unshielded twisted pair bus cable to reduce system cost. Slope control mode was added to the SN65HVD230 and SN65HVD231 devices to reduce the electromagnetic interference produced by the rise and fall times of the driver and resulting harmonics. These rise and fall slopes of the driver outputs can be adjusted by connecting a resistor from R_S (pin 8) to ground or to a logic low voltage, as shown in Figure 32. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 k Ω to achieve a ~ 15 V/ μ s slew rate, and up to 100 k Ω to achieve a ~ 2.0 V/ μ s slew rate as displayed in Figure 33.

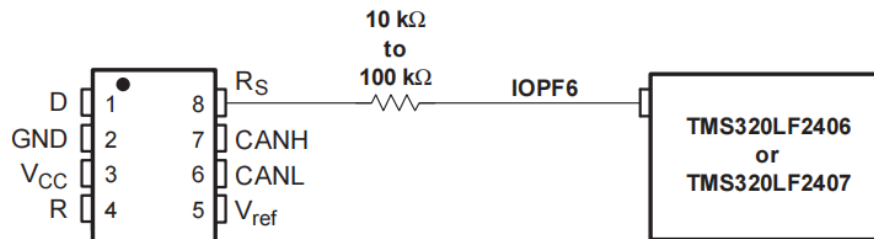


Figure 32. Slope Control/Standby Connection to a DSP



10.4.3 Standby Mode (Listen Only Mode) of the HVD230

If a logic high ($> 0.75 V_{CC}$) is applied to R_S (pin 8) in [Figure 30](#) and [Figure 32](#), the circuit of the SN65HVD230 enters a low-current, *listen only* standby mode, during which the driver is switched off and the receiver remains active. In this *listen only* state, the transceiver is completely passive to the bus. It makes no difference if a slope control resistor is in place as shown in [Figure 32](#). The μP can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900 mV typical) occurs on the bus. The μP , sensing bus activity, reactivates the driver circuit by placing a logic low (< 1.2 V) on R_S (pin 8).

10.4.4 The Babbling Idiot Protection of the HVD230

Occasionally, a runaway CAN controller unintentionally sends messages that completely tie up the bus (what is referred to in CAN jargon as a babbling idiot). When this occurs, the μP , MCU or DSP can engage the *listen-only* standby mode of the transceiver to disable the driver and release the bus, even when access to the CAN controller has been lost. When the driver circuit is deactivated, its outputs default to a high-impedance state (recessive).

10.4.5 Sleep Mode of the HVD231

The unique difference between the SN65HVD230 and the SN65HVD231 is that both driver and receiver are switched off in the SN65HVD231 when a logic high is applied to R_S (pin 8). The device remains in a very low power-sleep mode until the circuit is reactivated with a logic low applied to R_S (pin 8). While in this sleep mode, the bus-pins are in a high-impedance state, while the D and R pins default to a logic high.

10.4.6 Summary of Device Operating Modes

[Table 2](#) shows a summary of the operating modes for the SN65HVD230 and SN65HVD231. Please note that the SN65HVD232 is a basic CAN transceiver has only the normal high speed mode of operation; pins 5 and 8 are no connection (NC).



Device Functional Modes (continued)

Table 2. SN65HVD230 and SN65HVD231 Operating Modes

R _S Pin	MODE	DRIVER	RECEIVER	RXD Pin
LOW, V _(RS) < 1.2 V, strong pull down to GND	High Speed Mode	Enabled (ON) High Speed	Enabled (ON)	Mirrors Bus State ⁽¹⁾
LOW, V _(RS) < 1.2 V, 10 kΩ to 100 kΩ pull down to GND	Slope Control Mode	Enabled (ON) with Slope Control	Enabled (ON)	Mirrors Bus State
HIGH, V _(RS) > 0.75 V _{CC}	Low Current Mode	SN65HVD230: Standby Mode	Enabled (ON)	Mirrors Bus State
		SN65HVD231: Sleep Mode	Disabled (OFF)	High

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 3. SN65HVD230 and SN65HVD231 Driver Functions

DRIVER (SN65HVD230, SN65HVD231) ⁽¹⁾				
INPUT D	R _S	OUTPUTS		BUS STATE
		CANH	CANL	
L	V _(RS) < 1.2 V (including 10 kΩ to 100 kΩ pull down to GND)	H	L	Dominant
H		Z	Z	Recessive
Open	X	Z	Z	Recessive
X	V _(RS) > 0.75 V _{CC}	Z	Z	Recessive

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 4. SN65HVD230 Receiver Functions

RECEIVER (SN65HVD230) ⁽¹⁾		
DIFFERENTIAL INPUTS	R _S	OUTPUT R
V _{ID} ≥ 0.9 V	X	L
0.5 V < V _{ID} < 0.9 V	X	?
V _{ID} ≤ 0.5 V	X	H
Open	X	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

Table 5. SN65HVD231 Receiver Functions

RECEIVER (SN65HVD231) ⁽¹⁾		
DIFFERENTIAL INPUTS	R _S	OUTPUT R
V _{ID} ≥ 0.9 V	V _(RS) < 1.2 V (including 10 kΩ to 100 kΩ pull down to GND)	L
0.5 V < V _{ID} < 0.9 V		?
V _{ID} ≤ 0.5 V		H
X	V _(RS) > 0.75 V _{CC}	H
X	1.2 V < V _(RS) < 0.75 V _{CC}	?
Open	X	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

Table 6. SN65HVD232 Receiver Functions

RECEIVER (SN65HVD232) ⁽¹⁾	
DIFFERENTIAL INPUTS	OUTPUT R
V _{ID} ≥ 0.9 V	L
0.5 V < V _{ID} < 0.9 V	?
V _{ID} ≤ 0.5 V	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

Table 7. SN65HVD232 Driver Functions

DRIVER (SN65HVD232) ⁽¹⁾			
INPUT D	OUTPUTS		BUS STATE
	CANH	CANL	
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

(1) H = high level; L = low level; Z = high impedance



Termination is typically a $120\ \Omega$ resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 39). Split termination utilizes two $60\ \Omega$ resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

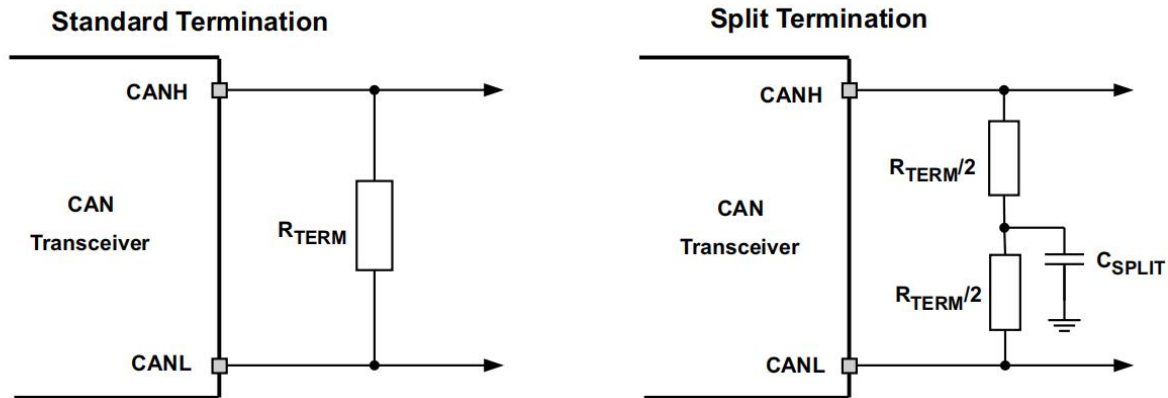


Figure 39. CAN Bus Termination Concepts

11.2.1.2 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (D pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (R pin).

12 Power Supply Recommendations

The SN65HVD23x 3.3 V CAN transceivers provide the interface between the 3.3 V μ Ps, MCUs and DSPs and the differential bus lines, and are designed to transmit data at signaling rates up to 1 Mbps as defined by the ISO 11898 standard.

To ensure reliable operation at all data rates and supply voltages, the V_{CC} supply pin of each CAN transceiver should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} and GND pins as possible. The TPS76333 is a linear voltage regulator suitable for supplying the 3.3-V supply.

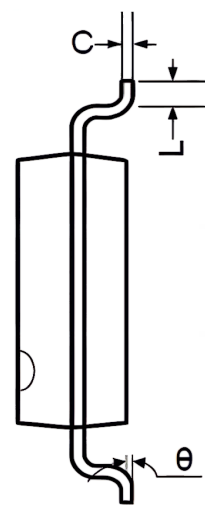
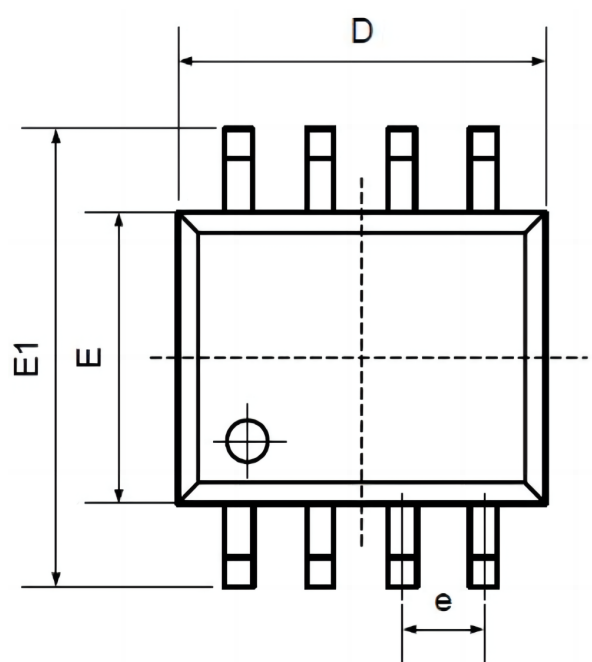


Order information

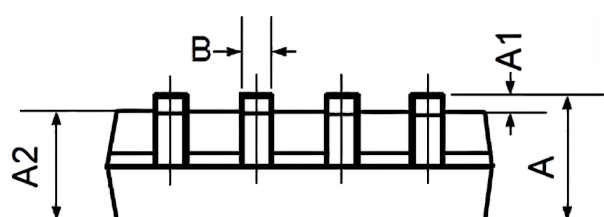
Order Number	Package	Package Quantity	Marking On The park
SN65HVD230DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD230DR
SN65HVD232DR-TUDI	SOP8	Tape,Reel,2500	SN65HVD232DR
SN65HVD232QDR-TUDI	SOP8	Tape,Reel,2500	SN65HVD232QDR



Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°





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