SISS27ADN-T1-GE3-VB Datasheet

P-Channel 30V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 30	0.004 at V_{GS} = - 10 V	- 52	39.5 nC
	0.005 at V_{GS} = - 4.5 V	- 47	

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Trench Power MOSFET
- 100% R_g Tested
- 100% UIS Tested
- Compliant to RoHS Directive 2002/95/EC

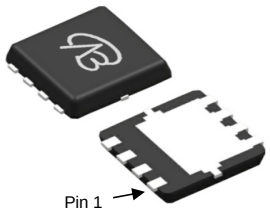
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

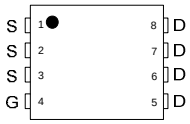
- Notebook Adapter Switch
- Notebook Load Switch

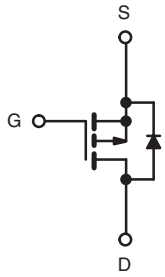
DFN 3x3

Top View Bottom View



Top View





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 52	A
	T_C = 70 °C		- 40	
	T_A = 25 °C		- 17.3[a, b]	
	T_A = 70 °C		- 13.8[a, b]	
Pulsed Drain Current		I_{DM}	- 150	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 35[d]	
	T_A = 25 °C		- 3.0[a, b]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 20	
Single-Pulse Avalanche Energy		E_{AS}	20	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	52	W
	T_C = 70 °C		33	
	T_A = 25 °C		3.7[a, b]	
	T_A = 70 °C		2.4[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[e, f]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a, c]	t ≤ 10 s	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.4	

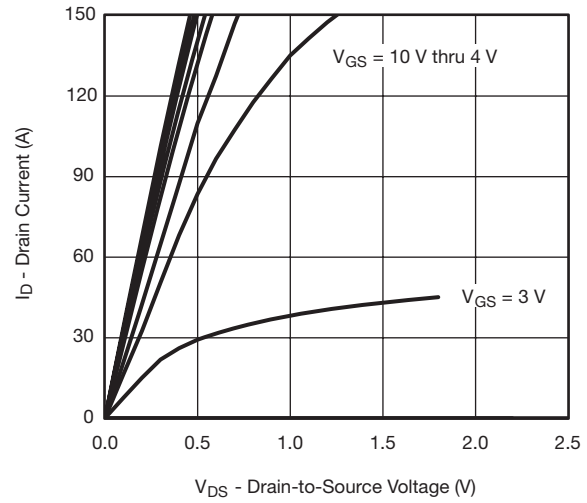
Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. Maximum under steady state conditions is 81 °C/W.
d. Package limited.
e. The PowerPAK 1212-8 is a leadless package.The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 23		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.0		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.0		- 2.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ - 10 V, V_{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 15 A		0.004		Ω
		V_{GS} = - 4.5 V, I_D = - 10 A		0.005		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 15 A		47		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		4427		pF
Output Capacitance	C_{oss}			452		
Reverse Transfer Capacitance	C_{rss}			430		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 10 A		84.5	126	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 10 A		39.5	60	
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			13.5		
Gate Resistance	R_g	f = 1 MHz	0.4	1.8	3.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω, $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		15	30	ns
Rise Time	t_r			13	26	
Turn-Off DelayTime	$t_{d(off)}$			55	100	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω, $I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		55	100	
Rise Time	t_r			42	80	
Turn-Off DelayTime	$t_{d(off)}$			52	100	
Fall Time	t_f			17	34	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	T_C = 25 °C			- 35	A
Pulse Diode Forward Current	I_{SM}				- 80	
Body Diode Voltage	V_{SD}	I_S = - 3 A, V_{GS} = 0 V		- 0.74	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		14	24	ns
Body Diode Reverse Recovery Charge	Q_{rr}			4	8	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			6		

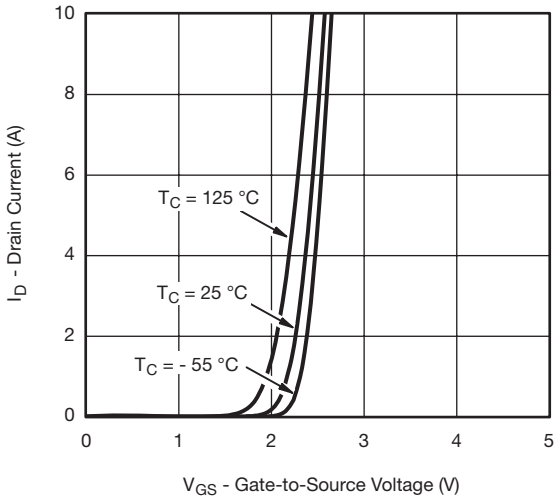
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

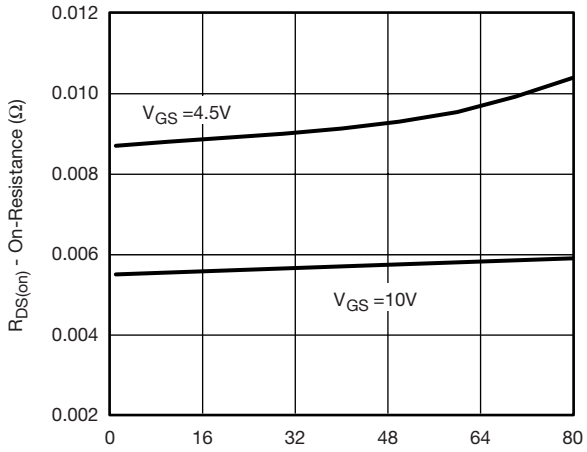
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



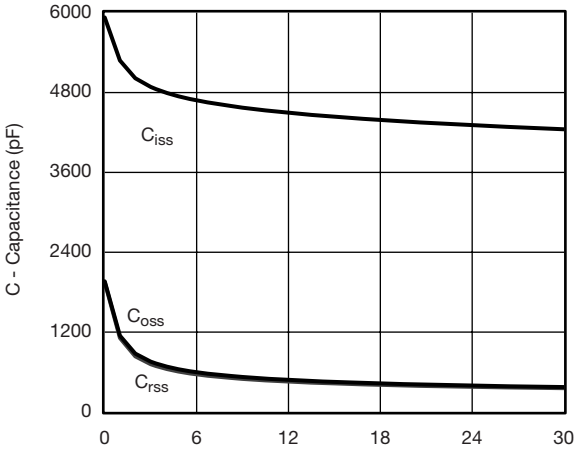
Output Characteristics



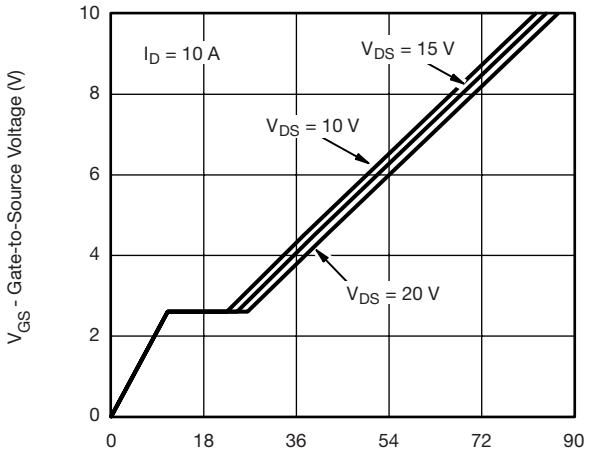
Transfer Characteristics



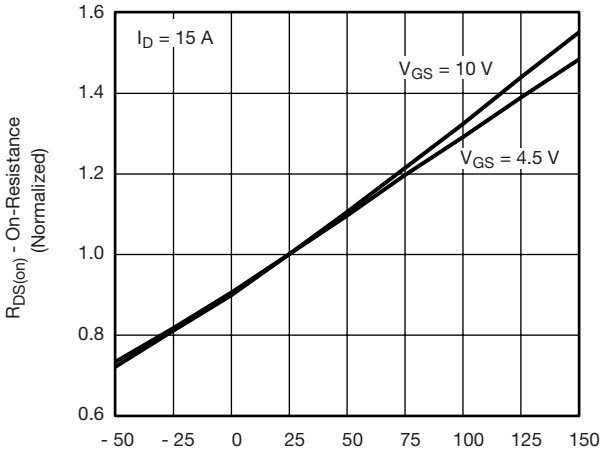
On-Resistance vs. Drain Current



Capacitance

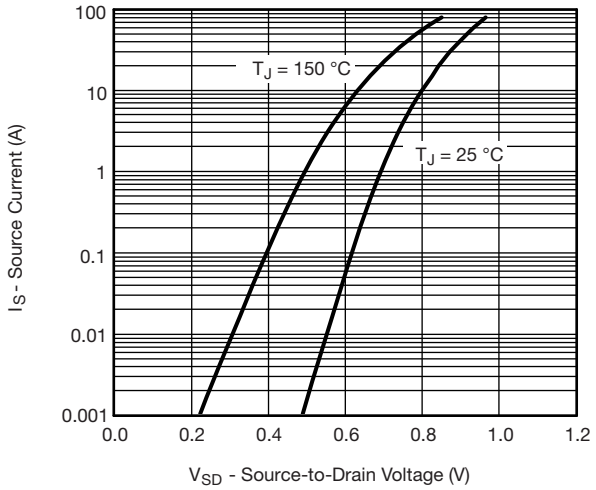


Gate Charge

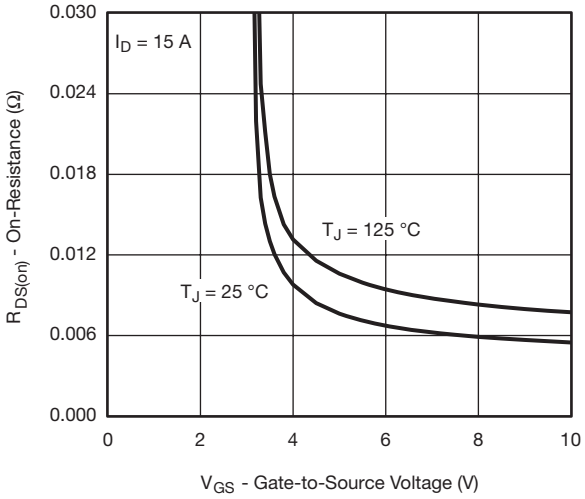


On-Resistance vs. Junction Temperature

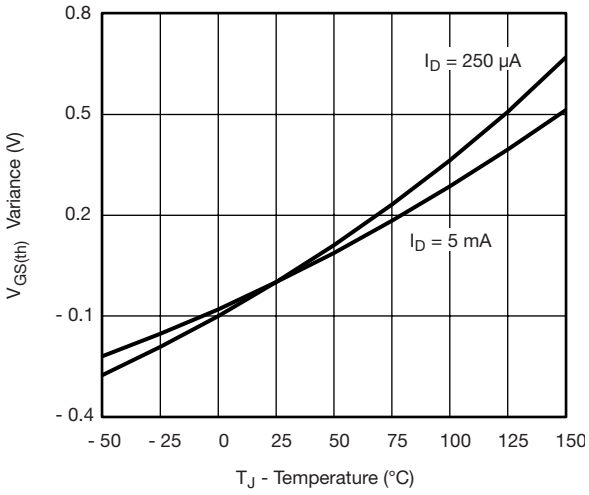
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



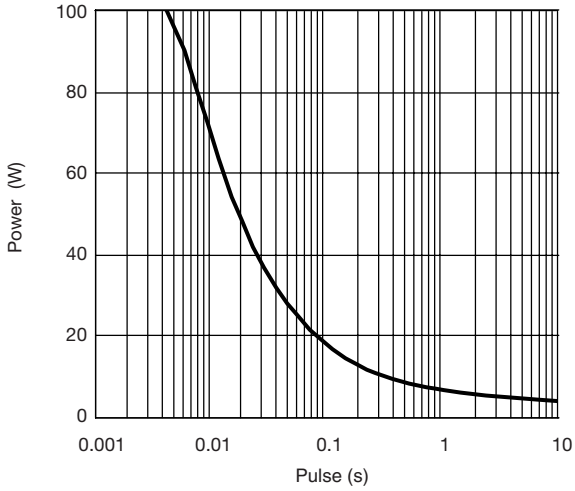
Source-Drain Diode Forward Voltage



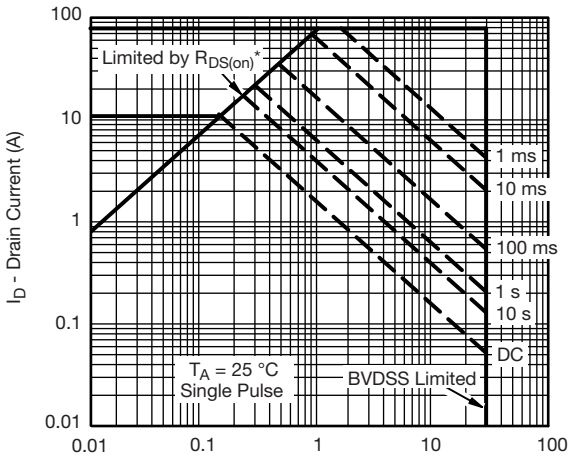
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



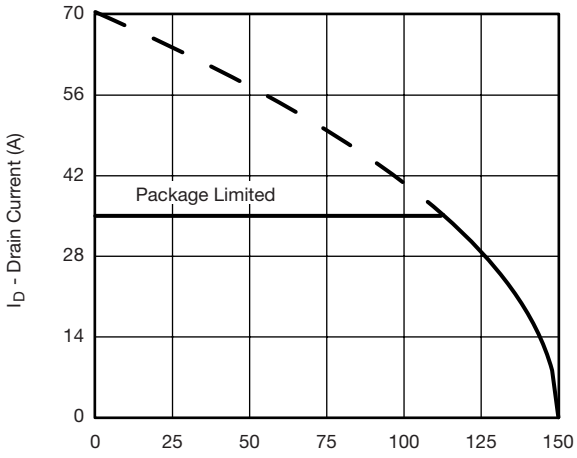
Single Pulse Power, Junction-to-Ambient



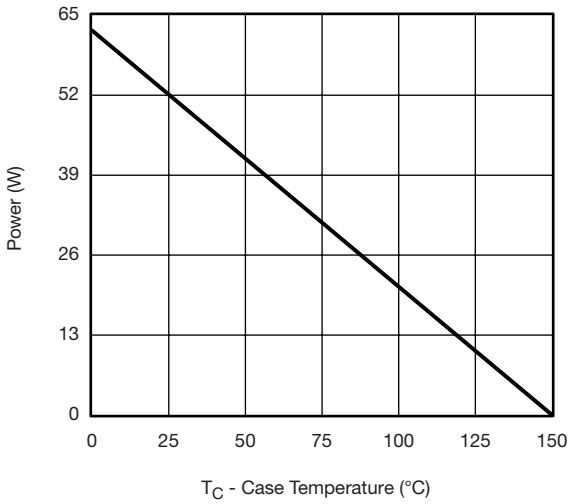
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

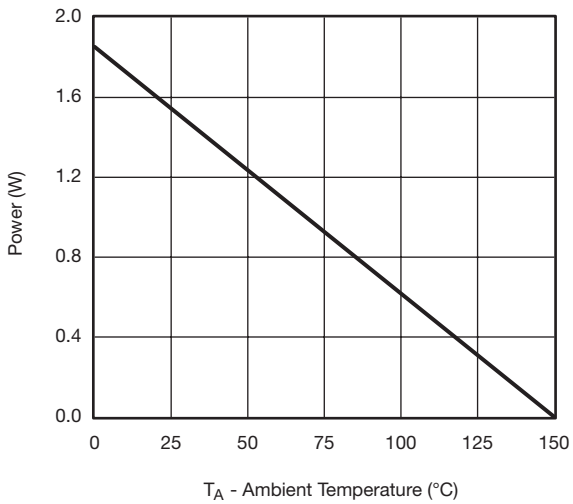
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



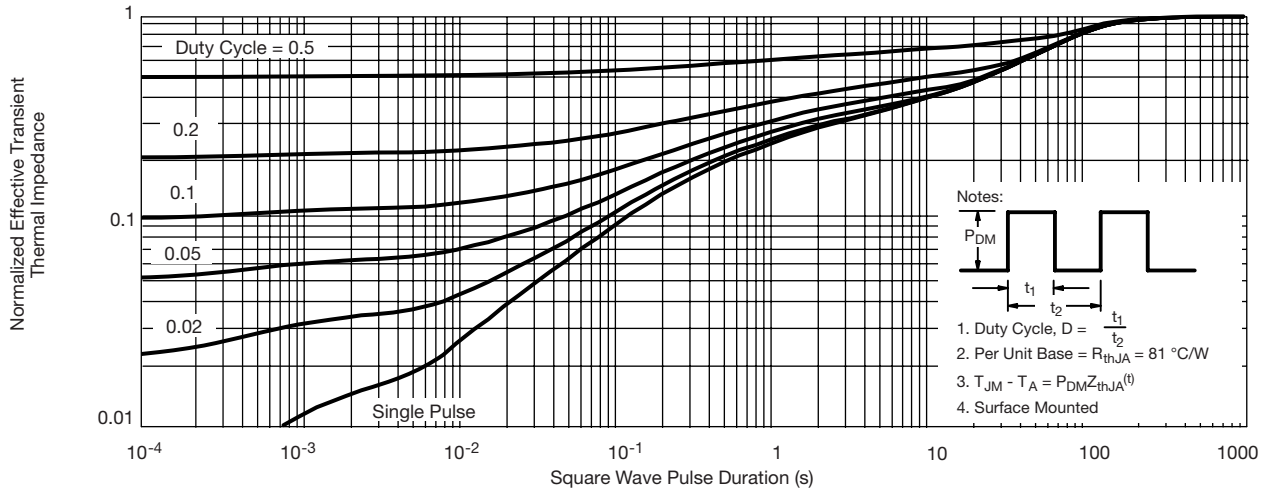
Power, Junction-to-Case



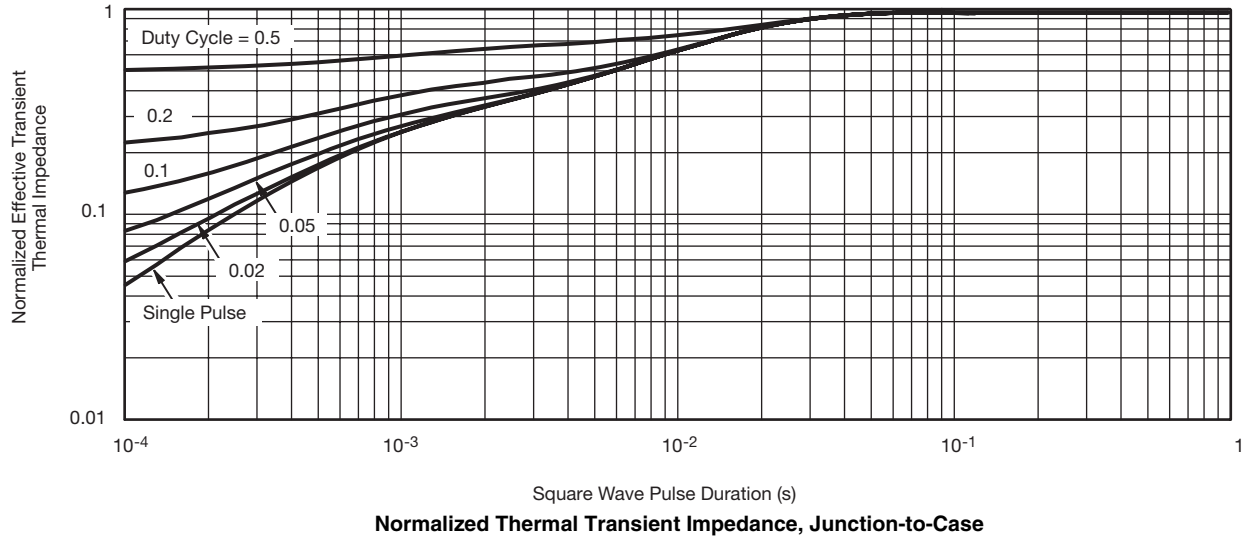
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

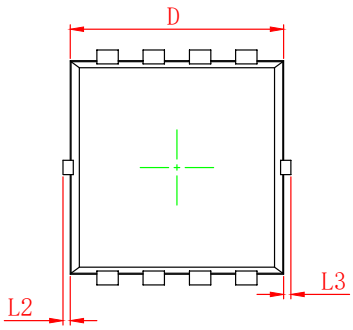


Normalized Thermal Transient Impedance, Junction-to-Ambient

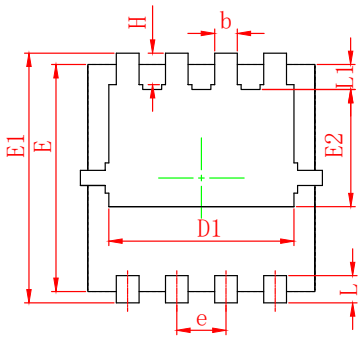


Normalized Thermal Transient Impedance, Junction-to-Case

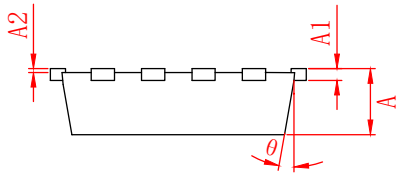
PDFNWB3×3-8L Package Outline Dimensions



Top View
[顶视图]



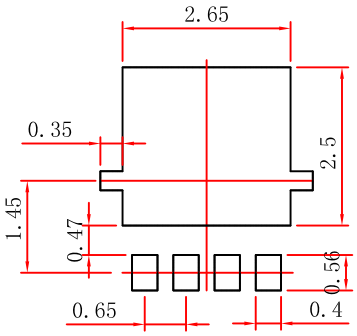
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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