XPC2444

17V, 12A, High-Efficiency Synchronous Step-Down Converter

FEATURES

- 2.7V to 17V Input Range with External 3.3V Bias
- 3.5V to 17V Input Range without External Bias
- Output Voltage Range: 0.6 V to 5.5 V
- 0.6V ± 1% Voltage Reference from −40°C to +125°C Junction Temperature Range
- COT Control for Ultra-fast Load-step Response
- Supports All Ceramic Output Capacitors
- Selectable FCCM or PSM Operation at Light Load
- Selectable Operation Switching Frequency (600kHz/800kHz/1MHz)
- Non-Latch for OCP, UVP, UVLO, and OTP Faults, Latch Off for OVP
- Differential Remote Sense Voltage for High Output Accuracy
- Open-drain Power-good Output
- Enable Control
- Programmable Soft-Start Time
- Programmable Valley Current Limit Level
- Monotonic Start-Up into Pre-Biased Outputs
- Output Voltage Tracking
- Compact 3mm × 4mm, 21-pin FCQFN Package
- RoHS Compliant and Halogen Free

APPLICATIONS

- Server, Storage and Network Equipment
- Telecom Infrastructure
- Point of Load (POL) Power Modules
- High Density DC-DC Converters

DESCRIPTION

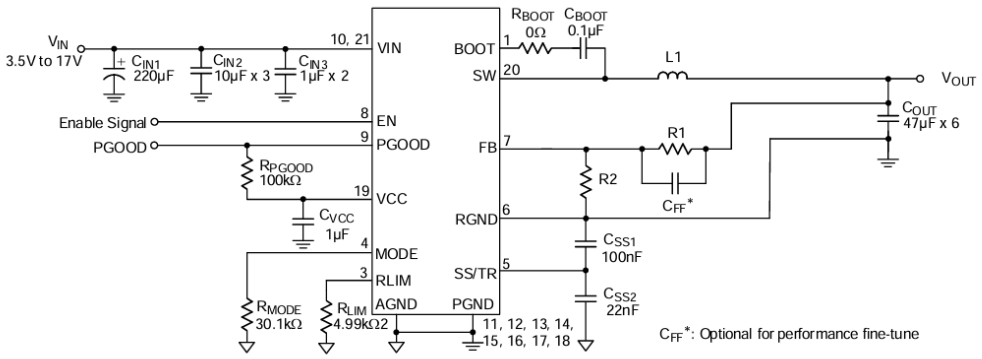
The XPC2444 is a high-performance, synchronous step-down converter that can deliver up to 12A output current with an input supply voltage range of 3.5V to 17V. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V ± 1% reference over the full operating junction temperature range and an integrated diode for bootstrap circuit to offer a very compact solution.

The XPC2444 adopts Constant On-Time control architecture that provides ultrafast transient response and further reduce the external-component count. In steady states, this part operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers a variety of functions for more design flexibility. The selectable switching frequency, current limit level and PWM operation modes makes the XPC2444 easy-to-use over wide application range. Independent enable control input pin and power good indicator are also provided for easy sequence control. To control the inrush current during the startup, the device provides a programmable soft start-up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit, OVP, UVP, input UVLO and OTP.

The XPC2444 is available in a thermally enhanced QFN-21L 3x4 (FC) package.

TYPICAL APPLICATION CIRCUIT



Notes:

1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Table 1. Suggested Component Selections for the Application of 600kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.8	3.32	10	0.4	88	282	1000 to 2200
1.2	10		0.68	88	282	470 to 1000
3.3	45.2		1.2	88	282	220 to 470
5	73.2		1.5	88	282	150 to 330

Table 2. Suggested Component Selections for the Application of 800kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.8	3.32	10	0.33	88	282	1000 to 2200
1.2	10		0.47	88	282	470 to 1000
3.3	45.2		1	88	282	220 to 470
5	73.2		1.2	88	282	150 to 330

Table 3. Suggested Component Selections for the Application of 1000kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.8	3.32	10	0.22	88	282	1000 to 2200
1.2	10		0.33	88	282	470 to 1000
3.3	45.2		0.68	88	282	220 to 470
5	73.2		1	88	282	150 to 330

Table 4. Suggested Inductors for Typical Application Circuit

Inductance (μH)	Part No.	I_{SAT} (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.22	VLBU1007090T R22L	57	0.18	10 x 7 x 9	TDK
0.33	VLBU1007090T R33L	39	0.18	10 x 7 x 9	TDK
0.4	VLBU1007090T R40L	30	0.18	10 x 7 x 9	TDK
0.47	744314047	20	1.35	6.9 x 6.9 x 4.8	WE
0.68	744393580068	52	1.41	8.8 x 8.3 x 7.8	WE
1	74439358010	38	2.1	8.8 x 8.3 x 7.8	WE
1.2	744325120	25	1.8	10.2 x 12.1 x 4.7	WE
1.5	744393580150	32	2.91	8.8 x 8.3 x 7.8	WE

Table 5. Suggested Capacitor for Typical Application Circuit

Capacitance (μF)	Part No.	Case Size	Component Supplier
10	GRM31CR71E106KA12L	1206	Murata
47	GRM31CR60J476ME19	1206	Murata

REVISION HISTORY

Release	Rev	Changes	Date
Release	1.0	Finalized	June-2024

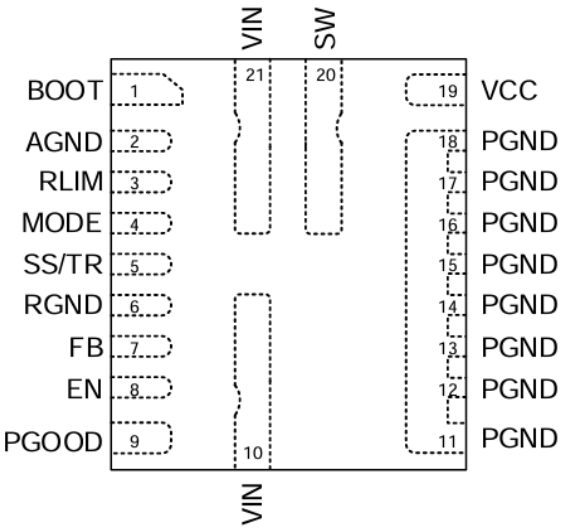
ORDERING INFORMATION

Part Number	Output Current (A)	Top Marking	MPQ
XPC2444Q21R	12	2444	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN Configuration and Description

TOP VIEW



QFN-21 3x4 (FC)

Pin Configuration

Pin	Name	Description
1	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.
2	AGND	Analog ground. Reference point for the internal control circuit. Connect AGND and PGND with a short trace and at only one point to reduce circulating currents.
3	RLIM	Valley current limit setup pin. Connect a resistor from this pin to AGND to set the valley current limit value. At least ±1% resistor is required.
4	MODE	Mode selection setup pin. The mode pin can be set to force continuous conduction mode (FCCM) or pulse skipping mode (PSM) for high light-load efficiency, and the operation switching frequency. At least ±1% resistor is required.
5	SS/TR	Soft-start and tracking control input. Connect a ceramic capacitor from this pin to RGND to program the soft-start time. The internal minimum start-up time is 1 ms (typ.). A minimum capacitor of 22nF on this pin is required for smooth charging. For the tracking function, the device can track the pin voltage as the reference for tracking applications because the SS/TR pin voltage can override the internal VREF.
6	RGND	Differential remote voltage sense. Connect this pin to the negative side of the remote voltage sense point. Short to GND as internal reference if the remote voltage sense is not used.
7	FB	Feedback voltage input. The pin is used to set the converter's output voltage via a resistor divider. It is suggested to place the feedback resistor divider as close to the FB pin as possible.
8	EN	Enable control input. A logic-high enables the converter; however, a logic low forces the device into shutdown mode. Do not leave this pin floating.
9	PGOOD	Open-drain, power-good indication output. It is pulled low if the feedback voltage is out of the PGOOD threshold, IC shuts down from fault state and EN goes low, and before the soft-start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
10, 21	VIN	Power input voltage. Support 3.5V to 17V input voltage. It is suggested to place decoupling input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
11, 12, 13 14, 15, 16, 17, 18	PGND	The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections.

19	VCC	3V internal LDO output. An external DC voltage source 3.3V±5% can be connected to this pin for less power losses on the internal LDO and supply both the internal circuitry and gate driver. Connect a 1μF, X7R ceramic capacitor as close to the VCC pin as possible. It is not recommended to connect VCC to supply other rails.
20	SW	Switch node. Output switching state between high-side MOSFET switching and low-side MOSFET switching of the power converter. Connect SW pin to the external inductor and bootstrap capacitor.

Absolute Maximum Ratings (1)

Parameter	Min	Max	Units
Supply Input Voltage, VIN	-0.3	18	V
Enable Pin Voltage, EN	-0.3	18	V
SW	-0.3	18	V
SW (25ns transient)	-5	25	V
VIN-SW	-0.3	18	V
VIN-SW (25ns transient)	-4	25	V
BOOT	-0.3	24	V
BOOT−SW	-0.3	6	V
VCC	-0.3	7.5	V
All Other Pins	-0.3	6	V
Power Dissipation, PD @ TA = 25°C	3.39		W
Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range	-65	150	°C
ESD Susceptibility HBM (Human Body Model)	2		kV

RECOMMENDED OPERATING CONDITIONS (2)

Parameter	Symbol	Min	Max	Units
VIN without external 3.3V bias	V_{IN}	3.5	17	V
VIN with external 3.3V bias		2.7	17	V
Output Voltage	V_{OUT}	0.6	5.5	V
External VCC bias	V_{CC_EXT}	3.12	3.6	V
Junction Temperature Range	T_{OJ}	-40	+125	°C

Thermal Information(3)

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four-layer XPC2444 EVB in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units

Junction-to-Ambient Thermal Resistance, QFN-14 2x3	θ_{JA}	50	°C/W
Junction-to- Case (top) Thermal Resistance, QFN-14 2x3	$\theta_{JC(top)}$	28	°C/W
Junction-to- Case (bottom) Thermal Resistance, QFN-14 2x3	$\theta_{JC(bottom)}$	1.38	°C/W

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) The device is not guaranteed to function outside its operating conditions.

(3) θJA is measured in the natural convection at TA = 25°C on a Four-layer Evaluation Board. θJC(top) is measured at the top of the package.

ELECTRICAL SPECIFICATIONS

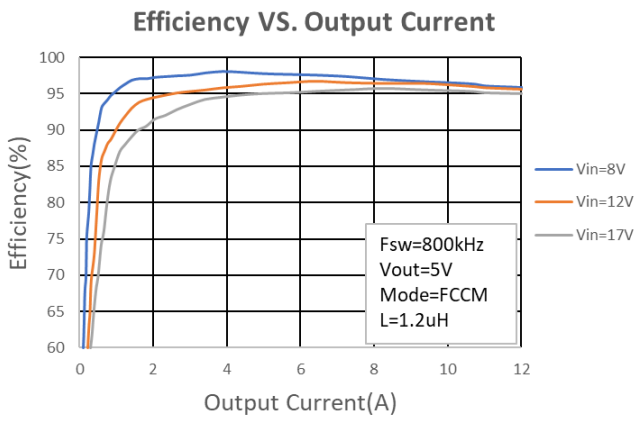
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

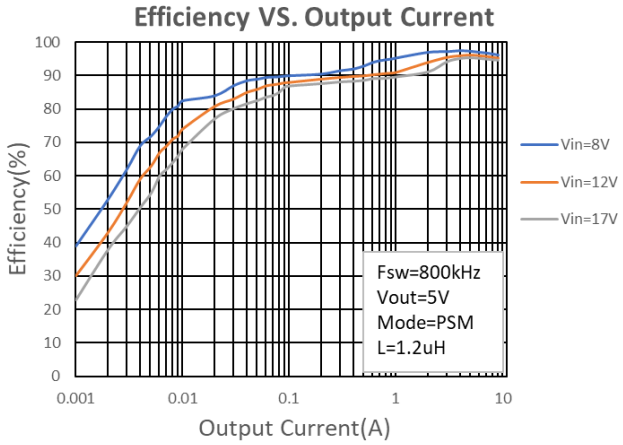
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current						
VIN Shutdown Current	Isd	V_{EN} = 0V		7	15	uA
VIN Quiescent Current	I_Q	V_{EN} = 2V, non-switching		1100	1300	uA
Logic Threshold						
EN Threshold Voltage	V_{EN_R}	V_{EN} Rising	1.175	1.225	1.3	V
EN Threshold Hysteresis	V_{EN_HYS}			200		mV
EN Pull-Down Current	I_{PD_EN}	V_{EN} = 2V		0.5	5	uA
VFB Voltage						
FB Voltage	VFB	TJ = −40°C to +125°C	0.594	0.6	0.606	V
Switching Frequency						
Switching Frequency	fSW1	R_{MODE}=0Ω, I_{OUT} = 0A, V_{OUT} = 1V	480	600	720	kHz
	fSW2	R_{MODE}=30.1kΩ, I_{OUT} = 0A, V_{OUT} = 1V	680	800	920	kHz
	fSW3	R_{MODE}=60.4kΩ, I_{OUT} = 0A, V_{OUT} = 1V	850	1000	1150	kHz
Internal MOSFET						
High Side ON Resistance	$R_{DS(ON)\_H}$	T_J = 25°C, VCC = 3V		12.8		mOhm
Low Side ON Resistance	$R_{DS(ON)\_L}$	T_J = 25°C, VCC = 3V		3.9		mOhm
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	TJ = 25°C			50	ns
Minimum Off-Time	t_{OFF_MIN}	TJ = 25°C			210	ns
Soft-Start and Tracking						
Soft-Start Time	t_{SS}	Internal soft-start time		1	1.5	ms
Soft-Start Charge Current	I_{SS_CHG}	VSS/TR = 0V		42		uA
Soft-Start Discharge Current	I_{SS_DISCHG}	VSS/TR = 1V		12		uA
Current Limit						
Current Limit Voltage Threshold	V_{LIM}	TJ = 25°C, valley current		1.2		V
I_{CS} to I_{OUT} Ratio	G_{CS} (I_{CS}/I_{OUT})	$I_{OUT} \geq$ 2A		20		uA/A
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	TJ = 25°C, valley current, R_{LIM} = 5kΩ		12		A
Low-Side Negative Current-Limit	I_{LIM_NEG}	TJ = 25°C, valley current		-9		A
UVLO						

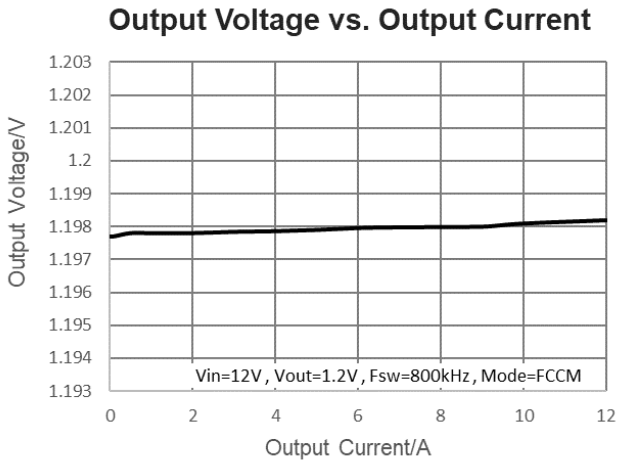
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

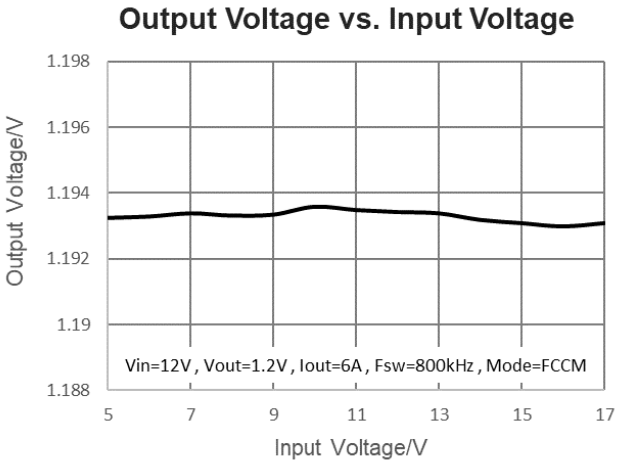
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
UVLO Rising Threshold	V_{UVLO_R}	V_{IN} rising, VCC_EXT = 3.3V	2.1	2.5	2.7	V
UVLO Hysteresis	V_{UVLO_HYS}	V_{IN} hysteresis		500		mV
LDO Output						
LDO Output Voltage	V_{CC}	I_{VCC} = 1mA	2.88	3	3.18	V
V_{CC} UVLO Rising Threshold	$V_{CC\_UVLO\_R}$	LDO rising	2.65	2.8	2.95	V
V_{CC} Hysteresis	$V_{CC\_UVLO\_HYS}$	LDO hysteresis		300		mV
LDO Output Current Limit	I_{LIM_LDO}			100		mA
Power Good						
Power Good Threshold	VTH_PGLH1	VFB rising threshold, PGOOD from low to high (GOOD)	89.5	92	95.5	%V_{FB}
	VTH_PGHL1	VFB falling hysteresis, PGOOD from high to low (FAULT)	113	115	119	%V_{FB}
	VTH_PGLH2	VFB rising threshold, PGOOD from high to low (FAULT)	102	105	109	%V_{FB}
	VTH_PGH2	VFB falling hysteresis, PGOOD from low to high (GOOD)	77	80	83	%V_{FB}
Power-Good Output Low Level Voltage	VPG_L_100	TJ = 25°C, VIN & VCC & VEN = 0V, PGOOD Pull up to 3.3V bias with 100k resistor		650	850	mV
	VPG_L_10	TJ = 25°C, VIN & VCC & VEN = 0V, PGOOD Pull up to 3.3V bias with 10k resistor		800	1000	mV
Power-Good Delay	tPGDLY_LH	TJ = 25°C, VTH_PGLH1 and VTH_PGLH2, PGOOD from low to high (GOOD)	0.6	0.8	1.0	ms
Output Over-Voltage and Under-Voltage Protections						
Output OVP Threshold	V_{OVP}	OVP detect	113	116	119	%V_{FB}
Output UVP Threshold	V_{UVP}	UVP detect	77	80	83	%V_{FB}
Over Temperature Protection						
Thermal Shutdown	Tsd			160		°C
Thermal Shutdown Hysteresis	ΔTsd			30		°C
Output Discharge Resistance						
Output Discharge Resistor	R_{DISCHG}	V_{EN} = 0V or Protection triggered		80	150	Ohm

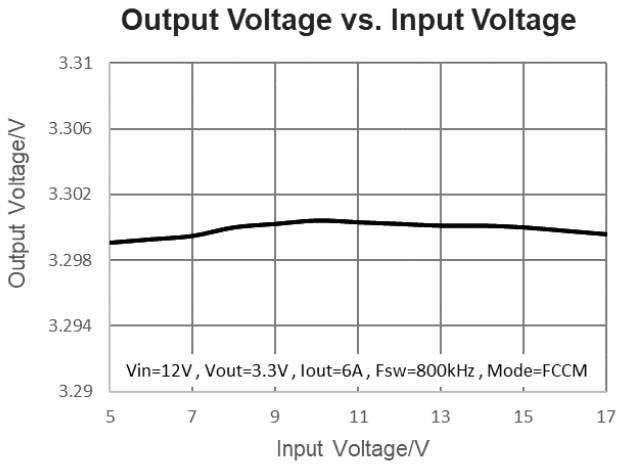
TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

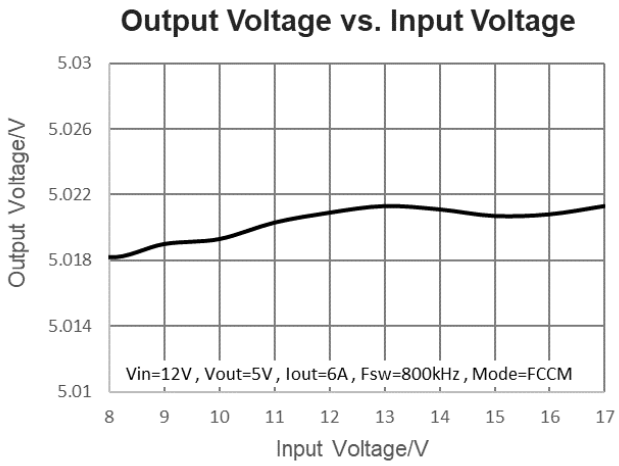




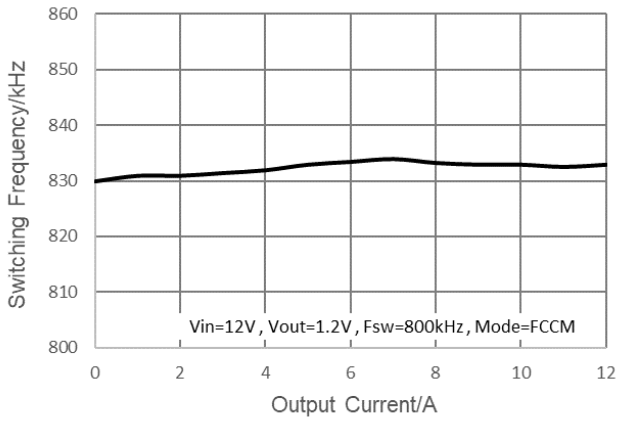




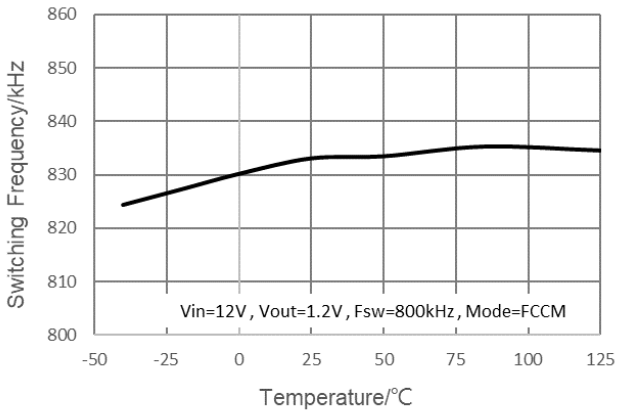




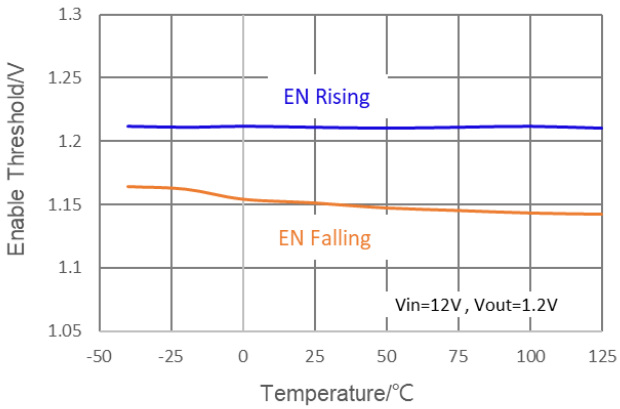
Switching Frequency vs. Output Current



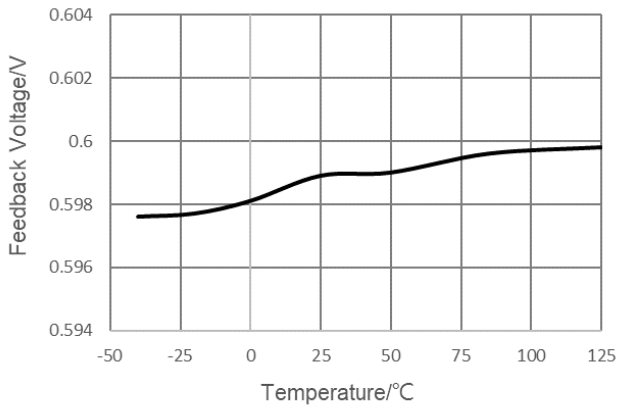
Switching Frequency vs. Temperature



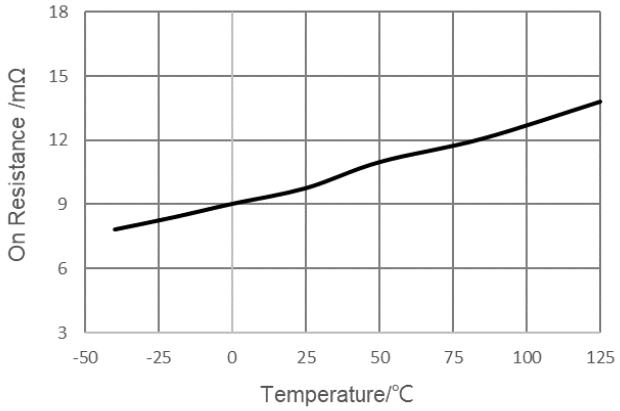
Enable Threshold vs. Temperature



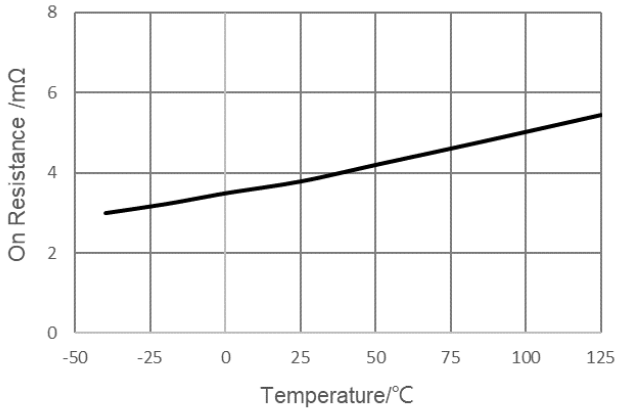
Feedback Voltage vs. Temperature



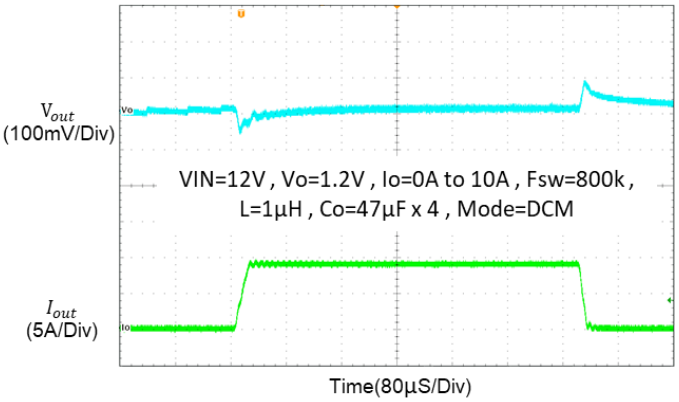
High-Side Rds(on) vs. Temperature



Low-Side Rds(on) vs. Temperature



Load Transient Response



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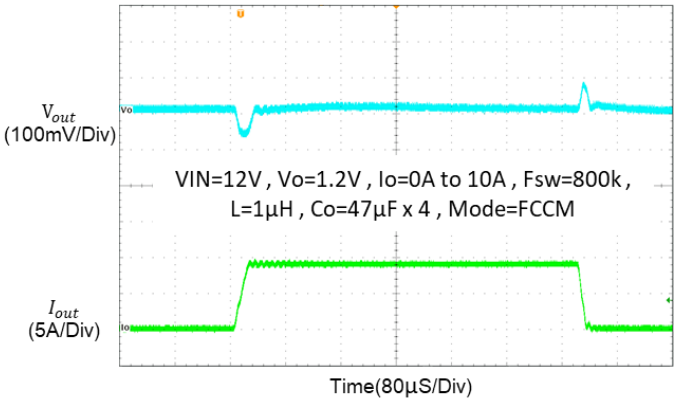

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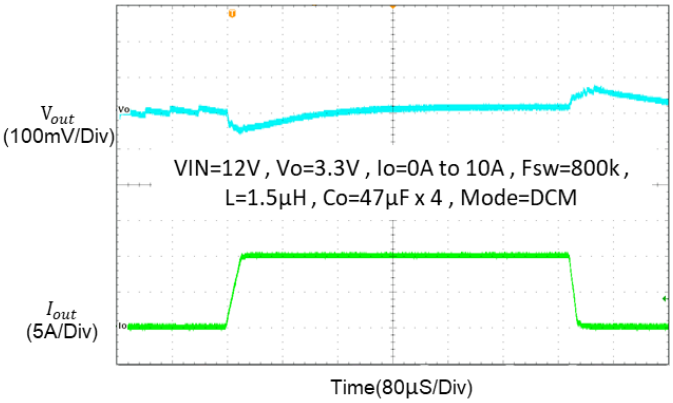

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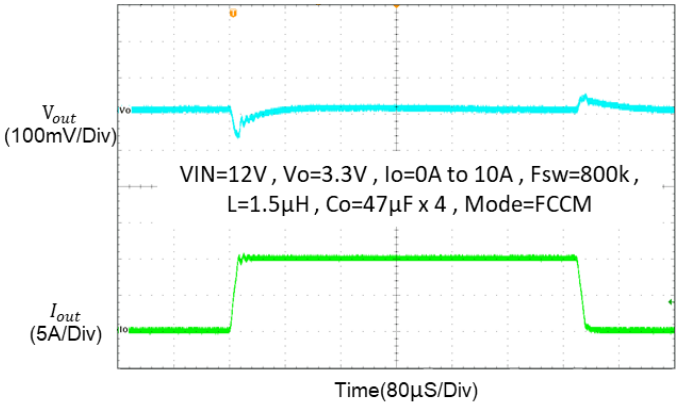
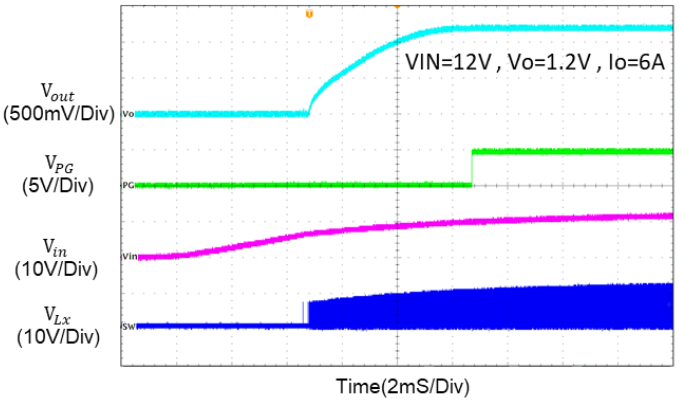
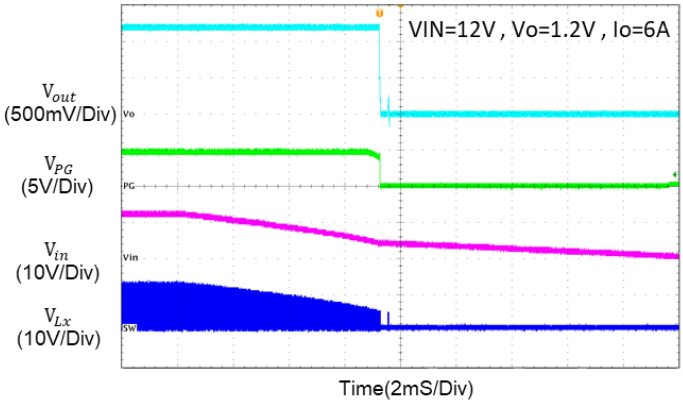


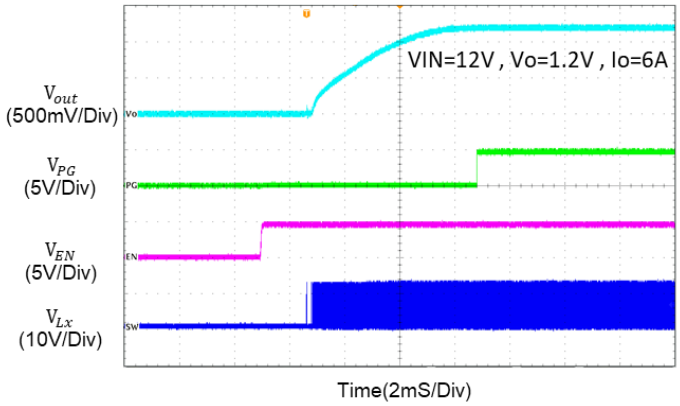
Power On from VIN



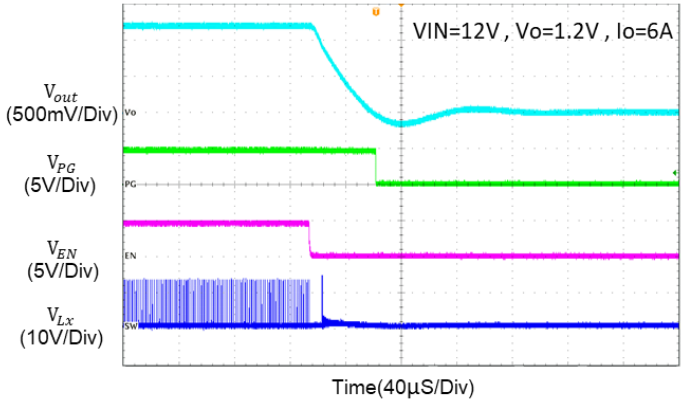
Power Off from VIN



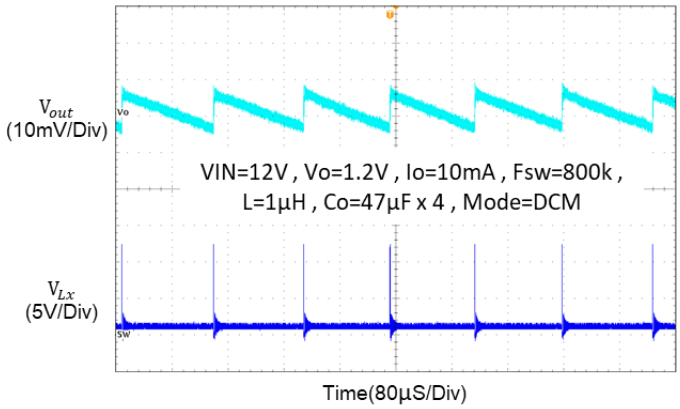
Power On from EN



Power Off from EN



Output Ripple Voltage



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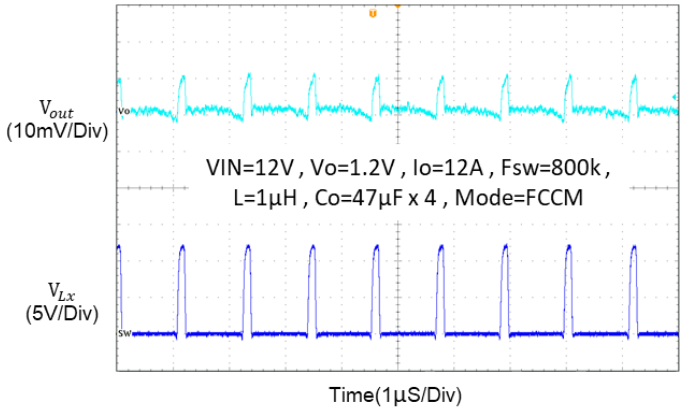

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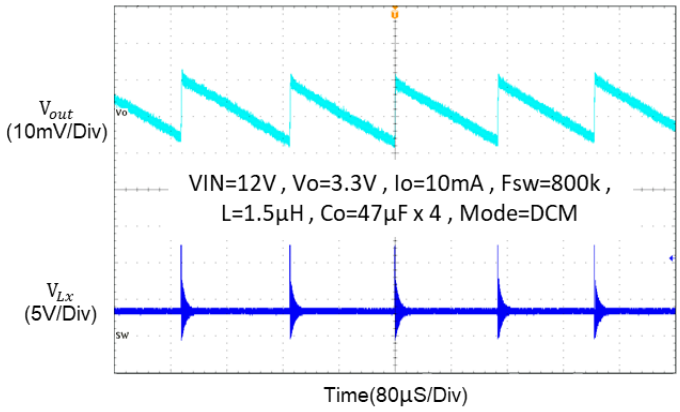
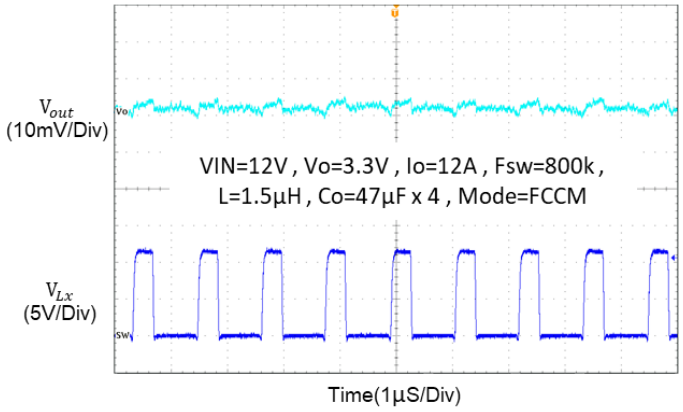
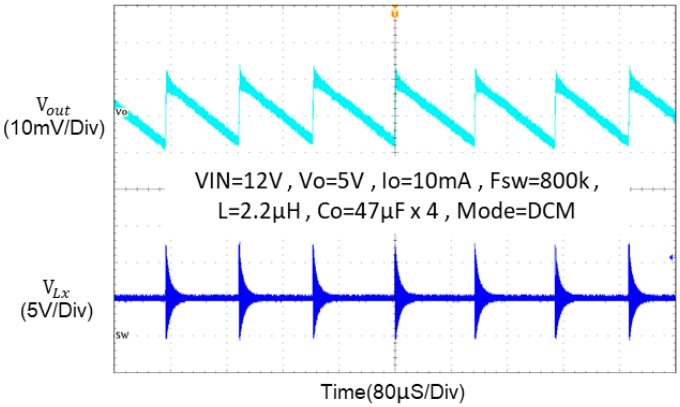


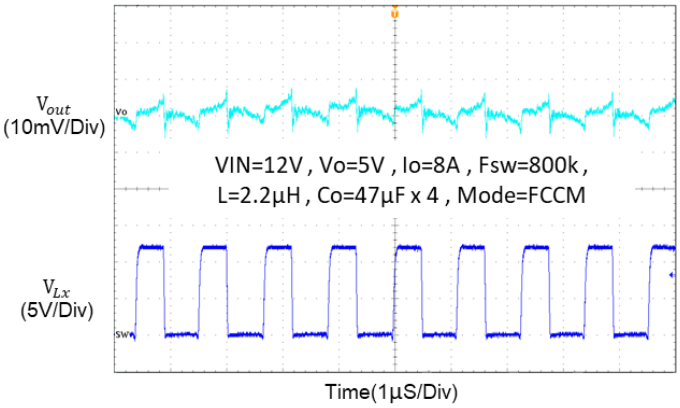
Output Ripple Voltage



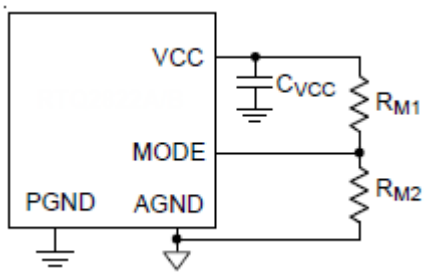
Output Ripple Voltage



Output Ripple Voltage



MODE SETTING

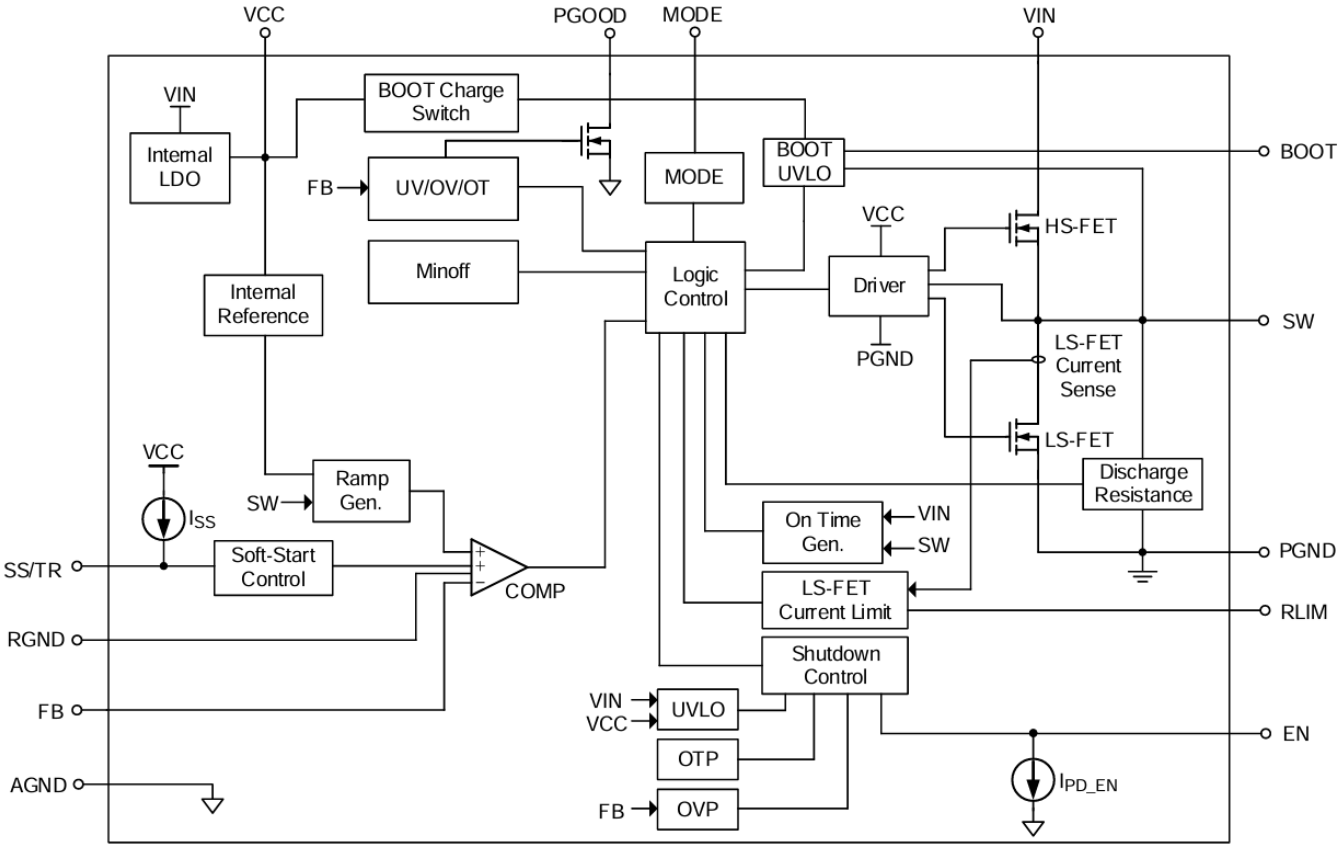


MODE Connection

Table 6. MODE Setting

Mode Pin Connections		Light Load Mode	Switching Frequency (kHz)
RM1 (kohm)	RM2 (kohm)		
0	No connection	PSM	600
No connection	243	PSM	800
No connection	121	PSM	1000
No connection	0	FCCM	600
No connection	30.1	FCCM	800
No connection	60.4	FCCM	1000

FUNCTIONAL DESCRIPTION



XPC2444 Block diagram

Operation

The XPC2444 is a high-efficiency synchronous step-down converter utilizing the proprietary Constant On-Time control architecture. The ultra-fast COT control enables the use of small capacitance to save the PCB space.

During normal operation, the internal high-side power switch (HSFET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET turns off, the low-side power switch (LSFET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has a similar shape to the inductor current. Via the feedback resistor network, this voltage ripple is compared with the internal reference. When the minimum off-time one-shot (210ns, max.) has timed out and the inductor current is below the current limit threshold, the one-shot is triggered again if the feedback voltage falls below the internal VREF (0.6V, typ.).

The XPC2444 supports stable operation with all low-ESR output capacitors (such as ceramic capacitors and low ESR polymer capacitors). The COT control architecture also features excellent transient response, further improving the output variation during high-frequency load transients, especially when a load suddenly increases. The conventional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. However, even with defined input and output voltages, a fixed ON-time means that the frequency has to increase at higher load levels to compensate for the power losses in the MOSFETs and the inductor. The XPC2444 COT control further adds a frequency locked loop system, which slowly adjusts the ON-time to compensate for the power losses without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the XPC2444 are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator that generates 3V at VCC. The voltage on VCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains the C_{BOOT} voltage is sufficient to turn-on the HSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is above the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VCC rail that can draw a current higher than the internal LDO's current limit from the VCC, then the VCC drops below the UVLO falling threshold and thereby shutting down the output of the XPC2444.

Enable, Start-Up, Shutdown and UVLO

The XPC2444 implements Under-Voltage Lock Out protection (UVLO) to prevent operation without fully turning on the internal power MOSFETs. The UVLO monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device stops switching. UVLO is a non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching and when the EN pin voltage falls below the turn-off threshold (V_{ENL}) it stops switching. When floated, the EN pin of the XPC2444 is internally pulled down to the ground.

When appropriate voltages are present on the VIN, VCC, and EN pins, the XPC2444 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1ms (typ.) will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, the capacitors can be placed between the SS/TR pin and both the AGND and RGND pins.

Use a 22nF capacitor for C_{SS2}, and a larger value ranging from 22nF to 220nF for C_{SS1}. If this external ramp rate is slower than the internal 1ms soft-start, the output voltage will be limited by the ramp rate on the SS/TR pin instead. The typical external soft-start time from 0% to 91.5% of VREF can be calculated by the equation below.

$$C_{SS1}(nF) + C_{SS2}(nF) = \frac{t_{SS}(ms) \times 42(\mu A)}{0.55V}$$

where C_{SS2} is required to be a minimum of 22nF while C_{SS1} is recommended 22nF to 220nF.

When the V_{EN} is lower than V_{EN_F}, the voltage of the SS/TR pin discharges to RGND.

Figure 1 below shows the typical power-up sequence of the device. When the voltage on the VIN and EN pins crosses the input undervoltage lockout rising threshold and EN input rising threshold. After the voltage on the VCC pin reaches the VCC undervoltage lockout rising threshold, the device will start switching if the voltage difference between the SS/TR pin and FB pin is equal to 100mV (i.e. VSS/TR − VFB = 100mV, typ.) after setting detection is completed. The SS/TR pin should NOT be left unconnected for soft-start control. After the VFB voltage rises above the V_{TH_PGLH1} (91.5% of the VREF, typ.), the PGOOD pin will enter a high impedance state after delay time tPGDLY (0.8ms, typ.).

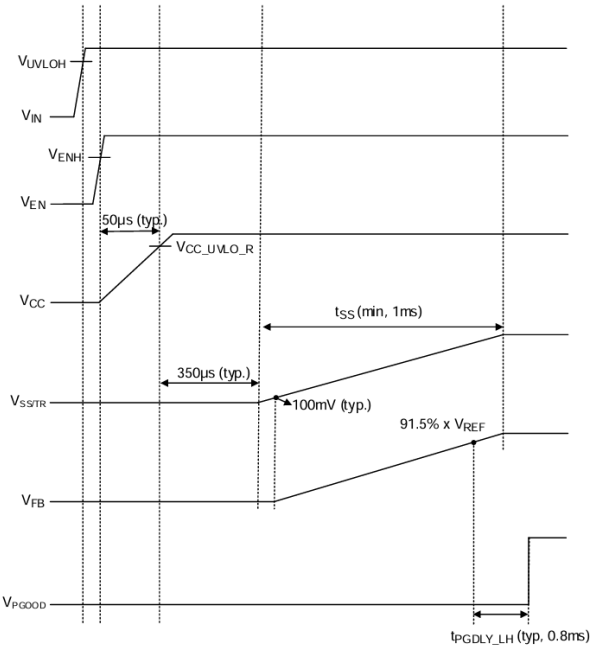


Figure 1. Power-on Sequence

Voltage Tracking and External Reference

The XPC2444 can replace the internal voltage reference (VREF) or track an external power rail by adding an external voltage signal to the SS/TR pin. The VFB will track this signal, which ranges from 0.3 V to 1.4 V. During startup, it is essential to ensure that the SS/TR pin voltage reaches 600mV or higher for proper operation. The Power-Good Output function is activated if VREF or an external voltage signal exceeds 550mV, and it is disabled if the external voltage signal at the SS/TR pin is lower than 500mV.

Pre-Biased

If there is a residual voltage on output voltage before startup, both of internal HSFET and LSFET are prohibited switching until the soft start ramp is higher than feedback voltage. When the soft start ramps cross above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated target.

Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero-current-detect circuitry which utilizing the LSFET $R_{DS(ON)}$ to sense the inductor current. The LSFET is turned off when the inductor current drops to zero, resulting in discontinuous operation (PSM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the feedback voltage falls below the feedback reference voltage. PSM operation maintains high efficiency at light load, while setting MODE to Forced PWM (FCCM) operation helps meet tight voltage regulation accuracy requirements.

BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high side MOSFET at any conditions. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. With such conditions when the BOOT to SW voltage falls below VBOOT_UVLO_F (2.3V, typ.), the device turns on the BOOT recharge path (200ns, typ.) to charge the BOOT capacitor.

Power-Good Output

The PGOOD pin is an open-drain power-good indicator which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal VFB. During soft-start, VPGOOD is actively held low and only allowed to become high after soft start is finished. If VFB rises above the VTH_PGLH1 (91.5% of the VREF, typ.), the PGOOD pin will be in high impedance and VPGOOD will be held high after a certain delay elapsed. When VFB falls below the PGOOD low threshold VTH_PGHL2 (80% of the VREF, typ.) or exceeds VTH_PGHL1 (116% of the VREF, typ.), the PGOOD pin will be pulled low. For VFB higher than VTH_PGHL1, VPGOOD can be pulled high again if VFB drops back to the PGOOD high threshold VTH_PGLH2 (106% of the VREF, typ.). Once being started-up, if any internal protection is triggered, PGOOD pin will be pulled low to GND. The internal open-drain pull-down device will pull the VPGOOD low. This is to prevent false flag operation for short excursions in output voltage, such as during line and load transients. The power-good indication profile is shown in figure2.

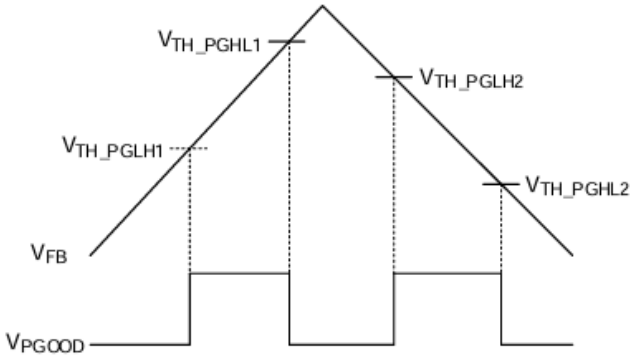


Figure 2. The Logic of PGOOD

Over-current Limit (OCP)

The XPC2444 features cycle-by-cycle current-limit protection on low-side MOSFETs and the protection prevents the device from catastrophic damage due to in output short circuit, overcurrent, or inductor saturation.

The low-side MOSFET valley current-limit protection is achieved by measuring the inductor current through the low-side MOSFET and mirroring the R_{LIM} pin with the ratio of G_{CS} using a resistor during the low-side on-

time. Once the inductor current through the low-side MOSFET is above the low-side MOSFET valley current-limit threshold (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the I_{LIM_L}; that is, another on-time can only be triggered when the inductor current goes below the I_{LIM_L}.
The output current-limit threshold can be calculated as below:

$$RLIM(\Omega) = \frac{VLIM}{GCS \times \left\{ILIM - \frac{(VIN - VOUT) \times VOUT}{VIN} \times \frac{1}{2 \times L \times fSW}\right\}}$$

Where V_{LIM} =1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (A).

Output Undervoltage Protection

The XPC2444 includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage VFB. If VFB drops below the undervoltage protection threshold VUVP (80% of the VREF, typ.), the UV comparator will go high to turn off both the internal high-side and low-side MOSFETs. The XPC2444 will enter output undervoltage protection with hiccup mode. During hiccup mode, the device will shut down for tHICCUP_OFF (8.5ms, typ.), and then attempt to recover automatically for tHICCUP_ON (2.4ms, typ.).

If the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resumes normal operation as soon as the overload or short circuit condition is removed.

Negative Current Limit

The XPC2444 also monitors inductor current during the "ON" state of the low-side MOSFET to prevent too large negative current flowing through the low-side MOSFET. Once the negative current exceeds the low-side switch negative current-limit threshold ILIM_NEG (−9A, typ.) , the device turns off the low-side MOSFET and turns on the high-side MOSFET for the on-time determined by VIN, VOUT and fSW. After the high-side MOSFET on-time expires, the low-side MOSFET turns on again. This behavior can keep the valley of negative current at ILIM_NEG to protect low-side MOSFET. Designers should choose appropriate inductance to avoid triggering ILIM_NEG during normal operation.

Output Overvoltage Protection

The XPC2444 includes an output overvoltage protection (OVP) circuit to limit output voltage and minimize output voltage overshoot. If the VFB goes above 116% of the VREF, the high-side MOSFET will be latched off and the PGOOD pin remains low until the VCC or EN is recycled. In the meantime, if the overvoltage condition still exists, the low-side MOSFET remains on to discharge output voltage until the low-side switch valley current reaches the negative current limit (ILIM_NEG). Once reaching the ILIM_NEG the low-side MOSFET is turned off temporarily around 700ns before it is turned on again.
The XPC2444 repeats in this cycle until the output voltage is brought down when the VFB goes below 50% of the VREF, the low-side MOSFET continues to turn on. The device needs EN or VIN to recycle to clear the OVP fault.

Output Quick Discharge

The XPC2444 features Output Quick Discharge (OQD) to mitigate overshoot before triggering the output overvoltage protection (OVP). When the VFB voltage exceeds 104% of the VREF but remains below the OVP threshold (116%, typ.), OQD is activated. During OQD, the high-side MOSFET is off, while the low-side MOSFET remains on until it reaches −9A (typ.) or the VFB voltage falls below 102%. Once the ILIM_NEG is reached, the low-side MOSFET is briefly turned off for 700ns before being turned on again. This sequence is repeated until the VFB voltage falls below 102% of the VREF. After completing 15 consecutive FCCM cycles, the XPC2444 exits the OQD. This OQD effectively reduces overshoot and ensures stable operation.

Output Voltage Discharge

When the XPC2444 is disabled by EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (80Ω, typ.) connected to ground. This function prevents the reverse current from flowing the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

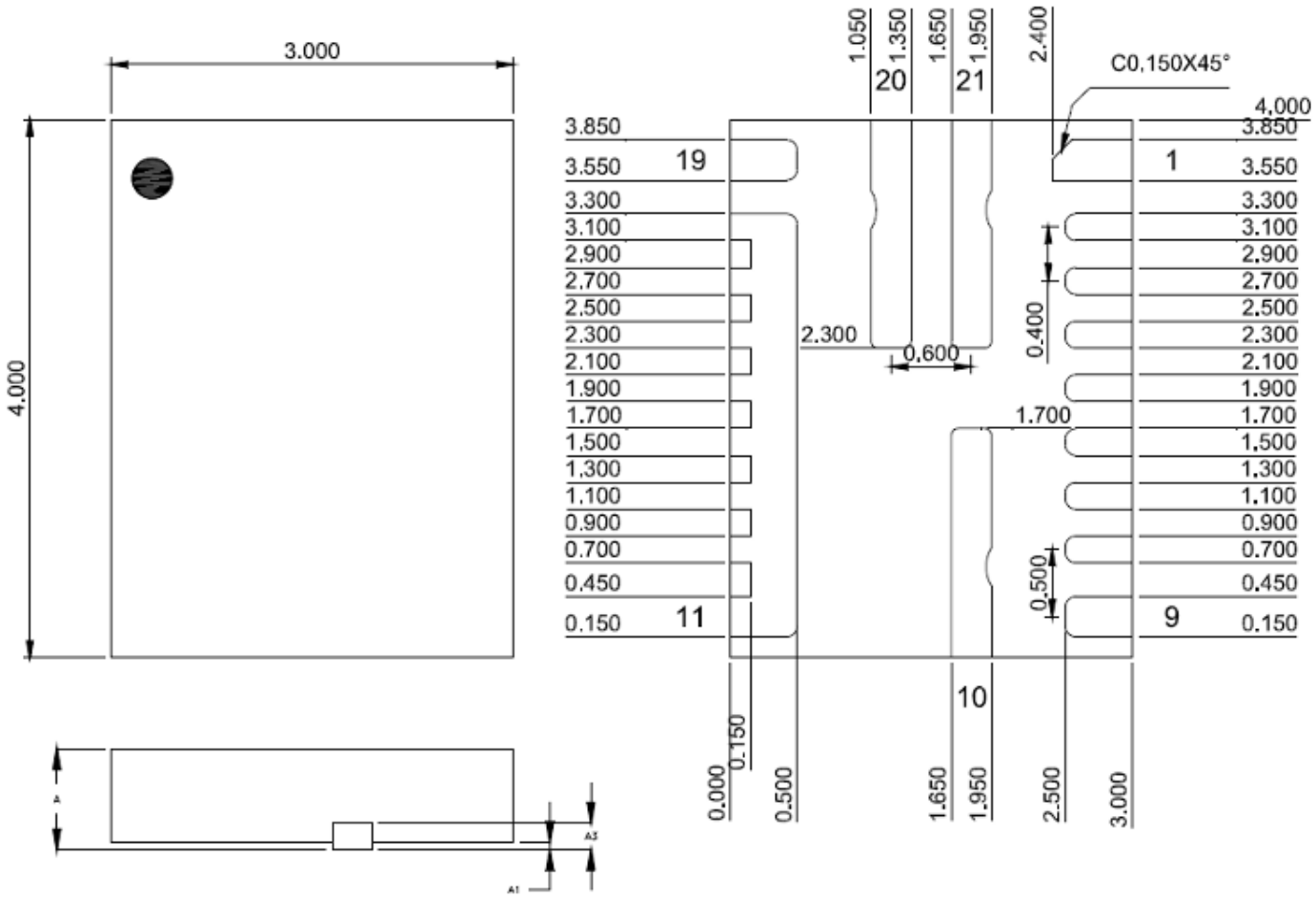
Over-Temperature Protection (OTP)

The XPC2444 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds the over temperature protection threshold (160°C, typ.). Once the junction temperature cools down by the over temperature protection hysteresis (30°C, typ.), the XPC2444 will resume normal operation with a complete soft-start. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Layout Guidelines

- A four-layer or six-layer PCB with maximum ground plane is recommended for good thermal performance.
- The traces of the main current paths should be kept wide and short.
- Recommend having equal input caps on each side of the IC. Place them as close to VIN pins as possible.
- Place the VCC decoupling capacitor in close proximity to VCC pin.
- Place the bootstrap cap, CBOOT, as close to IC as possible.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the XPC2444 to additional ground planes within the circuit board and on the bottom side.
- Keep analog components away from the SW and BOOT nodes to prevent noise pickup.
- Connect the feedback sense network behind via of output capacitor.

PHYSICAL DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

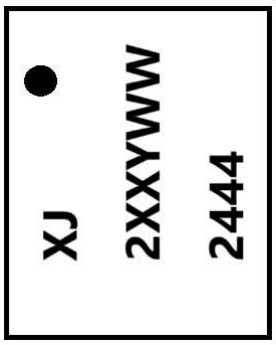
Tolerance
±0.050

MARKING AND REEL INFORMATION

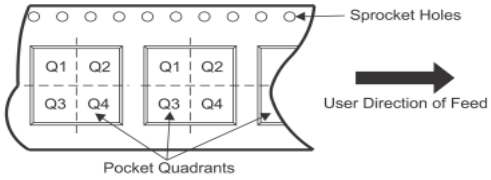
Package Marking & PQ information

XPC2444Q21R Marking

Format:



Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: Assembly location code: 2

b) 2nd & 3rd digit: Assembly lot number

XX means serial number for traceability, either of the 2 characters can be replaced by “0-9, A-Z, a-z”

c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

2. Line2: Product Name Code:

Product Name	P/N Code	Remark
XPC2444Q21R	2444	

3. Packing: 3K/reel