18×12 MATRIX LED DRIVER WITH AUTO BREATH

FEATURES

- 18 current sinks, 12 current switches, up to drive 216 LEDs or 72 RGBs.
- Programmable matrix size
- Individual 256-level PWM for dimming
- High-precision current sinks
  - Device-to-device error: ±7%
  - Channel-to-channel error: ±7%
- EMI and audible noise reduction
  - Spread spectrum function
  - Programmable slew rate control
- Programmable H/L logic
  - 1.4V/0.4V
  - 2.4V/0.6V
- Multiple-device clock synchronization by SYNC pin
- De-Ghost
- 10MHz 3.3V SPI interface
- 1MHz I²C interface, 16 selectable addresses
- Power supply: 2.7V~5.5V
- EQFP 7X7-48L package

APPLICATIONS

Smart speaker, Bluetooth speaker

Gaming device (Keyboard, Mouse etc.)

Mobile phone, PAD

GENERAL DESCRIPTION

AW20216SQPY is an 18x12 matrix LED driver programmed via SPI or I²C compatible interface. Each channel has individual 8-bit PWM current setting for brightness control.

The maximum global current of each channel is recommended to be 40mA configured via external resistor R_{EXT}.

Spread spectrum and slew rate control technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW20216SQPY can be turned off with minimum current consumption by either pulling the EN pin low or using the software reset.

AW20216SQPY is available in EQFP 7X7-48L package. It operates from 2.7V to 5.5V over the temperature range of -40°C to 105°C.

TYPICAL APPLICATION CIRCUIT

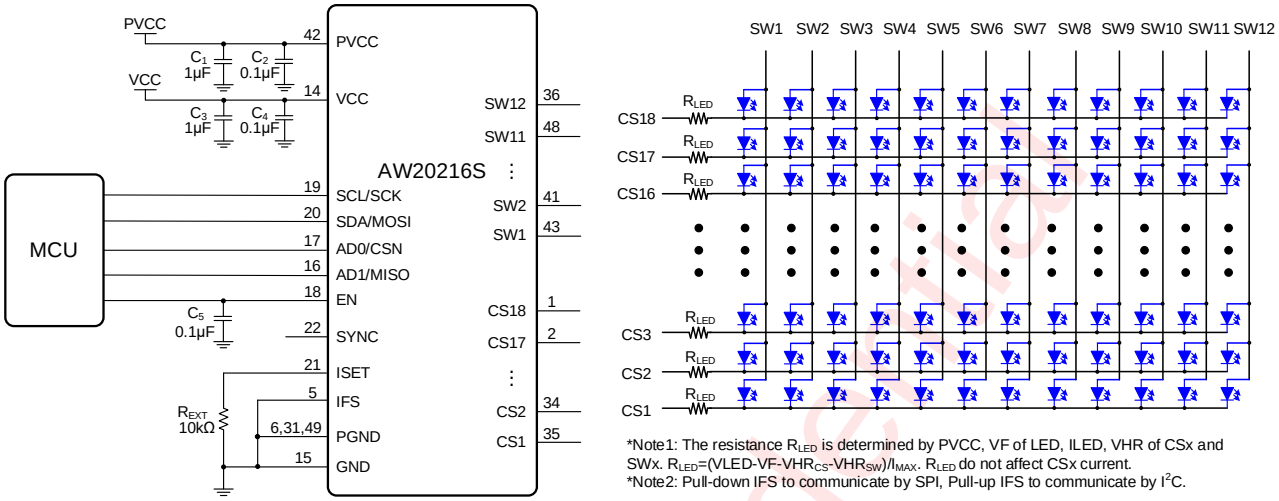
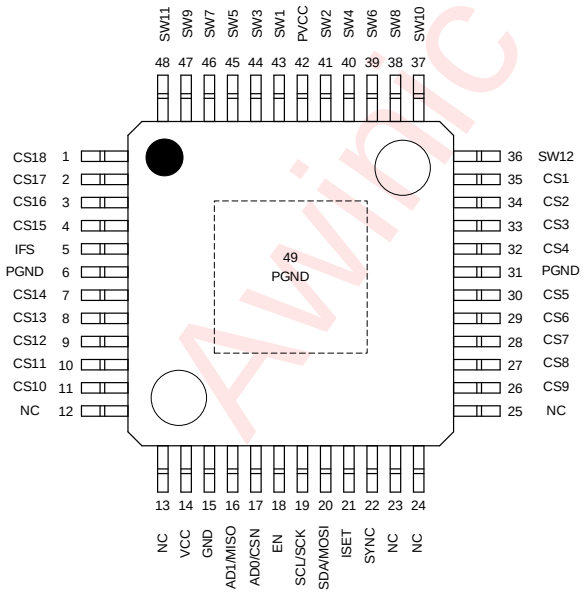


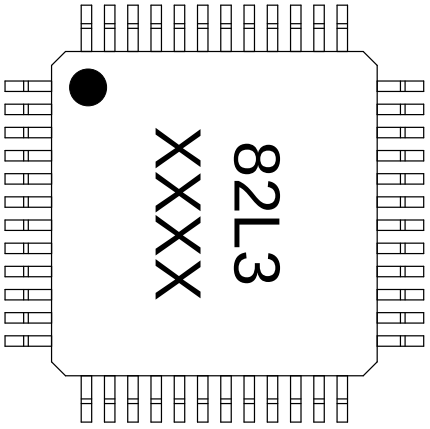
Figure 1 AW20216SQPY Application Circuit

PIN CONFIGURATION AND TOP MARK

AW20216SQPY
(Top View)



AW20216SQPY Marking
(Top View)



82L3 – AW20216SQPY
XXXX – Production Tracing Code

Figure 2 Pin Configuration and Top Marking

PIN DEFINITION

No.	NAME	DESCRIPTION
1~4	CS18~CS15	Current sink
5	IFS	Communication interface select pin. I²C is selected when IFS is high. SPI is selected when IFS is low. No floating.
6	PGND	Power ground
7~11	CS14~CS10	Current sink
12~13	NC	No connect
14	VCC	Power supply, 2.7V~5.5V
15	GND	Ground
16	AD1/MISO	I²C address select pin1 or SPI master input slave output.
17	AD0/CSN	I²C address select pin0 or SPI slave select.
18	EN	Standby the chip when EN is low, internally pulled down to GND with a resistor of 1MΩ
19	SCL/SCK	I²C clock input or SPI clock input. Pull up to VIO when configured as I²C.
20	SDA/MOSI	I²C data IO or SPI master output slave input. Pull up to VIO when configured as I²C.
21	ISET	When R_{EXT}=10kΩ, global current of LED is 40mA
22	SYNC	Synchronize pin, used to synchronize clock in multiple devices application, internally pulled down to GND with a resistor of 1MΩ
23~25	NC	No connect
26~30	CS9~CS5	Current sink
31	PGND	Power ground
32~35	CS4~CS1	Current sink
36~41	SW12, SW10, SW8, SW6, SW4, SW2	Current switches
42	PVCC	Current source power supply, 2.7V~5.5V
43~48	SW1,SW3, SW5,SW7, SW9,SW11	Current switches
49	PGND	Thermal Pad

FUNCTIONAL BLOCK DIAGRAM

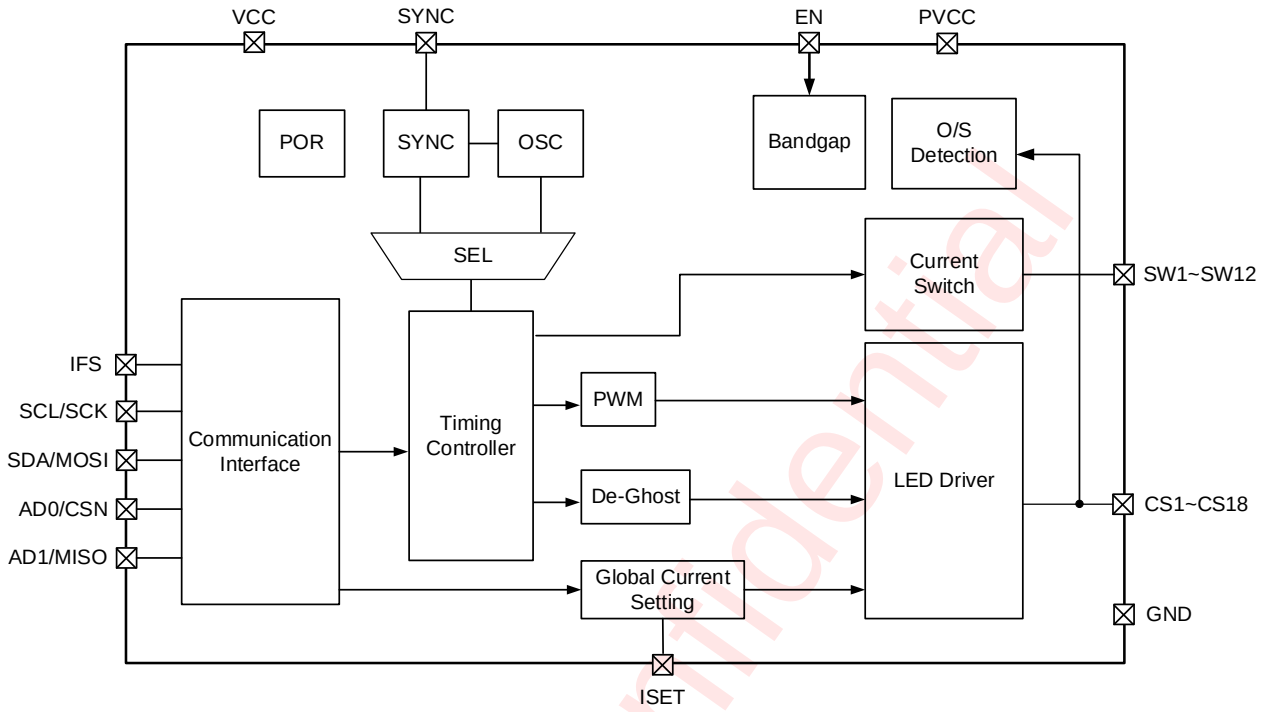
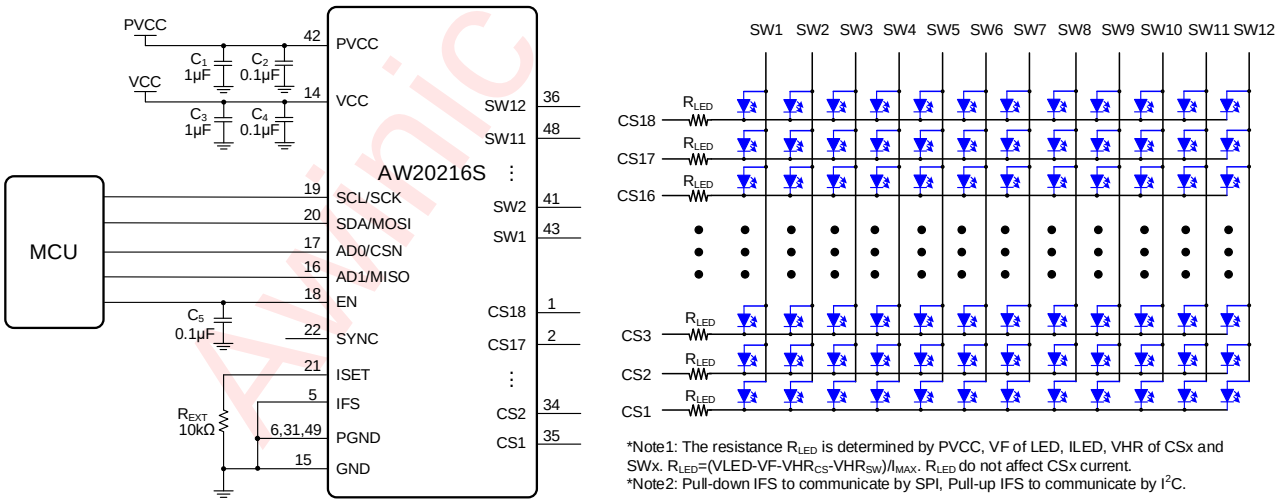


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUIT



*Note1: The resistance R_{LED} is determined by PVCC, VF of LED, ILED, VHR of CSx and SWx. R_{LED}=(VLED-VF-VHR_{CS}-VHR_{SW})/I_{MAX}. R_{LED} do not affect CSx current.
*Note2: Pull-down IFS to communicate by SPI, Pull-up IFS to communicate by I^2C.

Figure 4 Typical Application Circuit

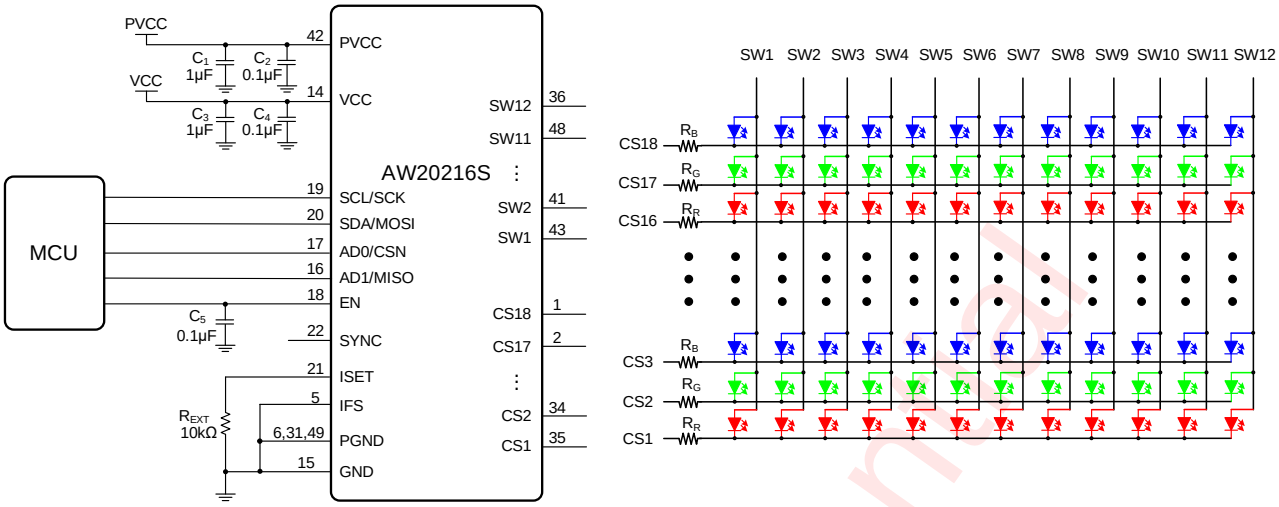
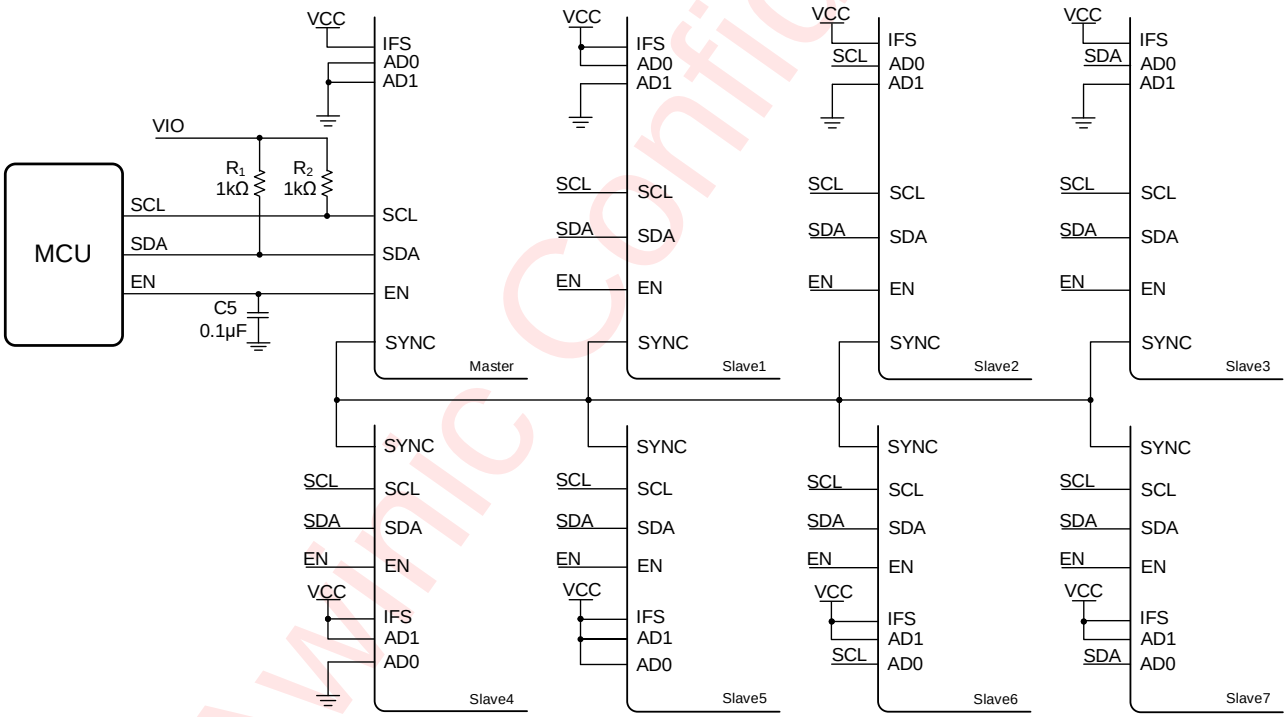


Figure 5 Typical Application Circuit (RGB)

Note3: The resistance R_R / R_G /R_B is determined by PVCC, $VF_{(R/G/B)}$ of LED, ILED, VHR of CSx and SWx. R_R / R_G /R_B=(PVCC- $VF_{(R/G/B)}$-VHR_{CS}-VHR_{SW})/I_{MAX}.



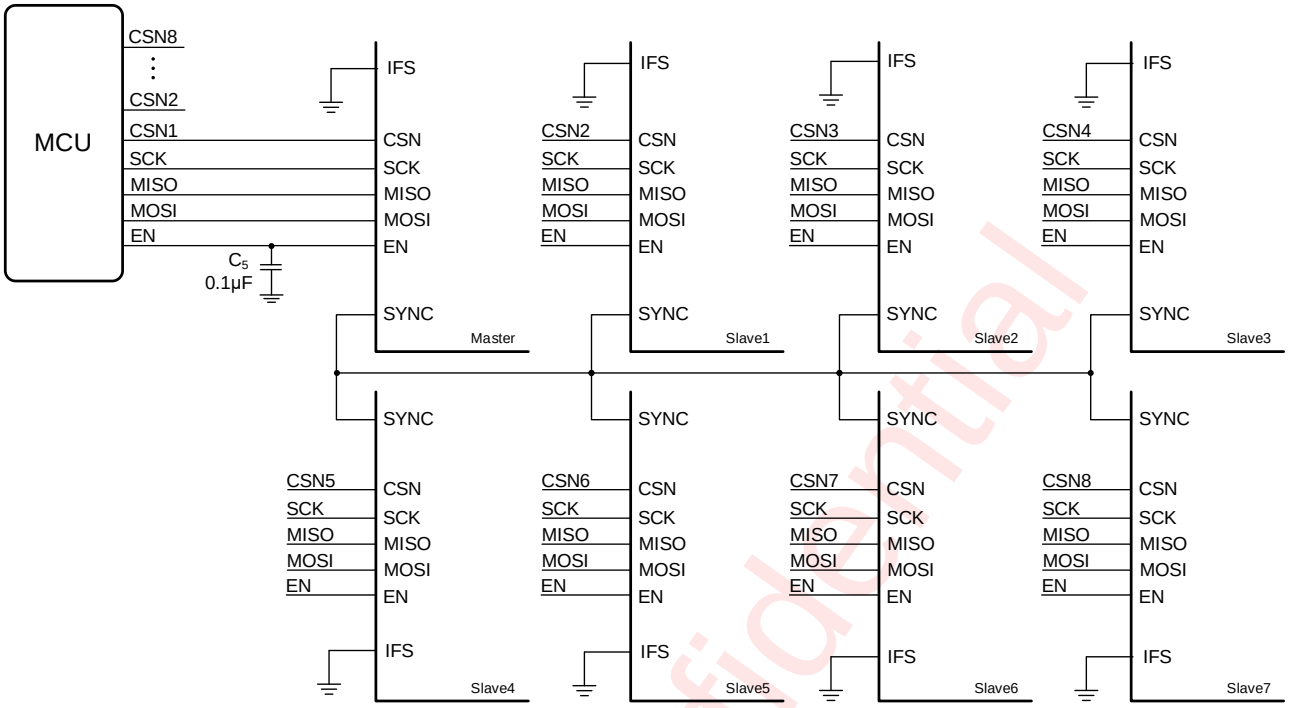


Figure 6 Typical Application Circuit (Eight Parts Synchronization)

Note4: One part is set as master mode, and all the other 7 parts set as slave mode (set master after set all slaves). Master mode or slave mode set by register SSCR (page0, address=0x28). Master part output master clock, and all slaves input the master clock.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW20216SQPY	-40°C~105°C	EQFP 7X7-48L	82L3	MSL3	ROHS+HF	2500 units/ Tray

ABSOLUTE MAXIMUM RATINGS (NOTE4)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Supply voltage range PVCC		-0.3V to 6V
Input voltage range	SCL/SCK, SDA/MOSI, EN, AD0/CSN, AD1/MISO	-0.3V to VCC
Output voltage range	SW1~SW12, CS1~CS18	-0.3V to PVCC
Voltage on ISET	ISET	-0.3V to 2V
Junction-to-ambient thermal resistance θ_{JA}		32.7°C/W
Operating free-air temperature range		-40°C to 105°C
Maximum operating junction temperature T_{JMAX}		160°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (NOTE2)		
HBM		±4kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F.02		±IT: 200mA

NOTE5: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024 (HBM). ESDA/JEDEC JS -002-2025 (CDM)

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Input voltage	2.7	3.6	5.5	V
PVCC	Input voltage	2.7	5	5.5	V
C_1, C_3	Input capacitance	1	1	22	μF
C_2, C_4, C_5	Input capacitance	0.1	0.1	1	μF
R_{EXT}	External resistor for setting sink current	10	10	20	kΩ
T_A	Operating free-air temperature range	-40	25	105	°C

ELECTRICAL CHARACTERISTICS

T_A=25°C, PVCC=VCC=3.6V (unless otherwise noted), R_{EXT}=20kΩ

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
VCC	Input operating range		2.7		5.5	V
I_{STB_VCC}	Standby current	V_{EN} =0V or CHIPEN = 0		1.3	5	μA
I_{ACT_VCC}	Quiescent current in active mode	V_{EN}=VCC, CHIPEN=1, all LEDs off		1.8		mA
I_{MAX}	Maximum sink current (CS1~CS18)	V_{LED}=0.5V	18.6	20	21.4	mA
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}=360mA		300		mV
	Current sink headroom voltage CSx	I_{SINK}=20mA		360		mV
I_{MATCH}	Device to device current error	All Channel's current set to 20mA	-7		7	%
$\triangle I_{LED}$	Channel to channel current error	All Channel's current set to 20mA	-7		7	%
F_{OSC}	OSC clock frequency		14.88	16	17.12	MHz
LOGIC (IFS)						
V_{IL}*NOTE	Input logic low	VCC=2.7V~5.5V			0.3	V
V_{IH}*NOTE	Input logic high	VCC=2.7V~5.5V	1.3			V
LOGIC (IFS=0) (SCL/SCK, SDA/MOSI, EN, AD0/CSN, AD1/MISO)						
V_{IL}*NOTE	Input logic low	VCC=2.7V~5.5V			0.6	V
V_{IH}*NOTE	Input logic high	VCC=2.7V~5.5V	2.4			V
LOGIC (IFS=1) (SCL/SCK, SDA/MOSI, EN, AD0/CSN, AD1/MISO)						
V_{IL}*NOTE	Input logic low	VCC=2.7V~5.5V, LGC=0			0.4	V
V_{IH}*NOTE	Input logic high	VCC=2.7V~5.5V, LGC=0	1.4			V
V_{IL}*NOTE	Input logic low	VCC=2.7V~5.5V, LGC=1			0.6	V
V_{IH}*NOTE	Input logic high	VCC=2.7V~5.5V, LGC=1	2.4			V
Timing						
T_{SCAN}	Period of scanning	PCCR.PWMFRQ[2:0] = 000, GCR.SWSEL[3:0] = 1011		216		μs
T_{DG}	Non-overlap time between SW			1		μs
T_{HOLD}	Delay time between the falling edge of CS18 and SWx			125		ns

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SETUP}	Delay time between the rising edge of SWx and CS1	PCCR.PWMFRQ[2:0] = 000		250		ns
T_{DLY}	Delay time of each CS group, there are 6 groups of CS	PCCR.PWMFRQ[2:0] = 000		125		ns

*NOTE: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

I²C INTERFACE TIMING

PARAMETER		FAST MODE			FAST MODE PLUS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
F_{SCL}	Interface clock frequency	-		400	-		1000	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	0.26		-	μs
T_{LOW}	Low level width of SCL	1.3		-	0.5		-	μs
T_{HIGH}	High level width of SCL	0.6		-	0.26		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	0.26		-	μs
$T_{HD:DAT}$	Data hold time	0		-	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	0.05		-	μs
T_R	Rising time of SDA and SCL	-		0.3	-		0.12	μs
T_F	Falling time of SDA and SCL	-		0.3	-		0.12	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	0.26		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	0.5		-	μs

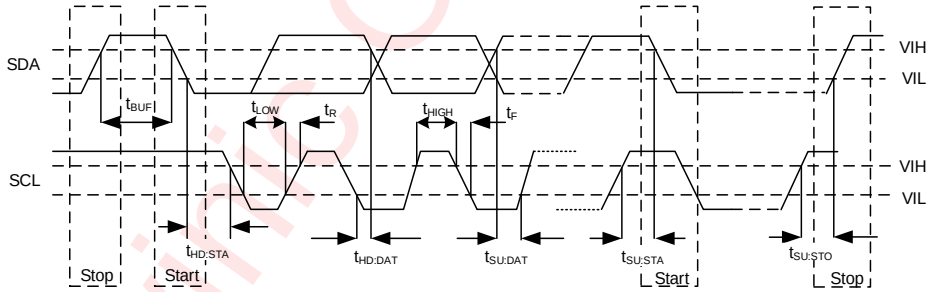


Figure 7 I²C Interface Timing

SPI INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency			10	MHz
T_{CSAS}	CS active setup time	30			ns
T_{CSAH}	CS active hold time	15			ns
T_{CSNS}	CS not active setup time	15			ns
T_{CSNH}	CS not active hold time	15			ns
T_{CH}	SCK high time	20			ns
T_{CL}	SCK low time	35			ns
T_{DS}	Data in setup time	10			ns
T_{DH}	Data in hold time	15			ns
T_{DO}	SCK falling edge to MISO data update time		12	42	ns

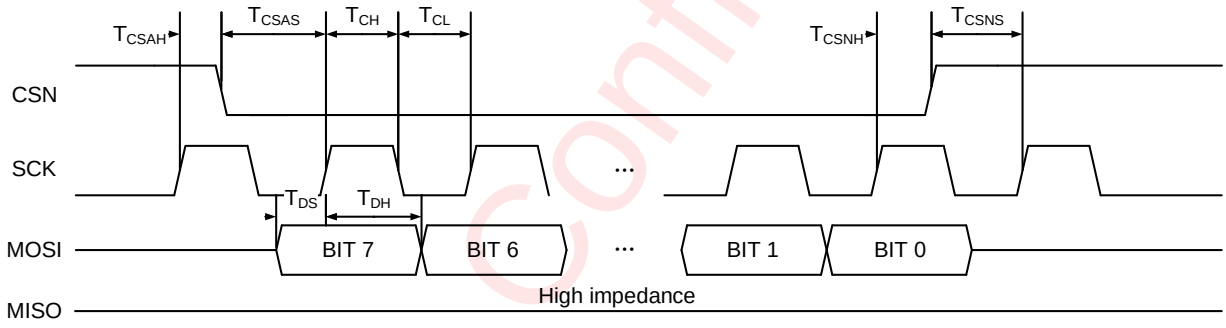


Figure 8 SPI Interface Input Timing

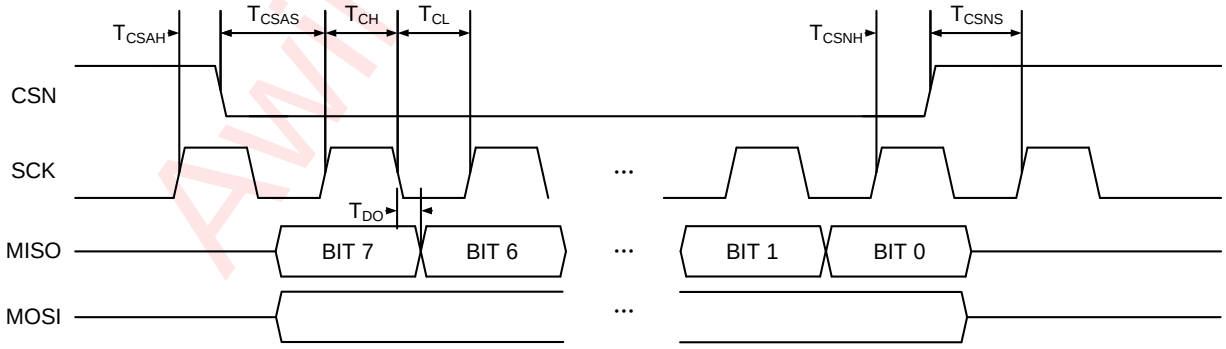


Figure 9 SPI Interface Output Timing

DETAILED FUNCTIONAL DESCRIPTION

OPERATION MODE AND RESET

POWER ON RESET (POR)

During initial power-up, AW20216SQPY is reset, and all registers are reset to default value, and LED driver is shut down.

Once the supply voltage VCC drops below the threshold voltage V_{POR_VCC} (2.0V), the power-on-reset will be activated to reset the device again. By reading the bit PUST of the register UVCR (page0, address=0x2A), it can be determined whether the device has been reset.

Below is the recommended operation timing:

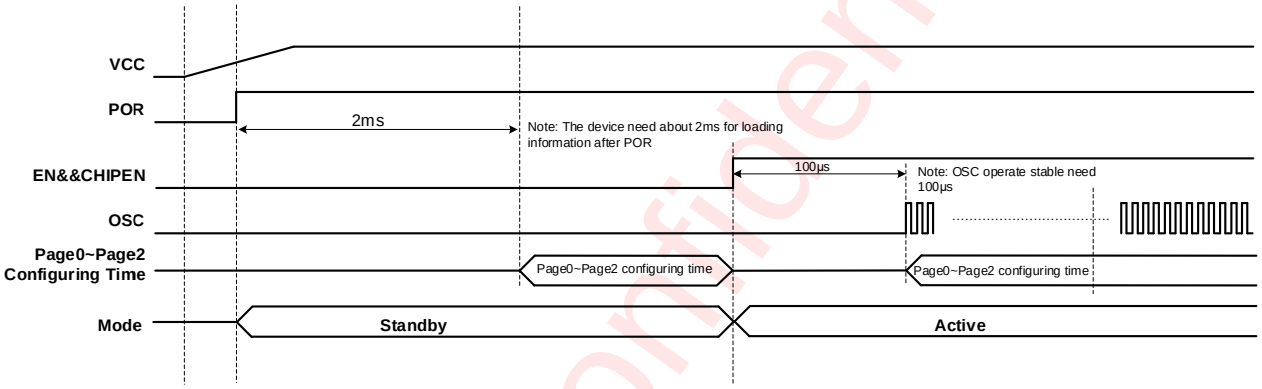


Figure 10 Power up Timing

SOFTWARE RESET

By writing 0xAE to register RSTN (page0, address=0x2F), the software reset is triggered. After software reset, all registers will be reset to the default value and enter into standby mode.

After the software reset command is input through SPI or I²C or power on reset, it needs to wait at least 2ms before any other SPI command can be accepted.

STANDBY MODE

When EN is pulled low or the bit CHIPEN of the register GCR (page0, address=0x00) is set to “0” or UVLO is triggered (UVFLG=1) in active mode, AW20216SQPY enters into standby mode automatically. In standby mode, all analog blocks are power down but the registers retain the data and keep it available via SPI or I²C.

When POR is triggered, the device enters into standby mode and all registers will be reset (more information is showed in POWER ON RESET).

ACTIVE MODE

When EN is in high level, and the bit CHIPEN of the register GCR (page0, address=0x00) is set to “1”, AW20216SQPY enters into the active mode.

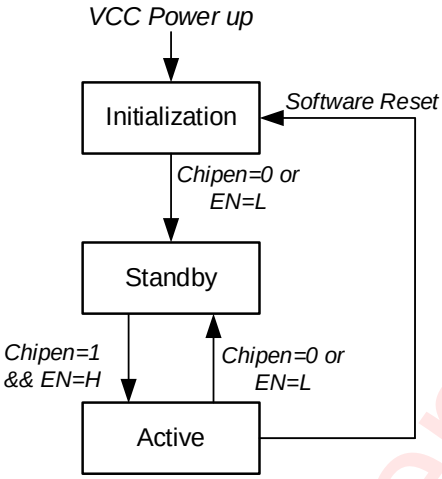


Figure 11 AW20216SQPY Operating Mode Transition

I²C INTERFACE

AW20216SQPY supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz. The pull-up resistor for the SDA and SCL can be selected from 1k to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1MHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C device supports continuous read and write operations.

DEVICE ADDRESS

The I²C device address is 7-bit (A7~A1), followed by the R/W bit A0 (Read=1/Write=0). Set A0 to "0" for writing and "1" for reading. The values of bits A4:A3 and bits A2:A1 are depended on the connection of pin AD0 and AD1. Separately, there are 4 options: VCC, GND, SCL and SDA. The A7 to A5 is "010" constantly. The device also supports using a broadcast slave address of 0x5A to access registers. All slave addresses as followed.

AD0	AD1	A7:A5	A4:A3	A2:A1	A0	Device Address	Broadcast Address
GND	GND	010	00	00	0/1	0x20	0x5A
GND	VCC		00	01		0x21	
GND	SCL		00	10		0x22	
GND	SDA		00	11		0x23	
VCC	GND		01	00		0x24	
VCC	VCC		01	01		0x25	
VCC	SCL		01	10		0x26	
VCC	SDA		01	11		0x27	
SCL	GND		10	00		0x28	
SCL	VCC	010	10	01	0/1	0x29	0x5A
SCL	SCL		10	10		0x2A	
SCL	SDA		10	11		0x2B	

AD0	AD1	A7:A5	A4:A3	A2:A1	A0	Device Address	Broadcast Address
SDA	GND		11	00		0x2C	
SDA	VCC		11	01		0x2D	
SDA	SCL		11	10		0x2E	
SDA	SDA		11	11		0x2F	

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

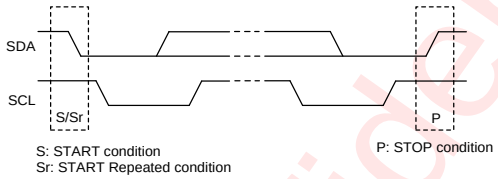


Figure 12 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

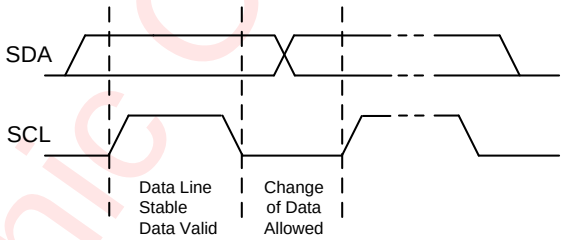


Figure 13 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

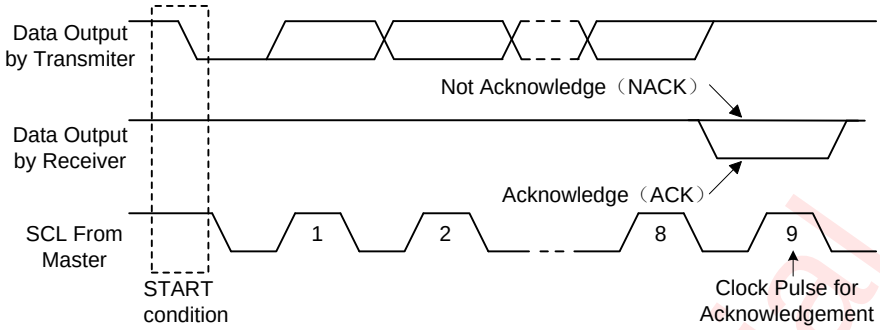


Figure 14 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master sends data byte to be written to the addressed register.
g) Slave sends acknowledge signal.
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g).
i) Master generates STOP condition to indicate write cycle end.

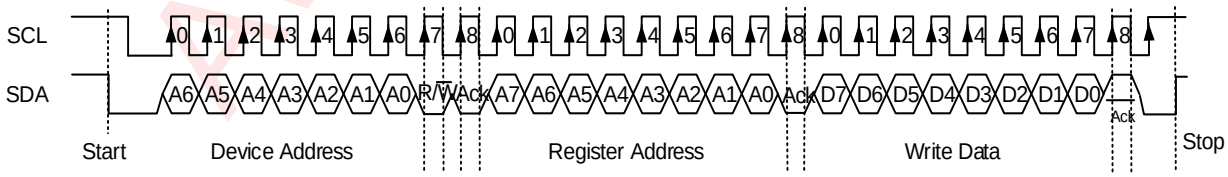


Figure 15 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit).
e) Slave sends acknowledge signal.
f) Master generates STOP condition followed with START condition or REPEAT START condition.
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle is ended.

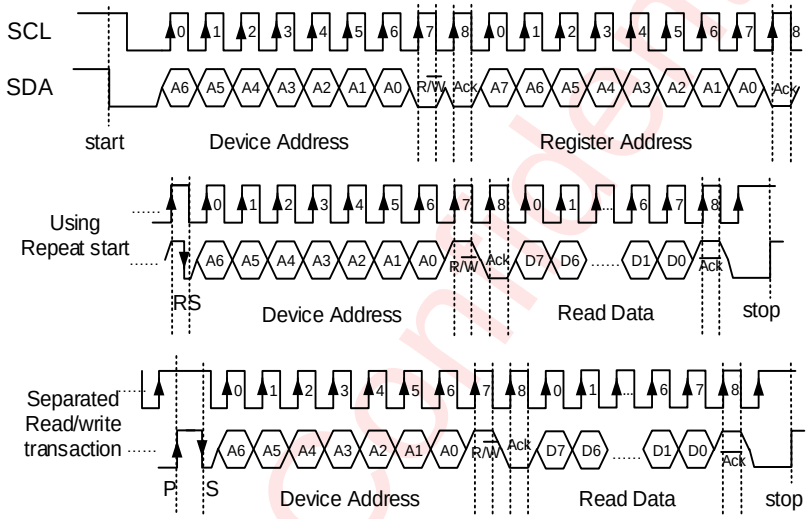


Figure 16 I²C Read Byte Cycle

SPI INTERFACE

AW20216SQPY supports the SPI serial bus and data transmission protocol in fast mode from 1MHz to 10MHz. This device operates as a slave on the SPI bus. SPI master controls write or read register of the device.

The SPI data format is 8-bit long. The first command byte is composed by 4-bit chip ID, 3-bit page ID and W/R bit, the command byte must be sent first, then is followed by register address and then the register data. In AW20216SQPY, the 4-bit chip ID is always 4'b1010, the 3-bit page ID can be set from 0 to 4. If W/R is 0, which will be write operation and master can write data into the register, If W/R is 1, which will be read operation and master can read data from the register.

BITS	D7:D4	D3:D1	D0
Value	1010	000: Page 0 001: Page 1 010: Page 2	0: Write 1: Read

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, data is sent from the master device to the slave device in MOSI, MISO will be unchanged.

Typical write:

(1) First of all, master sets CSN to low, to enable operation to the device.

(2) Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and write command.

(3) Then master sends the register address.

(4) Then master sends the data to write into register address sent before.

(5) Finally master pulls CSN high to finish the operation.

Automatic address increment write:

(1) – (3) Same as above.

(4) During the 8th rising edge of receiving the first data byte, the internal address pointer will increment by one. The next data byte sent to AW20216SQPY will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be written to AW20216SQPY.

(5) Finally master pulls CSN high to finish the operation.

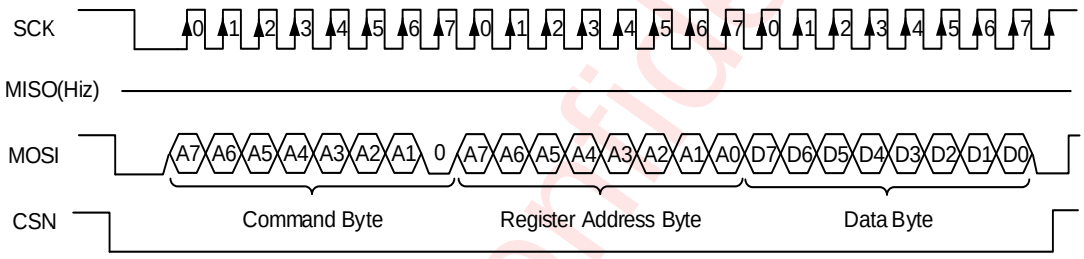


Figure 17 SPI Writing to AW20216SQPY (Typical)

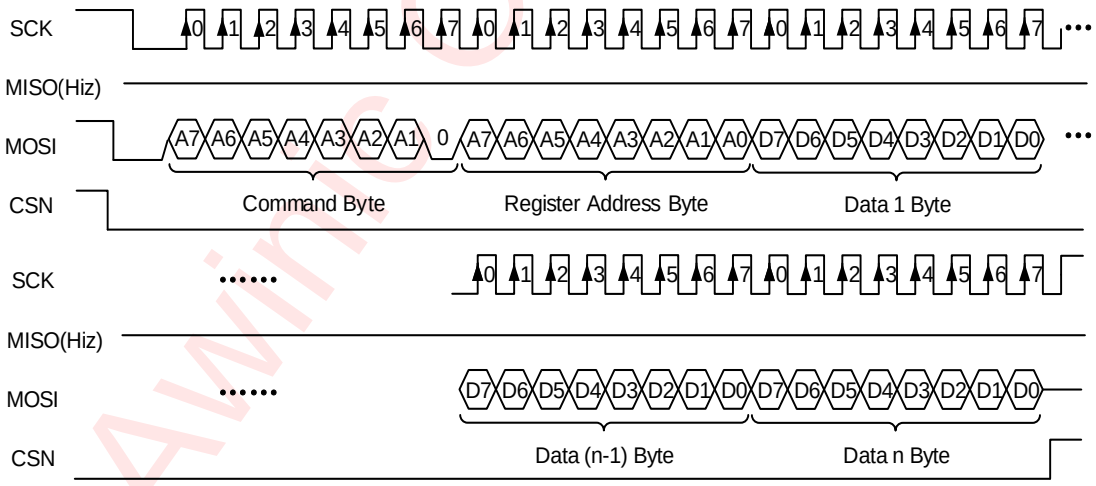


Figure 18 SPI Writing to AW20216SQPY (Automatic Address Increment)

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the read command data and register address will send in MOSI and read data will send back to master in MISO.

Typical read:

(1) First of all, master sets CSN to low, to enable operation to the device.

(2) Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and read command.

(3) Then master sends the register address.

(4) Then the device sends the data read out from register address sent before in MISO.

(5) Finally master pulls CSN high to finish the operation.

Automatic address increment read:

(1) – (3) Same as above.

(4) During the 8th rising edge of sending the first data byte, the internal address pointer will increment by one. The next data byte sent from AW20216SQPY will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be read from AW20216SQPY.

(5) Finally master pulls CSN high to finish the operation.

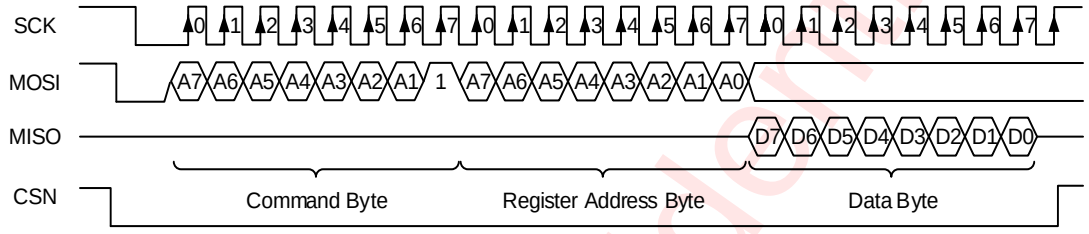


Figure 19 SPI Read from AW20216SQPY (Typical)

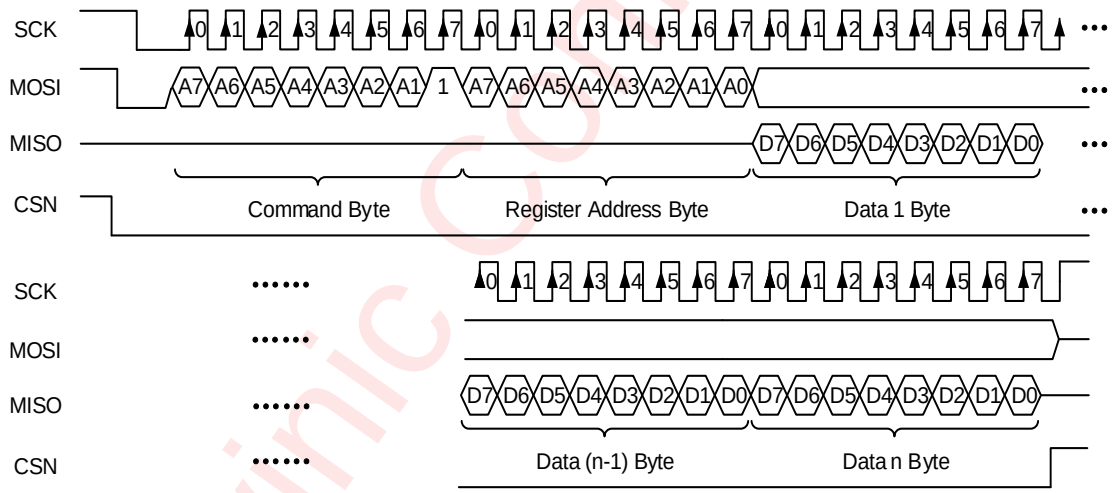


Figure 20 SPI Read from AW20216SQPY (Automatic Address Increment)

LED OPEN/SHORT DETECTION

AW20216SQPY supports LED open/short detection. When bits OSDE[1:0] of the register GCR (page0, address=0x00) are set to “11”, open detection is enabled, and the detection results can be read out via the registers OSR0~OSR35 (page0, address=0x03~0x26) when CHIPEN is “1”. Similarly, when set bits OSDE[1:0] of the register GCR (page0, address=0x00) to “10”, short detection is enabled, and the results also can be read out via the registers OSR0~OSR35 when CHIPEN is “1”. Each bit of OSR0~OSR35 store a LED’s open/short status. Each OSR register stores 6 LEDs open/short status in bit5~bit0. For example, OSR0 stores the status of LED0~LED5, in which MSB is status of LED5, and LSB is status of LED0.

	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	CS16	CS17	CS18
SW1	OSR0						OSR1						OSR2					
SW2	OSR3						OSR4						OSR5					
SW3	OSR6						OSR7						OSR8					
SW4	OSR9						OSR10						OSR11					
SW5	OSR12						OSR13						OSR14					
SW6	OSR15						OSR16						OSR17					
SW7	OSR18						OSR19						OSR20					
SW8	OSR21						OSR22						OSR23					
SW9	OSR24						OSR25						OSR26					
SW10	OSR27						OSR28						OSR29					
SW11	OSR30						OSR31						OSR32					
SW12	OSR33						OSR34						OSR35					

Figure 21 Open/Short Register

The valid detect result is determined by:

Short detection: V_{cs} > PVCC-VTH_{SHORT}

Open detection: V_{cs} < VTH_{OPEN}

VTH_{SHORT}: Threshold of short detection (VTH_{SHORT} = 1.5V, typical).

VTH_{OPEN}: Threshold of open detection (VTH_{OPEN} = 0.1V, typical).

The recommend configuration in PVCC=4.2V is:

- CS_MS = 0x40, (page0.CS_MS)
- 0x20 ≤ PWM[7:0] ≤ 0xFF, (page1.PWMn, n=0~215);
- CS_DS = 0xFF, (page2.CS_DSn, n=0~215);

LED DISPLAY AND CONTROL

LED DISPLAY CONTROL DESCRIPTION

The device supports up to 216 LEDs. The location of each LED is shown by the following figure. The parameter location in page1~page2 is the same as the LED.

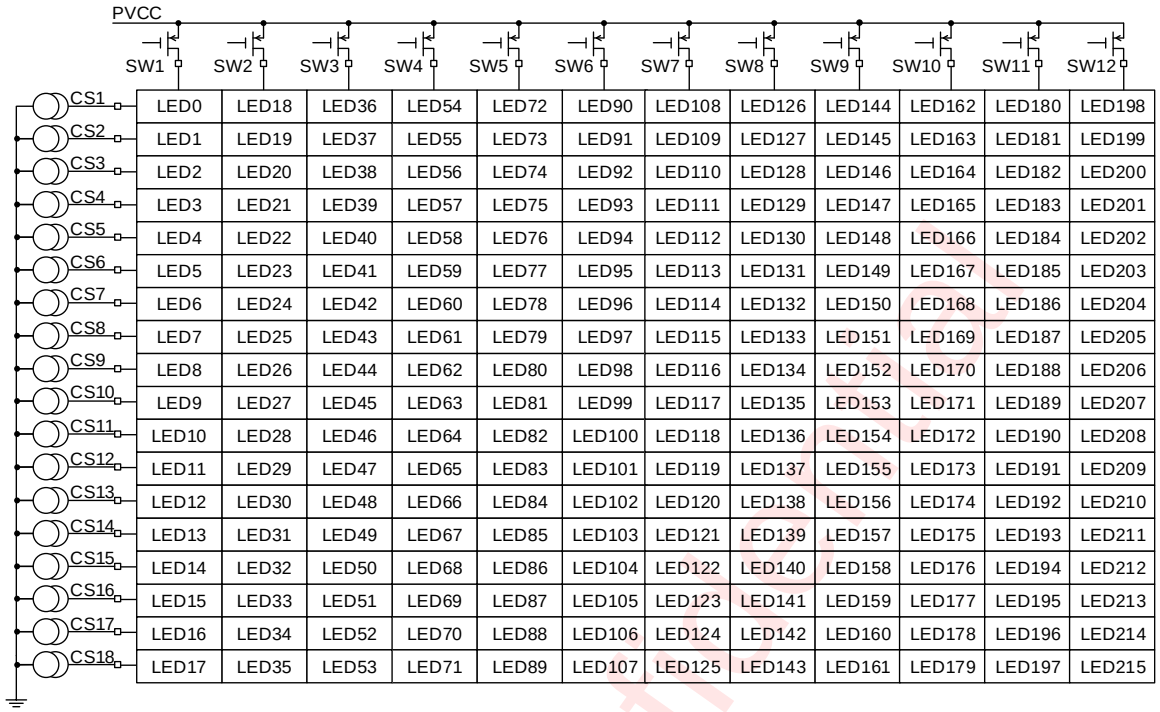


Figure 22 LED Location

In AW20216SQPY, each LED is controlled by PWM[7:0], register PWMx (page1, address=0x00~0xD7, x=0~215)

User can program above parameters to control each LED. Register PWM can control the brightness of LEDs. The figure below shows the LED current control model of AW20216SQPY.

Figure 23 LED Current Control Model

SCANNING TIMING

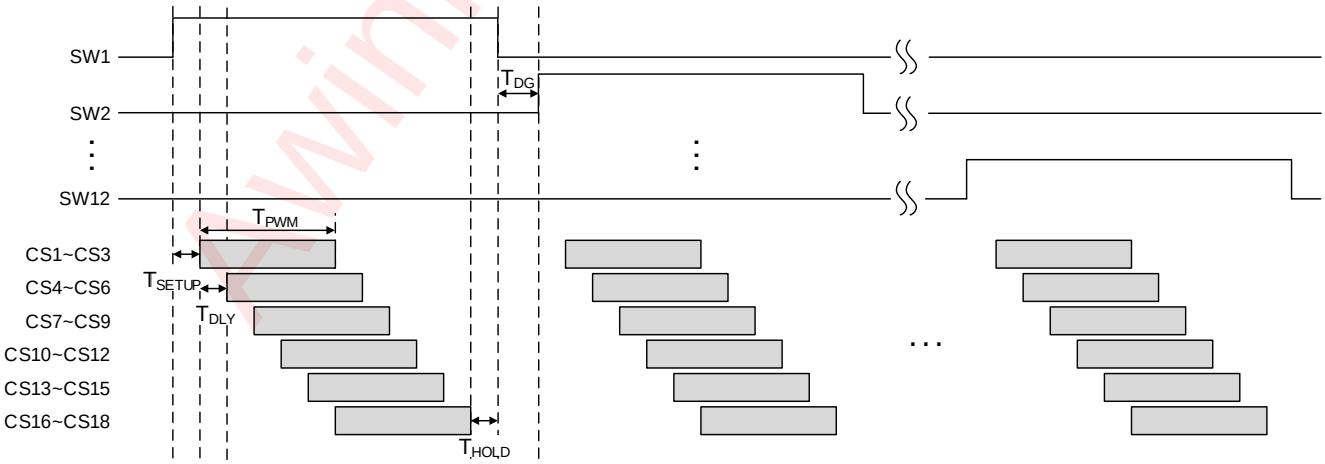


Figure 24 Scanning Timing

As shown in scanning timing figure, the SW1~SW11 is turned on by serial, LED is driven by CS1~CS18 within the SWx (x=1~12) active time. T_{DG} is the non-overlap between SW is De-Ghost time. T_{SETUP} is the delay time between the rising edge of SWx and CS1. SW Control 18 channels current sink (CS1~CS18). CS are divided

into 6 groups, and each group has a delay time, which is T_{DLY}. T_{PWM} is PWM active time when the register PWMx=0xFF (x=0~215), and T_{HOLD} is the time between the falling edge of CS18 and SWx. In addition, SW scanning number N (N=1~12) can be controlled by bits SWSEL[3:0] in register GCR. N is the sum of 1 and the value of SWSEL[3:0],when the value of SWSEL[3:0] is below 2'b1100. Otherwise N is 12.

When PCCR.PWMFRQ[2:0] = 000 (page0, address=0x29), the DUTY is:

$$DUTY = \frac{15.9375us}{0.25us + 5 \times 0.125us + 16us + 0.125us + 1us} \times \frac{1}{N}$$

Where T_{PWM} = 15.9375us, T_{SETUP}=0.25us, T_{DLY}=0.125us, T_{HOLD}=0.125us, and T_{DG}=1us. The period of PWM is 16us. N is the SW scanning number.

The average output current of LED_n (n=0~215) can be expressed by the following formula,

$$I_{LED} = \frac{K}{R_{EXT}} \times \frac{PWM_x}{256} \times DUTY$$

Where K = 400V, and R_{EXT} is the value of external resistor.

PWM MODULATION

PWM FREQUENCY

The PWM frequency is decided by bits PWMFRQ[2:0] of register PCCR (page0, address=0x29). Following table shows the relationship of PWM frequency and the PWMFRQ[2:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency higher than 20 kHz.

PWMFRQ[2:0]	000	001	010	011	100	101	110	111
PWM Freq.	62.5kHz	31.25kHz	15.6kHz	7.8kHz	3.9kHz	1.95kHz	975Hz	488Hz

EMI REDUCTION

SLEW RATE

AW20216SQPY supports programmed slew rate control, which can change the transition time of the LED current sink (CS1~CS18) on or off, so as to achieve the effect of reducing EMI. The slew rate control is configured by the bits SRR and SRF[1:0] of register SRCR(page0, address=0x2B).

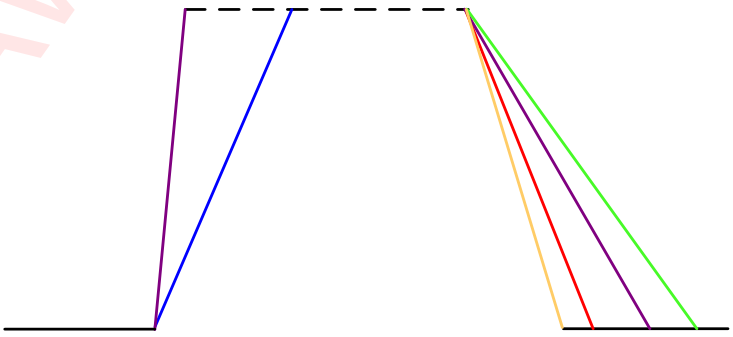


Figure 25 Slew Rate Control

SPREAD SPECTRUM

AW20216SQPY has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (page0, address=0x28) is set to "1", spread spectrum function is enabled. By setting the bit SSR in register SSCR (page0, address=0x28), four spread spectrum range 5%, 15%, 25% and 35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

DE-GHOST FUNCTION

To prevent the LED ghost effect, AW20216SQPY has integrated pull down voltage setting for each SWx (x=1~11) and pull up voltage setting for each CSx (x=1~18). The De-Ghost function is disabled when bit DG_ENB of register DGCR (page0, address=0x02) is set to "1", and the DG_ENB is "0" in default. Select the right SWx pull down voltage, SWPD[2:0] of register DGCR (page0, address=0x02) and CSx pull up voltage, CSPU[2:0] of register DGCR (page0, address=0x02) which eliminate the ghost LED for a particular matrix layout configuration, selecting the voltage setting will be sufficient to eliminate the LED ghost phenomenon.

Lower value of SWPD and Higher value of CSPU will have stronger De-Ghost ability to LED and may let LED have higher reverse voltage. Recommend setting is SWPD= 1.1V, CSPU= PVCC-1.3V (Reverse voltage of LED is around -2.6V, when PVCC=5V).

When AW20216SQPY works in low power mode and standby mode, the De-Ghost function should be disabled.

MULTIPLE DEVICE SYNCHRONIZATION

AW20216SQPY supports multiple device synchronization to drive more than 216 LEDs by cascade of multiple devices. In this application, all devices share a common clock, one device works as a master to output common clock on pin SYNC, and other devices work as slave to use external input clock from pin SYNC. Bit CLKOE and CLKSEL in Register SSCR (page0, address=0x28) select the clock input or output on pin SYNC.

CLKOE	CLKSEL	Device Clock Selection
0	0	Use Internal clock and pin SYNC is high-Z
1	0	Master, use internal clock and output it on pin SYNC
0	1	Slave, use external clock from pin SYNC
1	1	Forbidden

REGISTER CONFIGURATION

REGISTER CONTROL

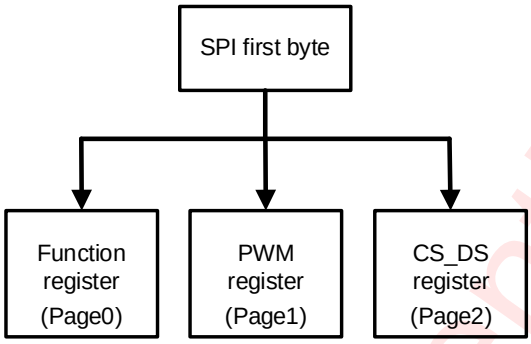


Figure 26 Register Control

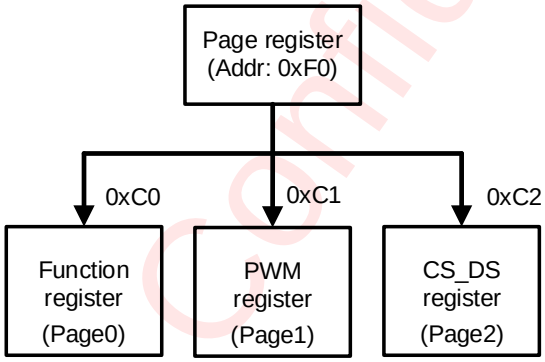


Figure 27 I2C Register Control

AW20216SQPY have three pages, and user can choose page0~page2 by changing first byte of SPI. In I²C, user can choose page0~page2 by writing 0xC0~0xC2 to the page register(address=0xF0) in any page. The page0 is activated by default.

REGISTER LIST

Page0: Function Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	GCR	R/W	SWSEL				LGC	OSDE		CHIPEN	0xB0
0x01	CS_MS	R/W	CS_MS								0x00
0x02	DGCR	R/W	DG_ENB	-	CSPU		-		SWPD		0x44
0x03 ~ 0x26	OSR0 ~ OSR35	R	-		LED0~LED215 Open/Short status register						0x00
0x27	OTCR	R/W	OTFLG	OTPD	OTDIS	TRFLG	TRTH		TROF		0x00
0x28	SSCR	R/W	CLKOE	CLKSEL	-	SSE	SRR		CLT		0x00

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x29	PCCR	R/W	PWMFRQ			-					0x00
0x2A	UVCR	R/W	REXT_ST		-		PUST	UVFLG	UVPD	UVDIS	0x00
0x2B	SRCR	R/W	-		OTH	STH	-	SRR	SRF		0x02
0x2F	RSTN	R/W	RSTN/ID								0x70
0xF0	PAGE	R/W	-					PAGE (only for I2C)			0x00

Page1: PWM Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	PWM0	R/W	PWM0								0x00
0x01	PWM1	R/W	PWM1								0x00
…	…	R/W	…								0x00
0xD7	PWM215	R/W	PWM215								0x00
0xF0	PAGE	R/W	-					PAGE (only for I2C)			0x00

Page2: Current Source Dot Switch Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	CS_DS0	R/W	CS_DS0								0x00
0x01	CS_DS1	R/W	CS_DS1								0x00
…	…	R/W	…								0x00
0xD7	CS_DS215	R/W	CS_DS215								0x00
0xF0	PAGE	R/W	-					PAGE (only for I2C)			0x00

REGISTER DETAILED DESCRIPTION

PAGE: Page Select Register (Page 0/1/2: Address 0xF0)

Bit	Symbol	R/W	Description	Default
7:0	PAGE	R/W	Page select (only for I²C) 0xC0: page0 0xC1: page1 0xC2: page2	0x00

GCR: Global Control Register (Page 0: Address 0x00)

Bit	Symbol	R/W	Description	Default
7:4	SWSEL	R/W	Active the SW number select 0000: SW1 active SW2~SW12 not active 0001: SW1~SW2 active SW3~SW12 not active 0010: SW1~SW3 active SW4~SW12 not active 0011: SW1~SW4 active SW5~SW12 not active 0100: SW1~SW5 active SW6~SW12 not active 0101: SW1~SW6 active SW7~SW12 not active	1011

Bit	Symbol	R/W	Description	Default
			0110: SW1~SW7 active SW8~SW12 not active 0111: SW1~SW8 active SW9~SW12 not active 1000: SW1~SW9 active SW10~SW12 not active 1001: SW1~SW10 active SW11~SW12 not active 1010: SW1~SW11 active SW12 not active 1011~1111: SW1~SW12 active	
3	LGC	R/W	Logic level select (only for IFS=1) 0: 1.4/0.4V 1: 2.4/0.6V	0
2:1	OSDE	R/W	Open/short detect enable 0x: Detect disable 10: Short detect 11: Open detect	00
0	CHIPEN	R/W	Chip enable 0: Disable 1: Enable	0

CS_MS: Current Source Main Switch (Page 0: Address 0x01)

Bit	Symbol	R/W	Description	Default
7:0	CS_MS	R/W	Current Source Main Switch, set to 0xFF to enable. Writing 0x40 to enter open/short detection mode.	0x00

DGCR: De-ghost Control Register (Page 0: Address 0x02)

Bit	Symbol	R/W	Description	Default
7	DG_ENB	R/W	De-Ghost disable 0: Enable 1: Disable	0
6	RESERVED	R	Reserved	1
5:4	CSPU	R/W	CS pull up select 00: PVCC-1.3V 01: PVCC-2.0V 10: PVCC-0.5V 11: PVCC	00
3:2	RESERVED	R	Reserved	01
1:0	SWPD	R/W	SW pull down select 00: 1.1V 01: 1.9V 10: 0.5V 11: GND	00

OSR0~OSR35: Open/Short Status Register (Page 0: Address 0x03~0x26)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00
5:0	OSR	R	Open/short status of LED0~LED215 0: Open/short not happen 1: Open/short happen	000000

OTCR: Over Temperature Control Register (Page 0: Address 0x27)

Bit	Symbol	R/W	Description	Default
7	OTFLG	R	Over temperature flag 0: Over-temperature not happen 1: Over-temperature happen	0
6	OTPD	R/W	Over-temperature(OT) protect disable 0: OT protect enable, when OT event occurs, device will clear GCR.CHIPEN to 0. 1: OT protect disable	0
5	OTDIS	R/W	Over-temperature detect disable 0: OT detect enable, when OT event occurs, OTCR.OTFLAG will be set. 1: OT detect disable	0
4	TRFLG	R	Thermal roll off status 0: Roll off not happen 1: Roll off happen	0
3:2	TRTH	R/W	Thermal roll threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00
1:0	TROF	R/W	Thermal roll off percentage of I_{OUT} 00: 100% 01: 75% 10: 55% 11: 30%	00

SSCR: Spread Spectrum Control Register (Page 0: Address 0x28)

Bit	Symbol	R/W	Description	Default
7	CLKOE	R/W	Clock output enable 0: Disable 1: Enable	0
6	CLKSEL	R/W	0: Use internal 16MHz OSC clock 1: Use clock input from pin SYNC	0

Bit	Symbol	R/W	Description	Default
5	RESERVED	R	Reserved	0
4	SSE	R/W	Spread spectrum enable 0: Disable 1: Enable	0
3:2	SSR	R/W	Spread spectrum range 00: ±5% 01: ±15% 10: ±25% 11: ±35%	00
1:0	CLT	R/W	Spread spectrum cycle time 00: 1980μs 01: 1200μs 10: 820μs 11: 660μs	00

PCCR: PWM Clock Control Register (Page 0: Address 0x29)

Bit	Symbol	R/W	Description	Default
7:5	PWMFRQ	R/W	PWM frequency selection 000: 62.5kHz 001: 32.25kHz 010: 15.6kHz 011: 7.8kHz 100: 3.9kHz 101: 1.95kHz 110: 977Hz 111: 488Hz	000
4:0	RESERVED	R	Reserved	00000

UVCR: UVLO Control Register (Page 0: Address 0x2A)

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	R_{EXT} status 00: Normal 10: R_{EXT} is open 01: R_{EXT} is short or OCP 11: Not defined	00
5:4	RESERVED	R	Reserved	00
3	PUST	R	Power-up reset status 0: Power-up reset not happen 1: Power-up reset happen	0

Bit	Symbol	R/W	Description	Default
2	UVFLG	R	UVLO status 0: UVLO not happen 1: UVLO happen	0
1	UVPD	R/W	UVLO protect disable 0: UVLO protect enable, when under-voltage event occurs, device will clear GCR.CHIPEN to 0. 1: UVLO protect disable	0
0	UVDIS	R/W	UVLO detect disable 0: UVLO detect enable, when under-voltage event occurs, UVCR.UVFLG will be set. 1: UVLO detect disable	0

SRCR: Open/Short Control Register (Page 0: Address 0x2B)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00
5	OTH	R/W	Open threshold 0: 0.1V 1: 0.2V	0
4	STH	R/W	Short threshold 0: PVCC-1.5V 1: PVCC-0.8V	0
3	RESERVED	R	Reserved	0
2	SRR	R/W	Slew rate control for LED output rising time 0: 1ns 1: 6ns	0
1:0	SRF	R/W	Slew rate control for LED output falling time 00: 1ns 01: 3ns 10: 6ns 11:10ns	10

RSTN: Reset Register (Page 0: Address 0x2F)

Bit	Symbol	R/W	Description	Default
7:0	RSTN	R/W	Write 0xAE to the register will reset all registers to their default value. The chip ID will be read out from the register.	0x70

PWMx (x=0~215): PWM Configure Register (Page 1: Address 0x00~0xD7)

Bit	Symbol	R/W	Description	Default
7:0	PWMx	R/W	PWM modulated	0x00

CS_DSx (x=0~215): Current Source Dot Switch Configure Register (Page 2: Address 0x00~0xD7)

Bit	Symbol	R/W	Description	Default
7:0	CS_DSx	R/W	Current Source Dot Switch, set to 0xFF to enable	0x00

APPLICATION INFORMATION

If the equipment has antenna, the IC should be far away from the antenna in order to avoid the EMI.

R_{EXT}

The selection of R_{EXT} determined the maximum LED0~LED215 current I_{max} as described in below formula (1).

$$I_{max} = \frac{K}{R_{EXT}} \quad (1)$$

When R_{EXT} = 10KΩ, I_{max} = 40mA, I_{switch} = 720mA.

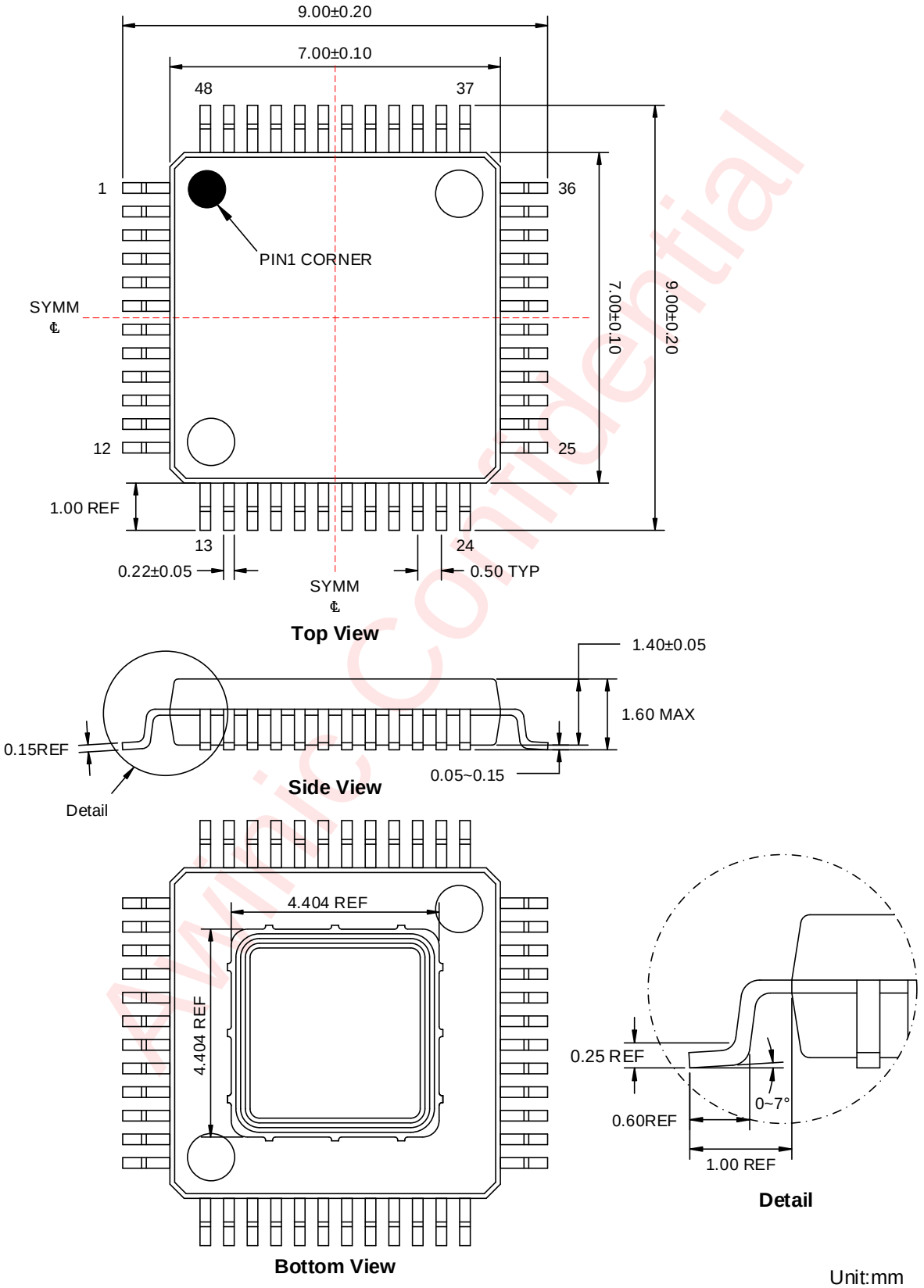
When R_{EXT} = 20KΩ, I_{max} = 20mA, I_{switch} = 360mA.

PCB LAYOUT CONSIDERATION

AW20216SQPY is an 18x12 matrix LED driver programmed via an SPI compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

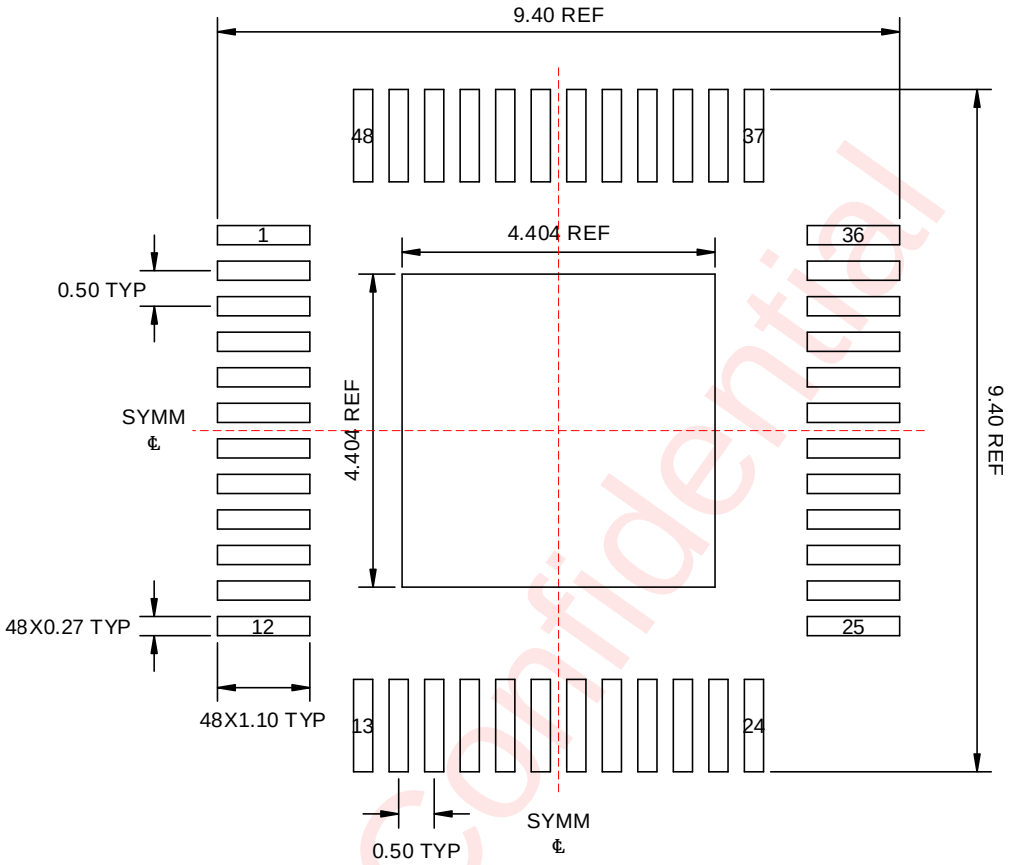
1. The C_1、C_2、C_3、C_4 、C_5 should be placed as close to the chip as possible.
2. The R_{EXT} should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal via as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

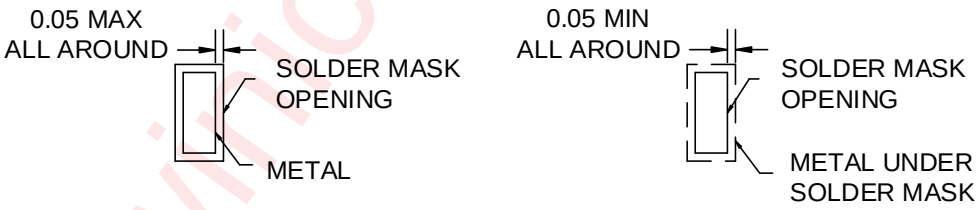
PACKAGE DESCRIPTION



Unit:mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov. 2025	Officially released
V1.1	Dec. 2025	1. Remove unnecessary registers and functional descriptions -- page25&29 2. Add led open/short detection description -- page20

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