

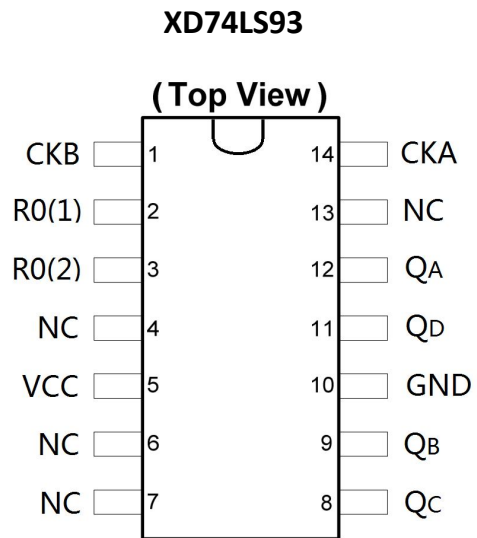
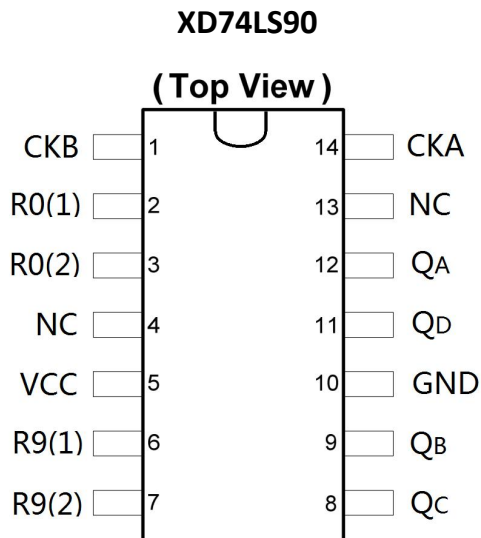
1. DESCRIPTION

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the **74LS90**, and the divide-by-eight for the **74LS93**.

All of these counters have a gated zero reset and the 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the QD output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

2. PIN CONFIGURATIONS



XD74LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

XD74LS90
BI-QUINARY

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

XD74LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

XD74LS93
RESET/COUNT FUNCTION TABLE

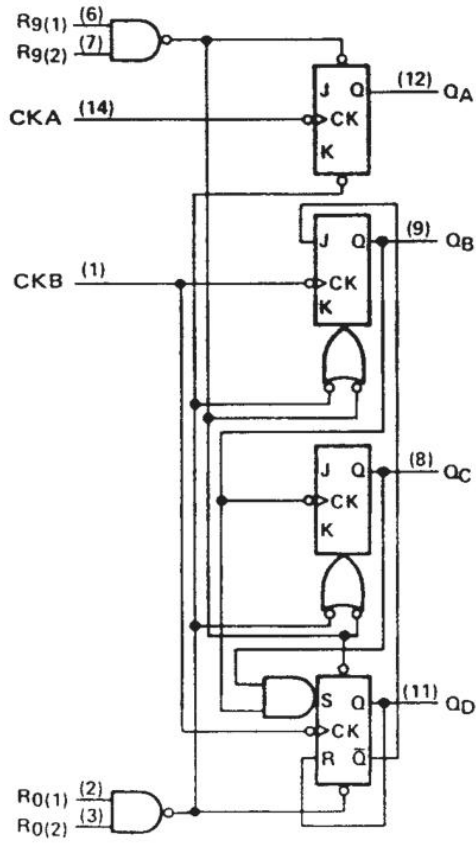
RESET INPUTS		OUTPUT			
R0(1)	R0(2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

XD74LS93
COUNT SEQUENCE

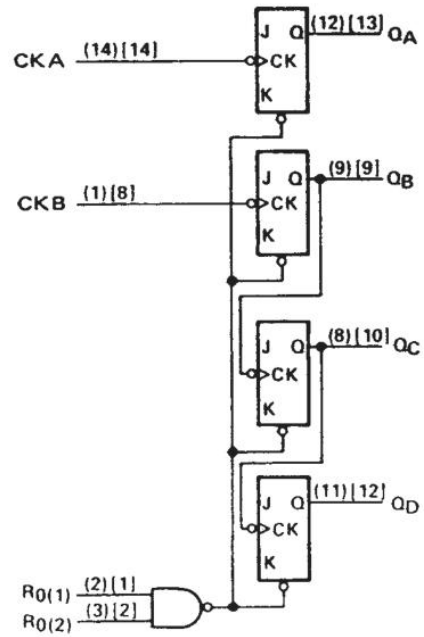
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

3. LOGIC DIAGRAMS

XD74LS90

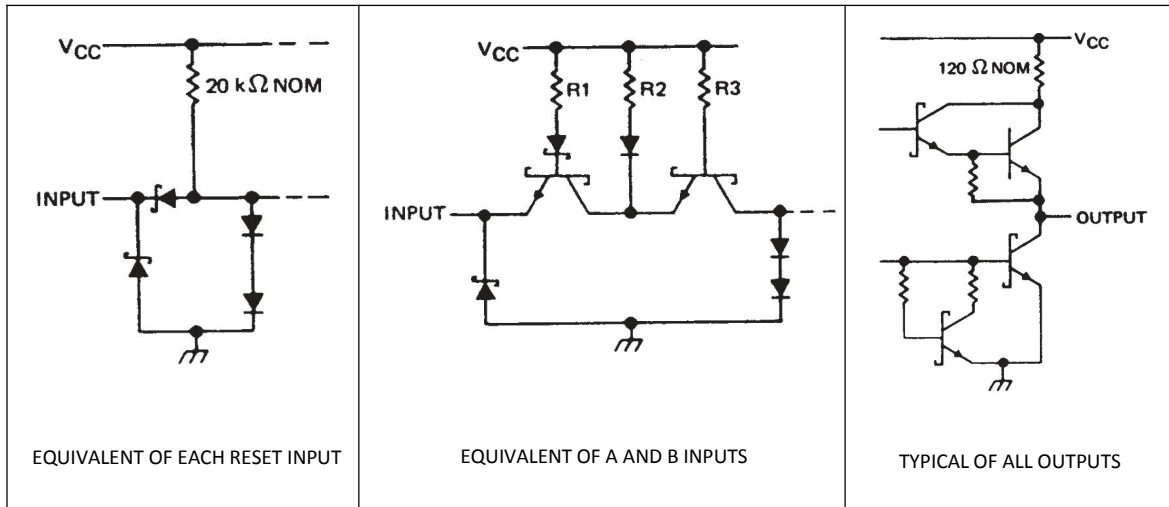


XD74LS93



4. SCHEMATICS OF INPUTS AND OUTPUTS

XD74LS90, XD74LS93



5. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} (see Note 1).....	7V
Input voltage, V_I : 74LS90, 74LS93.....	7V
Operating free-air temperature range: DIP package.....	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C

NOTES 1: Voltage values are with respect to the network ground terminal.

6. RECOMMENDED OPERATING CONDITIONS

			74LS90, 74LS93			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current				-400	μA
I _{OL}	Low-level output current				8	mA
f _{count}	Count frequency	A input	0		32	MHz
		B input	0		16	
t _w	Pulse duration	A input	15			ns
		B input	30			
		Reset inputs	30			
t _{su}	Reset inactive-state setup time		25			ns
T _A	Operating free-air temperature		0		70	°C

7. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			74LS90			UNIT
			MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA		-1.5	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} MAX, V _{IH} = 2 V, I _{OH} = -400 μA		2.7 3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX	I _{OL} = 1.6 mA		0.25 0.4	V
			I _{OL} = 3.2 mA		0.35 0.5	
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V		0.1	mA
		CKA	V _{CC} = MAX, V _I = 5.5 V		0.2	
		CKB			0.4	
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V		20	μA
		CKA			40	
		CKB			80	
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V		-0.4	mA
		CKA			-2.4	
		CKB			-3.2	
I _{OS}	Short-circuit output current [§]		V _{CC} = MAX		-20 -100	mA
I _{CC}	Supply current		V _{CC} = MAX		9 15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§ Not more than one output should be shorted at a time.

PARAMETER			TEST CONDITIONS [†]	74LS93			UNIT
				MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = V _{IL} MAX, V _{IH} = 2 V, I _{OH} = -400 μA	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX, I _{OL} = 4 mA	0.25	0.4		V
			I _{OL} = 8 mA	0.35	0.5		
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1	mA
		CKA or CKB	V _{CC} = MAX, V _I = 5.5 V			0.2	
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20	μA
		CKA or CKB				80	
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
		CKA				-2.4	
		CKB				-1.6	
I _{OS}	Short-circuit output current [§]		V _{CC} = MAX	-20		-100	mA
I _{CC}	Supply current		V _{CC} = MAX		9	15	mA

8. SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

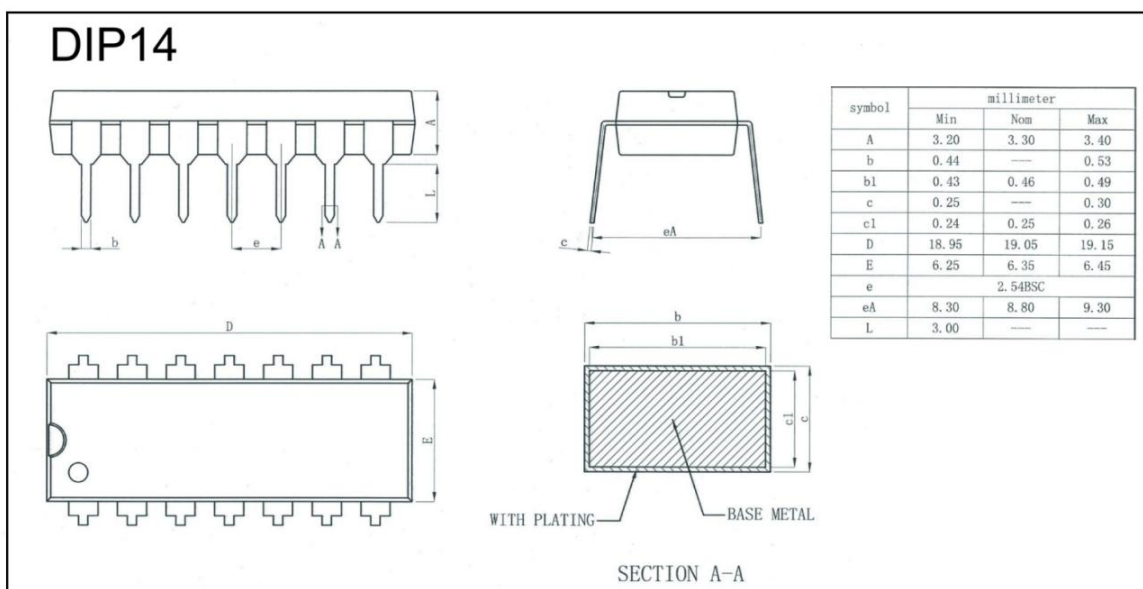
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	CKA	QA	C _L =15 pF,R _L =2kΩ,	32	42		32	42		MHz
	CKB	QB		16			16			
t _{PLH}	CKA	QA		10	16		10	16		ns
t _{PHL}		12		18		12	18			
t _{PLH}	CKA	QD		32	48		46	70		ns
t _{PHL}		34		50		46	70			
t _{PLH}	CKB	QB		10	16		10	16		ns
t _{PHL}		14		21		14	21			
t _{PLH}	CKB	QC		21	32		21	32		ns
t _{PHL}		23		35		23	35			
t _{PLH}	CKB	QD		21	32		34	51		ns
t _{PHL}		23		35		34	51	ns		
t _{PHL}	Set-to-0	Any		26	40		26	40		ns
t _{PLH}	Set-to-9	QA.QD		20	30					ns
t _{PHL}		QB.QC		26	40					

9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS90	XD74LS90	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000
XD74LS93	XD74LS93	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

10. DIMENSIONAL DRAWINGS



[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]