

## 60V N-Channel Power MOSFET

### Description

The STD20NF06L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications.

### General Features

- ①  $V_{DS}=60V, I_D=20A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$
- ② Special process technology for high ESD capability
- ③ High density cell design for ultra low  $R_{dson}$
- ④ Fully characterized avalanche voltage and current
- ⑤ Good stability and uniformity with high EAS
- ⑥ Excellent package for good heat dissipation

### Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

### Package Marking And Ordering Information

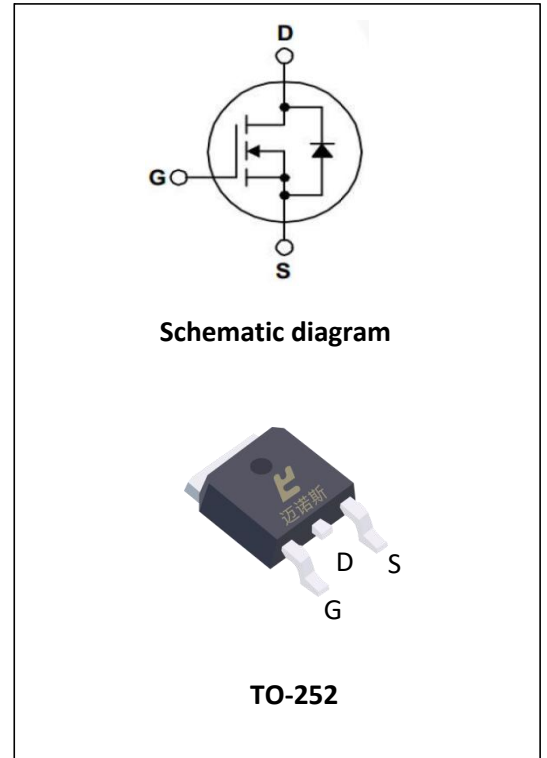
Ordering Codes	Package	Product Code	Packing
STD20NF06L	TO-252	STD20NF06L	Reel

### ABSOLUTE RATINGS (at $T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	20	A
$I_{DM}$	Drain Current-Pulsed <sup>(Note 1)</sup>	80	A
$P_D$	Maximum Power Dissipation( $T_C=25^\circ C$ )	44	W
$E_{AS}$	Single pulse avalanche energy <sup>(Note 2)</sup>	56	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

### Thermal Characteristic

Symbol	Parameter	Typ	Units
$R_{\theta JC}$	Junction-to-Case	3.4	$^\circ C/W$



## Electrical Characteristics (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
B <sub>VDS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>(Note 3)</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	--	25	35	mΩ
G <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =10A	--	11	--	S
<b>Dynamic Characteristics</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	--	670	--	pF
C <sub>OSS</sub>	Output Capacitance		--	76	--	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance		--	66	--	pF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V, R <sub>GEN</sub> =10Ω	--	19.2	--	nS
t <sub>r</sub>	Turn-on Rise Time		--	6.4	--	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		--	29.2	--	nS
t <sub>f</sub>	Turn-Off Fall Time		--	8.2	--	nS
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =48V, I <sub>D</sub> =10A V <sub>GS</sub> =10V	--	21	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	6.5	--	nC
<b>Drain-Source Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage(Note 3)	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	--	--	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	T <sub>j</sub> =25°C, I <sub>F</sub> =10A, di/dt=100A/μs <sup>(note3)</sup>	--	33.6	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	32.1	--	nc

### Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T<sub>j</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω
- 3.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

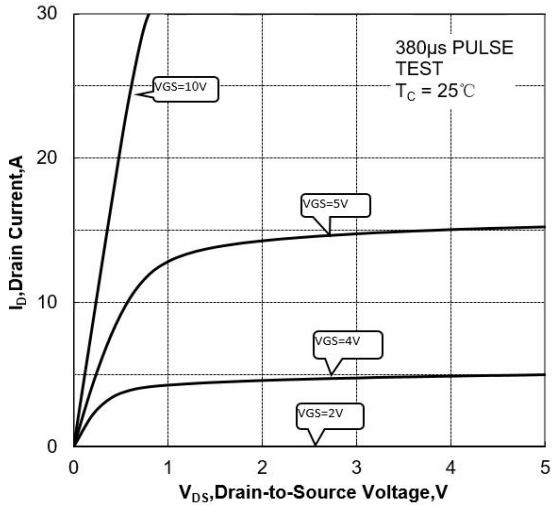


Figure 2 Transfer Characteristics

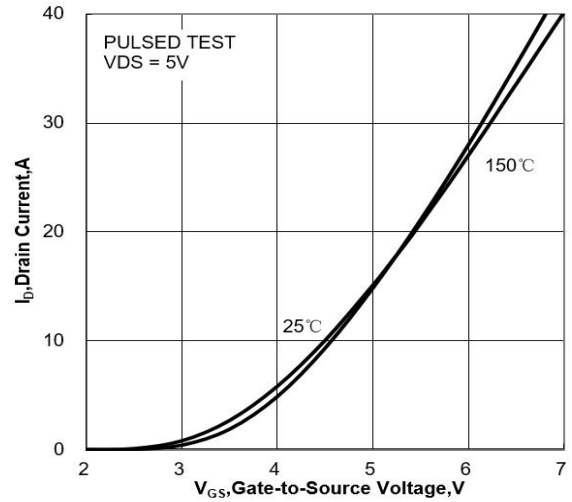


Figure 3 On-Resistance vs. ID and VGS

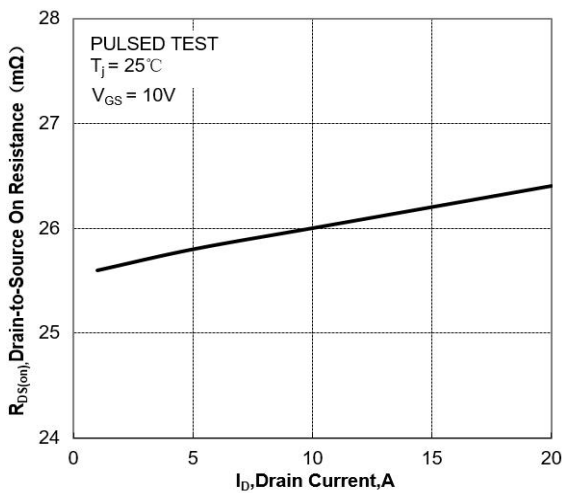


Figure 4 On-Resistance vs. Junction Temperature

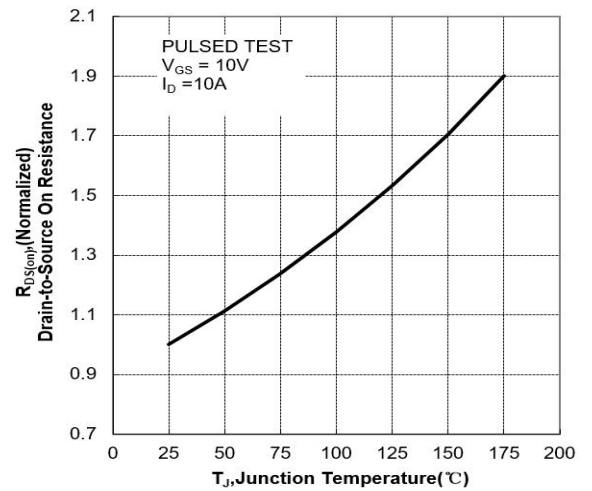


Figure 5 On-Resistance vs. VGS

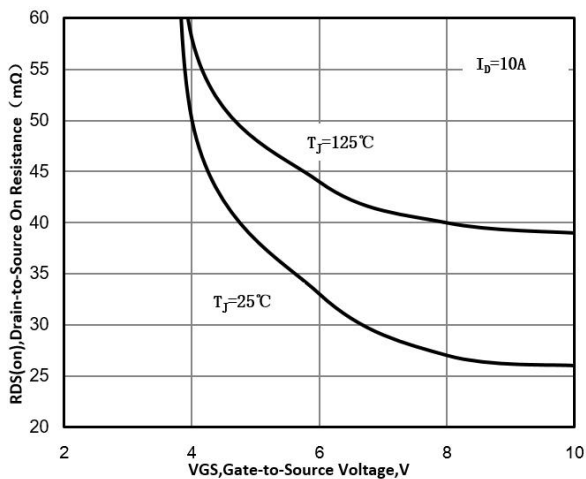


Figure 6 Body Diode Forward Voltage

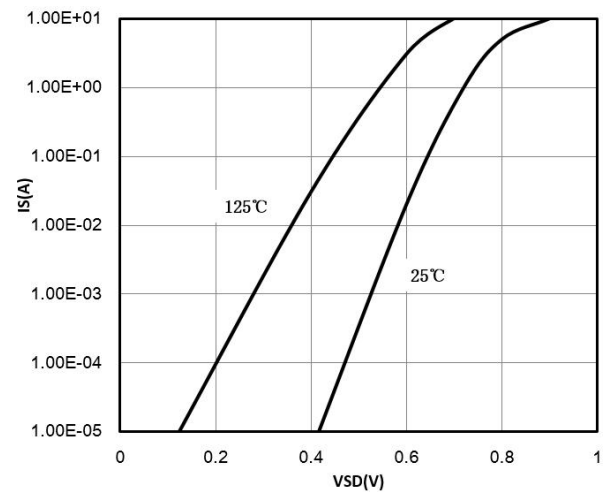


Figure 7 Gate-Charge Characteristics

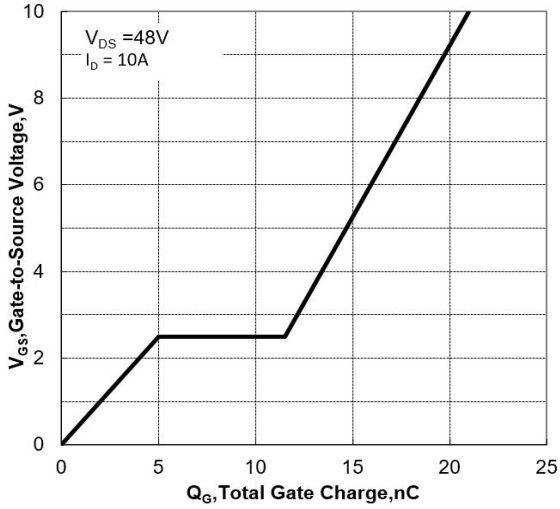


Figure 8 Capacitance Characteristics

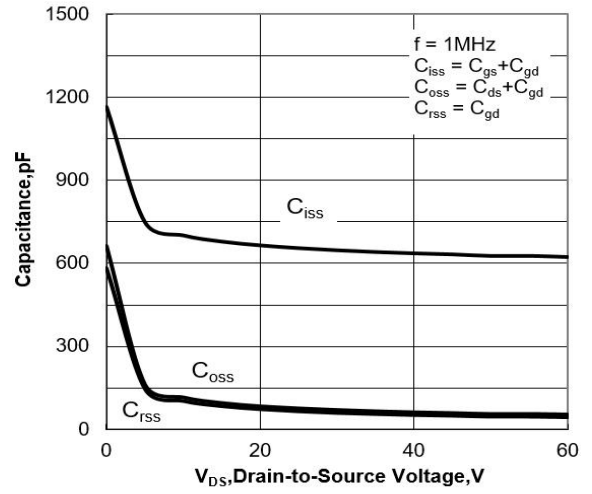


Figure 9 Maximum Forward Biased Safe Operation Area

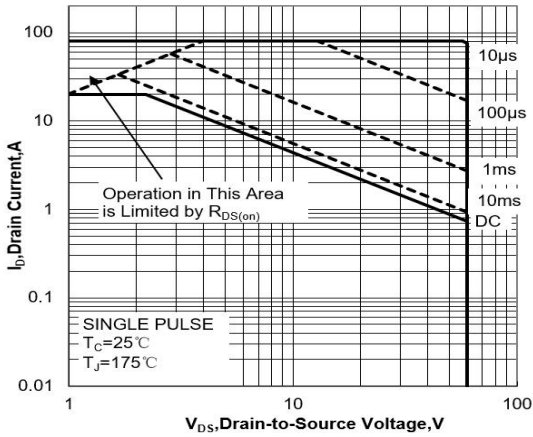


Figure 10 Single Pulse Power Rating Junction-to-Ambient

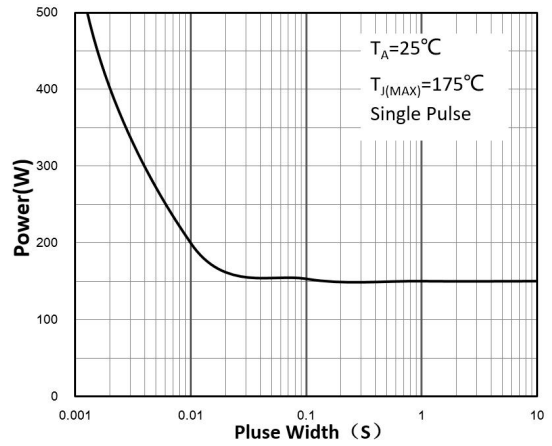
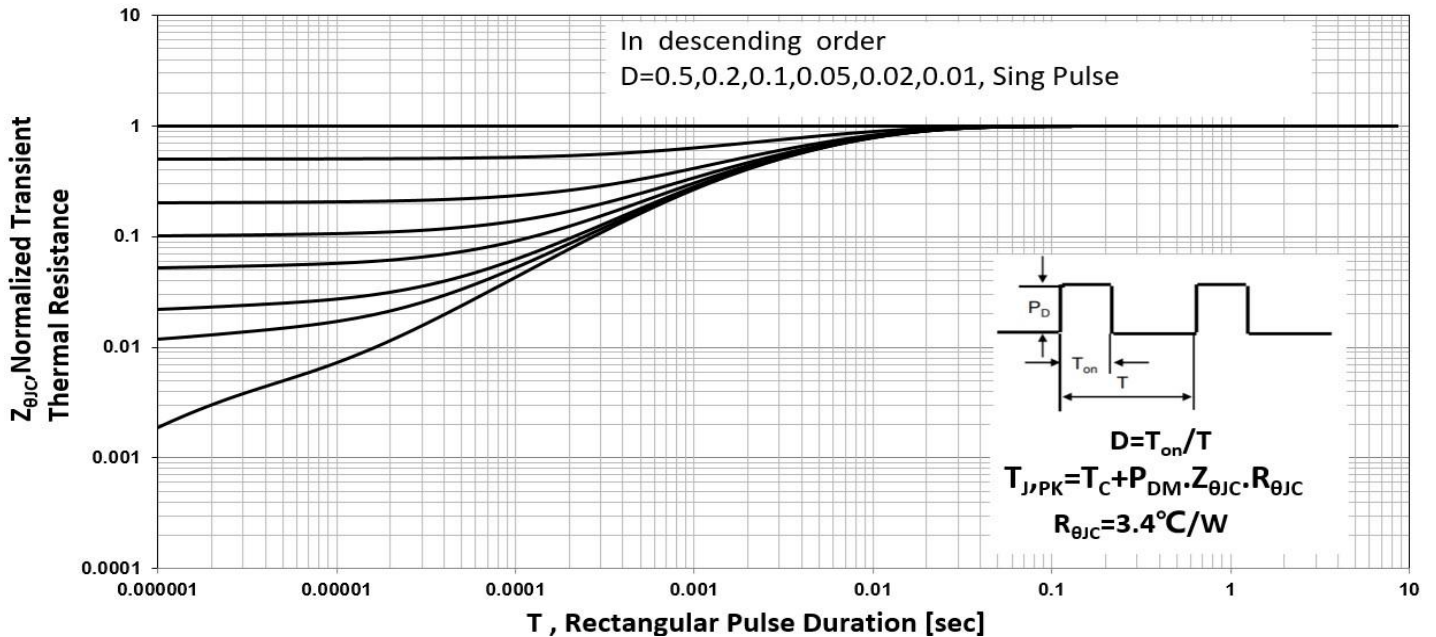
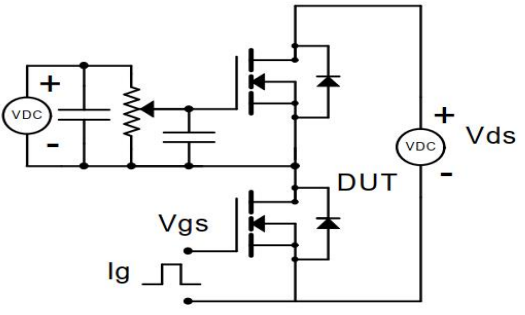
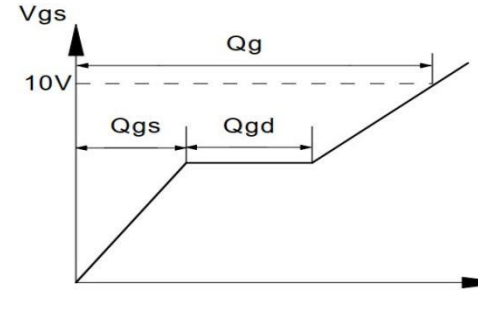
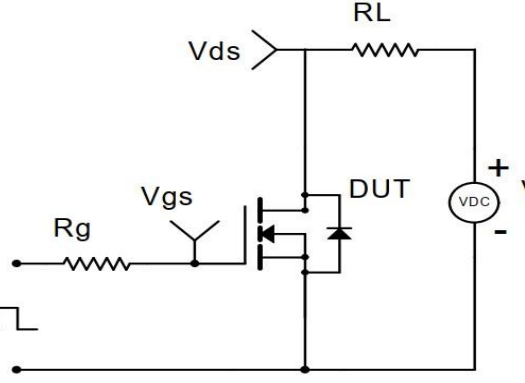
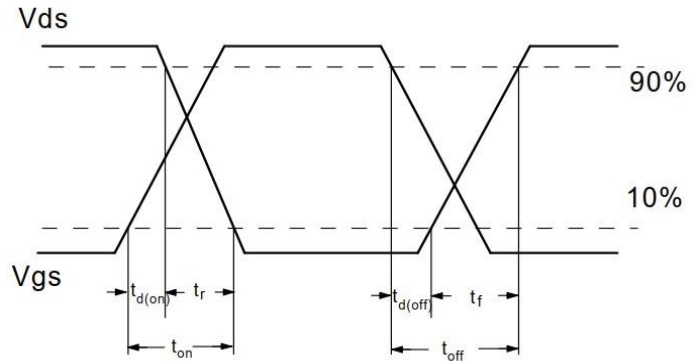
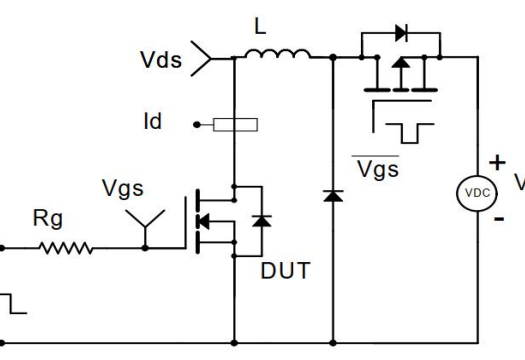
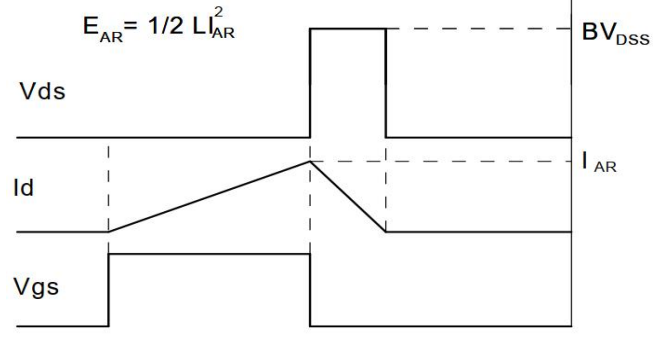
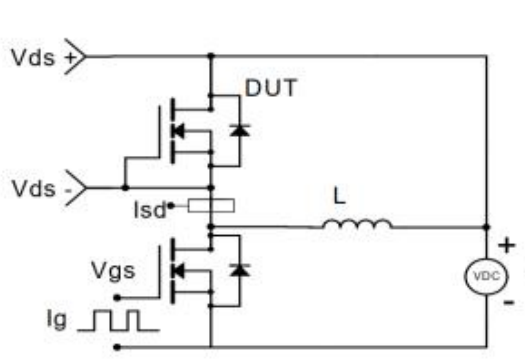
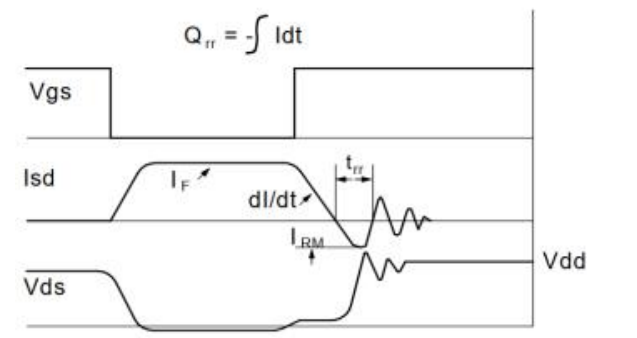


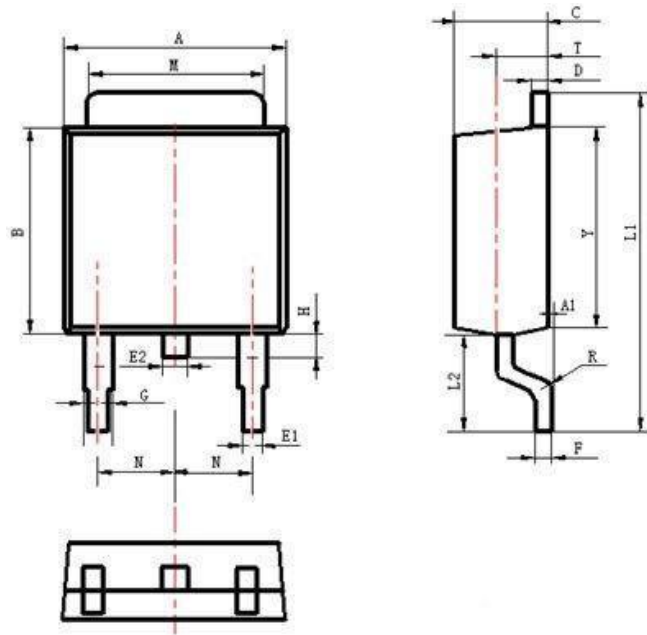
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Ig) through a resistor. The drain is connected to a DC source (VDC) through a resistor. The source is connected to ground. A second MOSFET is shown below, illustrating the gate voltage (Vgs) pulse.</p>	 <p>The graph plots Gate Voltage (Vgs) against Charge. It shows a linear ramp up to 10V, a constant plateau, and a linear ramp down. The total area under the curve is labeled Qg. The area under the ramp up is Qgs, and the area under the ramp down is Qgd.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (VDD). The source is connected to ground.</p>	 <p>The graph shows Vds and Vgs waveforms. Vds is high during the off-state and drops to a low level during the on-state. Vgs is a pulse. Key timing parameters are labeled: t<sub>d(on)</sub>, t<sub>r</sub>, t<sub>on</sub>, t<sub>d(off)</sub>, t<sub>f</sub>, and t<sub>off</sub>. The on-state Vds is shown at 90% and 10% levels.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to an inductor (L) and a DC source (VDD). The source is connected to ground.</p>	 <p>The graph shows Vds, Id, and Vgs waveforms. Vds shows a sharp peak during the switching transient. Id is a pulse. Vgs is a pulse. The equation <math>E_{AR} = 1/2 L I_{AR}^2</math> is shown. The peak Vds is labeled BV<sub>DSS</sub> and the peak Id is labeled I<sub>AR</sub>.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to an inductor (L) and a DC source (VDC). The source is connected to ground.</p>	 <p>The graph shows Vgs, Isd, and Vds waveforms. Vgs is a pulse. Isd shows a forward current (IF) and a reverse current (IRM) during the switching transient. Vds shows a reverse voltage spike. The equation <math>Q_{rr} = -\int Idt</math> is shown. Key timing parameters are labeled: t<sub>rr</sub> and dI/dt.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

**NOTE:**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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