13.5V, 10A Synchronous Boost Converter with Load Disconnect Control

Features

- Input Voltage Range :2.7V to 7V
- Output Voltage Range: 4.5V to 13.5V
- Integrated 12mΩ switching FET and 15mΩ rectifier FET
- Adjustable switching frequency up to 2MHz
- Resistor-programmable peak current limit up to 10 A for high pulse current
- 4ms built-in soft start time
- DCM Operation under light load
- Input Under-Voltage Lockout
- Over-Temperature Protection
- FCQFN 2.5*2-11L Package

Applications

- Laptop and Desktop Computers
- Smart Speakers
- Tablets and Handhelds
- Wireless Speakers

General Description

The AWP36210 is a 13.5V synchronous Boost converter. The AWP36210 integrates two low Rdson resistance power power FETs: A 12mΩ switching FET and a 15mΩ rectifier FET.

The device provides a high-efficiency and small-size power solution for portable equipment.

The AWP36210 uses the adaptive constant off time peak current mode control. AWP36210 has an internal feature to help improving light load efficiency. When output current is low, AWP36210 will go into DCM mode.

The AWP36210 includes configurable features include programmable cycle-by-cycle current limit and programmable switching frequency functions.The switching frequency in PWM mode is adjustable from 200kHz to 2MHz.

The AWP36210 also implements a built-in 4ms soft start function. In addition, the device provides thermal shutdown protection.

Typical Application Circuit

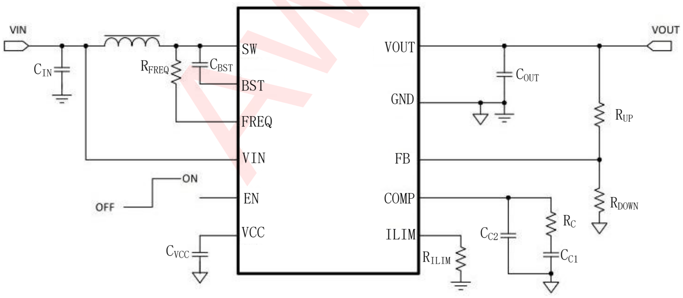
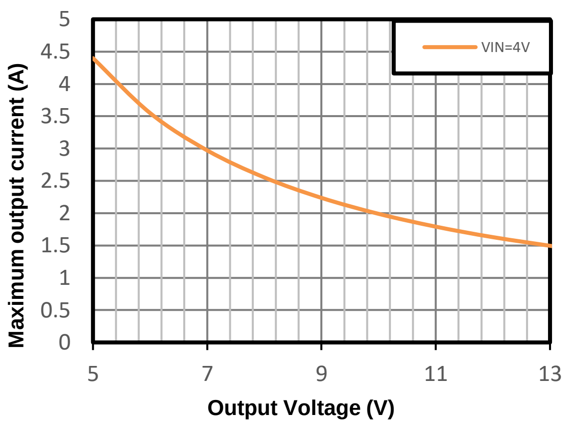


Figure 1 AWP36210 Typical Application Circuit



Maximum Output Current vs Output Voltage

Pin Configuration And Top Mark

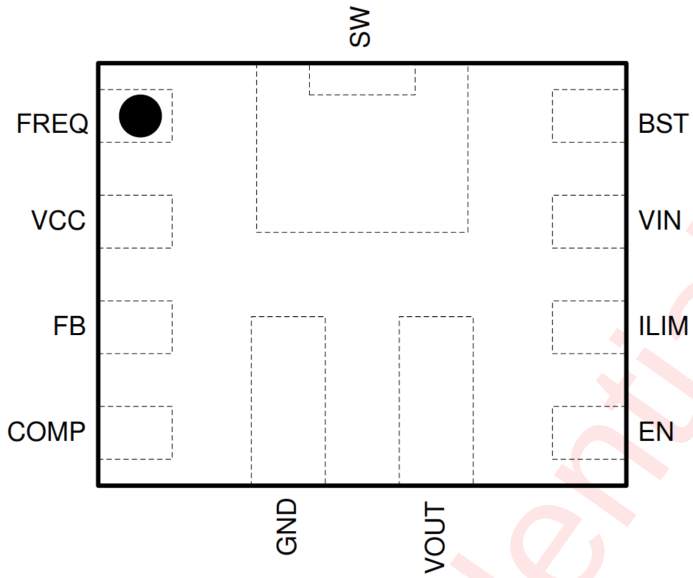


Figure 2 Pin Configuration

Pin Definition

No.	NAME	DESCRIPTION
1	FREQ	The switching frequency is programmed by a resistor between this pin and the SW. This pin can't be float in application.
2	VCC	Output of internal regulator, A ceramic capacitor of more than 4.7μF is required between this pin and ground.
3	FB	Feedback Input. FB senses the output voltage, connect FB with a resistor divider connected between the output and ground. FB is a sensitive node, keep FB away from SW and BST pin.
4	COMP	Output of internal error amplifier, loop compensation network connect to COMP and AGND .COMP is a sensitive node, keep COMP away from SW and BST pin.
5	GND	Power ground.
6	VOUT	Boost converter output.
7	EN	Enable pin. Pull high to turn on the IC, don't float.
8	ILIMIT	Adjustable LSFET peak current limit. Connect a resistor to AGND.
9	VIN	Input supply pin. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
10	BST	Boot strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
11	SW	Power switching pin of boost converter, common node of LSFET drain and HSFET source. Connect the coil to this pin and power input.

Functional Block Diagram

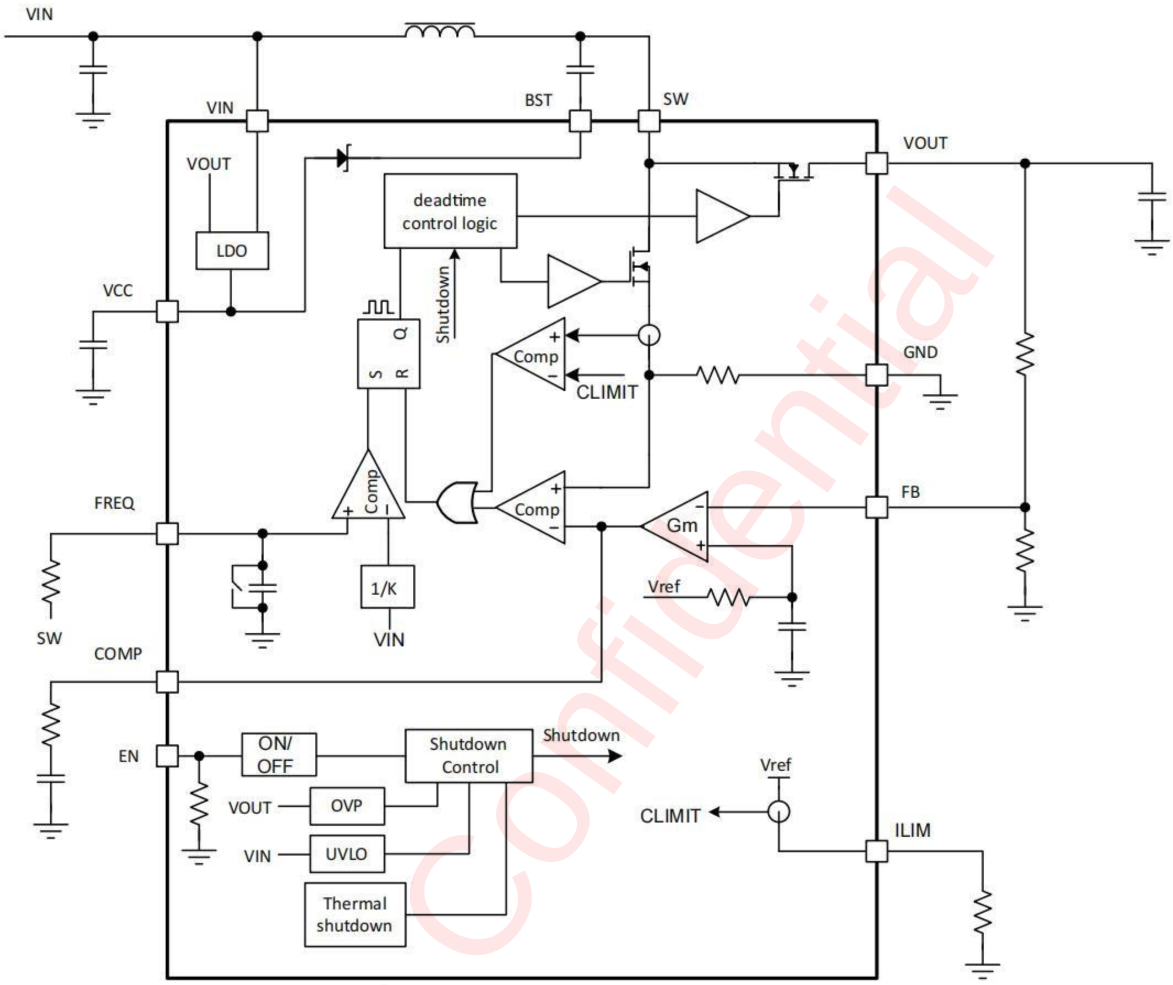


Figure 3 AWP36210

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP36210QNR	-40℃～85℃	FCQFN 2.5*2-11L	PVT4	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
BST Voltage	-0.3V to SW+6.5V
VIN, SW, VOUT voltage	-0.3V to 20V
FB, COMP, ILIMIT, VCC, FREQ EN voltage	-0.3V to 6.5V
Junction to ambient thermal resistance θ_{JA}(NOTE2)	53.4°C /W
Junction to case thermal resistance θ_{JC}(NOTE2)	0.7°C /W
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Measured on approximately 1" square of 1 oz copper.

Recommended Operating Conditions(NOTE3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	2.7		7	V
V_{OUT}	Output Voltage	4.5		13.5	V
V_{BST}	BST Voltage	0		SW+5	V
V_{SW}	SW	0		V_{OUT}	V
Others	FB, COMP, ILIMIT, VCC, FREQ, EN Voltage	0		5	V
T_A	Operating free-air temperature range	-40		85	℃

NOTE3: The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics

VIN = 2.7 V to 5.5 V and VOUT = 9 V, TJ = 25 °C , unless otherwise noted.

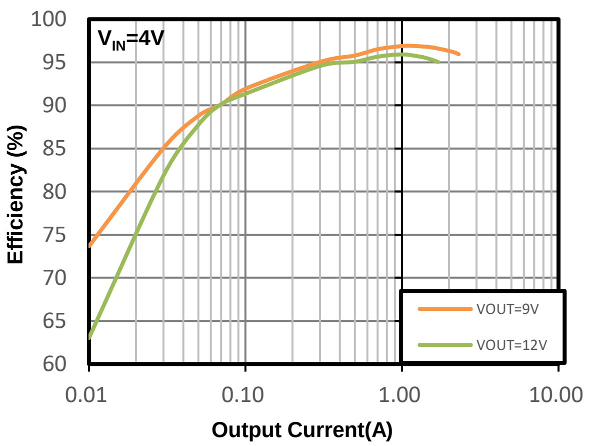
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	VIN operating range		2.7		7	V
V_{INUV}	VIN UVLO threshold voltage	when VIN < V_{INUV}, IC turn off, falling edge		2.5		V
V_{INUV_HYS}	VIN UVLO hysteresis voltage	after VIN > V_{INUV}+ V_{INUV_HYS}, IC restore operation		0.22		V
V_{CC}	VCC regulation voltage	I_{VCC}=2mA, VIN=6V		4.9		V
V_{CCUV}	VCC UVLO threshold voltage	VCC falling edge		2.1		V
V_{CCUV_HYS}	VCC UVLO hysteresis voltage			0.1		V
I_{Q_VIN}	Standby current into VIN pin	VIN=EN=4V, VBUS=12V, FB=1.3V		8.5		μA
I_{Q_VBUS}	Standby current into VBUS pin	VIN=EN=4V, VBUS=12V, FB=1.3V		120		μA
I_{SD_VIN}	Shutdown current	EN=0V, VIN=4V		1		μA
V_{OUT}	VOUT operating range		4.5		13.5	V
V_{FB}	Reference voltage at FB pin			1.2		V
G_M	Error amplifier trans-conductance(Note4)	FB=1.2V, COMP=1.5V		190		μS
I_{SOURCE}	COMP pin source current			30		μA
I_{SINK}	COMP pin sink current			30		μA
G_{CS}	COMP to current gain(Note4)			10		S
R_{ONLS}	Low side NFET on-resistance	IDS=0.5A		12		mΩ
R_{ONHS}	High side NFET on-resistance	IDS=0.5A		15		mΩ
I_{LKLS}	Low side FET leakage current	VSW=12V		4		μA
I_{LKHS}	High side FET leakage current	VBUS=12V, VSW=0V		1		μA
V_{BST}	High side driver supply voltage	BST-SW		5		V
V_{ILIM}	Reference voltage at ILIM			0.5		V

I_{LIM}	Peak LS NFET current limit	RLIM=75k Ohm, Ilimit=750K/RSET		10		A
		RLIM=150k Ohm, Ilimit=750K/RSET		5		A
f_{SW}	Switching frequency	R_{FREQ}=300k		500		kHz
t_{on_min}	Minimum LSFET on time(Note4)			250		ns
t_{off_min}	Minimum HSFET on time(Note4)			335		ns
V_{EN_H}	EN high threshold voltage	EN > V_{EN_H}, enable IC after t_{EN_ON}		1.2		V
V_{EN_L}	EN low threshold voltage	EN < V_{EN_L}, shutdown IC		1.0		V
I_{EN}	EN input current	VEN=1.3V		500		nA
$T_{STARTUP}$	FB Soft Startup time			4		mS
T_{SD}	Thermal shutdown temperature			150		°C
T_{SD_HYS}	Thermal shutdown hysteresis temperature			20		°C

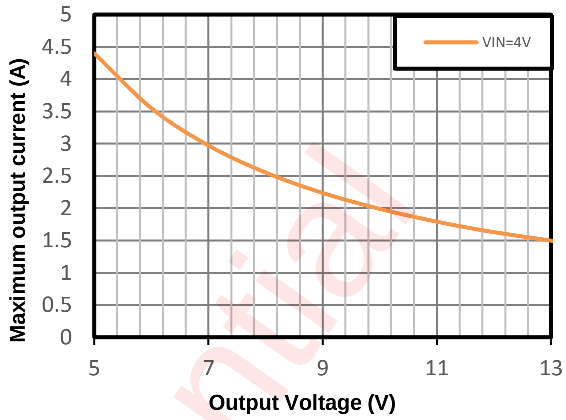
Note4：Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTICS

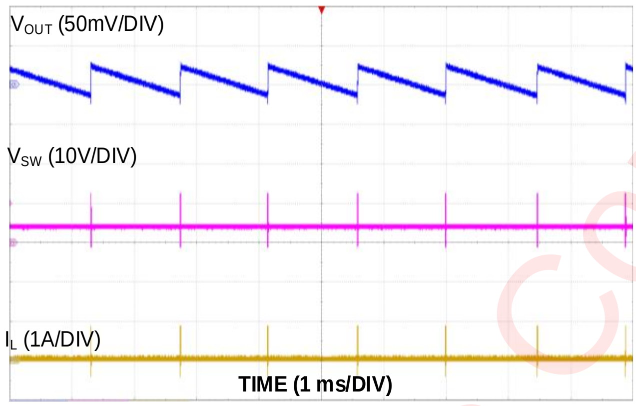
T_A=25°C , V_{IN}=4V, V_{OUT}=12V, C_{OUT} = 22 μF*3, L=2.2μH, Fs=500kHz, unless otherwise noted .



Efficiency vs Output Current

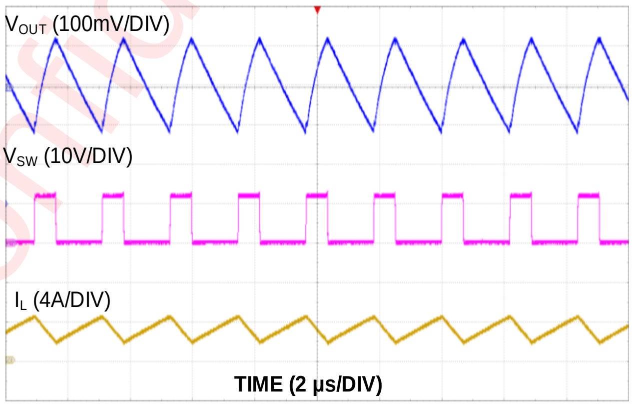


Maximum Output Current vs Output Voltage



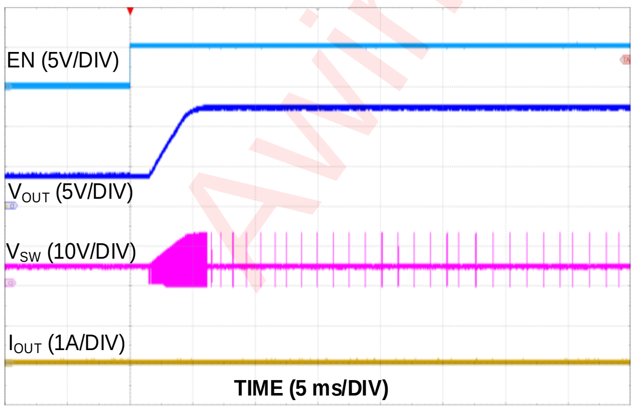
VIN = 4V VOUT = 12V IOUT = 0A

Output Ripple



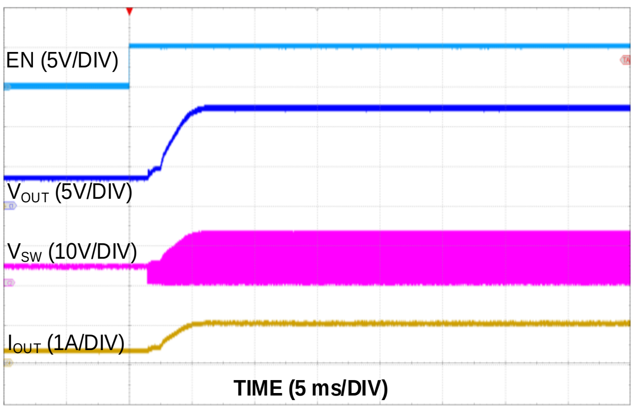
VIN = 4V VOUT = 12V IOUT = 1A

Output Ripple



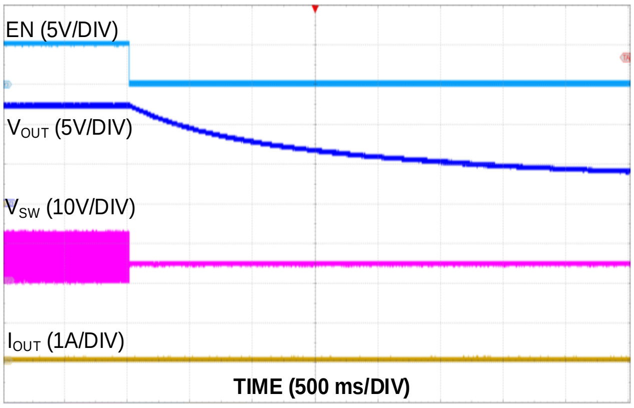
VIN = 4V VOUT = 12V IOUT = 0A

Startup from EN



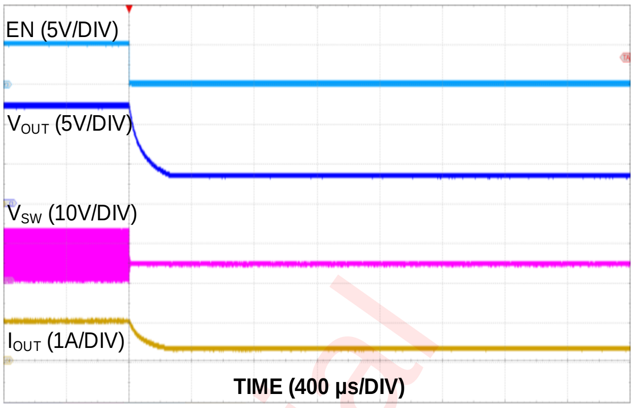
VIN = 4V VOUT = 12V IOUT = 1A

Startup from EN



V_{IN} = 4V V_{OUT} = 12V I_{OUT} = 0A

Shutdown from EN



V_{IN} = 4V V_{OUT} = 12V I_{OUT} = 1A

Shutdown from EN

Detailed Functional Description

Overview

The AWP36210 is a synchronous boost converter designed for delivering the switch peak current up to 10A and output voltage up to 13.5 V. AWP36210 has an internal feature to help improving light load efficiency. When output current is low, AWP36210 will go into DCM mode.

The AWP36210 provides the excellent line and load transient response with the minimal output capacitor. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The AWP36210 supports the adjustable switching frequency up to 2MHz. The device implements a programmable cycle-by-cycle current limit to protect the device from overload during the boost operation phase.

Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage exceeds 2.7 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.5 V and 2.7 V.

Enable and Disable

When the input voltage is above UVLO rising threshold of 2.7 V and the EN pin is pulled high above 1.2 V, the AWP36210 is enabled. When the EN pin is pulled below 1 V, the AWP36210 goes into the shutdown mode and stops switching.The device stops switching in shutdown mode and consumes less than 3-μA current. Because of the body diode of the high-side rectifier FET, the input voltage goes through the body diode and appears at the VOUT pin at shutdown mode.

Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, the AWP36210 starts to ramp up the output voltage.

After the turn-on phase ends (typical 4 ms), The AWP36210 regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 4 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges.

Adjustable Cycle-by-Cycle Switching Current Limit

The peak switch current limit can be set by a resistor connecting with the ILIMIT pin. The relationship between the current limit and the resistor is determined by Equation 1

$$R_{LIMIT} = \frac{750}{I_{LIMIT}} \tag{1}$$

Where RLIMIT is the resistor for setting the current limit, with the unit of kΩ, ILIMIT is switching peak current limit, with the unit of A. For instance, when the resistor value is 75 kΩ, the switch peak current limit is 10 A.

Adjustable Switching Frequency

The AWP36210 features of a wide adjustable switching frequency ranging up to 2MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin. This pin cannot be left floating in the application. Use Equation 2 to calculate the resistor value for a desired frequency.

$$\frac{1}{\text{Freq}} = T_{SW} = R_{Freq} \times 6 \times 10^{-6} + 2 \times 10^{-4} \quad (2)$$

Where RFreq is the resistor for setting the frequency, with the unit of kΩ, Freq is switching frequency, with the unit of kHz. For instance, when the resistor value is 300 kΩ, the switching frequency is 500 kHz.

Bootstrap Voltage (BST)

The AWP36210 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100 nF. A ceramic capacitor with an X5R or X7R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C(typical).

Device Functional Modes

AWP36210 operates at the adaptive constant off time peak current mode control (CMCOT). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the adaptive off timer end or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

Application Information

Setting the switching Frequency

The switching frequency of the AWP36210 is set at 500 kHz. Use Equation 2 to calculate the required resistor value. For a target switching frequency of 500 kHz, The calculated value is 300 kΩ.

Setting the Cycle-By-Cycle Current Limit

The current limit of the AWP36210 could be programmed by an external resistor. Use Equation 1 to calculate the required resistor value. For a target current limit of 10 A, the calculated resistor value is 75 kΩ.

Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. If R1=200k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

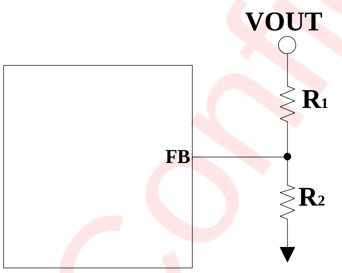


Figure 4 Setting the Output Voltage

Selecting the Inductor

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{0.4 \times F_{SW} \times I_{OUT\_MAX}} \quad (4)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

AWP36210 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT\_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{2 \times F_{SW} \times L} \quad (5)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Selecting the Maximum Output current

Under different conversion ratios, the maximum load capability should follow the guidelines in Figures 5 and 6. Exceeding the recommended current may cause chip damage.

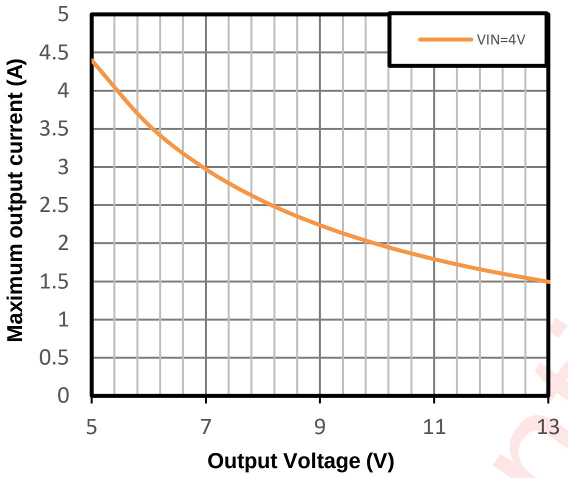


Figure 5 Maximum Output Current vs Output Voltage

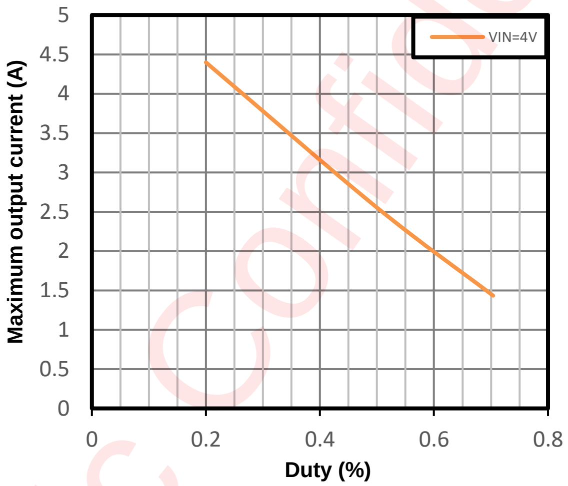


Figure 6 Maximum Output Current vs Duty

Selecting the Output Capacitors

The Boost Output capacitor CBD and disconnection FET Output capacitor COUT are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken in to account when selecting these capacitors. It is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 44uF capacitors. Depending on the specific ripple and transient performance requirements, the output capacitance value should be appropriately increased to ensure compliance with design specifications.

Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22μF input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF was selected for this design example.

Selecting the VCC Capacitor

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of CVCC should be at least 10 times greater than the value of CBST, and should be a good quality, low ESR, ceramic capacitor. CVCC should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7 μF was selected for this design example.

PCB Layout Consideration

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems.

The checklist below is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di/dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;

2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling;

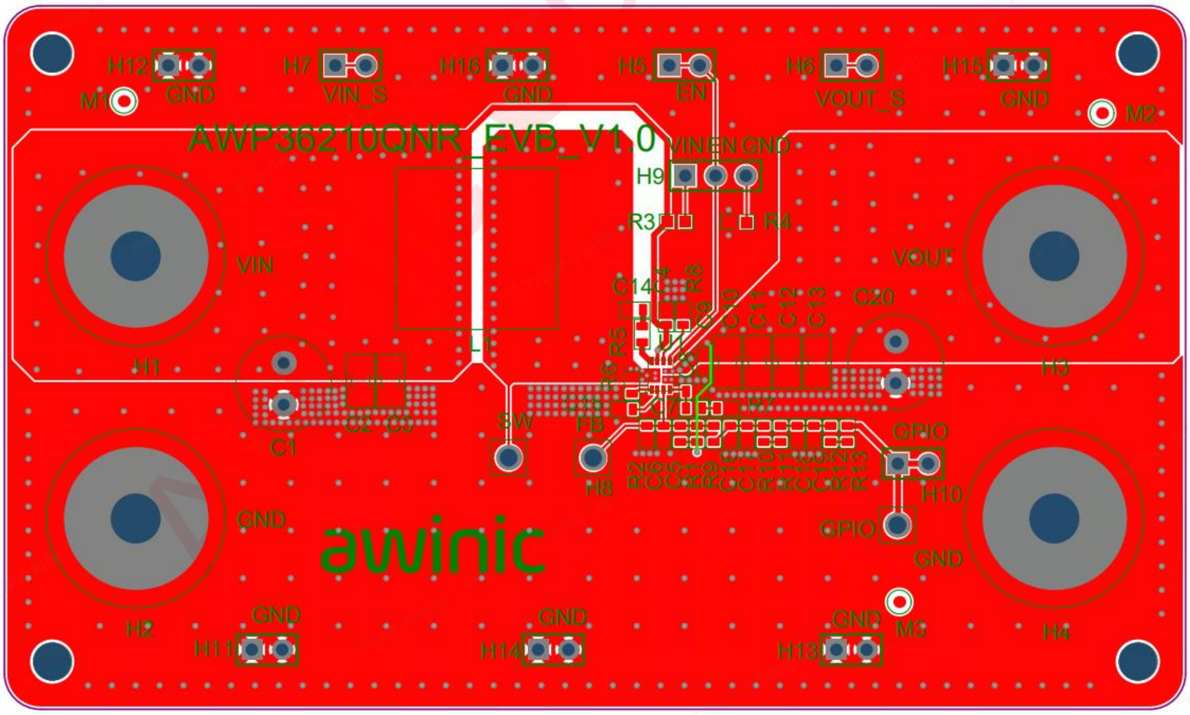
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise;

4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (e.g., VOUT, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation;

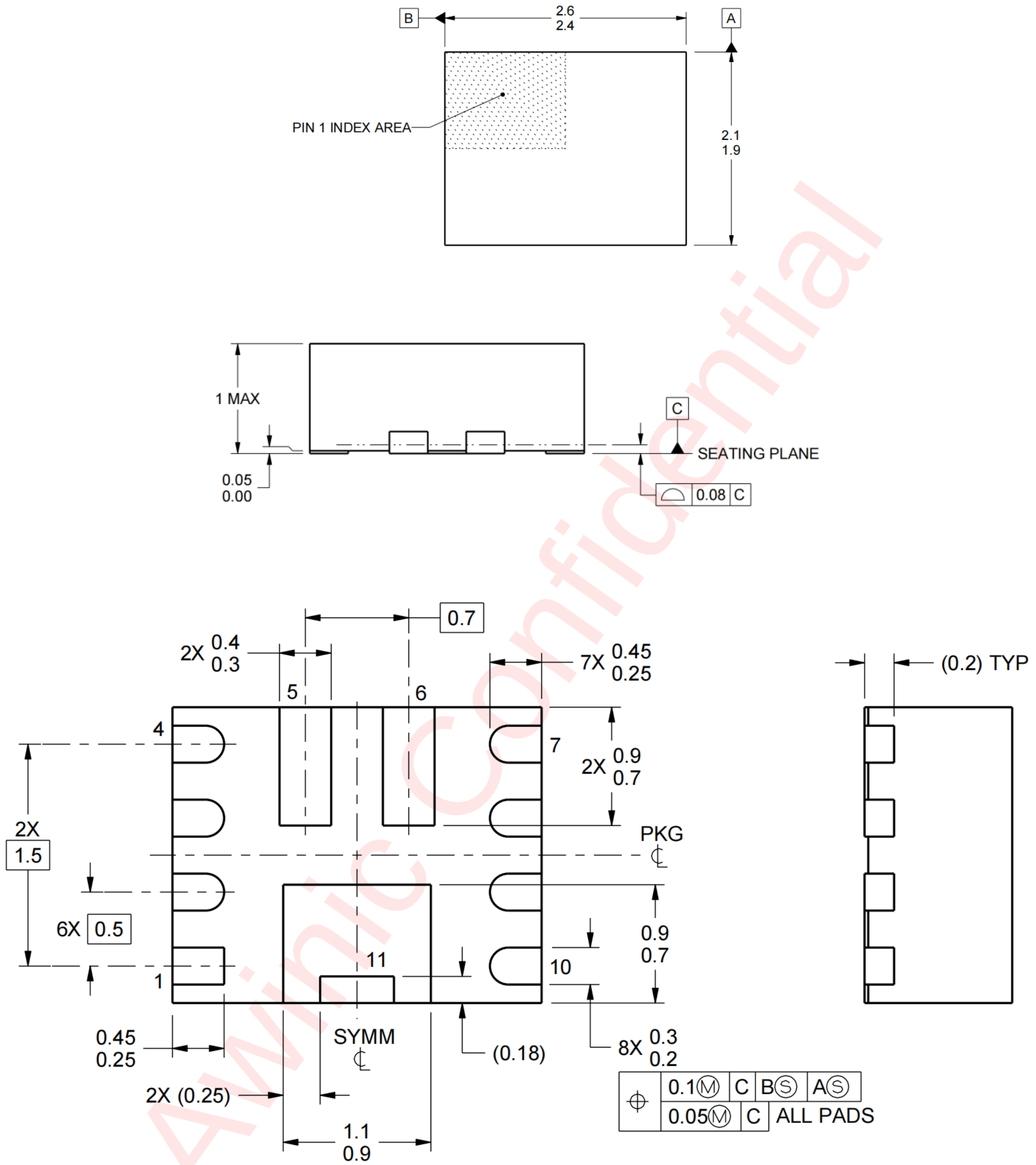
5. Place the input capacitor being close to the VIN pin and the PGND pin in order to reduce the input supply ripple;

6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace;

7. Use a separate ground trace to connect the feedback, compensation, frequency set, and the current limit set circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.



Package Description



Revision History

Version	Date	Change Record
V1.0	Aug. 2025	Officially released.
V1.1	Sep. 2025	Update *Overview.* (P9)
V1.2	Nov. 2025	1. Update *Typical Application Circuit*. (P1) 2.Update *Absolute Maximum Ratings*. (P4)

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.