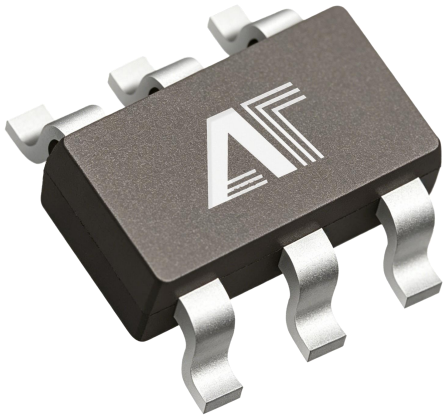
AOTE SEMICONDUCTOR



Single channel D-class trigger

SN74LVC1G175

Product Data Sheet

AOTE DCC
RELEASE

Summary :

The SN74LVC1G175 single channel D-class trigger can operate within a supply voltage range of 1.65V to 5.5V.

The SN74LVC1G175 device has asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is at high level, data from input pin (D) is transmitted to output pin (Q) on the rising edge of clock (CLK). When $\overline{CLR}$ is at a low level, Q will be forced to a low level regardless of the clock edge or data on D.

The device is packaged in SOT23-6 and SC70-6. The working temperature range is from -40°C to+125°C.

Product features

- Small Package: SOT23-6、SC70-6
- Working voltage range: 2.0V~5.5V
- Low power consumption: 0.1μA (typical value)
- Working temperature range: -40°C~+125°C
- Input voltage up to 5.5V
- High Output driver: When powered by3.0V,output driver±24mA
- Ioff supports live insertion, partial power-off mode, and reverse drive protection

Applications

- Enterprise Switch
- Telecommunications infrastructure
- Server
- Healthcare and Fitness
- PC/Laptop
- Motor driver

Packaging and Order Description

Product Name	Order Model	Temperature Range (℃)	boxed type	screen printing	MSL(3)	Packing Specification
SN74LVC1G175	SN74LVC1G175DCKR	-40℃ ~+125℃	SC70-6	D65	MSL3	Tape and Reel, 3000
	SN74LVC1G175DBVR	-40℃ ~+125℃	SOT23-6	C755	MSL3	Tape and Reel, 3000

Attention:

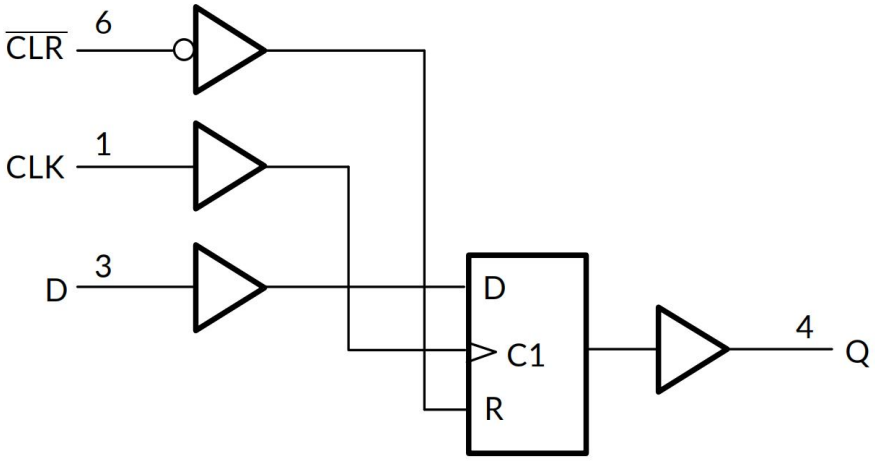
(1) This information is the latest data for the current version. If these data are updated, they will be promptly updated on our official website without further notice.

(2) Silk screen printing may have additional codes for internal control traceability of products (including data codes and supplier codes) or marking the place of origin.

(3) MSL, Humidity sensitivity level classified according to JEDEC industry standards.

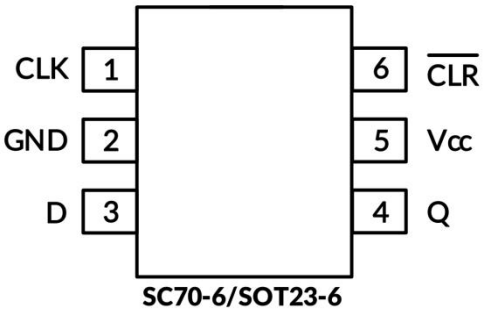
(4) equivalent SOT363

◆ Logic diagram (Positive Logic)



◆ On-product information:

• Footage image



Pin	Pin Name	I/O	Function Description
1	CLK	I	clock input
2	GND	P	grounding
3	D	I	data input
4	Q	O	data output
5	Vcc	P	power supply
6	$\overline{CLR}$	I	Clear data input

◆ Menu

Input			Output
$\overline{CLR}$	**CLK**	**D**	**Q**
H	↑	L	L
H	↑	H	H
H	H or L	X	Qo
L	↑	X	L

H=high level L=low level X=Irrelevant

◆ Absolute maximum rating Within the natural ventilation temperature range (unless otherwise specified)

	Parameter		Min	Max	Unit
VCC	Power supply voltage range		-0.5	6.5	V
VI	Input voltage range		-0.5	6.5	V
Vo	The voltage range applicable to any output under high impedance or power-off conditions		-0.5	6.5	V
Vo	The voltage range applicable to any output in either high or low level state		-0.5	VCC+0.5	V
IIK	Input clamp current V_I <0		-	-50	mA
IOK	Output clamp current V_O <0		-	-50	mA
IO	Continuous output current		-	±50	mA
	Continuous current through V_{CC} or GND		-	±100	mA
• current parameters					
θ JA	Thermal resistance to the environment	SOT23-6	-	230	°C/W
		SC70-6	-	265	
• current parameters					
temperature parameter	Junction temperature, TJ		-65	150	°C
	Storage temperature range, Tstg		-65	150	

◆ ESD level

The following ESD information is only applicable to sensitive equipment operated within an ti-static protection zones

_	nominal value	Unit
human model	±2000	V
Charged Device Model	±1000	
Mechanical Model	±200	

ESD sensitivity warning

The scope of ESD damage can range from minor performance degradation to complete equipment failure. Precision integrated circuits may be more susceptible to damage as very small parameter changes can result in devices not meeting their published parameter specifications.

Attention:

(1) This only represents the limit values obtained by the product under testing conditions, and does not mean that the product can work normally under these conditions or other parameter conditions beyond the specifications. Exceeding the range specified by the absolute maximum rated value above will cause damage to the product, and it is impossible to predict the working state of the product outside of the above conditions. If the product operates under conditions other than those mentioned above for a long time, it may affect its performance.

(2) If the input and output current ratings are followed, it may exceed the input and output negative voltage ratings.

(3) The value of VCC is provided in the recommended working condition table.

(4) The thermal impedance of the package is calculated according to JESD-51 standard:

(5) The maximum power consumption is a function of TJ (MAX), R θ JA, and TA. The maximum power consumption at any ambient temperature is Po=(TJ (MAX) - TA)/R θ JA, which is suitable for packaging directly soldered to PCB.

◆ Electrical Characteristics

Within the natural ventilation temperature range (typical test conditions are: TA=+25 ° C, full temperature=-40 ° C~125 ° C)

◆ Recommended working conditions

Parameter	Symbol	Test conditions	Min	Max	Unit
power supply voltage	Vcc	work	1.65	5.5	V
High level input voltage	V_{IH}	VCC =1.65V - 1.95V	0.75 x Vcc	-	V
		VCC=2.3V - 2.7V	1.7		
		VCC=3V - 3.6V	2		
		VCC=4.5V - 5.5V	0.7 x Vcc		
Low level input voltage	V_{IL}	VCC =1.65V - 1.95V	-	0.25 x Vcc	V
		VCC=2.3V- 2.7V		0.7	
		VCC=3V - 3.6V		0.8	
		VCC=4.5V - 5.5V		0.3 x Vcc	
input voltage	V_I	-	0	5.5	V
output voltage	V_O	-	0	Vcc	V
High level output current	I_{OH}	VCC =1.65V	-	-4	mA
		VCC=2.3V		-8	
		VCC=3V		-16	
				-24	
		VCC=4.5V		-32	
Low level output current	I_{OL}	VCC =1.65V	-	4	mA
		VCC=2.3V		8	
		VCC=3V		16	
				24	
		VCC=4.5V		32	
Input conversion up or down rate	t_r, t_f	V_{CC} =1.8±0.15V,2.5V±0.2V	-	20	ns/V
		VCC=3.3V ±0.3V		10	
		VCC=5V ±0.5V		10	
Working temperature range under natural ventilation conditions	T_A	-	-40	+125	℃

All unused input ports of the device must be kept at VCC or GND to ensure proper operation of the device

◆ DC characteristics

Parameter	Test conditions	Vcc	temperature	Min	Typ	Max	Unit
V_{OH}	I_{OH} = -100μA	1.65V-5.5V	Full temperature	VCC-0.1	-	-	V
	I_{OH} = -4mA	1.65V		1.2			
	I_{OH} = -8mA	2.3V		1.9			
	I_{OH} = -16mA	3V		2.4			
	I_{OH} = -24mA			2.3			
	I_{OH} = -32mA	4.5V		3.8			
V_{OL}	I_{OH} = 100μA	1.65V-5.5V	Full temperature	-	-	0.1	V
	I_{OH} = 4mA	1.65V		-	-	0.45	
	I_{OH} = 8mA	2.3V		-	-	0.3	
	I_{OH} = 16mA	3V		-	-	0.4	
	I_{OH} = 24mA			-	-	0.55	
	I_{OH} = 32mA	4.5V		-	-	0.55	
I_I Data or control input	V_I =5.5V orGND	0V - 5.5V	+25°C Full temperature	-	±0.1	±5	μA
I_{off}	V_I or V_O=5.5V	0V	+25°C Full temperature	-	±0.1	±10	μA
I_{CC}	V_I =5.5V or GND, I_O=0	1.65V - 5.5V	+25°C Full temperature	-	0.1	10	μA
Δ_{ICC}	One input at Vcc-0.6V, Other inputs at VCC or GND	3V - 5.5V	Full temperature	-	-	500	μA
C_i Input capacitance	V_I =Vcc orGND	3.3V	+25°C	-	4	-	pF

(1) All unused input ports of the device must be kept at VCC or GND to ensure proper operation of the device.

(2) The limit value is 100% production testing conducted at 25°C. Ensure the limitation of the working temperature range by utilizing the correlation of statistical quality control (SQC) methods.

(3) Typical values represent the most likely parameter specifications determined during characterization. The actual typical values may vary over time and will also depend on the application and configuration.

◆ timing requirements Within the natural ventilation temperature range

Parameter	input	output	temperature	Vcc=1.8V ±0.15V		Vcc =2.5 V±0.2V		Vcc =3.3V ±0.3V		Vcc =5V ±0.5V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
f_{clock}	-		-40°C to 85°C	-	30	-	65	-	100	-	155	MHz
			-40°C to 125°C	-	-	-	-	-	100	-	155	
t_w	CLK High or low		-40°C to 85°C	8	-	4	-	3	-	2	-	ns
			-40°C to 125°C	-		-	-	3		2		
	$\overline{CLR}$ low		-40°C to 85°C	12		5	-	3.4		2		
			-40°C to 125°C	-		-	-	3.4		2		
t_{su}	Data		-40°C to 85°C	10.4	-	4.6	-	3.2	-	2	-	ns
			-40°C to 125°C	-		-	-	3.2		2		
	$\overline{CLR}$ inactive		-40°C to 85°C	8.4		3.8	-	2.6		1.8		
			-40°C to 125°C	-		-	-	2.6		1.8		
t_h			-40°C to 85°C	0.5	-	0.5	-	0.5	-	0.5	-	ns
			-40°C to 125°C	-		-	-	0.5	-	0.5		

This parameter is ensured by design and/or characteristics and has not been tested in production

◆ Switch characteristics

Within the natural ventilation temperature range (typical test conditions are): CL=15pF

Parameter	input	output	temperature	Vcc=1.8V ±0.15V		Vcc =2.5 V±0.2V		Vcc =3.3V ±0.3V		Vcc =5V ±0.5V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
f_{max}	-		-40°C to 85°C	30	-	65	-	100	-	155	-	MHz
t_{pd}	CLK		-40°C to 85°C	2.5	25.5	2	13	1.4	9.5	1	7	ns
	$\overline{CLR}$		-40°C to 125°C	2.5	23	2	10	1.2	9.7	1	6	

This parameter is ensured by design and/or characteristics and has not been tested in production

◆ Job characteristics

Within the natural ventilation temperature range (typical test conditions are) : CL=30pF or 50pF

Parameter	Input	output	temperature	Vcc=1.8V ±0.15V		Vcc =2.5 V±0.2V		Vcc =3.3V ±0.3V		Vcc =5V ±0.5V		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
f_{max}	-		-40°C to 85°C	30	-	65	-	100	-	155	-	MHz
t_{pd}	CLK	Q	-40°C to 85°C	2.7	27.5	2.2	14.1	1.6	11	1.5	8.2	ns
			-40°C to 125°C	2.7	28.3	2.2	15	1.6	11.5	1.5	9	
	$\overline{CLR}$	Q	-40°C to 85°C	2.7	24.5	2.2	11	1.5	9	1.3	7	
			-40°C to 125°C	2.7	25	2.2	12	1.5	9.5	1.3	7.5	

This parameter is ensured by design and/or characteristics and has not been tested in production

◆ Job characteristics

TA=25°C

Parameter		Test conditions	V_{CC} =1.8V Typ	V_{CC} =2.5V Typ	V_{CC} =3.3V Typ	V_{CC} =5V Typ	Unit
Cpd	Powerconsumption capacitor	f=10MHz	12	16	21	24	pF

◆ Typical parametric curves

Note: The charts and tables provided later in this document are statistical summaries based on a limited number of samples and are for reference only.
Unless otherwise specified, the testing conditions are TA=+25 ° C.

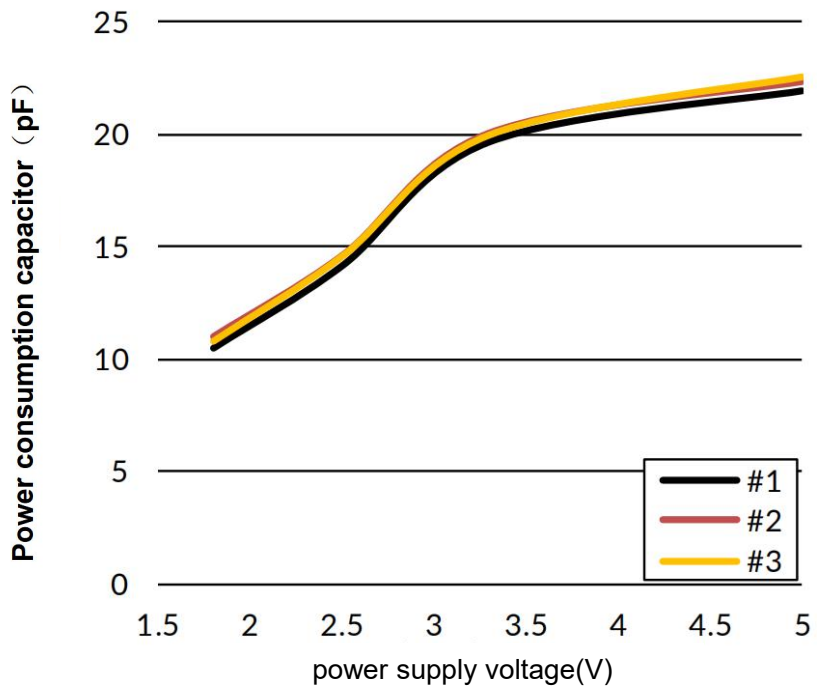
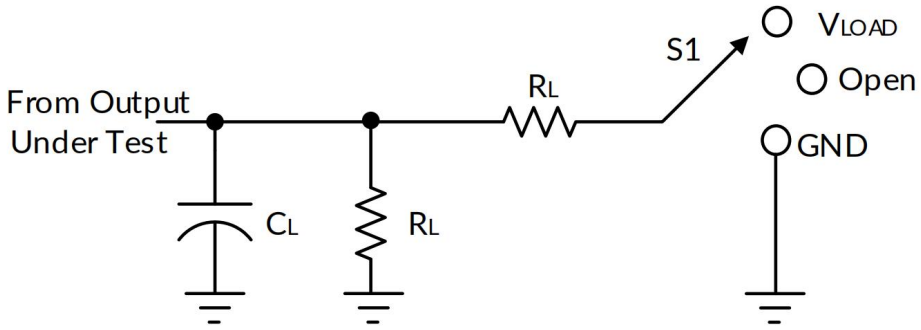


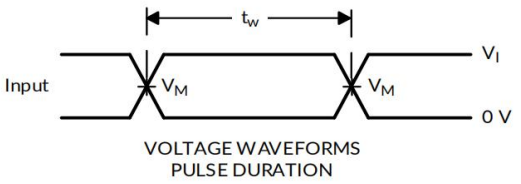
Figure 1. Relationship between voltage and capacitance

◆ Parameter measurement information

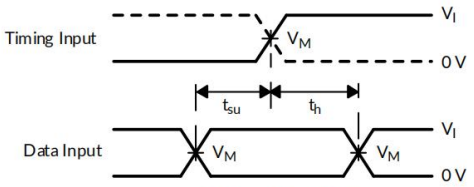


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

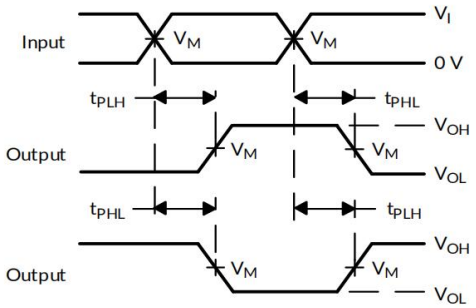
VCC	INPUTS		VM	VLOAD	CL		RL		VΔ
	VI	tr/tf							
1.8V±0.15V	VCC	≤2ns	VCC/2	2 x VCC	15pF	30pF	1KΩ	1KΩ	0.15V
2.5V±0.2V	VCC	≤2ns	VCC/2	2 x VCC	15pF	30pF	1KΩ	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	15pF	30pF	1KΩ	500Ω	0.3V
5V±0.5V	VCC	≤2.5ns	VCC/2	2 x VCC	15pF	30pF	1KΩ	500Ω	0.3V



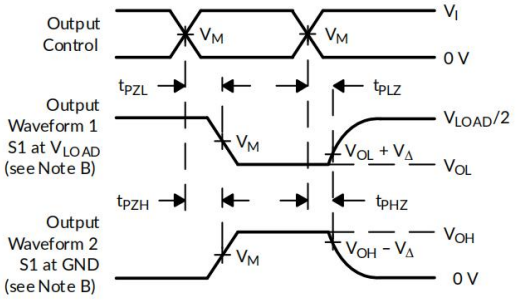
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

Note: A.CL includes probe and fixture capacitors.
B. Waveform 1 is used for outputs with internal conditions, where the output is low unless disabled by the output controller. Waveform 2 is used for outputs with internal conditions, where the output is high unless disabled by the output controller.
C. All input pulses are provided by a generator with the following characteristics: PRR≤10MHz, Zo=50Ω
D. Output one measurement at a time, with a transition for each measurement.
E. T_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. T_{PZL} and t_{PZH} are the same as t_{en}.
G. T_{PLH} and t_{PHL} are the same as t_{pd}.
H.Not all parameters and waveforms are applicable to all devices.

◆ Detailed description

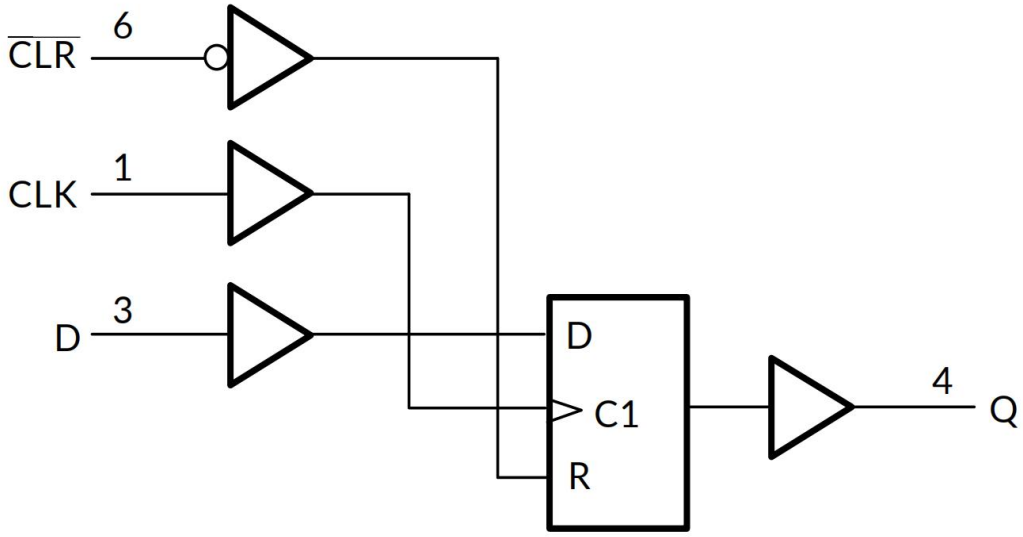
Overview:

The SN74LVC1G175 single-channel D flip-flop can operate within a supply voltage range of 1.65V to 5.5V.

The SN74LVC1G175 device features an asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is high, data from the input pin (D) is transmitted to the output pin (Q) on the rising edge of the clock (CLK). When $\overline{CLR}$ is low, Q is forced to a low level regardless of the clock edge or data at D.

This device can be used in I_{off} power-off applications. When powered off, the I_{off} circuit disables the output to prevent backflow current from damaging the device.

Functional Block Diagram



Feature Description

The SN74LVC1G175 device features a wide operating voltage range of 1.65V to 5.5V, supports voltage-level shifting with a step-down configuration, and allows input voltage presence even when Vcc=0V.

Application and Design

Multiple SN74LVC1G175 devices can be used in series to create shift registers of any length. In this example, we use four SN74LVC1G175 devices to form a 4-bit serial shift register. By connecting all CLK inputs to a common clock pulse and connecting each output of one device to the next, we can store and load 4-bit values as needed. We demonstrated loading a 4-bit value of 1101 into memory by setting serial input data to each required memory bit, and by sending clock pulses to each bit, we sequentially moved all stored bits from left to right (A → B → C → D)

Typical applications:

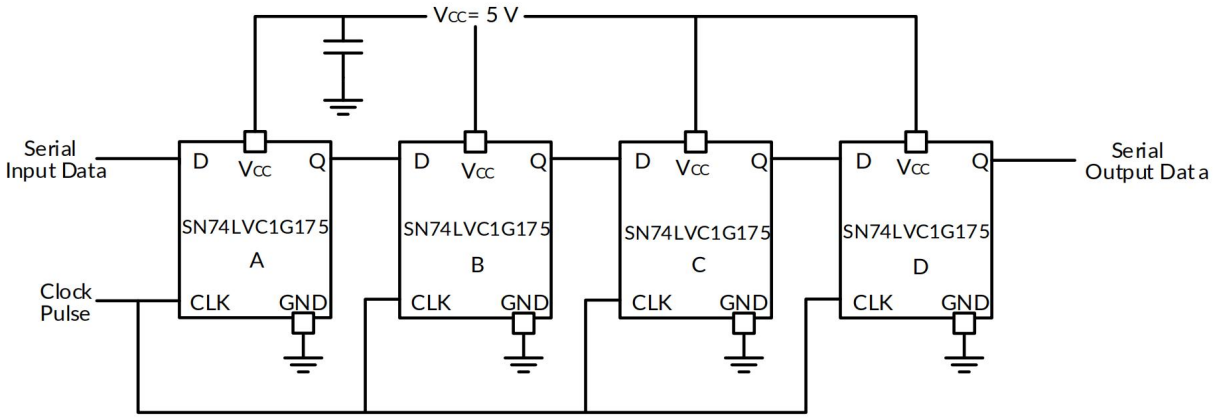


Figure 3.4 Bit Serial Shift Register

Table 1. Stored Data Values

Serial input data	Storage A	Storage B	Storage C	Storage D
1	0	0	0	0
0	1	0	0	0
1	0	1	0	0
1	1	0	1	0
0	1	1	0	1

Design requirements:

SN74LVC1G175 adopts CMOS technology and has balanced output driving capability. It is necessary to strictly avoid bus contention, as this may result in driving currents exceeding the rated limit. SN74LVC1G175 allows the use of digital control signals to store digital signals. To achieve optimal performance, the input signal should be strictly maintained around 0V or Vcc.

Power recommendations

The power pins should be equipped with good bypass capacitors to prevent power interference. For devices powered by a single power source, it is recommended to use a 0.1F capacitor; For devices with multiple VCC pins, it is recommended to use capacitors with 0.01 μ F or 0.022 μ F for each power pin. Multiple bypass capacitors can be connected in parallel to suppress noise of different frequencies. Usually, capacitors with 0.1 μ F and 1 μ F are used in parallel. The bypass capacitor should be installed as close as possible to the power supply pin.

◆ PCB layout design

Precautions for PCB layout design:

When using multi bit logic devices, the input pins should not be suspended. In practical applications, some functions of digital logic devices are often idle, such as using only two inputs from the three input gate or enabling only three gates from the four buffer gate. These unused input pins should not be left hanging, as undefined external connection point voltage will cause abnormal device operation. The following specifies the rules that must be followed in all situations. All idle input pins must be connected to a high or low bias to eliminate the risk of floating. The specific logic level that needs to be applied to the idle pin depends on the device's functional characteristics. The conventional approach is to connect it to GND or VCC, depending on the actual convenience.Unless the device is a transceiver, the output terminal can be suspended. If the transceiver has an output enable pin, the output part of the device will be disabled when the pin is active. This does not disable the input part of the I/O port, so when the output is disabled, the input end is also prohibited from floating.

PCB layout diagram:

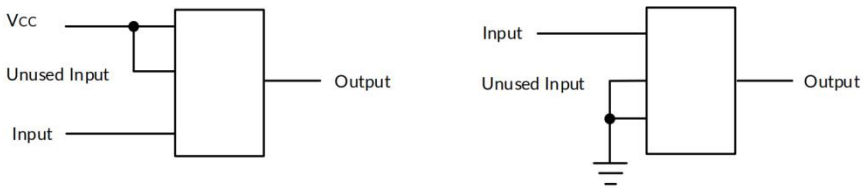
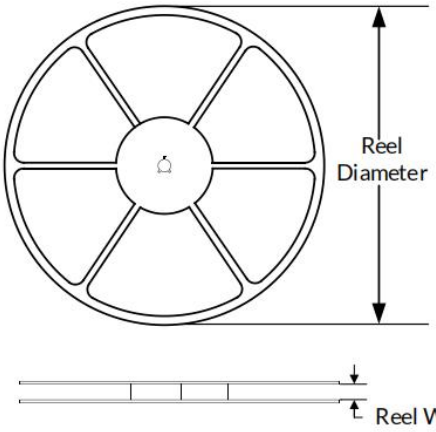


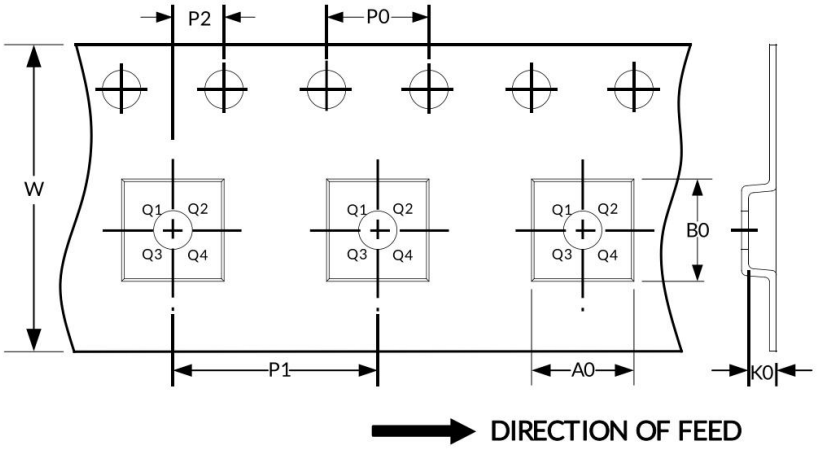
Figure 4. PCB layout diagram

◆ Packaging specifications size

REEL DIMENSIONS



TAPE DIMENSION



Attention: The pictures are for reference only. Please use the physical object as the standard

◆ Key parameter table

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-6	7″	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

Attention:
All dimensions are nominal sizes.
Excluding plastic wrap or metal protrusions with a maximum of 0.15 millimeters on each side.

◆ Packaging specifications and dimensions

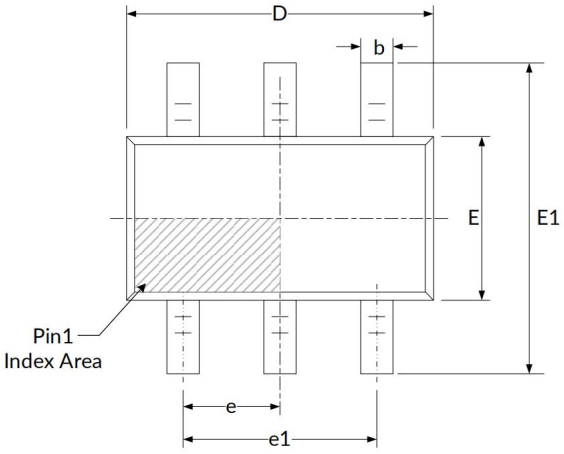
Attention:

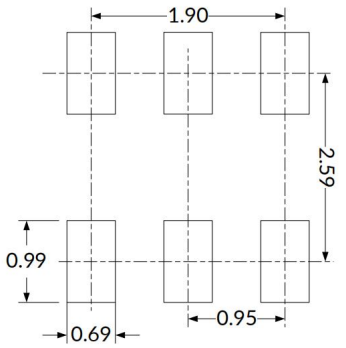
1、Excluding plastic wrap or metal protrusions with a maximum of 0.15mm on each side.

2、BSC (Basic Center Spacing), where the "basic" spacing is the nominal spacing.

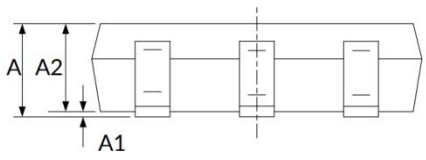
3、This image is subject to change without prior notice

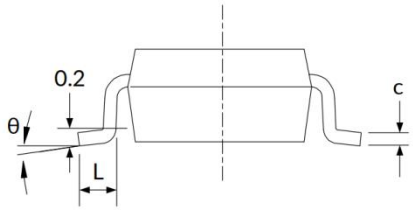
SOT23-6





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions (in millimeters)		Dimensions (in inches)	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

◆ Packaging specifications and dimensions

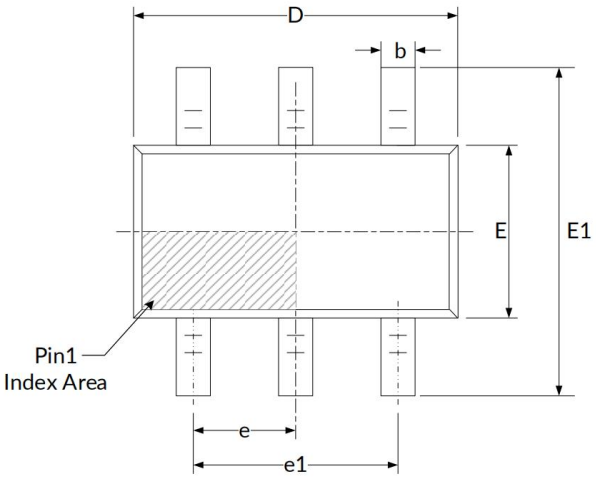
Attention:

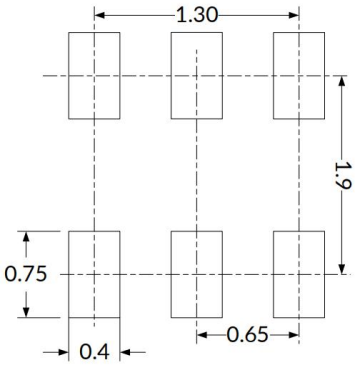
1、Excluding plastic wrap or metal protrusions with a maximum of 0.15mm on each side.

2、BSC (Basic Center Spacing), where the "basic" spacing is the nominal spacing.

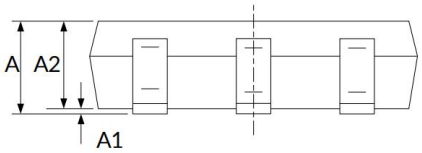
3、This image is subject to change without prior notice

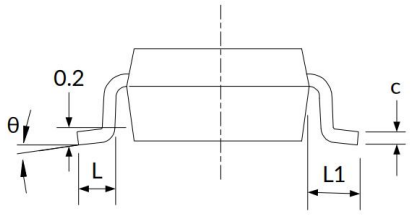
SC70-5





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions (in millimeters)		Dimensions (in inches)	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 (BSC)		0.026 (BSC)	
el	1.300 (BSC)		0.051 (BSC)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

◆ Attention

- AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.
- Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.
- Contact technical support for customized validation in critical applications (medical devices, industrial control).
- This document is valid until December 31, 2026 Updates will be notified on the official website.
- For further clarification on technical specifications or application solutions, please contact us through official channels: