

1.5A Ultra Low Dropout Linear Regulator with Bias

Features

- Input voltage range: 0.5 to 5.5V
- Bias voltage range: 2.5V to 5.5V
- Adjustable and Fixed Voltage Version Available (0.5V to 3.5V)
- Output Voltage Accuracy: $\pm 0.5\%$ @ 25°C
 $\pm 1\%$ @ Full Temperature
- Very Low Bias Input Current: typical 32 μ A
- Very Low Bias Input Current in Shutdown: <1 μ A
- Low dropout voltage: typical 85mV@1.5A(1.2V output)
- High PSRR: typical 70dB @ 1kHz($I_{OUT}=150$ mA, 1.2V output)
- Noise: typical 72 μ Vrms ($I_{OUT}=30$ mA, BW=10Hz to 100kHz, 1.2V output)
- 1.2V Logic Level Enable Input for ON/OFF Control
- Built-in Output Short Protection: Typical 0.8A
- Fast Load Transient Response
- Thermal Shutdown Protection
- FOWLP 1.200mmX0.800mmX0.300mm-6B package

Applications

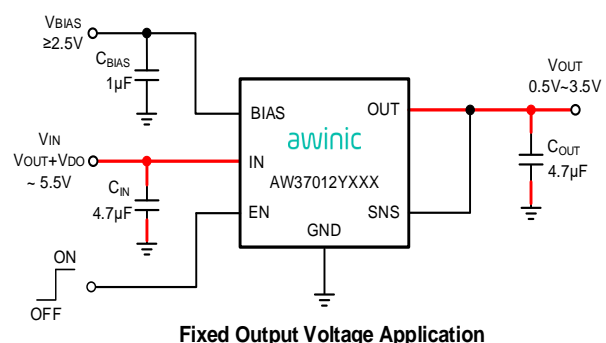
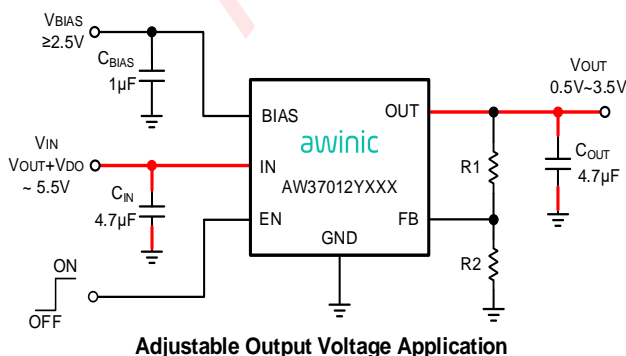
Battery-powered equipment

Smart phone

Digital camera, STB

Other portable electronic device

Typical Application Circuit



General Description

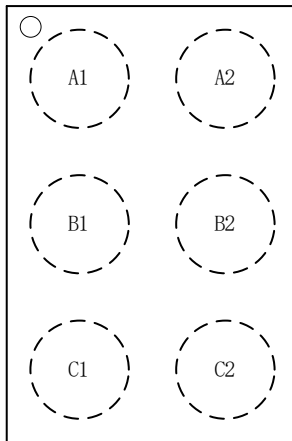
AW37012DXXX is a high accuracy voltage regulator, which provides 1.5A of current. It is equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The feature of ultra low dropout voltage is ideal for applications where output voltage is very close to input voltage. AW37012DXXX also features low IQ consumption, high PSRR, low Noise, good load transient response and smooth soft-start.

AW37012DXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

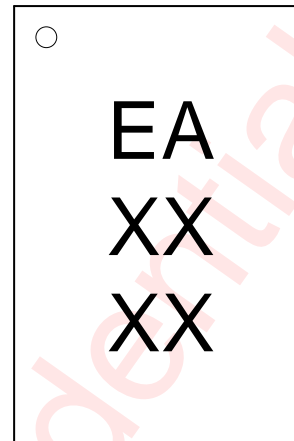
AW37012DXXX is designed to work with a 4.7 μ F or more input ceramic capacitor, a 1 μ F or more bias ceramic capacitor and a 4.7 μ F or more output ceramic capacitor. The low power dissipation and good dynamic response make AW37012DXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Pin Configuration And Top Mark

**AW37012DADJFOR
(Top View)**



**AW37012DADJFOR Marking
(Top View)**



EA – AW37012DADJFOR

XX/XX – Production Tracing Code

Pin Definition

No.	NAME	DESCRIPTION
A1	OUT	Regulated output voltage pin. Put a 4.7 μ F or more ceramic capacitor at the output pin.
A2	IN	Input supply pin. Put a 4.7 μ F or more bypass capacitor at the power supply.
B1	FB (ADJ devices)	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
	SNS (Fix Volt devices)	Output voltage Sensing Input. Connect to V_{OUT} on the PCB to output the voltage corresponding to the part version.
B2	EN	Chip enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground.
C2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit. Put a 1 μ F or more ceramic capacitor at the bias pin.

Functional Block Diagram

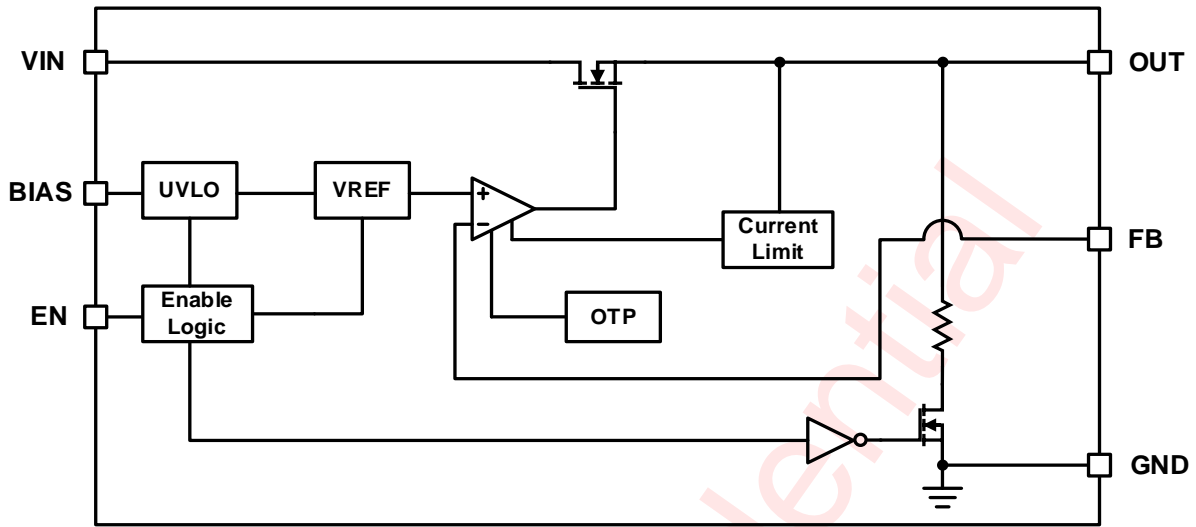


Figure 1 V_{OUT} Adjustable Version

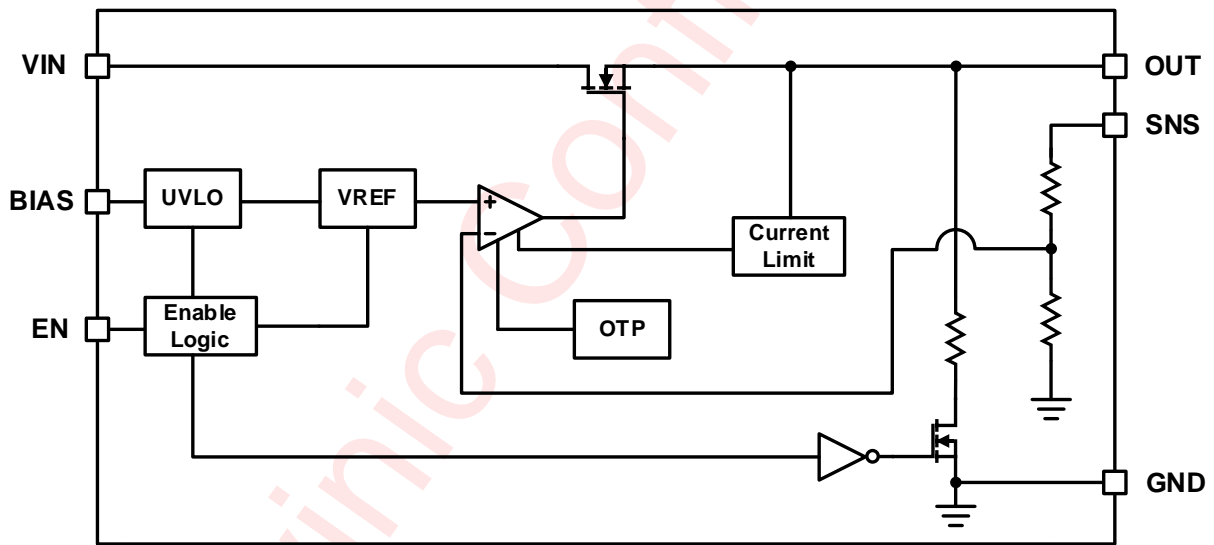


Figure 2 V_{OUT} Fixed Version

Typical Application Circuit

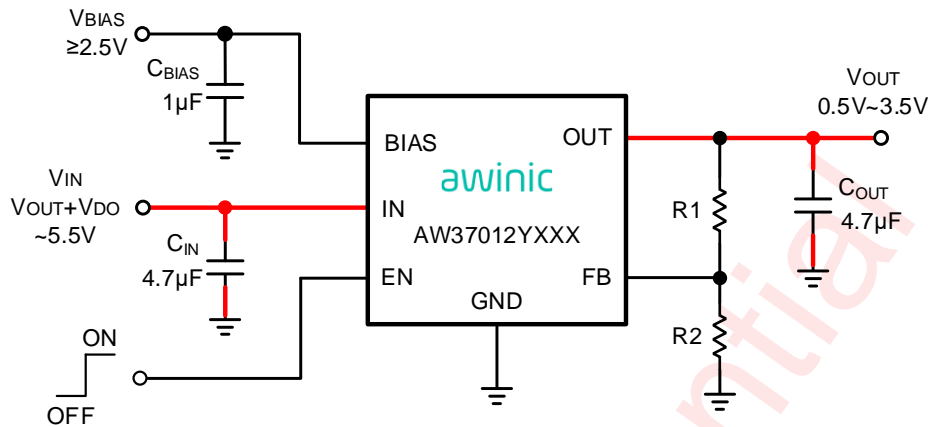


Figure 3 AW37012DXXX Adjustable Version Application Circuit

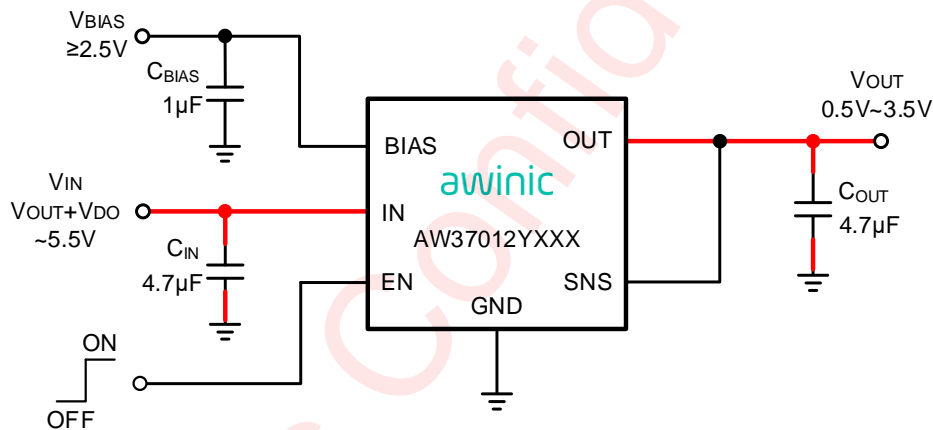


Figure 4 AW37012DXXX Fixed Version Application Circuit

Notice for typical application circuits:

A ceramic capacitor has different temperature characteristics and bias dependencies depending on the size, manufacture or part number of a capacitor. Careful evaluation is required. For adjustable voltage versions, when the V_{OUT} is $>3.0V$, the effective capacitance of C_{OUT} is greater than $4.7\mu F$, and a $10\mu F$ or more C_{OUT} is recommended.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37012DADJFOR	$-40^{\circ}C \sim 85^{\circ}C$	FOWLP 1.200mmX0.80 0mmX0.300mm -6B	EA	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Input voltage range	-0.3V to 6.0V
BIAS voltage range	-0.3V to 6.0V
Enable control voltage range	-0.3V to 6.0V
Output voltage range	-0.3V to $(V_{IN}+0.3V) \leq 6.0$
Maximum operating junction temperature T_{J_MAX}	150°C
Operating free-air temperature range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
Junction-to-ambient thermal resistance θ_{JA} ^(NOTE2)	101.8°C/W
ESD	
HBM (Human body model) ^(NOTE3)	±2kV
CDM(Charged device model) ^(NOTE4)	±1.5kV
Latch-Up	
Latch-Up ^(NOTE5)	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient follows JEDEC 2S2P standards, and is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: JS-001:2023.

NOTE4: All pins. Test Condition: JS-002:2022.

NOTE5: Test Condition: JESD 78F.02: 2023.

Electrical Characteristics

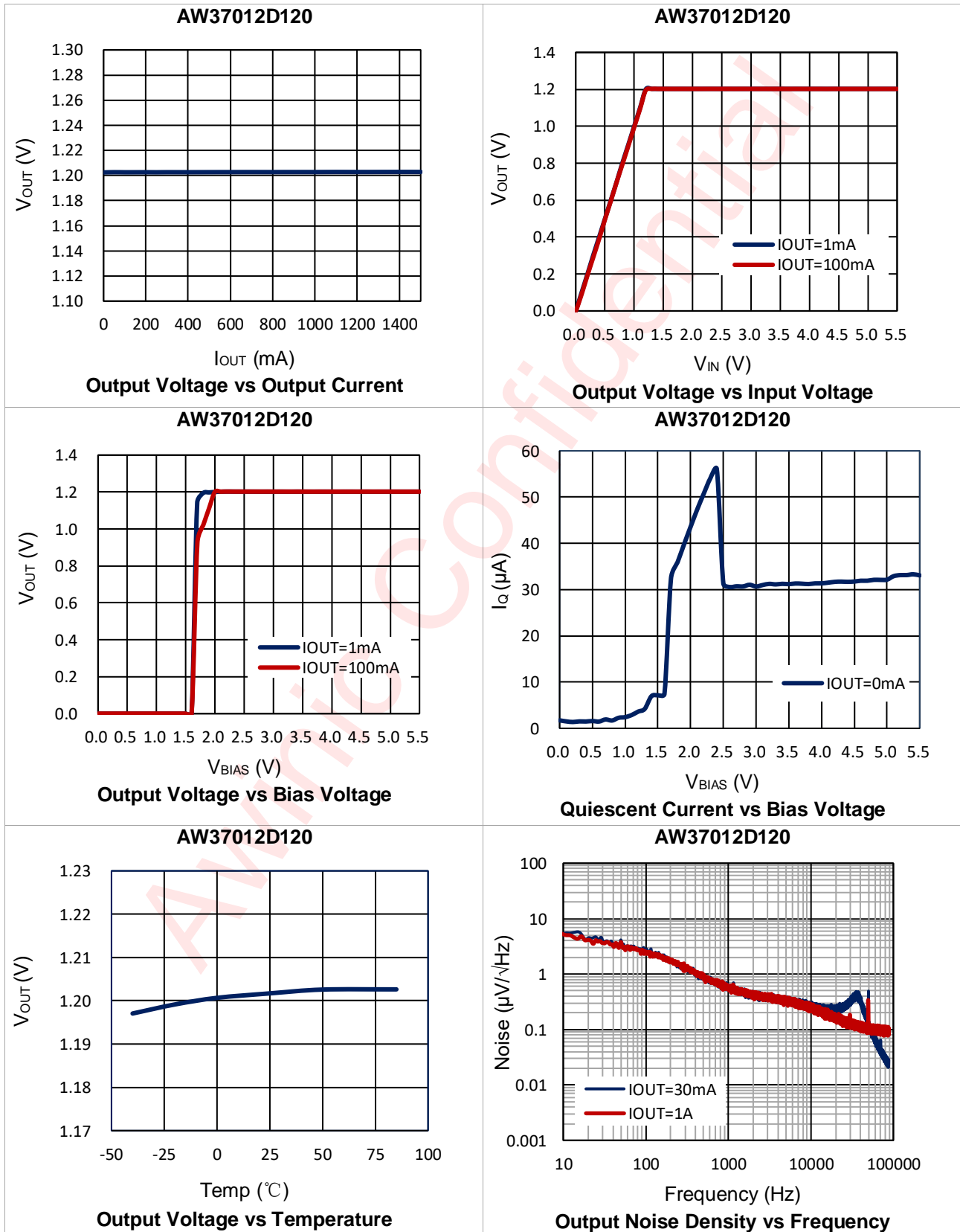
$V_{BIAS}=2.5V$ or $V_{BIAS} \geq V_{OUT}+1.6V$, and $V_{IN}=V_{OUT(SET)}+0.3V$, $I_{OUT}=1mA$, $C_{IN}=4.7\mu F$, $C_{OUT}=4.7\mu F$, $C_{BIAS}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		$V_{OUT}+V_{DO}$		5.5	V
V_{BIAS}	BIAS Voltage Range		2.5		5.5	
V_{UVLO}	Under-Voltage Lockout	V_{BIAS} Rising		1.65		V
		Hysteresis		0.1		
V_{FB}	Reference Voltage		0.497	0.5	0.503	V
V_{OUT_ACC}	Output Voltage Accuracy	$T_A=25^\circ C$	-0.5		0.5	%
		$-40^\circ C \leq T_A \leq 85^\circ C$	-1		1	
$LINE_{Reg}$	V_{IN} Line Regulation	$V_{OUT}+0.3V \leq V_{IN} \leq V_{BIAS}$		0.1		mV
	V_{BIAS} Line Regulation	$2.5V$ or $(V_{OUT} + 1.6 V) \leq V_{BIAS} \leq 5.5 V$		0.1		mV
$LOAD_{Reg}$	Load Regulation	$I_{OUT} = 1mA$ to $1.5 A$		1		mV
I_{FB}	FB Pin Operating Current	$V_{FB}=0.5V, V_{EN}=V_{BIAS}=3.0V$		0.01		μA
I_{Q_BIAS}	Bias Pin Quiescent Current	$V_{BIAS}=3V, I_{OUT}=0mA$		32		μA
I_{SD_BIAS}	Bias Pin Shutdown Current	$V_{EN}<0.36V$		0.01	1	μA
V_{IN_DO}	V_{IN} Dropout Voltage	$V_{BIAS}=3.0V, V_{OUT}=1.2V$ $I_{OUT}=1.5A,$ $V_{OUT}=98\%*V_{OUT(SET)}$		85		mV
V_{BIAS_DO}	V_{BIAS} Dropout Voltage	$V_{IN}=V_{BIAS}, V_{OUT}=1.2V$ $I_{OUT}=1.5A,$ $V_{OUT}=98\%*V_{OUT(SET)}$		0.86		V
V_{ENH}	EN Threshold Voltage	EN Input Voltage "H"	0.84			V
V_{ENL}		EN Input Voltage "L"			0.36	V
R_{DISC}	Auto Discharge Resistance	$V_{BIAS}=4.0V, V_{EN}<0.36V,$ $V_{OUT} = 0.5V$		150		Ω
I_{EN}	EN Pull Down Current	$V_{EN}=V_{BIAS}=5.5V$		0.55	1	μA
I_{LIM}	Output Current Limit	$V_{OUT}=90\%*V_{OUT(SET)}$	1500			mA
I_{SC}	Short Current Limit	$V_{OUT}=0V$		$0.35 \times I_{LIM}$		mA
$PSRR_{V_{IN}}$	Power Supply Ripple Rejection	$V_{OUT}=1.2V, V_{BIAS}=2.8V,$ $V_{IN}=1.7V+0.2V_{pp},$ $I_{OUT}=150mA, f=1kHz$		70		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PSRR_ V _{BIAS}	Power Supply Ripple Rejection	V _{OUT} =1.2V, V _{IN} =1.7V, V _{BIAS} =2.8V+0.2V _{pp} , I _{OUT} =150mA, f=1kHz		75		dB
V _N	Output Voltage Noise	V _{OUT(SET)} =1.2V, I _{OUT} =30mA BW=10Hz to 100kHz		30× V _{OUT} / V _{REF}		μVrms
T _{on}	Turn-On Time	From assertion of V _{EN} to V _{OUT} =90% V _{OUT} , V _{OUT} = 1.2 V		150		μs
T _{SDH}	Thermal Shutdown Threshold	Temperature Rising		165		°C
T _{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		135		°C

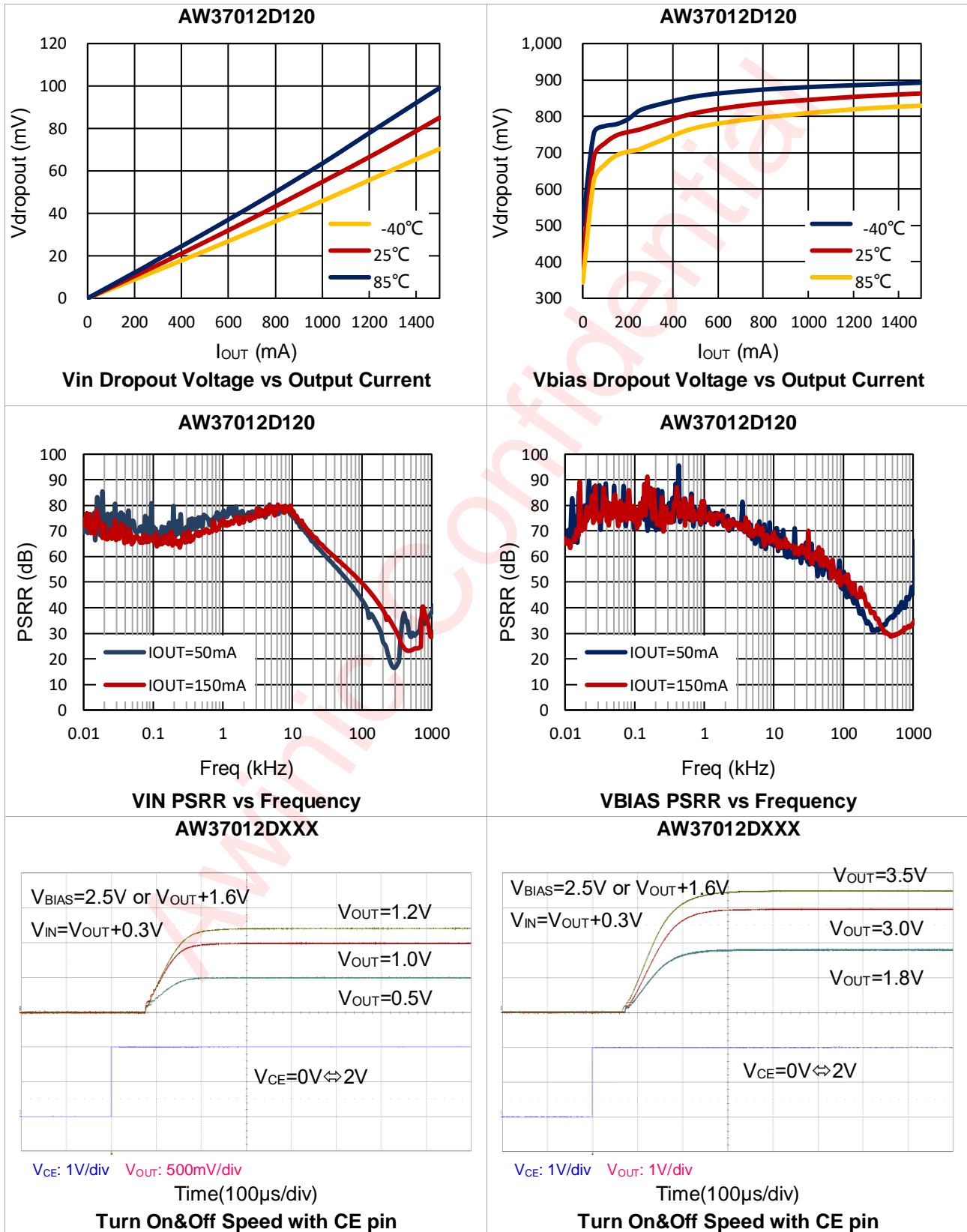
Typical Characteristics

$V_{BIAS}=2.5V$ or $V_{BIAS} \geq V_{OUT}+1.6V$, and $V_{IN}=V_{OUT(SET)}+0.3V$, $I_{OUT}=1mA$, $C_{IN}=4.7\mu F$, $C_{OUT}=4.7\mu F$, $C_{BIAS}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified.



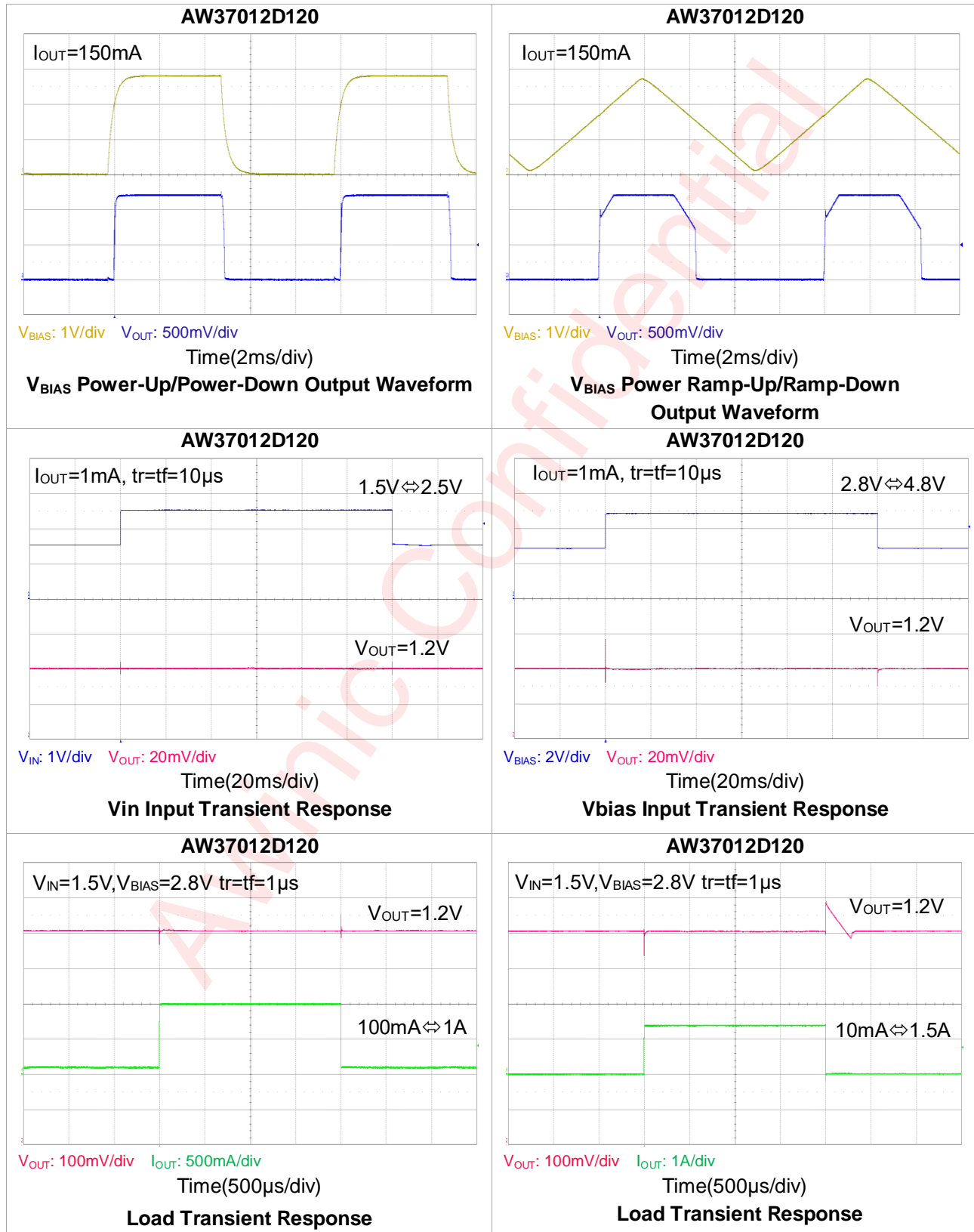
Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless otherwise noted.



Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless otherwise noted.



Detailed Functional Description

AW37012DXXX is a high accuracy, low dropout voltage, fast load transient response LDO. After powered on, with EN pin assertion, feedback voltage and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate.

Enable Operation

AW37012DXXX uses EN pin to realize enable operation. Applying proper value of voltage to EN pin can make IC enable/disable.

If the voltage of EN pin is less than 0.36V, AW37012DXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is open making output discharge through a 150Ω resistor to Ground.

If the voltage of EN pin is more than 0.84V, AW37012DXXX is guaranteed to be enabled. In this state, the auto discharge MOSFET is closed, and AW37012DXXX regulates output voltage to the designed value of voltage. A 0.55μA pull down current to Ground is built-in at EN pin, making sure that the IC is disabled when EN pin floats. If Enable function is not required, EN pin should be connected directly to IN pin.

Adjustable Output Voltage Setting

The output voltage of the AW37012DXXX can be adjusted from 0.5V to 3.5V. When FB pin connected to the resistor divider the output voltage is the nominal output voltage multiplied by the resistors divider ratio, see following equation.

$$V_{OUT_ADJ} = V_{FB} \left(1 + \frac{R1}{R2} \right)$$

Where:

- V_{OUT_ADJ} is output voltage of the circuit with resistor divider
- V_{FB} is 0.5V , the LDO's reference voltage

The value of R2 are suggested not over 50kΩ. Typical application circuits gives the connections for the adjustable output voltage application.

Output Current Limit

AW37012DXXX integrates output current limit function, protecting IC from excessive current . When the load is excessively heavy, AW37012DXXX limits the current flowing through the IC to a typical value current which is about 50% more than the rated output current. This value is specially designed, so that IC is protected properly and the output capability is not influenced either.

Meanwhile, AW37012DXXX integrates fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37012DXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 165°C, AW37012DXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls

below to 135°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

Auto Discharge

AW37012DXXX makes output voltage decrease quickly when in disable state or thermal shutdown state, benefit from integrating auto discharge function.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37012DXXX advises to use a 4.7 μ F or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit, the input decoupling capacitor is necessary to be connected as close as possible to the V_{IN} pin for ensuring the device stability.

OUT pin: Output Capacitor C_{OUT}

AW37012DXXX advises to use a 4.7 μ F or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit. For adjustable voltage versions, when the V_{OUT} is >3.0V, choose a 10 μ F or more C_{OUT} .

BIAS pin: BIAS Capacitor C_{BIAS}

AW37012DXXX advises to use a 1 μ F or more X5R or X7R ceramic capacitor at BIAS pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A475ME01	10V, X5R, 0402	MURATA	4.7	μ F
C_{OUT}	GRM155R60J475ME47	6.3V, X5R, 0402	MURATA	4.7	μ F
	GRM155R60J106ME18	6.3V, X5R, 0402	MURATA	10	μ F
C_{BIAS}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μ F

Application InformAtion

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta ja}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_MAX} = 150^\circ\text{C}$:

$$PD_{MAX_ABS} = (T_{J_MAX} - T_A) / R_{\theta ja}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where $T_{J_REC} = 125^\circ\text{C}$:

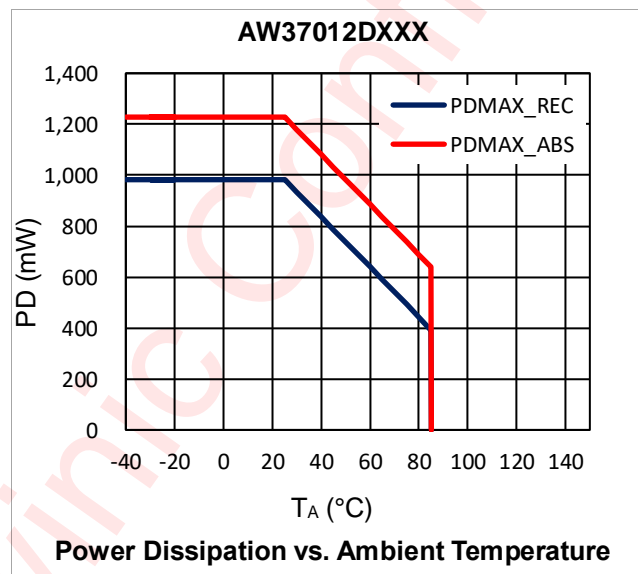
$$PD_{MAX_REC} = (T_{J_REC} - T_A) / R_{\theta ja}$$

The actual power being dissipated in the device can be represented by Equation below:

$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



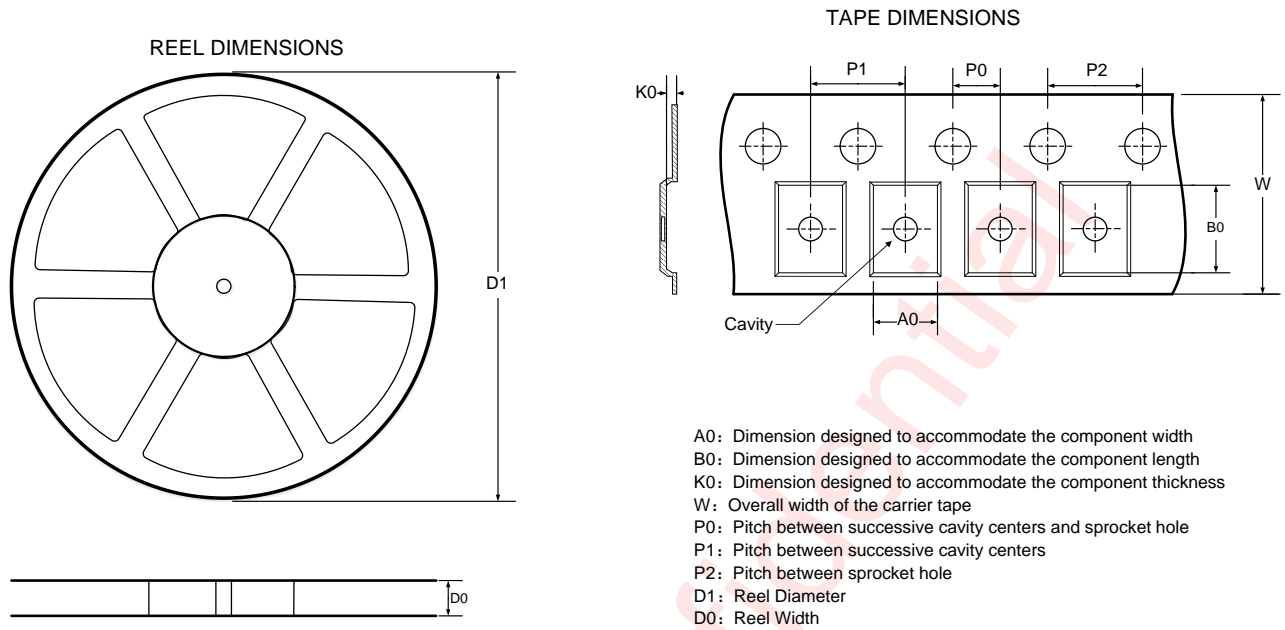
The above graphs show the maximum power dissipation of the respective package at $T_{J_REC} = 125^\circ\text{C}$ and $T_{J_MAX} = 150^\circ\text{C}$. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

PCB Layout Consideration

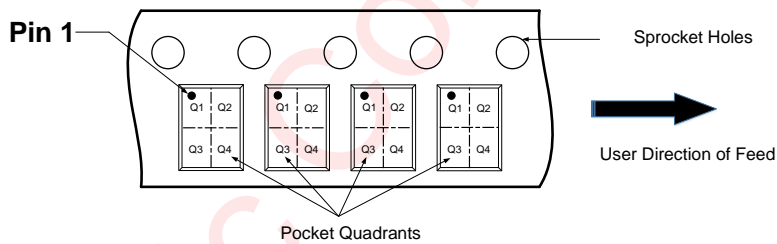
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN, OUT and BIAS pin are the large current input and output of the chip, make IN, OUT, BIAS, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient via holes below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



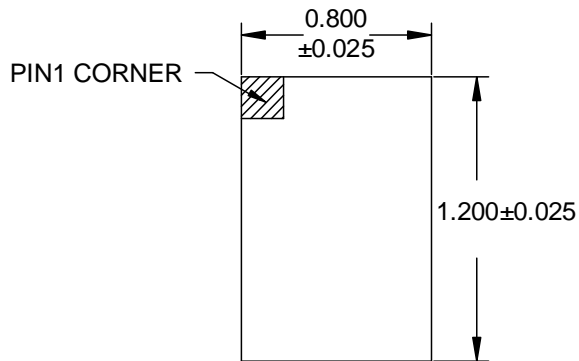
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

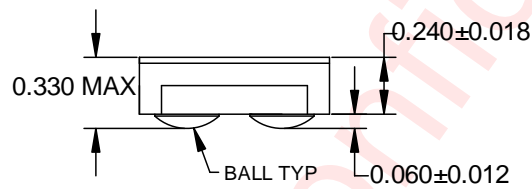
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	0.90	1.30	0.42	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

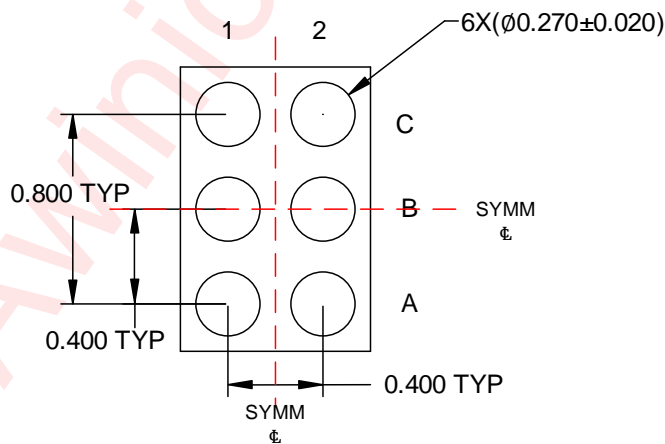
Package Description



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jul. 2024	Officially released

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