

4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

Features

- AEC-Q100 Qualified With Following Results:
 - Device Operating Temperature Grade 1: -40°C to +125°C
 - Device HBM ESD Classification: Class 3A
 - Device CDM ESD Classification: Class C3
- 1.2V~3.6V on A Port and 1.65V~5.5V on B Port($V_{CCA} \leq V_{CCB}$)
- Maximum Data Rates:100Mbps(Push Pull)
- This Device Can Only Translate Push-pull CMOS Logic Outputs
- No Direction-Control Signal Required
- Qualified for Automotive Applications
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, All Output are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Support Ultra-Low Power Consumption Mode with OE Pin is Low Voltage Level
- ESD Protection Exceeds AEC-Q100
 - A Port:
 - 4KV Human-Body Model (ANSI/ESDA/JEDEC JS-001-2023)
 - 1KV Charged-Device Model (ANSI/ESDA/JEDEC JS-002-2022)
 - B Port:
 - 15KV Human-Body Model (ANSI/ESDA/JEDEC JS-001-2023)
 - 1KV Charged-Device Model (ANSI/ESDA/JEDEC JS-002-2022)

Applications

- Telematics
- Advanced Driver Assistance System (ADAS)
- Automotive information

General Description

AW39214-Q1 is a 4-bit high-performance voltage-level translator without direction control signal, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (V_{CCA} and V_{CCB}). V_{CCA} can be supplied with any voltage between 1.2V and 3.6V. V_{CCB} can be supplied with any voltage between 1.65V and 5.5V. The range of supply voltages makes the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V).

The AW39214-Q1 is designed so that the OE input circuit is supplied by V_{CCA} . When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade1) and is suitable for use in automotive applications.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AW39214-Q1	TSSOP-14L	4.96mm ×4.4mm
	QFN 2X1.7-12L	2mm ×1.7mm

Typical Application Circuit

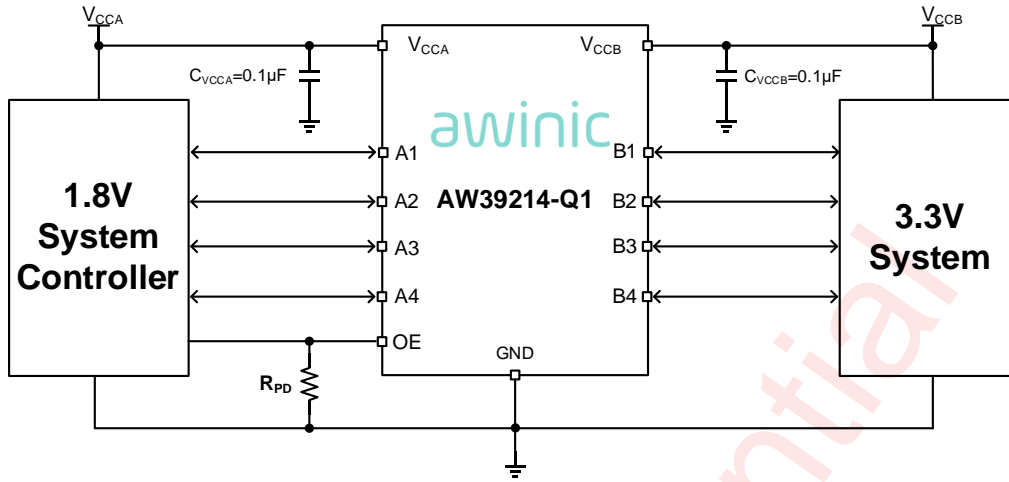
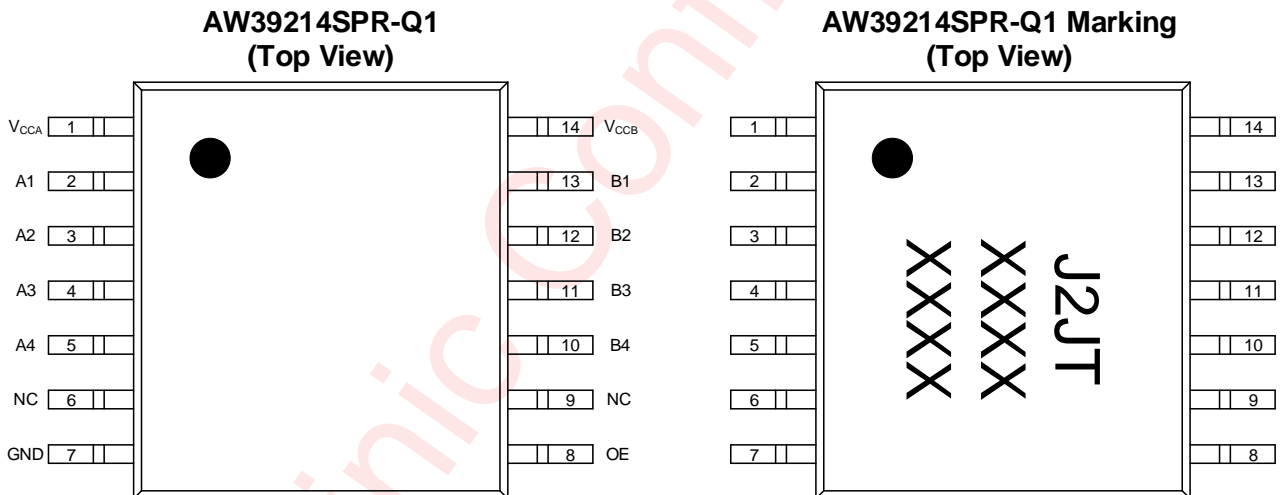


Figure 1 Typical Application Circuit of AW39214-Q1

Pin Configuration And Top Mark

TSSOP-14L



J2JT - AW39214SPR-Q1
XXXX/XXXX - Production Tracing Code

QFN 2X1.7-12L

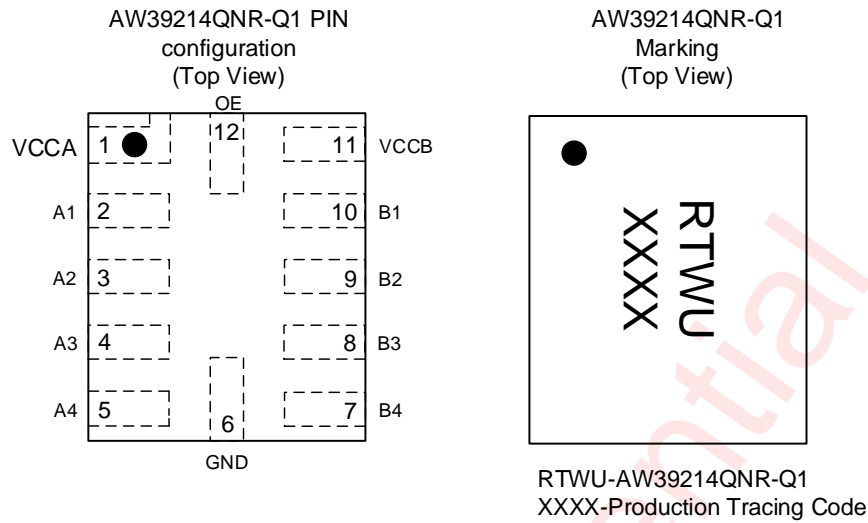


Figure 2 Pin Configuration and Top Mark

Pin Definition

NAME	NO.		DESCRIPTION
	TSSOP-14L	QFN 2X1.7-12L	
V _{CCA}	1	1	A-port supply voltage. $1.2V \leq V_{CCA} \leq 3.6V$, $V_{CCA} \leq V_{CCB}$.
A1	2	2	Input/output A1.
A2	3	3	Input/output A2.
A3	4	4	Input/output A3.
A4	5	5	Input/output A4.
NC	6	/	No connection. Not internally connected.
GND	7	6	Ground.
OE	8	12	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Active HIGH, Referenced to V _{CCA} .
NC	9	/	No connection. Not internally connected.
B4	10	7	Input/output B4.
B3	11	8	Input/output B3.
B2	12	9	Input/output B2.
B1	13	10	Input/output B1.
V _{CCB}	14	11	B-port supply voltage. $1.65V \leq V_{CCB} \leq 5.5V$.

Functional Block Diagram

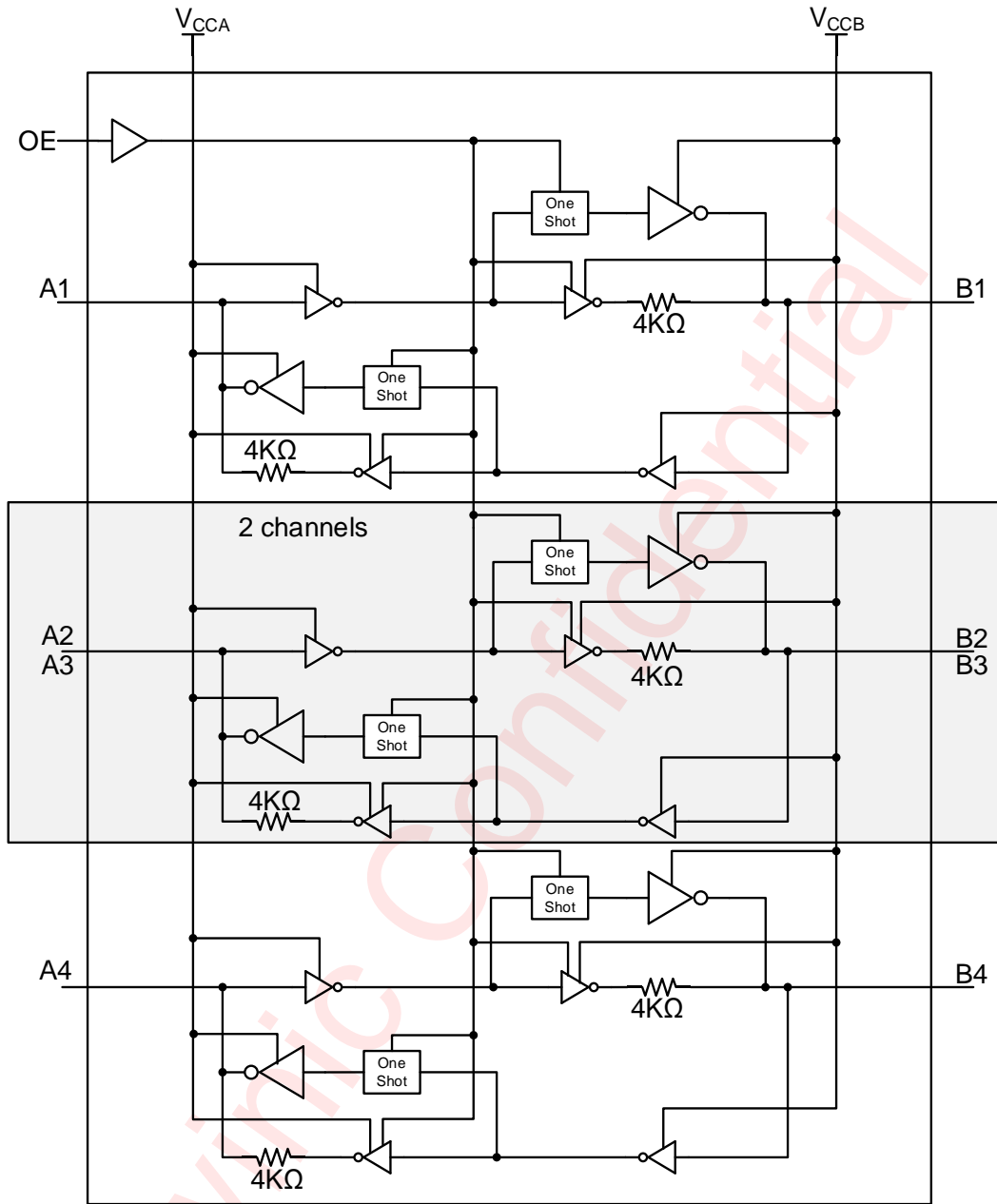


Figure 3 AW39214-Q1 Function Block

Typical Application Circuits

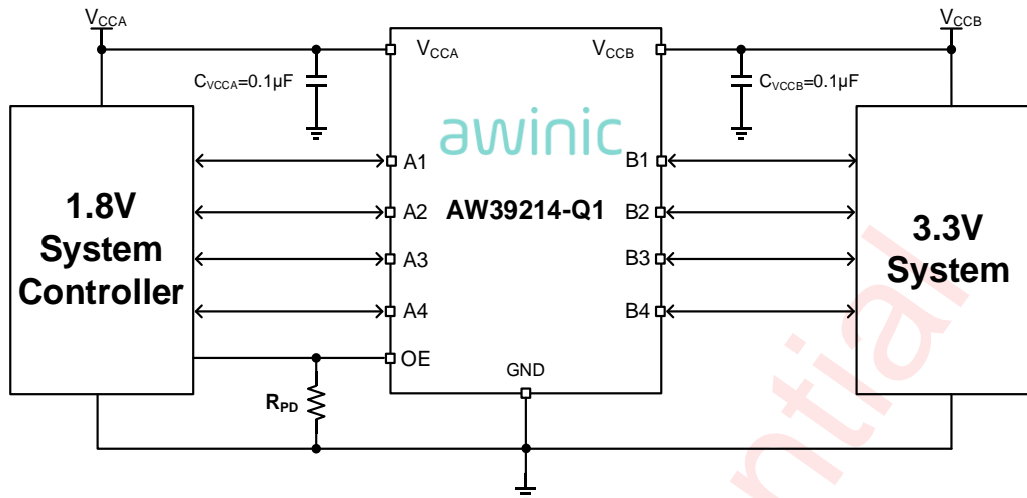


Figure 4 Typical Application Circuit of AW39214-Q1

Notice for typical application circuits:

1. In any case, the A/B Ports Voltage cannot be higher than the V_{CCA}/V_{CCB} voltage. Otherwise, the leakage current will flow from A/B Ports to V_{CCA}/V_{CCB} .
2. The device driving the A/B ports must have the driving capacity at least $\pm 2\text{mA}$.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW39214SPR-Q1	-40°C~125°C	TSSOP-14L	J2JT	MSL1	RoHS + HF	3000 units/ Tape and Reel
AW39214QNR-Q1	-40°C~125°C	QFN 2X1.7-12L	RTWU	MSL1	RoHS + HF	3000 units/ Tape and Reel

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETERS			MIN	MAX	UNIT
V_{CCA}	Supply voltage		-0.5	6.5	V
V_{CCB}			-0.5	6.5	
V_I	Input voltage range	A port	-0.5	6.5	V
		B port	-0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state	A port	-0.5	6.5	V
		B port	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state ⁽²⁾	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			± 50	mA
	Continuous current through V_{CCA} , V_{CCB} , or GND			± 100	mA
Storage temperature T_{STG}			-65	150	°C
Lead temperature (soldering 10 seconds)				260	°C

(1) Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

ESD Ratings

		VALUE	UNIT
Human-body model (HBM) ⁽¹⁾	A port	$\pm 4K$	V
	B port	$\pm 15K$	
Charged-device model (CDM) ⁽²⁾	A port	$\pm 1K$	
	B port	$\pm 1K$	
Latch-Up ⁽³⁾		+IT: 200 -IT: -200	mA

(1) The human body model is a 100pF capacitor discharged through a 1.5k Ω resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2023

(2) Test method: ANSI/ESDA/JEDEC JS-002-2022

(3) Test method: JESD78F.02-2023

Recommended Operating Conditions ⁽¹⁾⁽²⁾

SYMBOL	PARAMETERS	CONDITIONS		MIN	MAX	UNIT
V _{CCA}	Supply voltage			1.2	3.6	V
V _{CCB}	Supply voltage			1.65	5.5	V
V _{IH}	High-level input voltage	Data inputs	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~5.5V	V _{CCI} × 0.65 ⁽³⁾	V _{CCI}	V
		OE	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~5.5V	V _{CCA} ×0.65	5.5	V
V _{IL}	Low-level input voltage	Data inputs	V _{CCA} =1.2V~5.5V V _{CCB} =1.65V~5.5V	0	V _{CCI} × 0.35 ⁽³⁾	V
		OE input	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~5.5V	0	V _{CCA} ×0.35	V
V _O	Voltage range applied to any output in the high-impedance or power-off state	A-port	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~5.5V	0	3.6	V
		B-port		0	5.5	V
Δt/ΔV	Input transition rise or fall rate	A-port inputs	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~5.5V		40	ns/V
		B-port inputs	V _{CCA} =1.2V~3.6V V _{CCB} =1.65V~3.6V		40	ns/V
			V _{CCA} =1.2V~3.6V V _{CCB} =4.5V~5.5V		30	ns/V
T _A	Operating free-air temperature T _A			-40	125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.

(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

(3) V_{CCI} is the supply voltage associated with the input port.

Thermal Information

THERMAL METRIC		AW39214SPR-Q1	AW39214QNR-Q1	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	131.76	TBD	°C/W
R _{θJC}	Junction-to-case thermal resistance	51.92	TBD	
R _{θJB}	Junction-to-board thermal resistance	90.16	TBD	
Ψ _{JT}	Junction-to-board thermal resistance	3.4	TBD	
Ψ _{JB}	Junction-to-top characterization param	88.52	TBD	

Electrical Characteristics

DC Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITIONS	V _{CCA} (V)	V _{CCB} (V)	T _A (°C)	MIN	TYP	MAX	UNIT
V _{OHA}	I _{OH} = -20μA	1.2	1.4~3.6	1.65~5.5	25	V _{CCA} -0.4	1.1		V
					-40~125				
V _{OLA}	I _{OL} = 20μA	1.2	1.4~3.6	1.65~5.5	25		0.08	0.4	V
					-40~125				
V _{OHB}	I _{OH} = -20μA			1.65~5.5	-40~125	V _{CCB} -0.4			V
V _{OLB}	I _{OL} = 20μA			1.65~5.5	-40~125			0.4	V
I _I	OE	V _I = V _{CC1} or GND	1.2~3.6	1.65~5.5	25		±1		μA
					-40~125		±5		
I _{off}	A port	V _I or V _O = 0~3.6V	0	0~5.5	25		±1		μA
					-40~125		±10		
	B port	V _I or V _O = 0~5.5V	0~3.6	0	25		±1		μA
					-40~125		±10		
I _{oz}	A or B port	OE = GND	1.2~3.6	1.65~5.5	25		±1		μA
					-40~125		±10		
I _{CCA}		V _I = V _{CC1} or GND, I _O = 0	1.2	1.65~5.5	25		0.06		μA
			1.4~3.6	1.65~5.5	-40~125		15		
			3.6	0	-40~125		10		
			0	5.5	-40~125		-10		
I _{CCB}		V _I = V _{CC1} or GND, I _O = 0	1.2	1.65~5.5	25		3.0		μA
			1.4~3.6	1.65~5.5	-40~125		15		
			3.6	0	-40~125		-10		
			0	5.5	-40~125		10		
I _{CCA} +I _{CCB}		V _I = V _{CC1} or GND, I _O = 0	1.2	1.65~5.5	25		3.06		μA
			1.4~3.6	1.65~5.5	-40~125		30		
I _{CCZA}		V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2	1.65~5.5	25		0.05		μA
			1.4~3.6	1.65~5.5	-40~125		15		
I _{CCZB}		V _I = V _{CC1} or GND, I _O = 0, OE = GND	1.2	1.65~5.5	25		3.3		μA
			1.4~3.6	1.65~5.5	-40~125		15		
C _i	OE		1.2~3.6	1.65~5.5			4		pF

C _{io}	A port		1.2~3.6	1.65~5.5			6	pF
	B port		1.2~3.6	1.65~5.5			13	pF

(1) V_{CCI} is the supply voltage associated with the input port.

(2) V_{CCO} is the supply voltage associated with the output port.

Timing Requirements: V_{CCA} = 1.2V

T_A = 25°C, V_{CCA} = 1.2V

			V _{CCB} =1.8V	V _{CCB} =2.5V	V _{CCB} =3.3V	V _{CCB} =5V	UNIT
			TYP	TYP	TYP	TYP	
Data rate			20	20	4	2	Mbps
t _w	Pulse duration	Data inputs	50	50	250	500	ns

Timing Requirements: V_{CCA} = 1.5V ± 0.1V

Over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1 V(unless otherwise noted)

			V _{CCB} =1.8V ±0.15V		V _{CCB} =2.5V ±0.2V		V _{CCB} =3.3V ±0.3V		V _{CCB} =5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			40		40		40		40		Mbps
t _w	Pulse duration	Data inputs	25		25		25		25		ns

Timing Requirements: V_{CCA} = 1.8V ± 0.15V

Over recommended operating free-air temperature range, V_{CCA}=1.8V ± 0.15V(unless otherwise noted)

			V _{CCB} =1.8V ±0.15V		V _{CCB} =2.5V ±0.2V		V _{CCB} =3.3V ±0.3V		V _{CCB} =5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			60		60		60		60		Mbps
t _w	Pulse duration	Data inputs	17		17		17		17		ns

Timing Requirements: V_{CCA} = 2.5V ± 0.2 V

Over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2 V(unless otherwise noted)

			V _{CCB} =2.5V±0.2V		V _{CCB} =3.3V±0.3V		V _{CCB} =5V±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			100		100		100		Mbps
t _w	Pulse duration	Data inputs	10		10		10		ns

Timing Requirements: $V_{CCA} = 3.3V \pm 0.3V$ Over recommended operating free-air temperature range, $V_{CCA} = 3.3V \pm 0.3V$ (unless otherwise noted)

			$V_{CCB}=3.3V\pm 0.3V$		$V_{CCB}=5V\pm 0.5V$		UNIT
			MIN	MAX	MIN	MAX	
Data rate			100		100		Mbps
t_w	Pulse duration	Data inputs	10		10		ns

Switching Characteristics: $V_{CCA} = 1.2V$ $T_A = 25^\circ C$, $V_{CCA} = 1.2V$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}=1.8V$	$V_{CCB}=2.5V$	$V_{CCB}=3.3V$	$V_{CCB}=5V$	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	13	10.5	9.7	9.2	ns
	B	A	10	8.3	7.9	36	
t_{en}	OE	A	1	1	1	1	μs
		B	1	1	1	1	
t_{dis}	OE	A	320	320	320	330	ns
		B	150	110	150	110	
t_{rA}, t_{fA}	A-port rise and fall times		6	6	160	200	ns
t_{rB}, t_{fB}	B-port rise and fall times		3	3	2	2	ns
$t_{sk(o)}$	Channel-to-channel skew		0.5	0.5	0.5	0.5	ns

Switching Characteristics: $V_{CCA} = 1.5V \pm 0.1V$ Over recommended operating free-air temperature range, $V_{CCA} = 1.5V \pm 0.1V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}=1.8V\pm 0.15V$		$V_{CCB}=2.5V\pm 0.2V$		$V_{CCB}=3.3V\pm 0.3V$		$V_{CCB}=5V\pm 0.5V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			t_{pd}	A	B	15.9		13.1		13	
	B	A	17.2		15		14.7		16.7		
t_{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t_{dis}	OE	A	340		280		280		300		ns
		B	400		350		430		300		
t_{rA}, t_{fA}	A-port rise and fall times		7.1		7.1		7.1		7.1		ns
t_{rB}, t_{fB}	B-port rise and fall times		6.5		5.2		4.8		4.7		ns

$t_{sk(o)}$	Channel-to-channel skew	0.7	0.7	0.7	0.7	ns
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Switching Characteristics: $V_{CCA} = 1.8V \pm 0.15V$

Over recommended operating free-air temperature range, $V_{CCA} = 1.8V \pm 0.15V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}=1.8V \pm 0.15V$		$V_{CCB}=2.5V \pm 0.2V$		$V_{CCB}=3.3V \pm 0.3V$		$V_{CCB}=5V \pm 0.5V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	14.0		10.7		9.8		9.5		ns
	B	A	15.0		11.4		10.6		10.1		
t_{en}	OE	A	1		1		1		1		μs
		B	1		1		1		1		
t_{dis}	OE	A	280		250		250		250		ns
		B	380		260		400		260		
t_{rA}, t_{fA}	A-port rise and fall times		6.2		6.1		6.1		6.1		ns
t_{rB}, t_{fB}	B-port rise and fall times		5.8		5.2		4.8		4.7		ns
$t_{sk(o)}$	Channel-to-channel skew		0.7		0.7		0.7		0.7		ns

Switching Characteristics: $V_{CCA} = 2.5V \pm 0.2V$

Over recommended operating free-air temperature range, $V_{CCA} = 2.5V \pm 0.2V$ (unless otherwise noted)

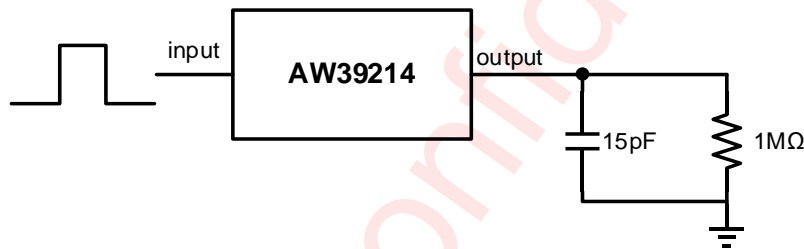
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}=2.5V \pm 0.2V$		$V_{CCB}=3.3V \pm 0.3V$		$V_{CCB}=5V \pm 0.5V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		9.3		8.2		7.7	ns
	B	A		9.6		8.6		7.4	
t_{en}	OE	A		1		1		1	μs
		B		1		1		1	
t_{dis}	OE	A		220		220		220	ns
		B		260		400		260	
t_{rA}, t_{fA}	A-port rise and fall times			5.0		5.0		5.0	ns
t_{rB}, t_{fB}	B-port rise and fall times			4.6		4.8		4.7	ns
$t_{sk(o)}$	Channel-to-channel skew			0.5		0.5		0.5	ns

Switching Characteristics: $V_{CCA} = 3.3V \pm 0.3V$

Over recommended operating free-air temperature range, $V_{CCA} = 3.3V \pm 0.3V$ (unless otherwise noted)

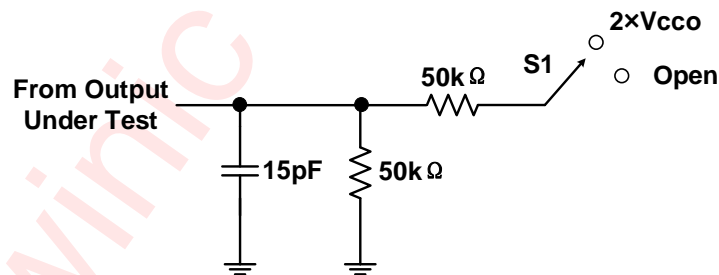
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB}=3.3V\pm 0.3V$		$V_{CCB}=5V\pm 0.5V$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B		7.7		7.0	ns
	B	A		7.9		6.8	
t_{en}	OE	A		1		1	μs
		B		1		1	
t_{dis}	OE	A		280		280	ns
		B		400		260	
t_{rA}, t_{fA}	A-port rise and fall times			4.5		4.5	ns
t_{rB}, t_{fB}	B-port rise and fall times			4.1		4.7	ns
$t_{sk(o)}$	Channel-to-channel skew			0.7		0.7	ns

Test Information



Test Circuit for Data Rate, Pulse Duration, Propagation Delay, Rise Time and Fall Time

Figure 5 Load Circuit of Push-Pull Driver



TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open

Figure 6 Load Circuit for Enable-Time and Disable-Time Measurement

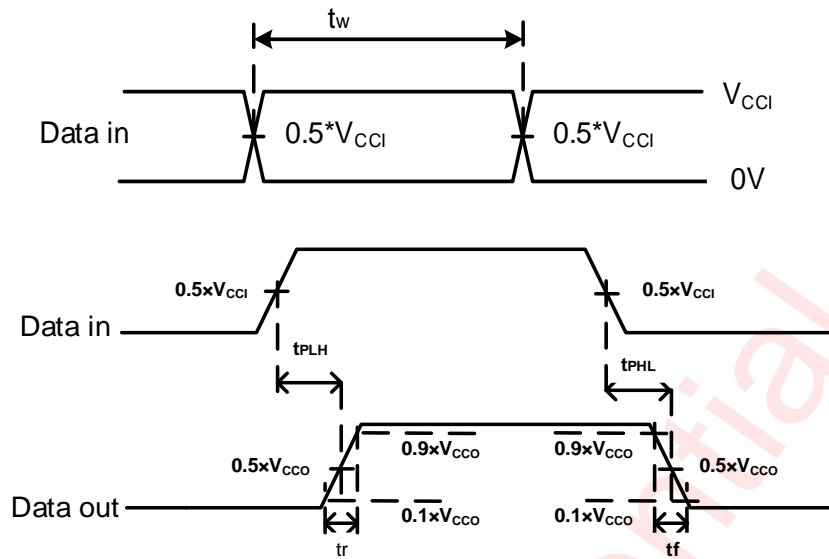


Figure 7 Timing Parameter Definition

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR_10 MHz, $Z_o = 50 \Omega$, $dv/dt \geq 1V/ns$.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. V_{CCI} is the V_{CC} associated with the input port.
- F. V_{CCO} is the V_{CC} associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

Detailed Functional Description

The AW39214-Q1 is a 4-bit high-performance voltage-level translator without direction control signal, which is a non-inverting converter and can be used to convert digital signal with mixed-voltage systems. Port A can support I/O voltages from 1.2 V to 3.6 V, while Port B is able to support I/O voltage range from 1.65 V to 5.5V. The chip uses a transmission gate architecture with an rising edge rate accelerator (one-shot), to increase overall data rate. This device can only translate push-pull CMOS logic outputs.

One-shot Architecture

The AW39214-Q1 architecture (see Functional Block Diagram) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the AW39214-Q1 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at $V_{CCO} = 1.2V$ to $1.8V$, 50Ω at $V_{CCO} = 1.8V$ to $3.3V$, and 40Ω at $V_{CCO} = 3.3V$ to $5V$.

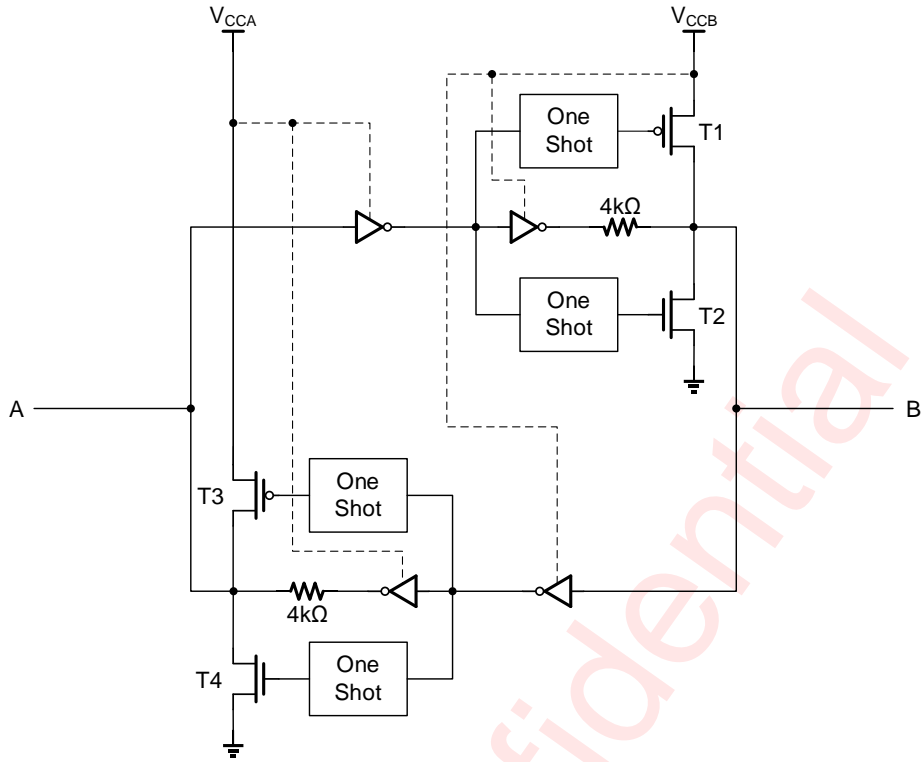
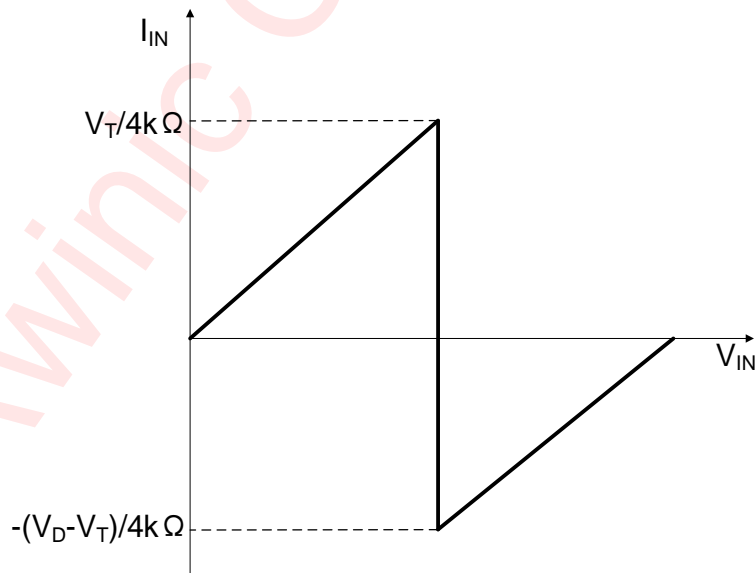


Figure 8 Architecture of AW39214-Q1 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the AW39214-Q1 are shown in Figure 9. For proper operation, the device driving the data I/Os of the AW39214-Q1 must have a minimum drive capability of $\pm 2\text{mA}$.



A. V_T is the input threshold voltage of the AW39214 (typically $V_{CC}/2$).
B. V_D is the supply voltage of the external driver.

Figure 9 Typical I_{IN} vs V_{IN} Curve

Output Load Considerations

It is recommended that a PCB layout with short PCB layout length:

1. Avoid excessive capacitive load triggers ONE-SHOT circuit falsely;
2. It can ensure that the round trip delay of any reflection is less than a single ONE-SHOT duration;
3. Improve signal integrity.

Meanwhile, the pulse width of the ONE-SHOT circuit is approximately 10ns, which determines the maximum output load capacitance that the chip can drive. For very heavy output capacitive loads, the one-shot accelerator will time-out before the output is fully pulled to high level, at which case the signal transmission will be distorted. So the ONE-SHOT duration design requires a trade-off between dynamic power consumption, capacitive load driving capability and maximum data rate. The signal t_w at the maximum translation rate should be greater than the maximum pulse width of the ONE-SHOT circuit, and the delay caused by the output capacitive load should be less than the maximum pulse width of the ONE-SHOT circuit.

Enable and Disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pullup or Pulldown Resistors on I/O Lines

As mentioned previously the AW39214-Q1 is designed with low static drive strength to drive capacitive loads of up to 70pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50k Ω . For this reason the AW39214-Q1 is not recommended for use in open drain driver applications such as 1-Wire or I2C. For these applications, the AW39124-Q1 level translator is recommended.

Device Functional Modes

The AW39214-Q1 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

Application Information

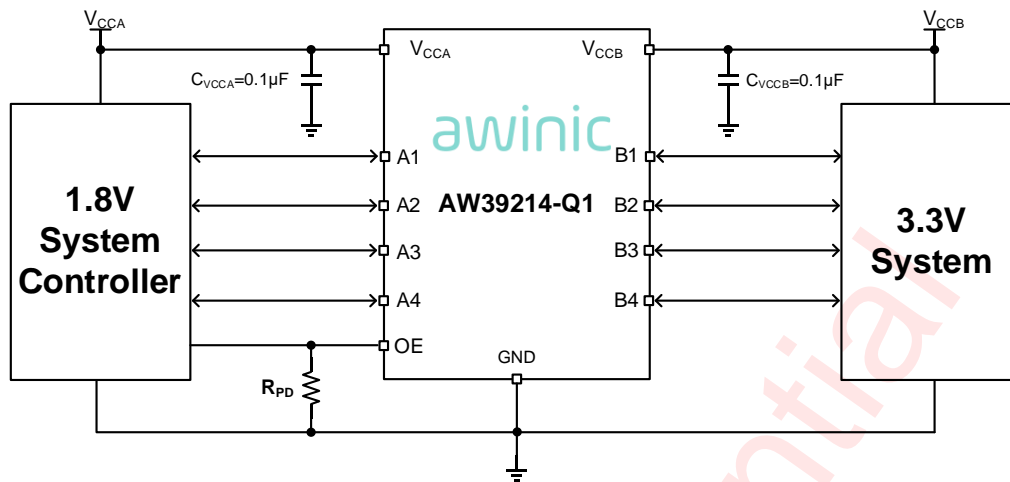


Figure 10 AW39214-Q1 Application Circuit

The AW39214-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. Any external pulldown or pullup resistors are recommended larger than 50kΩ.

Design Requirements

For this design example, use the parameters listed in Table 1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2V to 3.6V
Output voltage range	1.65V to 5.5V

Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range

- Use the supply voltage of the device that is driving the AW39214-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

- Output voltage range

- Use the supply voltage of the device that the AW39214-Q1 device is driving to determine the output voltage range.

- It is not recommended to have the external pullup or pulldown resistors. If mandatory, it is recommended the value should be larger than 50kΩ.

- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL} . Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5k\Omega)$$

$$V_{OL} = V_{CCx} \times 4.5k\Omega / (R_{PU} + 4.5k\Omega)$$

where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 4.5 k Ω is the counting the variation of the serial resistor 4k Ω in the I/O line

Power Supply Recommendations

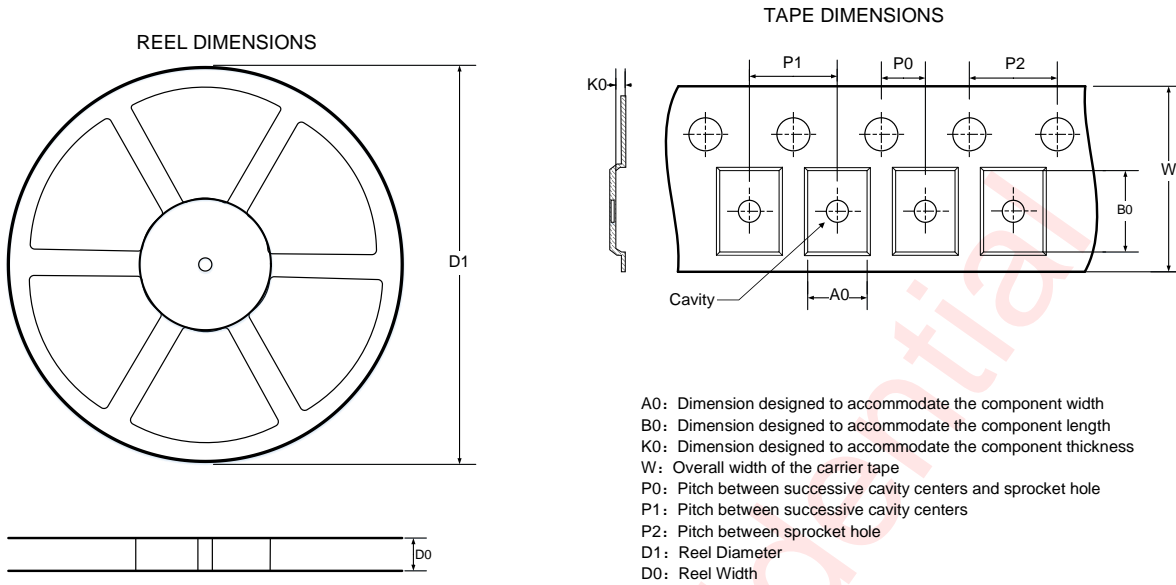
During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The AW39214-Q1 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

Vcc Capacitor Selection

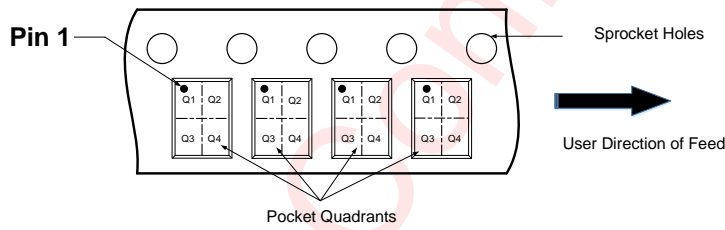
The device is a 4-bit high-performance voltage-level translator that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, recommend 0.1 μ F or larger than 0.1 μ F.

Tape And Reel Information

TSSOP-14L



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



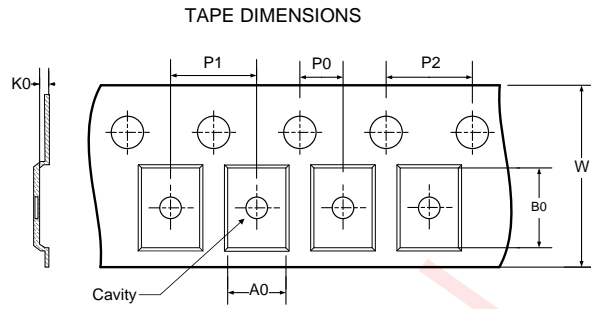
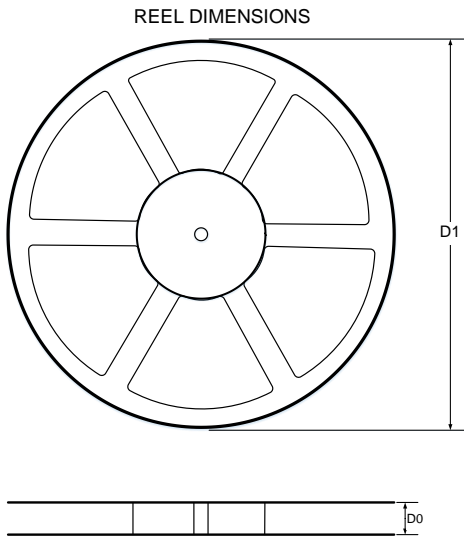
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.8	5.4	1.5	2	8	4	12	Q1

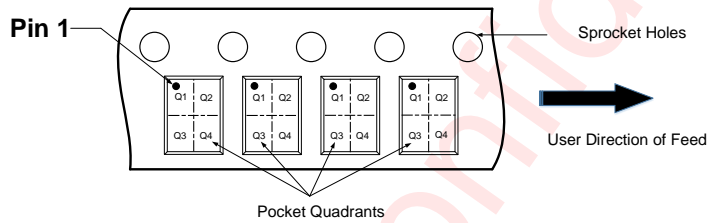
All dimensions are nominal

QFN 2X1.7-12L



- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
- D1: Reel Diameter
- D0: Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

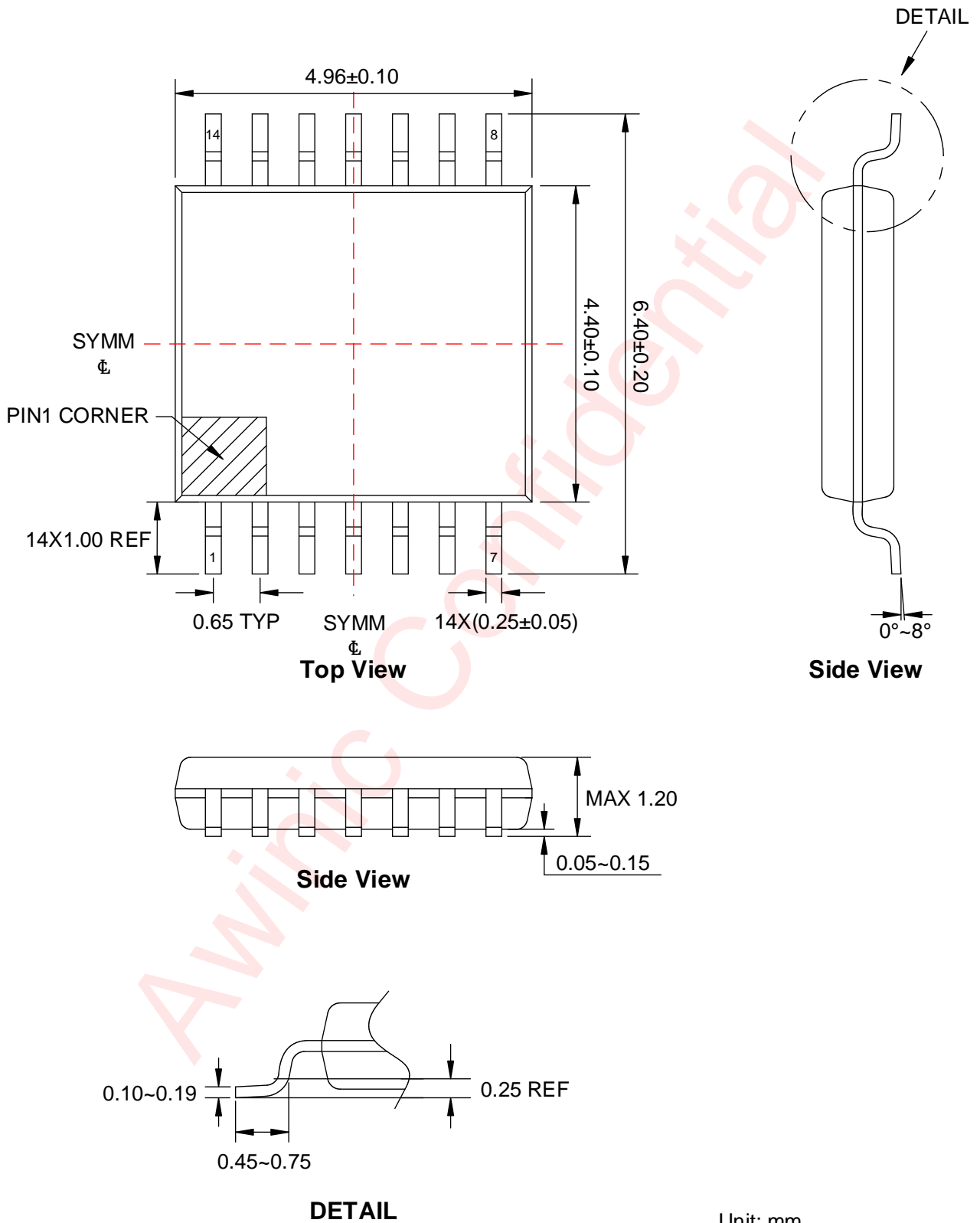
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	9.5	1.9	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

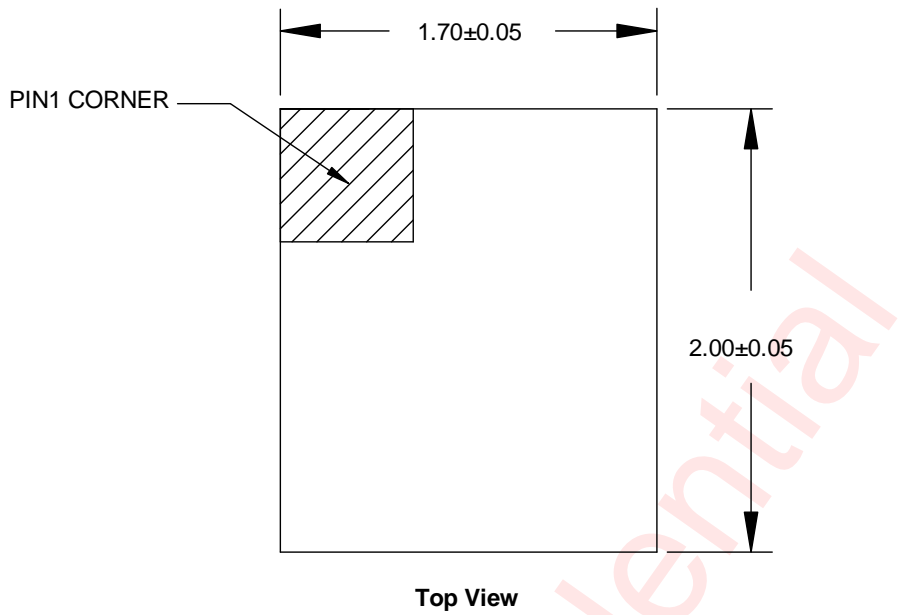
Package Description

TSSOP-14L

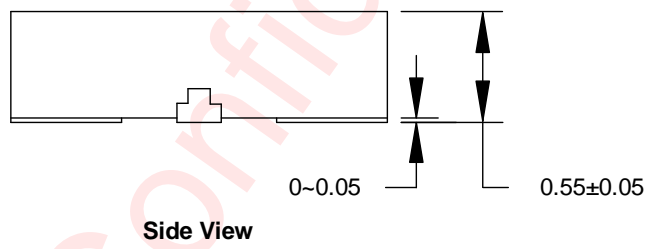


Unit: mm

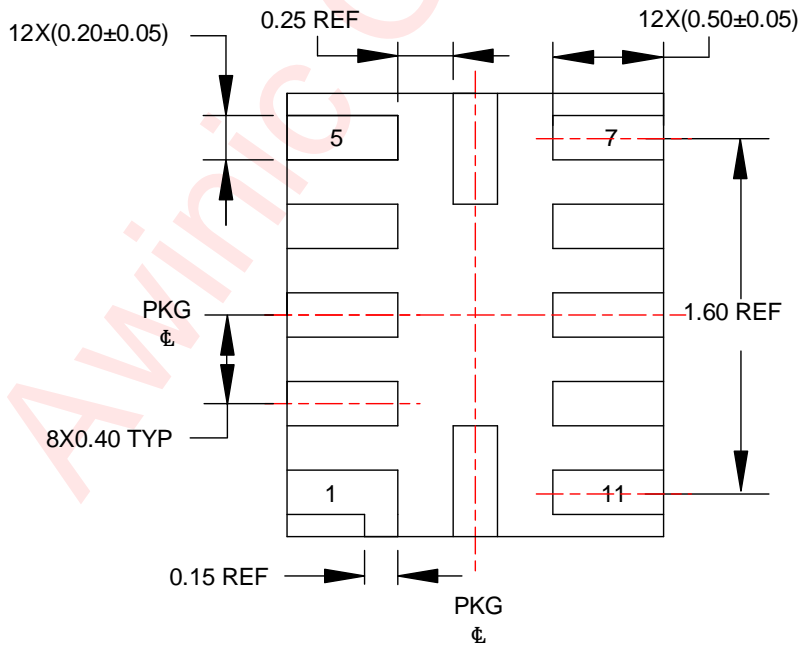
QFN 2X1.7-12L



Top View



Side View

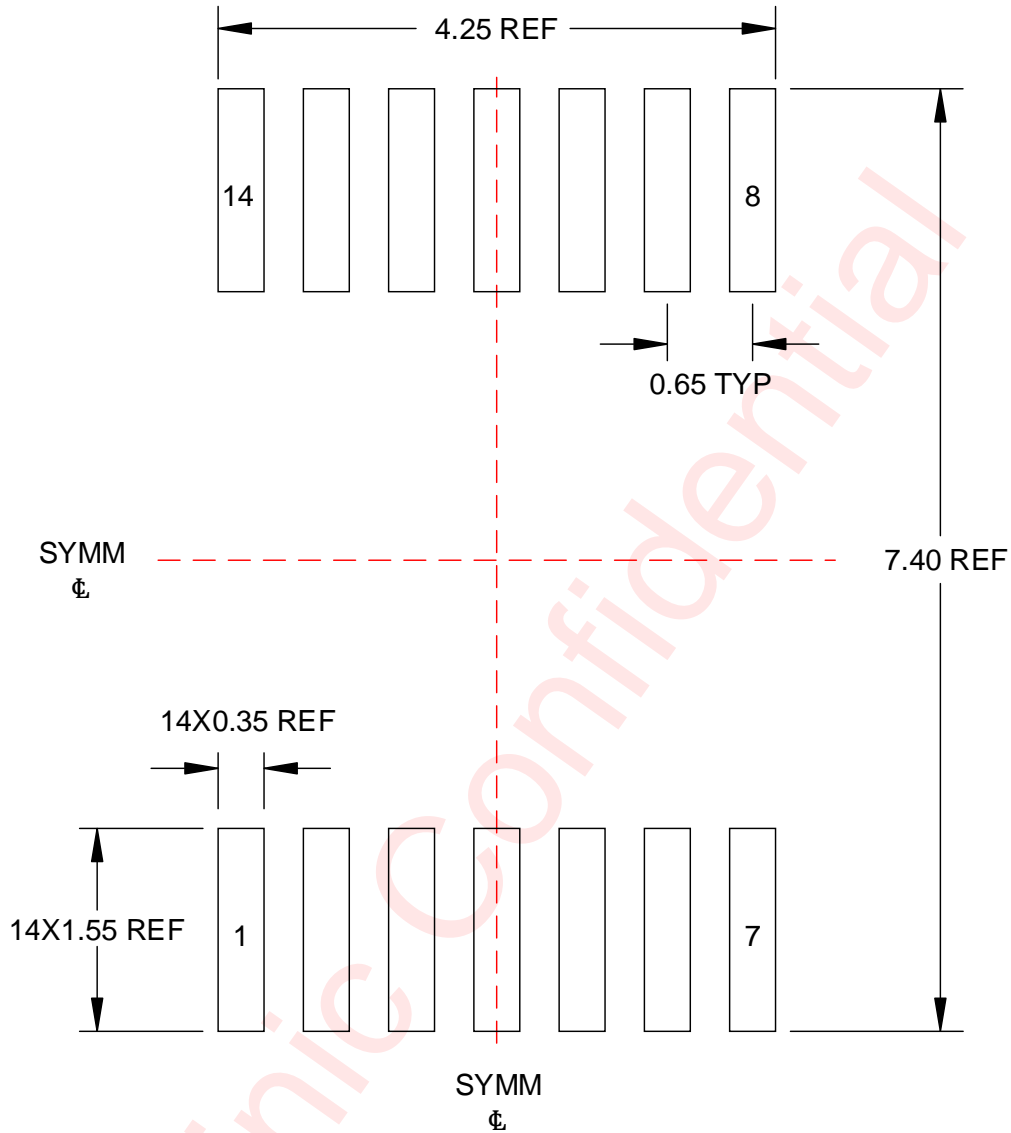


Bottom View

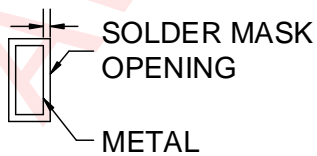
Unit: mm

Land Pattern Data

TSSOP-14L

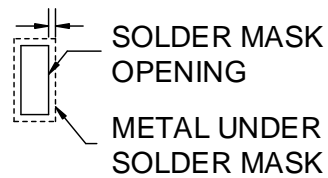


0.05 MAX
All AROUND



NON-SOLDER MASK DEFINED

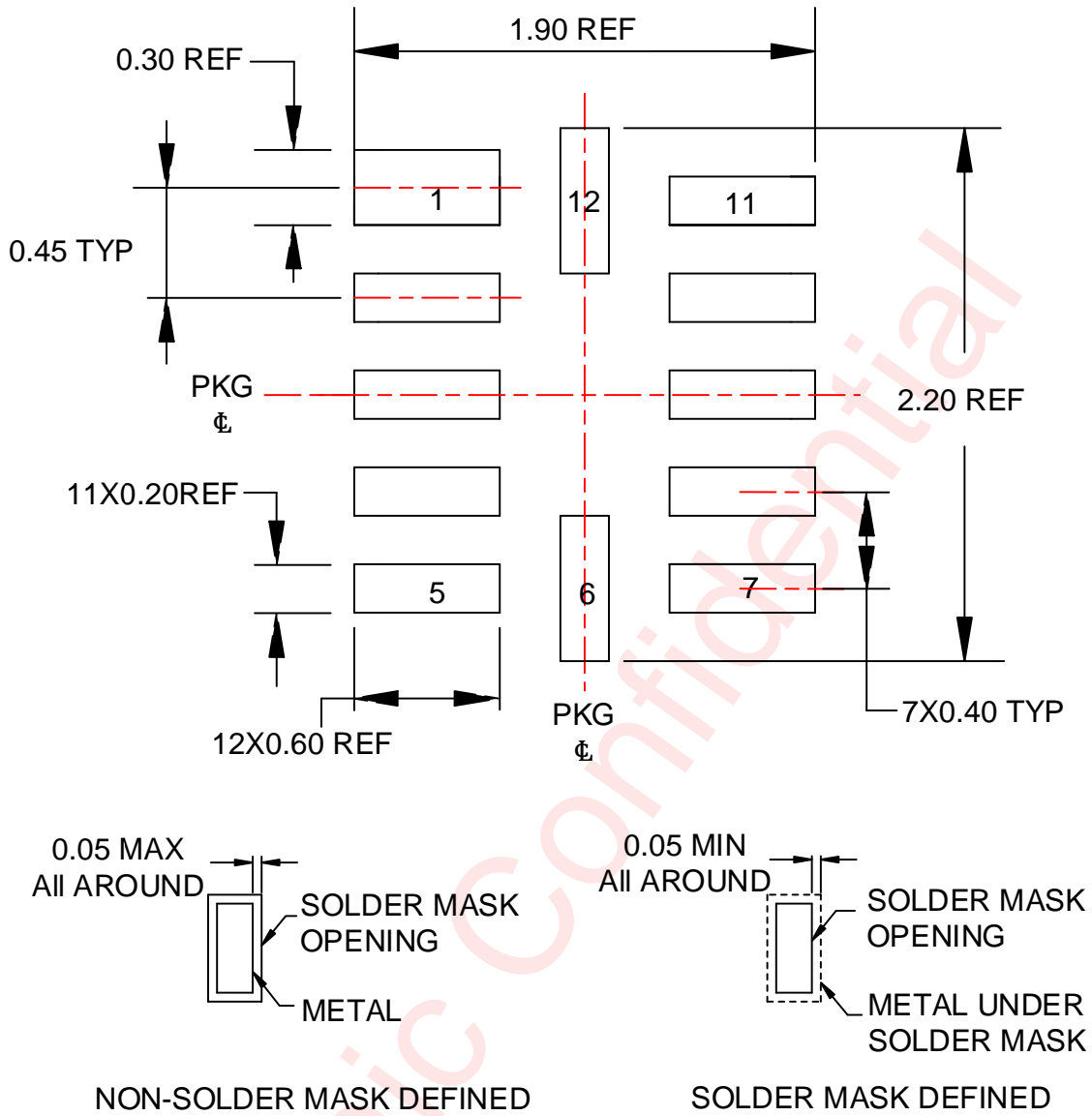
0.05 MIN
All AROUND



SOLDER MASK DEFINED

Unit: mm

QFN 2X1.7-12L



Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb. 2024	Officially released
V1.1	Aug.2024	1、 Update <i>Features</i> .(P1) 2、 Update <i>Switching Characteristics: V_{CCA} = 1.2V</i> .(P9)
V1.2	Nov.2024	1、 Update <i>Land Pattern Data</i> .(P19)
V1.3	Feb.2026	1. Added QFN 2X1.7-12L package information to <i>Device Information..</i> (P1) 2. Added QFN 2X1.7-12L pin configuration to <i>Pin Configuration And Top Mark.</i> (P3) 3. Added QFN 2X1.7-12L pin description table to <i>Pin Definition.</i> (P3) 4. Added QFN 2X1.7-12L information table to <i>Ordering Information.</i> (P5) 5. Added QFN 2X1.7-12L thermal metrics to <i>Thermal Information.</i> (P7) 6. Added QFN 2X1.7-12L information to <i>Tape And Reel Information.</i> (P19) 7. Added QFN 2X1.7-12L information to <i>Package Description.</i> (P21) 8. Added QFN 2X1.7-12L information to <i>Land Pattern Data.</i> (P23)

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