# Over-Voltage Protection Load Switch with Surge Protection

## Features

- Wide Input Voltage range from 3.1V to 28V
- 5A continuous current capability
- Input maximum voltage rating: 29$V_{DC}$
- Integrated ultra-low Ron switch: typical 20mΩ
- Adjustable Over-Voltage Lockout (OVLO)
- Fast Over-Voltage Protection turn-off response: typical 50ns
- Surge Protection compliant with IEC61000-4-5 up to ±100V
- Input system ESD protection
  - IEC 61000-4-2 Contact discharge: ±8kV
  - IEC 61000-4-2 Air gap discharge: ±15kV
- Reverse-Current Protection (RCP)
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)
- WLCSP 2.54mm×1.49mm×0.555mm-15B, 0.5mm pitch package

## Applications

- Smartphones
- Tablets
- Charging Ports

## General Description

The AW32105 is a high input voltage, large current and ultra-low Ron load switch bidirectional blocking.

The AW32105 is turned off very fast once the input voltage exceeds the OVP threshold to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages to 29$V_{DC}$. The AW32105 provides a default OVP threshold of 23V typical, and the OVP threshold can be adjusted from 4V to 24V through external OVLO pin.

The AW32105 has all time Reverse Current Protection regardless of the ENB logic level. Once the voltage on OUT is higher than IN for RCP trigger voltage, the RCP circuit disables the power switch. Two AW32105 chips can be used in parallel to support dual power inputs connecting to the same charging circuit.

The AW32105 OVP load switch features surge protection, an internal clamp circuit protects the device from surge voltages up to +/-100V. It also features over-temperature protection that prevents itself from thermal damaging.

## Typical Application Circuit

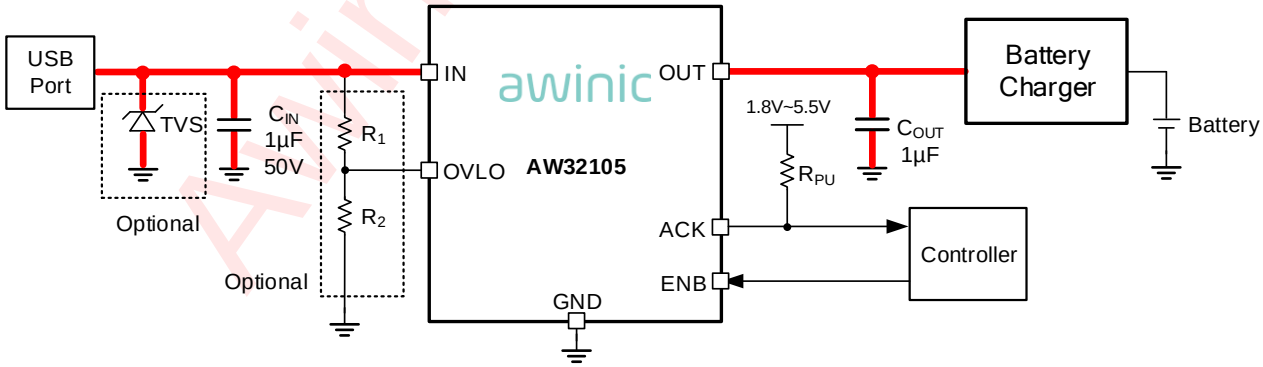


**Figure 1 AW32105 Typical Application Circuit**

$R_1$ and $R_2$ are used for OVP threshold adjustment, to use default OVP threshold, connect OVLO to ground.

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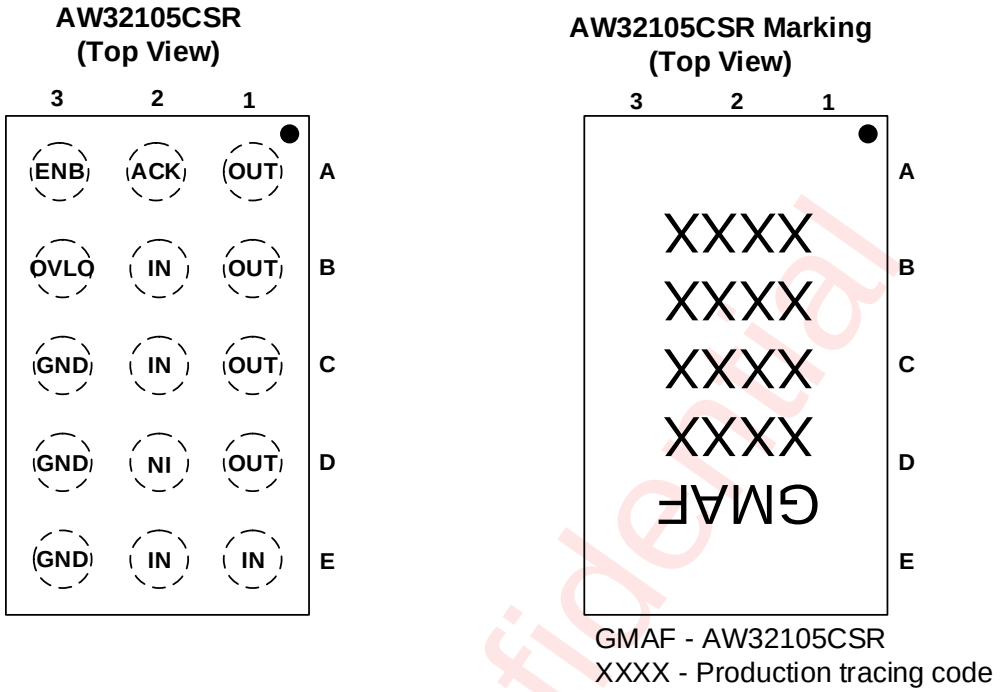
## Pin Configuration and Top Mark




GMAF - AW32105CSR
XXXX - Production tracing code

**Figure 2 Pin Configuration and Top Mark**

## Pin Definition

| Pin | Name | Description |
|---|---|---|
| A1, B1, C1, D1 | OUT | Switch output |
| E1, B2, C2, D2, E2 | IN | Switch input and device power supply |
| A2 | ACK | Power good flag, active-low, open-drain output.<br>When $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, ACK is pulled low, otherwise it's hi-Z state |
| A3 | ENB | Enable pin, active low |
| B3 | OVLO | OVP threshold adjustment pin |
| C3, D3, E3 | GND | Device ground |



## Functional Block Diagram

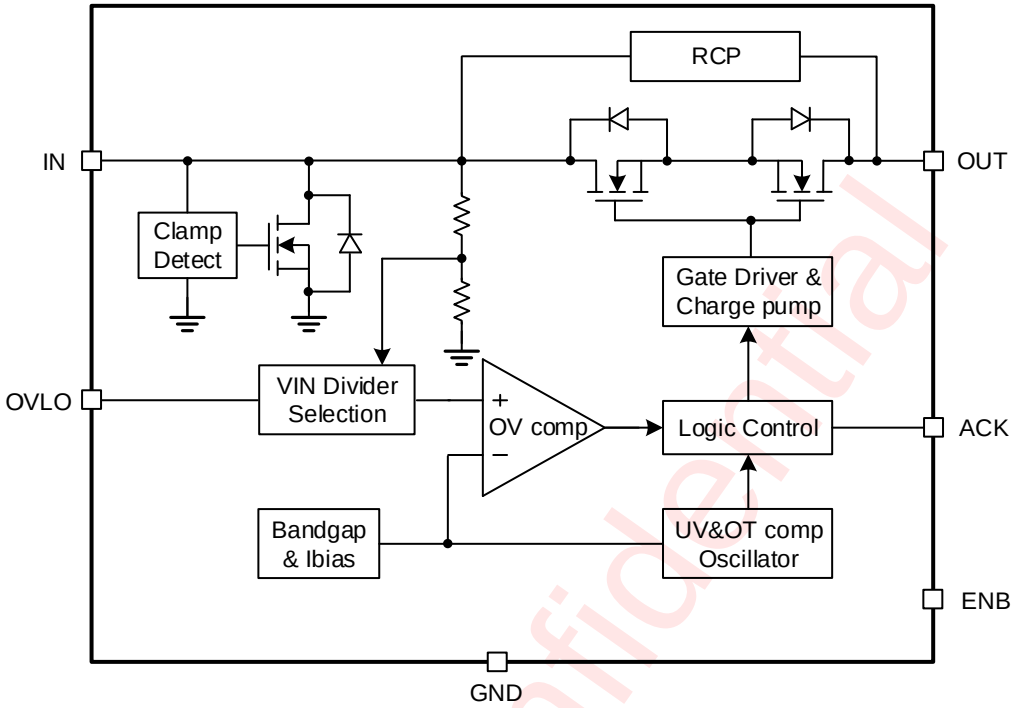



**Figure 3 Functional Block Diagram**



## Typical Application Circuits

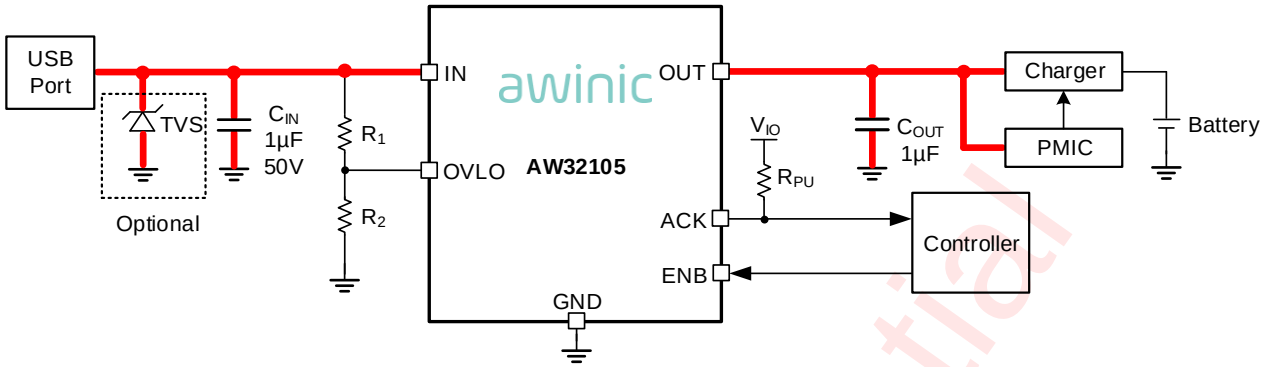



**Figure 4 AW32105 application with one charging input**

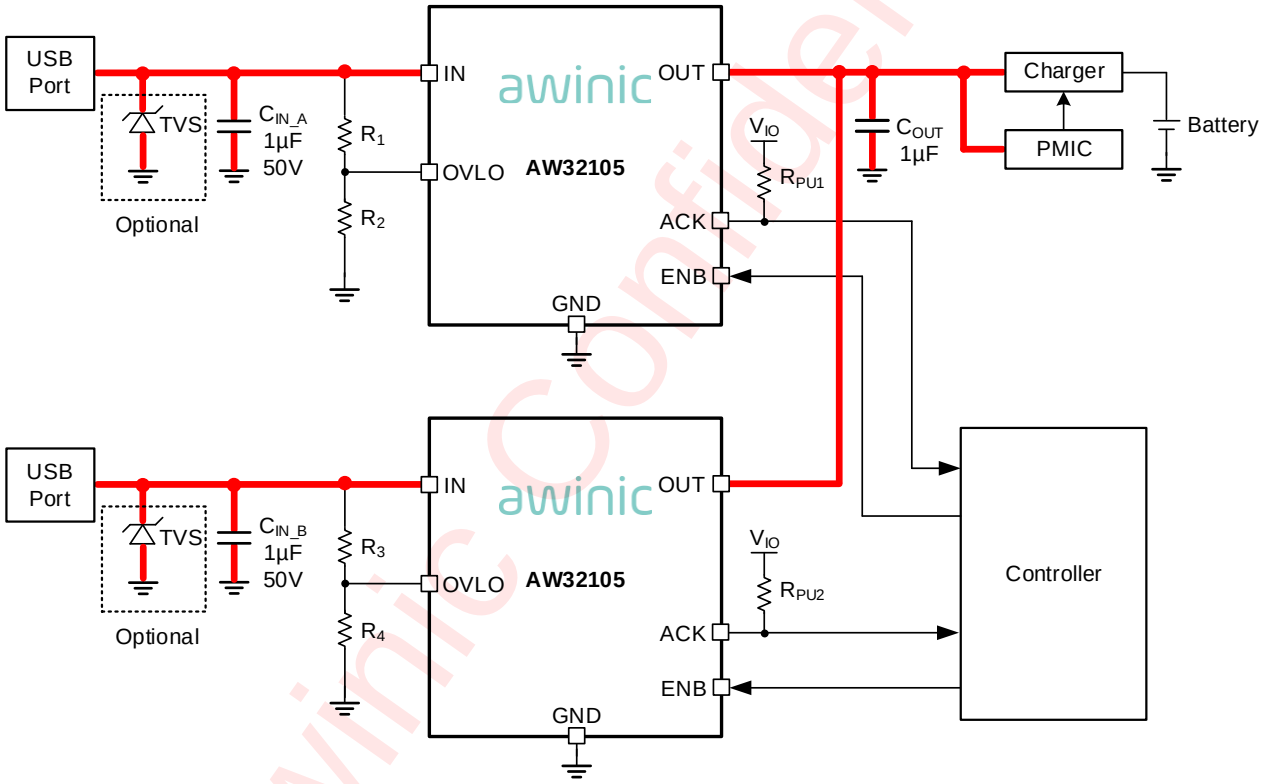



**Figure 5 AW32105 application with two charging inputs**

***Notice for Typical Application Circuits:***

1. If VBUS is required to pass surge voltage greater than 100V, external TVS is needed, the maximum clamping voltage of the TVS should be below 30V.
2. When the default OVP threshold is used, connect OVLO pin to GND directly or through a 0Ω resistor. **OVLO pin cannot be left floating.**
3. If $R_1$ $R_2$, $R_3$ and $R_4$ are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
4. If ACK is not used, it can be left floating, or short to GND.



5. $C_{IN}$ = 1μF is recommended for typical application, larger $C_{IN}$ is also acceptable. The rated voltage of $C_{IN}$ should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW32105 is used, the rated voltage of $C_{IN}$ should be 50V.
6. $C_{OUT}$ minimum is recommended to be 1μF. The rated voltage of $C_{OUT}$ should be larger than the OVP threshold. For example, if the OVP threshold is 23V, the rated voltage of $C_{OUT}$ should be 50V.

## Ordering Information

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW32105CSR | -40°C ~ 85°C | WLCSP 2.54mm×1.49mm ×0.555mm -15B | GMAF | MSL1 | ROHS+HF | 9000 units/ Tape and Reel |



## Absolute Maximum Ratings (NOTE 1)

| PARAMETERS | | RANGE |
|---|---|---|
| Supply voltage range IN | | -0.3V to 29V |
| Input voltage range | OVLO, ENB | -0.3V to 29V |
| Output voltage range | OUT | -0.3V to 27V |
| | ACK | -0.3V to 6V |
| Continuous current of switch IN-OUT(NOTE2) | | 5A |
| Peak switch current on IN and OUT pin(10ms) (NOTE2) | | 8A |
| Junction-to-ambient thermal resistance $\theta_{JA}$ | | 72°C /W |
| Maximum operating junction temperature $T_{JMAX}$ | | 150°C |
| Operating free-air temperature range | | -40°C to 85°C |
| Storage temperature $T_{STG}$ | | -65°C to 150°C |
| Lead temperature (soldering 10 seconds) | | 260°C |
| ESD | | |
| Human Body Model (All pins, per ESDA/JEDEC JS-001-2017) | | ±2kV |
| Charged Device Model (All pins, per ESDA/JEDEC-JS-002-2018) | | ±1.5kV |
| IEC61000-4-2 system ESD on IN pin with 1μF $C_{IN}$ | Contact discharge | ±8kV |
| | Air gap discharge | ±15kV |
| Latch-Up | | |
| Test condition: JESD78E | | ±200mA |
| Surge | | |
| IEC61000-4-5 test with 2Ω equivalent series resistance | | ±100V |

*NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

*NOTE2: Limited by thermal design.*

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Input DC voltage | 3.1 | | 28 | V |
| $V_{OVLO\_RNG}$ | OVP threshold adjustable range | 4 | | 24 | V |
| $C_{IN}$ | Input capacitance | | 1 | 100 | μF |
| $C_{OUT}$ | Output load capacitance | | 1 | 100 | μF |



## Electrical Characteristics

$V_{IN}$=5V, $V_{ENB}$=0V, $C_{IN}$=1μF, $C_{OUT}$=1μF, $T_A$ = 25°C for typical values (unless otherwise noted).

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IN\_CLAMP}$ | Input clamp voltage | $I_{IN}$ = 10mA | 30 | 32.2 | | V |
| $R_{ON}$ | On resistance | $V_{IN}$ = 5V, $I_{OUT}$ = 1A, see Figure 6 | | 20 | 30 | mΩ |
| $I_Q$ | IN on-state quiescent current | $V_{IN}$ = 5V, $V_{OVLO}$ = 0V, $I_{OUT}$ = 0A | | 96 | 140 | μA |
| | | $V_{IN}$ = 20V, $V_{OVLO}$ = 0V, $I_{OUT}$ = 0A | | 193 | 260 | μA |
| $I_{SD}$ | IN on-state quiescent current | $V_{ENB}$ = 5V, $V_{IN}$ = 5V, $I_{OUT}$ = 0A | | 13 | 25 | μA |
| | | $V_{ENB}$ = 5V, $V_{IN}$ = 20V, $I_{OUT}$ = 0A | | 39 | 60 | μA |
| $I_{LEAK\_IN}$ | IN off-state leakage current | $V_{ENB}$ = 5V, $V_{IN}$= 5V, $V_{OUT}$=0V | | 13 | 25 | μA |
| | | $V_{ENB}$ = 5V, $V_{IN}$ = 20V, $V_{OUT}$ = 0V | | 39 | 60 | μA |
| $I_{LEAK\_OUT}$ | OUT off-state leakage current | $V_{ENB}$ = 5V, $V_{OUT}$ = 5V, $V_{IN}$ = 0V | | 2.2 | 8 | μA |
| | | $V_{ENB}$ = 5V, $V_{OUT}$ =20V, $V_{IN}$ = 0V | | 25 | 45 | μA |
| $I_{LEAK\_RCP}$ | RCP leakage current | $V_{ENB}$ = 0V, $V_{OUT}$ = 5V, $V_{IN}$ = 0V | | 2.2 | 8 | μA |
| $I_{IN\_OVLO}$ | Input current at over-voltage condition | $V_{IN}$ = 5V, $V_{OVLO}$ = 3V, $V_{OUT}$ = 0V | | 90 | 140 | μA |
| $V_{OVLO\_TH}$ | OVLO set threshold | | 1.15 | 1.20 | 1.25 | V |
| $V_{OVLO\_SEL}$ | External OVLO select threshold | OVLO rising | 0.19 | 0.26 | 0.33 | V |
| | | Hysteresis | | 0.06 | | V |
| $I_{LEAK\_OVLO}$ | OVLO pin leakage current | $V_{OVLO}$ = $V_{OVLO\_TH}$ | -0.2 | | 0.2 | μA |
| **Protection** | | | | | | |
| $V_{IN\_OVLO}$ | OVP trip level | $V_{IN}$ rising | 22.5 | 23 | 23.5 | V |
| | | Hysteresis | | 0.45 | | V |
| $V_{IN\_UVLO}$ | UVLO trip level | $V_{IN}$ rising | | 2.95 | 3.08 | V |
| | | Hysteresis | | 0.1 | | V |
| $V_{trig}$ | RCP trigger voltage | $V_{trig}$ = $V_{OUT}$-$V_{IN}$ | 15 | 35 | 55 | mV |
| $T_{SDN}$ | Shutdown temperature | | | 150 | | °C |
| $T_{SDN\_HYS}$ | Shutdown temperature hysteresis | | | 20 | | °C |



## Electrical Characteristics (Continued)

$V_{IN}$=5V, $C_{IN}$=1μF, $C_{OUT}$=1μF, $T_A$ = 25°C for typical values (unless otherwise noted).

| Symbol | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Digital Logical Interface** | | | | | | | |
| $V_{OL}$ | ACK output low voltage | $I_{SINK}$ = 6mA | | | | 0.5 | V |
| $I_{LEAK\_ACK}$ | ACK leakage current | $V_{IO}$ = 5V, ACK de-asserted | | -0.5 | | 0.5 | μA |
| $V_{IH}$ | ENB input high voltage | | | 0.8 | | | V |
| $V_{IL}$ | ENB input low voltage | | | | | 0.4 | V |
| $I_{LEAK\_ENB}$ | ENB leakage current | $V_{ENB}$ = 5V, $V_{IN}$= 0V | | | | 1 | μA |
| $R_{ENB}$ | ENB pull-down resistance | $V_{ENB}$ = 2V, $V_{IN}$ = 5V | | | 1 | | MΩ |
| **Timing Characteristics (see Figure 7 and Figure 8)** | | | | | | | |
| ten | Enable Time | From ENB to $V_{OUT}$ = 10% of $V_{IN}$; (Including 15ms debounce time); $V_{IN}$ = 5V; $C_{OUT}$ = 100μF; $R_{LOAD}$ = 100Ω | | | 16 | | ms |
| $t_{TLH}$ | VOUT rise time | $V_{OUT}$ from 10% to 90% $V_{IN}$; $C_{OUT}$ = 100μF; $R_{LOAD}$ = 100Ω | $V_{IN}$ = 5V | | 2.5 | | ms |
| | | | $V_{IN}$ = 20V | | 2 | | ms |
| $t_{OFF\_OVP}$ | The delay time between $V_{IN}$ over voltage and switch turn-off | $C_{OUT}$= 1μF, $R_L$= 100Ω, OVLO=GND, $V_{IN}$ > $V_{IN\_OVLO}$ to $V_{OUT}$ stop rising, $V_{IN}$ initial 20V, 85V surge test, $T_A$=25℃ | | | 50 | | ns |
| $t_{degl}$ | RCP de-glitch time | From $V_{OUT}$>$V_{IN}$+35mV to switch off | | | 3.6 | | ms |
| $t_{dis(RCP)}$ | RCP turn off time | From $V_{OUT}$>$V_{IN}$+88mV to switch off | | | 10 | | μs |
| $t_{ON}$ | turn-on time | ENB to $V_{OUT}$ = 90% $V_{IN}$; $C_{OUT}$ = 100μF; $R_{LOAD}$ = 100Ω | $V_{IN}$ = 5V | | 19 | | ms |
| | | | $V_{IN}$ = 20V | | 17 | | ms |
| $t_{START}$ | Start-up time | ENB to ACK low; $C_{OUT}$ = 100μF; $R_{LOAD}$ = 100Ω | | | 30 | | ms |
| $t_{OFF}$ | turn-off time | ENB to $V_{OUT}$ = 10% $V_{IN}$; $C_{OUT}$ = 100μF; $R_{LOAD}$ = 100Ω | $V_{IN}$ = 5V | | 23 | | ms |
| | | | $V_{IN}$ = 20V | | 23 | | ms |

## Waveforms and Test Circuits

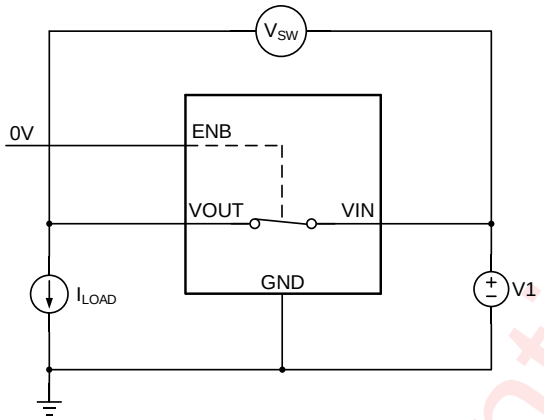



**Figure 6 On resistance Measurement Test Circuit**

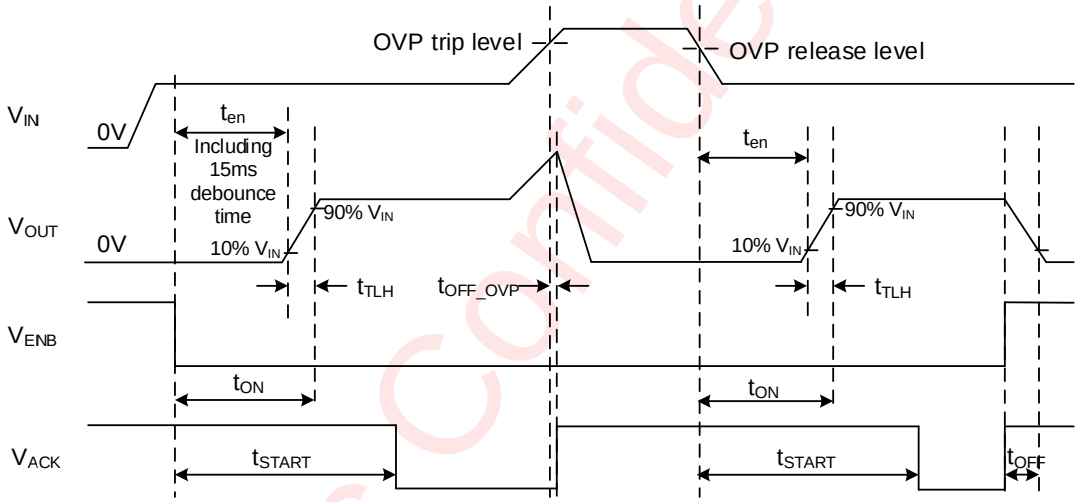
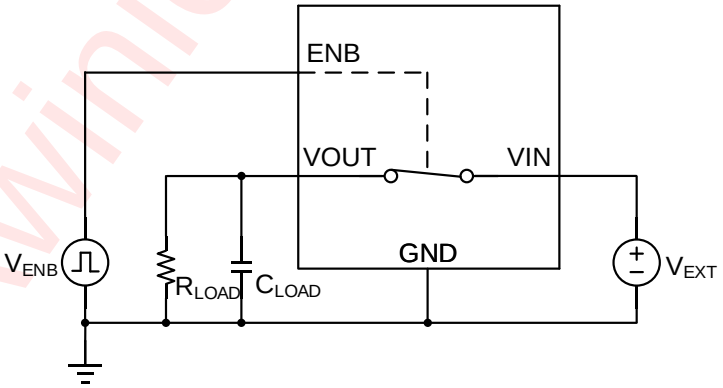



**Figure 7 Operating Waveforms and Timing Definitions**




Test condition are $V_{IN}$=3.1V to 20V, $C_{LOAD}$=100μF, $R_{LOAD}$=100Ω, where:

$R_{LOAD}$=Load resistance.

$C_{LOAD}$=Load capacitance.

$V_{EXT}$=External voltage source applied to VIN pin for measurements.

**Figure 8 Waveform and Timing Measurements Test Circuit**



# Typical Characteristics

Ambient temperature is 25°C, $V_{IN}$ =5V, $V_{ENB}$=0V, $V_{OVLO}$=0V, $C_{IN}$ = $C_{OUT}$=1μF, unless otherwise noted.

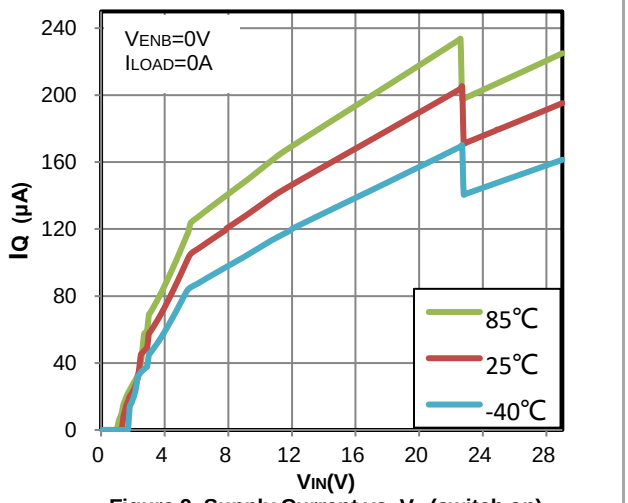



Figure 9 Supply Current vs. $V_{IN}$(switch on)

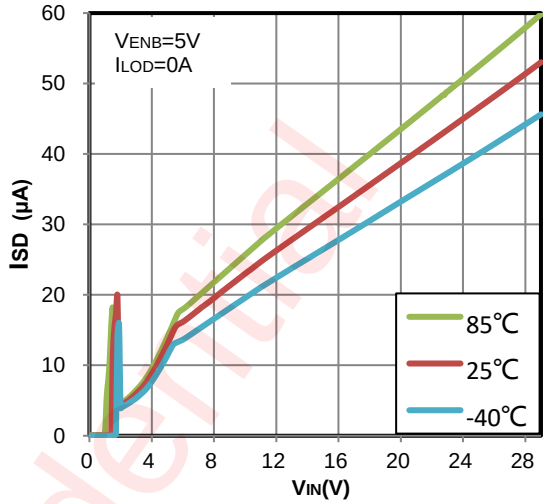



Figure 10 Supply Current vs. $V_{IN}$(switch off)

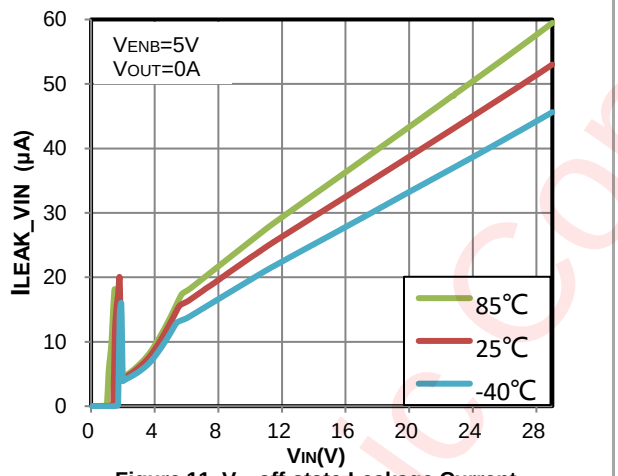



Figure 11 $V_{IN}$ off-state Leakage Current

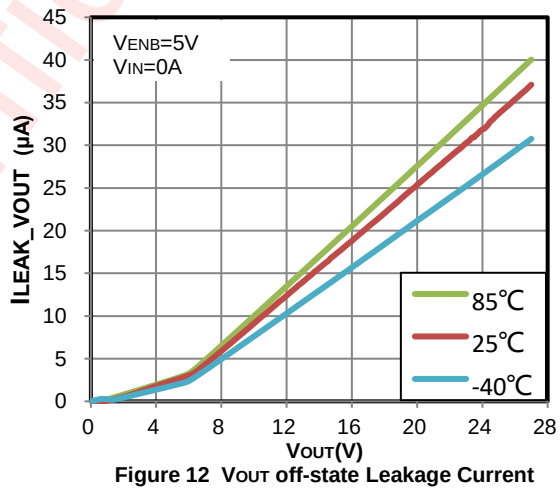



Figure 12 $V_{OUT}$ off-state Leakage Current

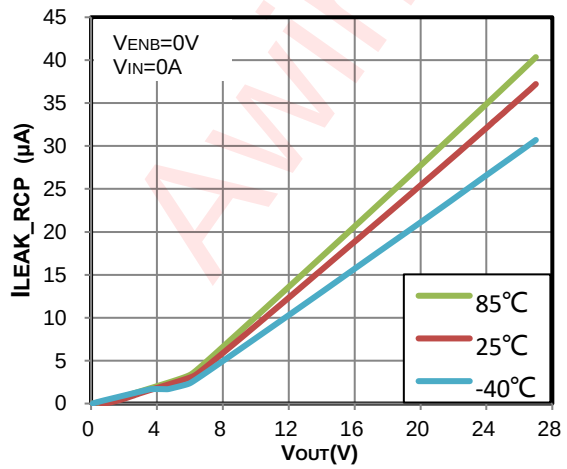



Figure 13 RCP leakage Current vs. $V_{OUT}$

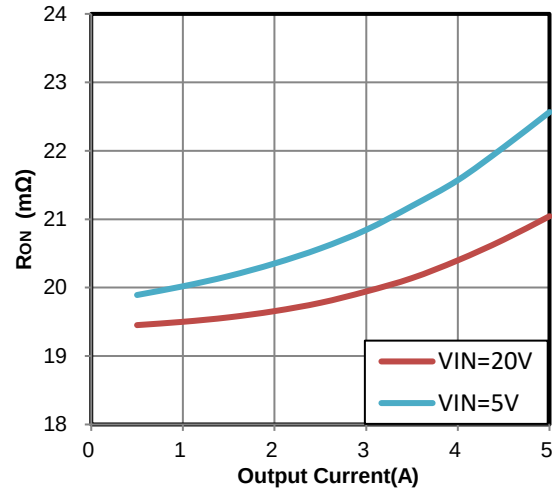



Figure 14 $R_{ON}$ vs. Output Current



## Typical Characteristics (Continued-1)

Ambient temperature is 25°C, $V_{IN}$ =5V, $V_{ENB}$=0V, $V_{OVLO}$=0V, $C_{IN}$ = $C_{OUT}$=1μF, unless otherwise noted.

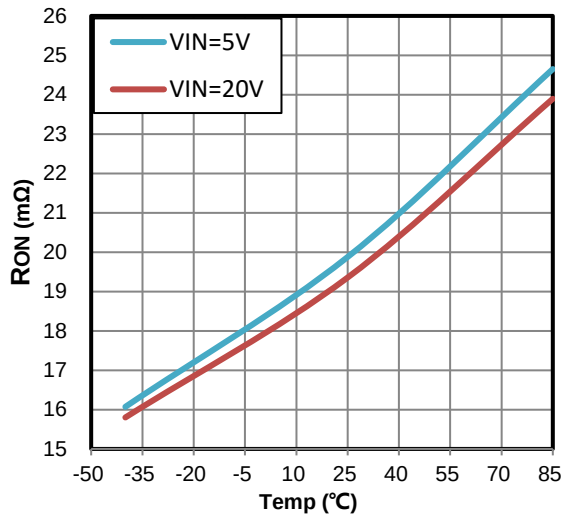



Figure 15 RON vs. Temperature

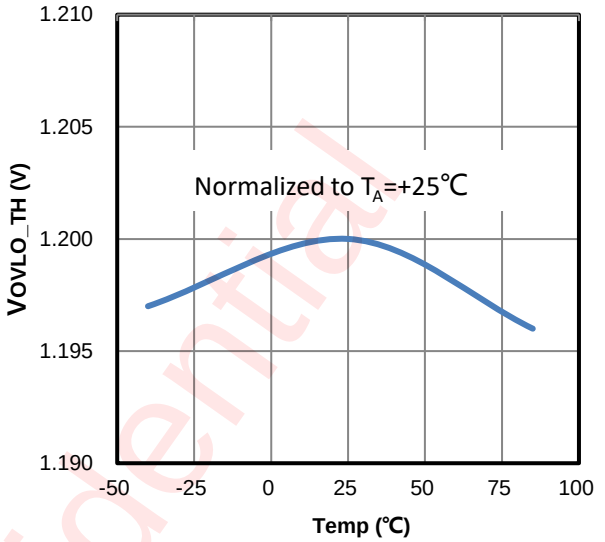



Figure 16 OVLO set threshold vs. Temperature

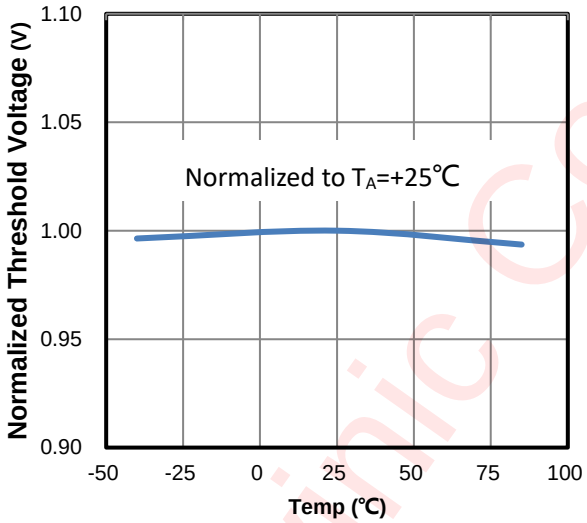



Figure 17 OVP threshold vs. Temperature

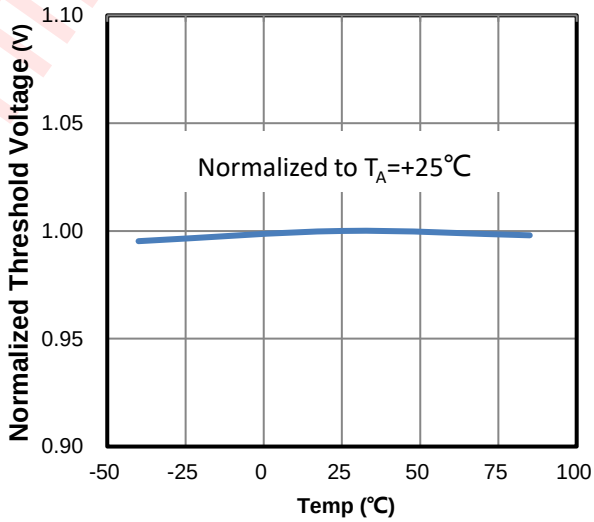



Figure 18 UVLO threshold vs. Temperature

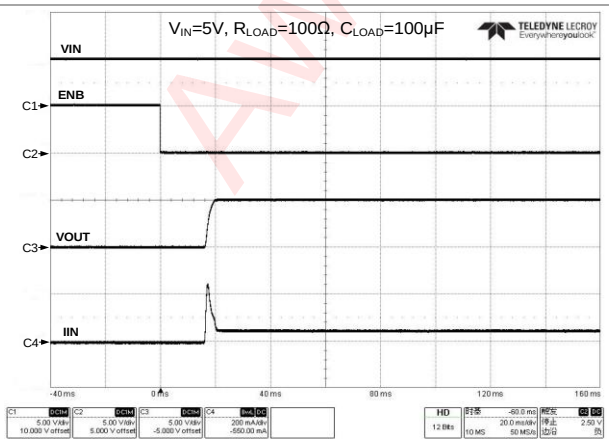



Figure 19 Turn-On Time and Inrush Current at 5V

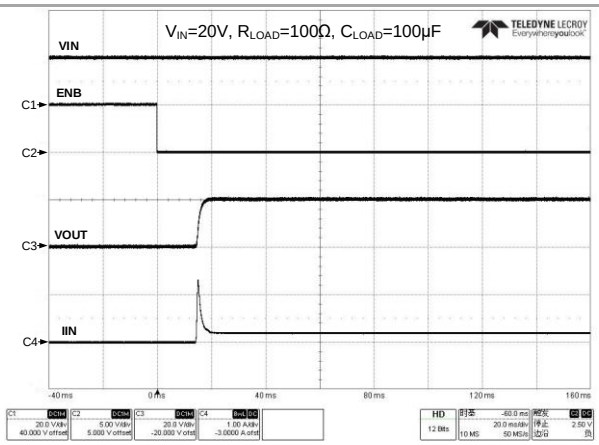



Figure 20 Turn-On Time and Inrush Current at 20V

## Typical Characteristics (Continued-2)

Ambient temperature is 25°C, $V_{IN}$ =5V, $V_{ENB}$=0V, $V_{OVLO}$=0V, $C_{IN}$ = $C_{OUT}$=1μF, unless otherwise noted.

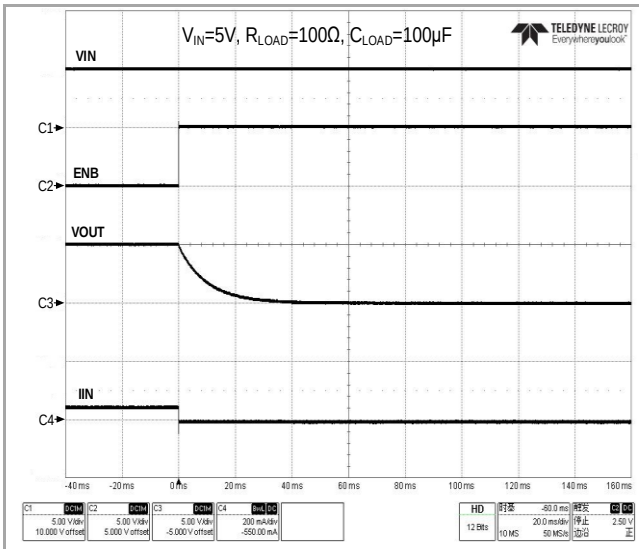



Figure 21 Turn-Off Time at 5V

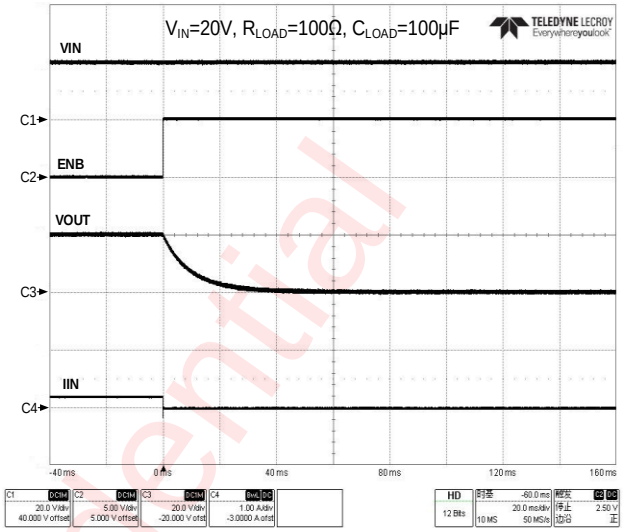



Figure 22 Turn-Off Time at 20V

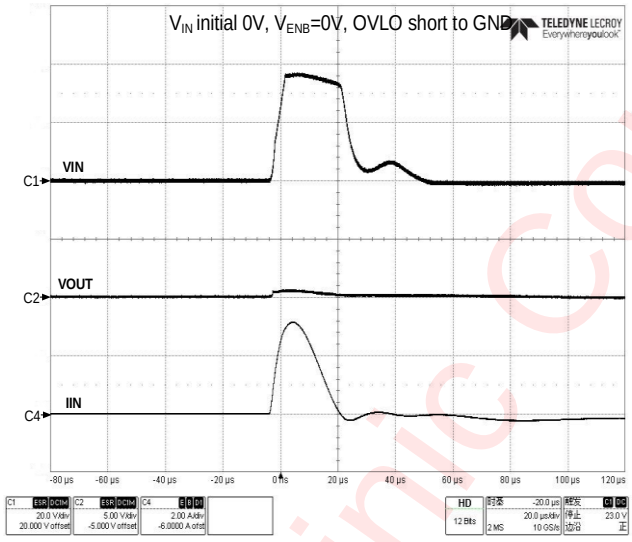



Figure 23 100V Surge Voltage with Device

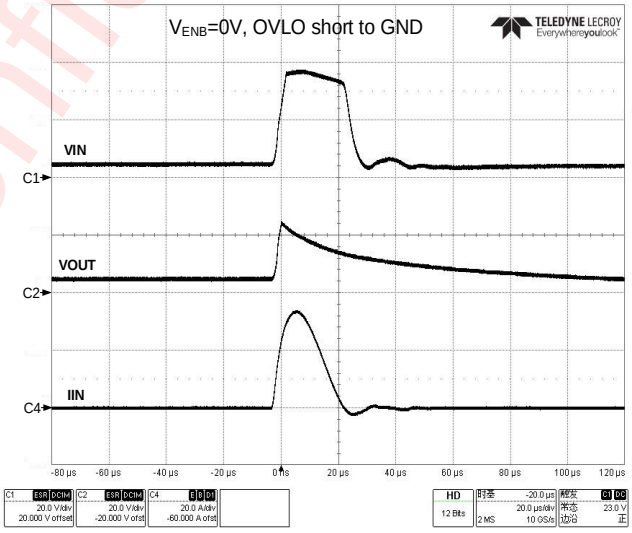



Figure 24 Surge Voltage with Device at VIN=5V

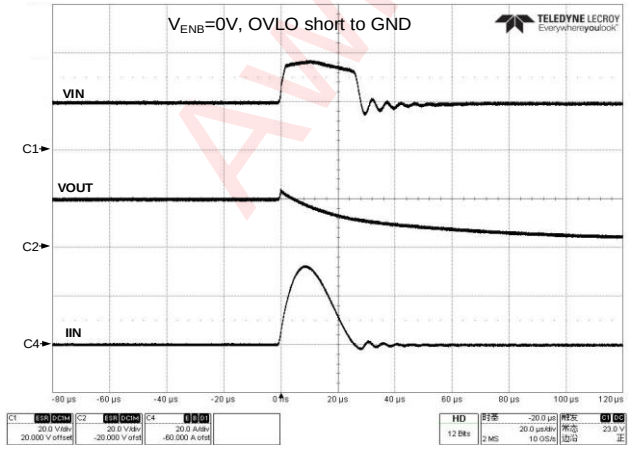



Figure 25 Surge Voltage with Device at VIN=20V



# Functional Description

## Device Operation

If the AW32105 is enabled and the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on. ACK will be driven low about 30ms after VIN valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 50ns. If ENB is pulled high, or input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

Table1. AW32105 Function and Logic Table

| ENB | VIN | VOUT | ACK | Operation Mode |
|---|---|---|---|---|
| L | $<V_{IN\_UVLO}$ | X | Hi-Z | Under-voltage lockout, switch open. (UVLO fault) |
| L | $V_{IN\_UVLO}<V_{IN}<V_{IN\_OVLO}$ | X | L | Enabled, switch closed, charging path on. (Normal on) |
| L | X | X | Hi-Z | Over-temperature protection, switch open. (OTP fault) |
| L | $>V_{IN\_OVLO}$ | X | Hi-Z | Over-voltage lockout, switch open. (OVP or OVLO fault) |
| H | X | X | Hi-Z | Disable, switch open. (Normal off) |
| X | X | $V_{OUT}>V_{IN}$ | Hi-Z | Reverse current protection, switch open. (RCP fault) |

Note: H=logic high level, L=logic low level, Hi-Z=high-impedance(off-state), X= don't care.

## Surge Protection

The AW32105 integrates a clamp circuit to suppress input surge voltage. For surge voltages between $V_{IN\_OVLO}$ and $V_{IN\_CLAMP}$, the switch will be turned off but the clamp circuit will not work. For surge voltages greater than $V_{IN\_CLAMP}$, the internal clamp circuit will detect surge voltage level and discharge the surge energy to ground. The device can suppress surge voltages up to 100V.

## Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until $V_{IN}$ falls below the OVP falling trip level.

## OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

For example, if we select $R_1$ = 1MΩ and $R_2$ = 100kΩ, then the new OVP threshold calculated from the above formula is 13.2V. The OVP threshold adjustment range is from 4V to 24V. When the OVLO pin voltage $V_{OVLO}$ exceeds $V_{OVLO\_SEL}$ (0.26V typical), $V_{OVLO}$ is compared with the reference voltage $V_{OVLO\_TH}$ (1.2V typical) to judge whether input supply is over-voltage.

## ACK Output

The device features an open-drain output ACK, it should be connected to the system I/O rail through a pull-up



resistor. If the device is enabled and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$, ACK will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, or ENB is pulled high, the switch will be turned off and ACK will be pulled high. The pull up resistor value is recommended to be 10KΩ to 200KΩ.

### Reverse Current Protection

AW32105 has all time reverse current protection regardless of the ENB logic level. Once the voltage on $V_{OUT}$ is higher than $V_{IN}$ for 35mV, the RCP circuit is triggered after a 3.6ms de-glitch time. If the voltage gap is greater than 88mV, RCP triggers disables the power switch.

During the startup deglitch time, if the device detects the $V_{OUT}$ voltage is higher than $V_{IN}$ by 35mV, the power switch does not turn on.

The RCP circuit helps by providing the capability of parallel connection of two USB charging ports to a single charger input, without backward leakage.



# Application Information

### Capacitors Selection

$C_{IN}$ = 1μF, $C_{OUT}$ = 1μF is recommended for typical application, larger $C_{IN}$, $C_{OUT}$ is also acceptable.

The rated voltage of $C_{IN}$ should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW32105 is used, the rated voltage of $C_{IN}$ should be 50V. The rated voltage of $C_{OUT}$ should be larger than the OVP threshold. For example, if the OVP threshold is 23V, the rated voltage of $C_{OUT}$ should be 35V or higher. The recommended value of capacitors and boundary values can refer to the following table:

| Capacitor | Typical Value (μF) | Boundary Value (μF) |
|---|---|---|
| $C_{IN}$ | 1 | 0.1~100 |
| $C_{OUT}$ | 1 | 0.1~100 |

### Resistors Selection

The default OVLO voltage is 23V, when using default OVP threshold, it is recommended to connect OVLO to ground or through 0Ω resistor. When $R_1$ and $R_2$ are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision. When ($R_1$+$R_2$) is larger, the clamping voltage of OUT is smaller. It is recommended to select $R_1$ = 1MΩ, $R_2$ can calculate the value according to the required OVP threshold. The calculation formula is as follows: the typical value of $V_{OVLO\_TH}$ is 1.2V, and the adjustable range of $V_{IN\_OVLO}$ is 4V ~ 24V.

$$V_{IN\_OVLO} = \frac{R_1+R_2}{R_2} V_{OVLO\_TH}$$

The recommended value of resistors and boundary values can refer to the following table:

| Resistor | Typical Value (Ω) | Boundary Value (Ω) |
|---|---|---|
| $R_1$ | 1M | 1K~10M |
| $R_2$ | 100K | Determined by $R_1$ |

### TVS (if used)

First of all, the working voltage of TVS should be determined. TVS with $V_{RWM}$ ≥ 10V can be selected for 5V charging port, TVS with $V_{RWM}$ ≥ 12V can be selected for 9V charging port, and TVS with $V_{RWM}$ ≥ 24V can be selected for 20V charging port. Secondly, it is necessary to meet the requirement of surge protection capability. Assuming that the customer wants to select a TVS with a voltage of 300V, the TVS should meet the requirement of $I_{PP}$ ≥ 300V / 2 Ω = 150A. When selecting the model of external TVS, the maximum clamping voltage of the TVS should be below **30V**. Too high clamping voltage of TVS will cause damage to OVP chip.



## PCB Layout Consideration

To make fully use of the performance of AW32105, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor $C_{IN}$ on the top layer (same layer as the AW32105) and close to IN pin, and place the output capacitor $C_{OUT}$ on the top layer (same layer as the AW32105) and close to OUT pin.

2. If external TVS is used, IN pin routing passes through the external TVS firstly, and then connect AW32105.

3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

4. If $R_1$ and $R_2$ are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.

5. The power trace from USB connector to AW32105 may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.

6. Use rounded corners on the power trace from USB connector to AW32105 to decrease EMI coupling.

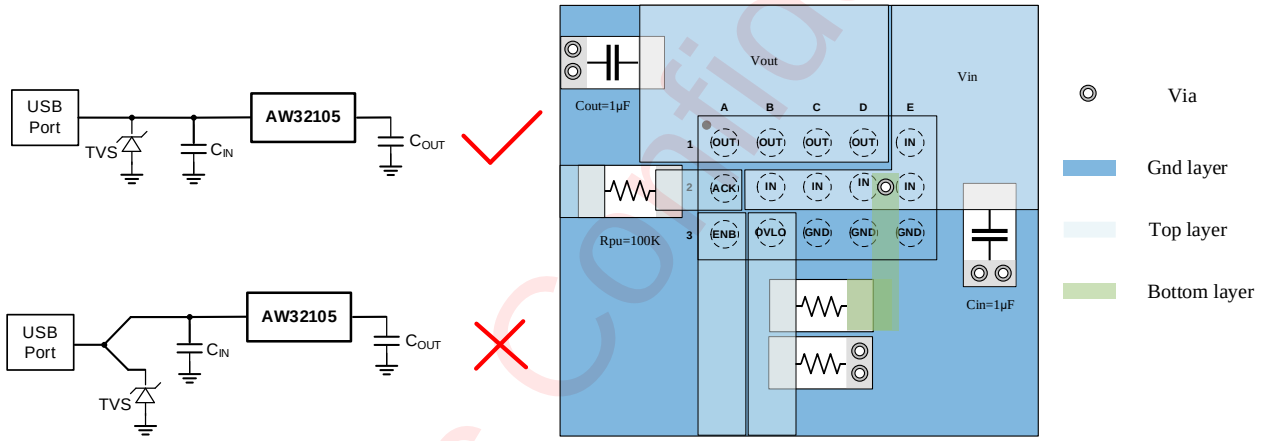


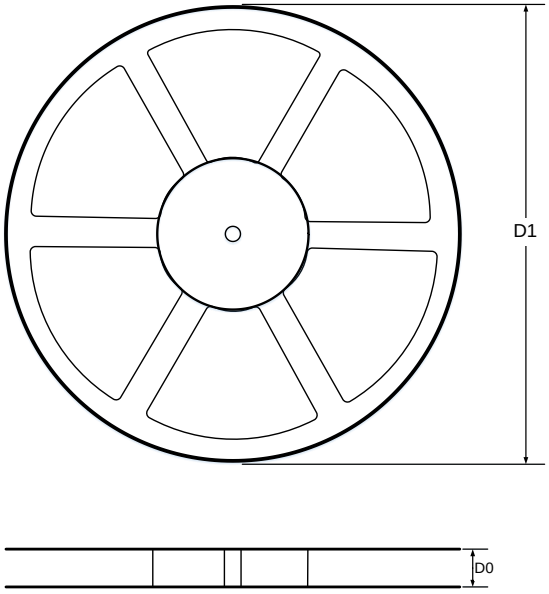

**Figure 26 External Components Placements and PCB Layout Example**



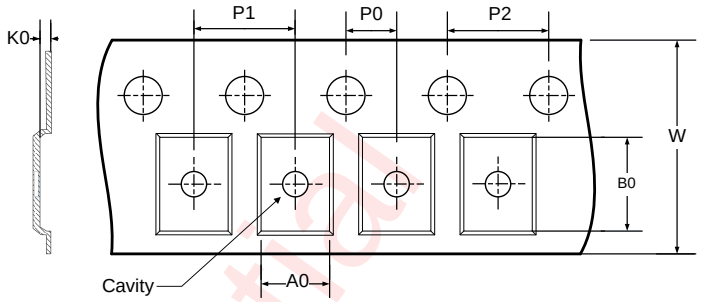
 

# Tape and Reel Information

REEL DIMENSIONS

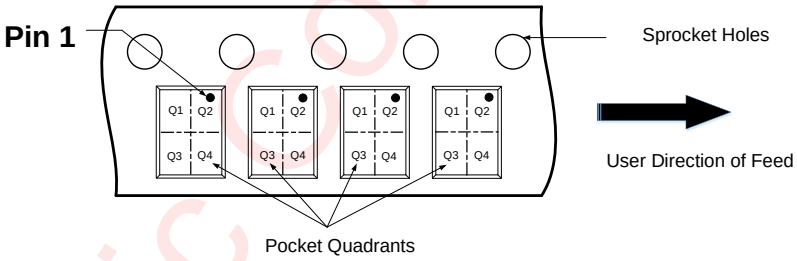



TAPE DIMENSIONS




A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

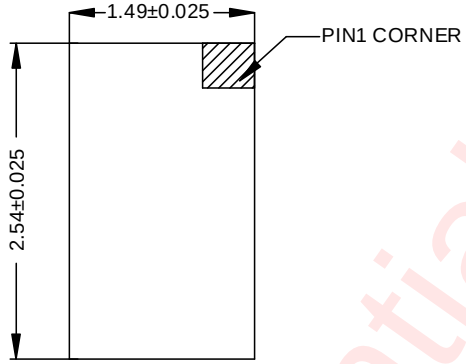
| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| 330 | 12.5 | 1.7 | 2.72 | 0.72 | 2 | 4 | 4 | 12 | Q2 |

**All dimensions are nominal**

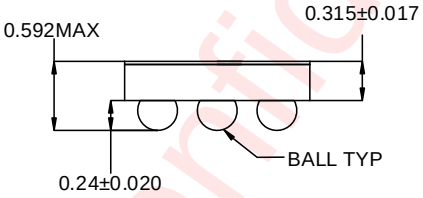


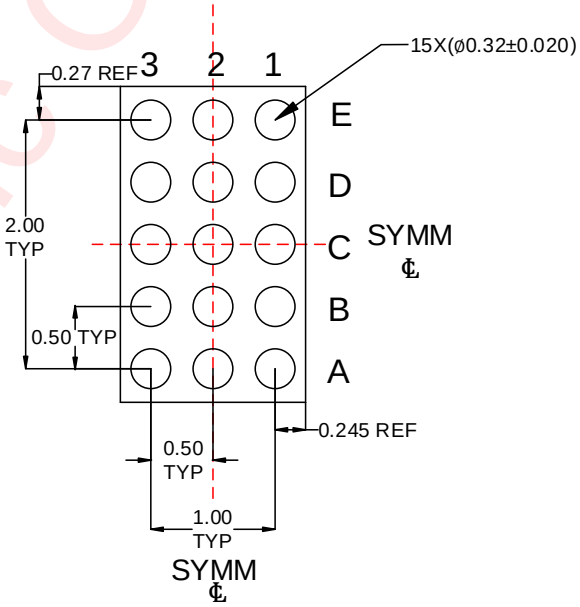
## Package Description




Top View




Side View



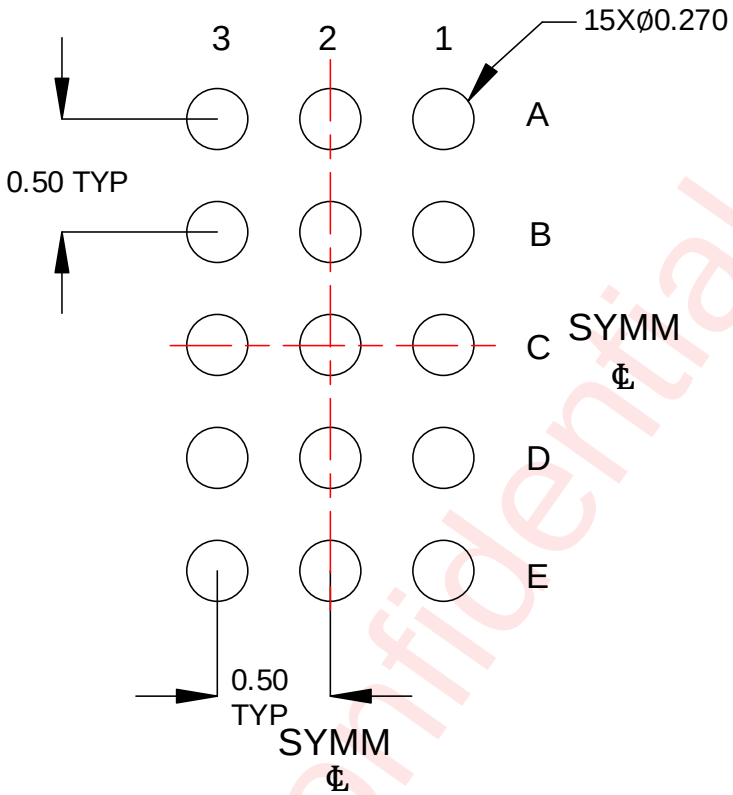

Bottom View

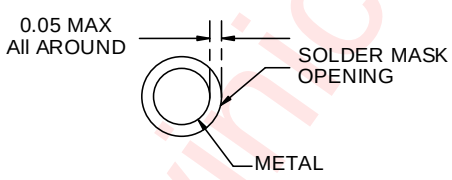
Unit:mm



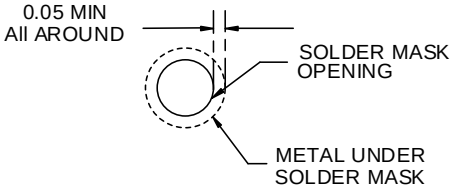
 

## Land Pattern Data




NON-SOLDER MASK DEFINED




SOLDER MASK DEFINED

Unit: mm



# Revision History

| Version | Date | Change Record |
|---|---|---|
| V1.0 | Jan. 2022 | Datasheet V1.0 released. |
| V1.1 | Jul. 2024 | Added air gap discharge ESD capability. |



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