Power Distribution Switch with Adjustable Current Limit

Features

- Integrated P-channel MOSFET power switch
- Input voltage: 2.5V to 5.5V
- 0.4~2.5A adjustable current Limit:
- Switch on-resistance(typ.):
  Rdson=65mΩ at V_{IN}=5V
- ±9% current limit accuracy at 1A(typ.)
- Reverse current protection
- Internal EN pull-down resistor
- Under voltage lockout
- Over temperature protection
- Quick Output Discharge(QOD)
  - ✧ AW35015CD/AW35065CD: Auto QOD
  - ✧ AW35015C/AW35065C: No QOD
- SOT23-5L package
- Certificated by UL(AW35015C/AW35015CD)
  UL 62368-1: 2021, file no. E532659

General Description

The AW35015CD/15C/65CD/65C is a P-channel MOSFET power distribution switch which intended for high-side load-switching applications. The device integrates adjustable current limit function with an external resistor from ISET pin to ground.

The AW35015CD/15C/65CD/65C also features fast short-circuit response, under voltage lockout, over temperature protection, reverse current protection. The AW35015CD and AW35065CD builds in quick output discharge function.

Set adjustable current limit:

AW35015CD AW35015C	I_{LIMIT}=6800/R_{SET}
AW35065CD AW35065C	I_{LIMIT}=26000/R_{SET}

Applications

USB Ports

Power Distribution Switch

Notebook and Desktop Computer

High-Definition Television(HDTV)

Typical Application Circuit

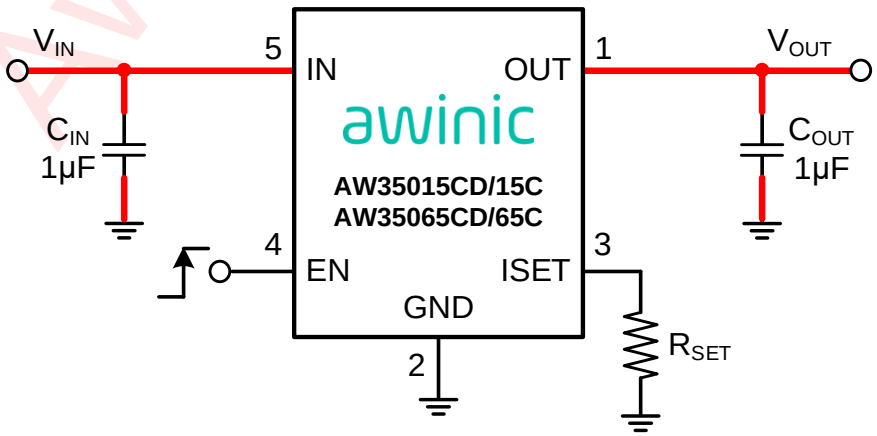
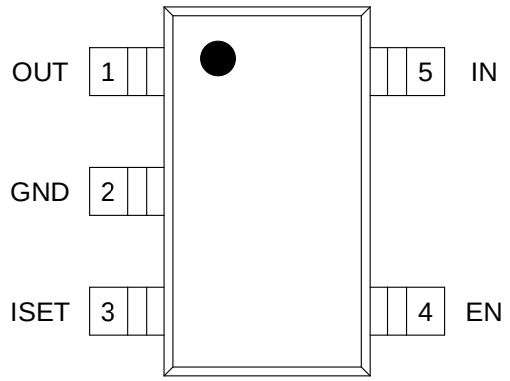


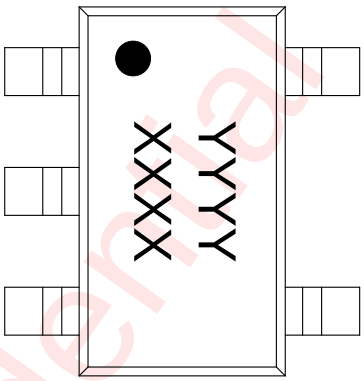
Figure 1 Typical Application Circuit of AW35015CD/15C/65CD/65C

Pin Configuration And Top Mark

AW35015CD/15C/65CD/65CSTR
(Top view)



AW35015CD/15C/65CD/65CSTR
Marking
(Top view)



YYYY - AW35015CD/AW35015CSTR
AW35065CD/AW35065CSTR
XXXX - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
1	OUT	Output pin
2	GND	Ground
3	ISET	Current limit threshold setting pin
4	EN	Chip enable (Active High)
5	IN	Power supply input

Functional Block Diagram

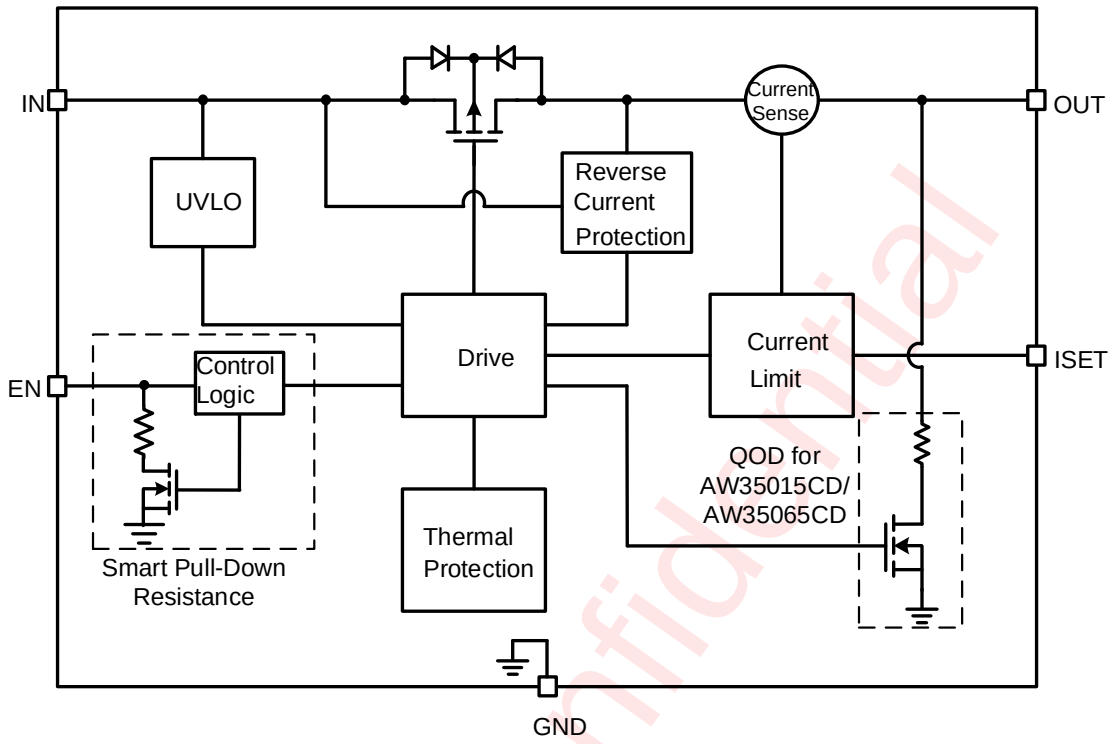


Figure 3 Functional Block Diagram

Typical Application Circuits

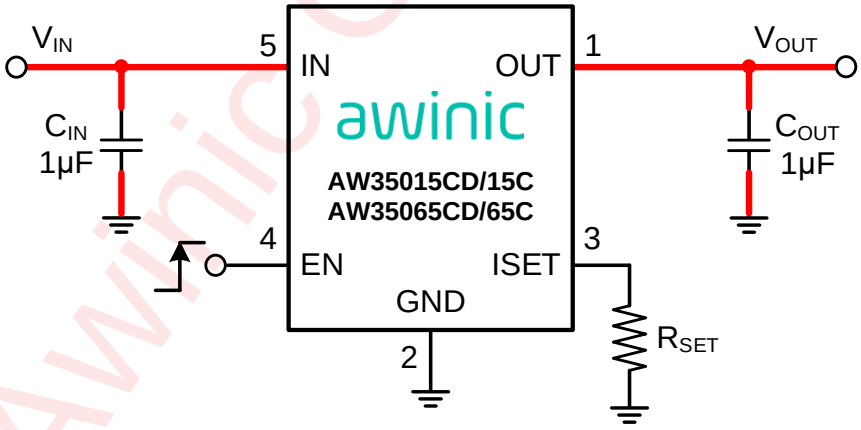


Figure 4 Typical Application Circuit of AW35015CD/15C/65CD/65C

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35015CDSTR	-40°C ~ 85°C	SOT23-5L	D9LU	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35015CSTR	-40°C ~ 85°C	SOT23-5L	1XTE	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35065CDSTR	-40°C ~ 85°C	SOT23-5L	AFAV	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35065CSTR	-40°C ~ 85°C	SOT23-5L	0LCC	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
EN Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current for V_{IN} ≥ 2.5V(NOTE 2)		2.5A
Maximum Peak Switch Current for V_{IN} ≥ 2.5V(NOTE 3)		3A
Junction-to-ambient thermal resistance θ_{JA}(NOTE 4)		158.9°C/W
Junction-to-case thermal resistance θ_{JC}		57°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 5)		±2kV
CDM(Charged Device Model) (NOTE 6)		±1.5kV
Latch-Up		
Test Condition: JEDEC78E		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	2.5		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance	0.1	1		μF

Electrical Characteristics

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 1μF, I_{IN}≤ 2.5A.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Input quiescent current	V_{IN}=5.0V, V_{EN}=5.0V, I_{OUT}=0A			30		μA
I_{SD}	Shutdown current from IN to GND	V_{IN}=5.0V, V_{EN}=0V			0.32	1	μA
I_{LEAKEN}	EN pin leakage current	V_{IN}=0V, V_{EN}=5.5V			0.52	1	μA
POWER SWITCH							
R_{dson}	Internal switch MOSFET on-state resistance	V_{IN}=5.0V, V_{EN}=high, I_{OUT}=500mA			65		mΩ
R_{EN}	EN pin pull down resistor	V_{IN}=5V, V_{EN}=0.1V			9.2		MΩ
R_{DIS}	Output discharge resistance	V_{IN}=5.0V, V_{EN}=low, I_{OUT} Sinking 2mA (for AW35015CD/AW35065CD)			75		Ω
t_R	Output rise time	V_{IN}=5.0V, C_{OUT}=1μF, R_L=100Ω		1.0	1.5	2.0	ms
t_{ON}	Switch turn on time			1.5	2.3	3.2	ms
t_F	Output fall time	V_{IN}=5.0V, C_{OUT}=1μF, R_L=100Ω	AW35015C/AW35065C		120		μs
			AW35015CD/AW35065CD		93		μs
t_{OFF}	Switch turn off time		AW35015C/AW35065C		130		μs
			AW35015CD/AW35065CD		99		μs
V_{IH}	EN input high threshold level			1.4			V
V_{IL}	EN input low threshold level					0.4	V
CURRNET LIMIT							
I_{LIMIT}	Current limit threshold	VOUT=4V	R_{SET}=2.72kΩ for AW35015CD/15C R_{SET}=10.4kΩ for AW35065CD/65C	2000	2500	3000	mA
			RSET=3.4kΩ for AW35015CD/15C R_{SET}=13kΩ for AW35065CD/65C	1790	2000	2330	
			RSET=6.8kΩ for AW35015CD/15C R_{SET}=26kΩ for AW35065CD/65C	910	1000	1090	
			RSET=17kΩ for AW35015CD/15C R_{SET}=65kΩ for AW35065CD/65C	250	400	550	

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 1μF, I_{IN}≤ 2.5A.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{IOS}	Response time to short circuit	V_{IN}=5.0V		10		μs
t_{OCP}	Current limit response time	V_{IN}=5.0V, I_{OUT}=1.5 × I_{LIMIT}		100		μs
UNDER VOLTAGE LOCKOUT						
V_{UVLO}	UVLO threshold voltage	V_{IN} rising		2.3	2.5	V
V_{UVLO_HYS}	UVLO hysteresis	V_{IN} falling		95		mV
REVERSE VOLTAGE PROTECT						
V_{REV}	Reverse voltage trip point	V_{EN}=High, V_{OUT} > V_{IN}		43		mV
I_{REV}	Reverse leakage current	V_{OUT}=5V, V_{IN}=0V, V_{EN}=0V		0.68		μA
I_{REV_ACT}	Reverse activation current	V_{IN}=5V, C_{OUT}=1μF, V_{OUT} > V_{IN}		0.6		A
I_{REV_PRO}	Reverse protection current	V_{OUT} - V_{IN} > V_{REV}		5		μA
THERMAL PROTECTION						
T_{SD}	Thermal shutdown threshold			155		°C
T_{SD_HYS}	Thermal shutdown hysteresis			25		°C

Timing Diagram

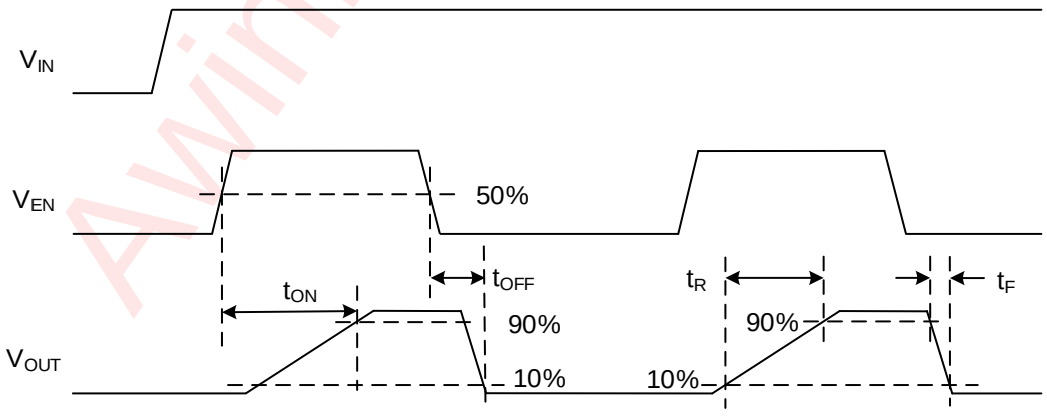


Figure 5 AW35015CD/15C/65CD/65C Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

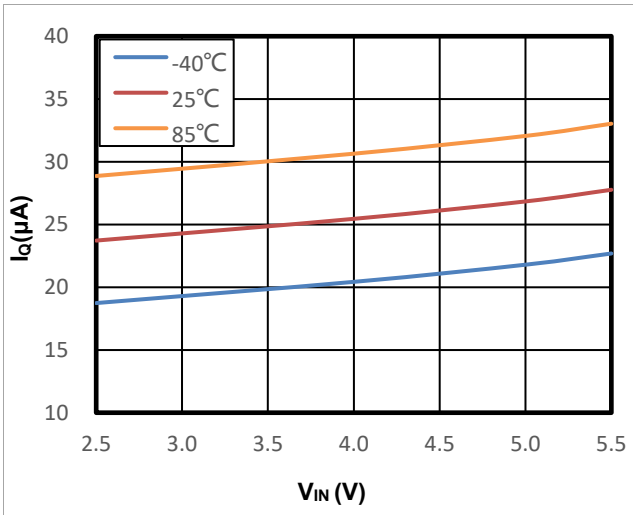


Figure 6 Quiescent Current vs. V_{IN}, No load

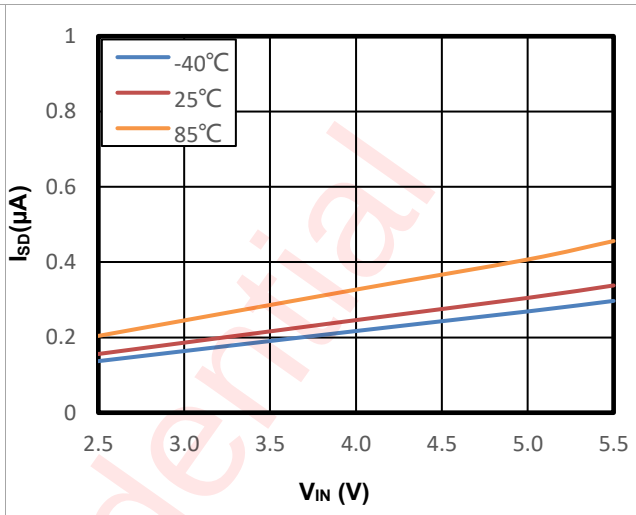


Figure 7 IN Shutdown Current vs. V_{IN}

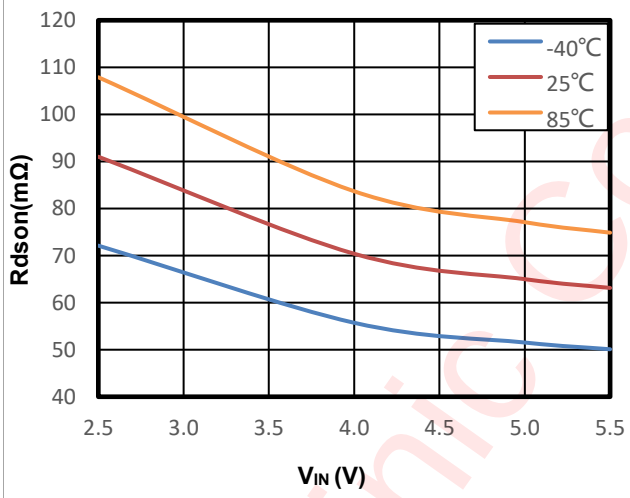


Figure 8 Rdson vs. V_{IN}(IOUT=500mA)

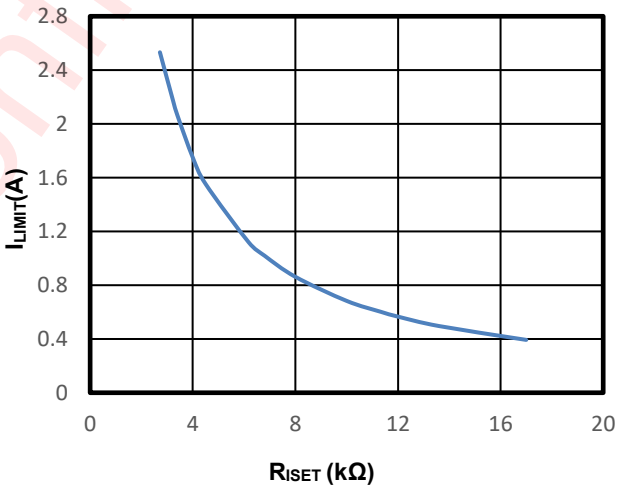


Figure 9 I_{LIMIT} vs. R_{ISET}

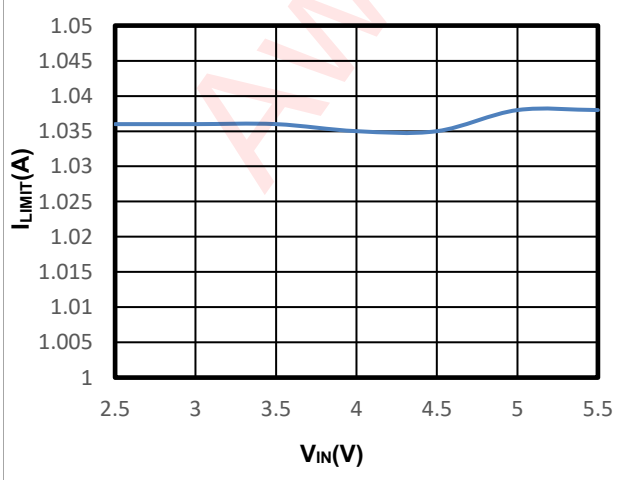


Figure 10 I_{LIMIT} vs. V_{IN}

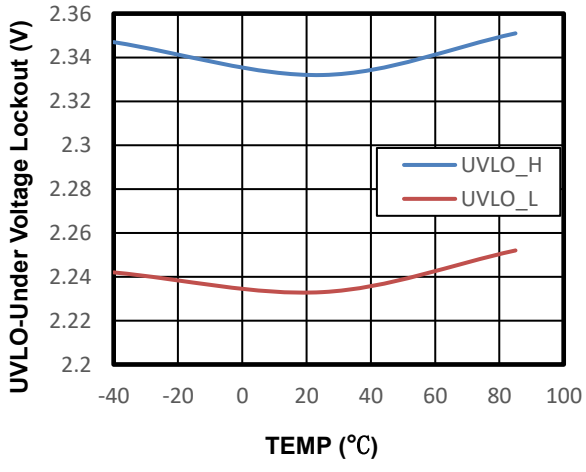
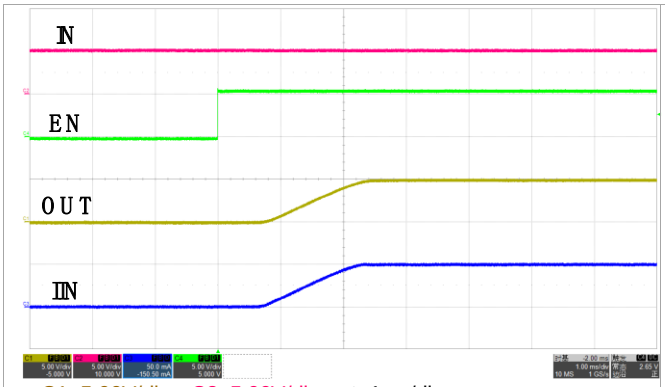


Figure 11 UVLO vs. TEMP

Typical Characteristics (continued)

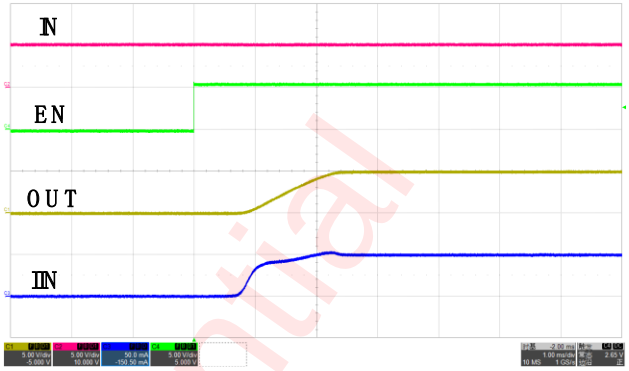
Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.



C1: 5.00V/div C2: 5.00V/div t=1ms/div
C3: 50mA/div C4: 5.00V/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=1μF，Set I_{LIMIT}=1.0A，R_L=100Ω

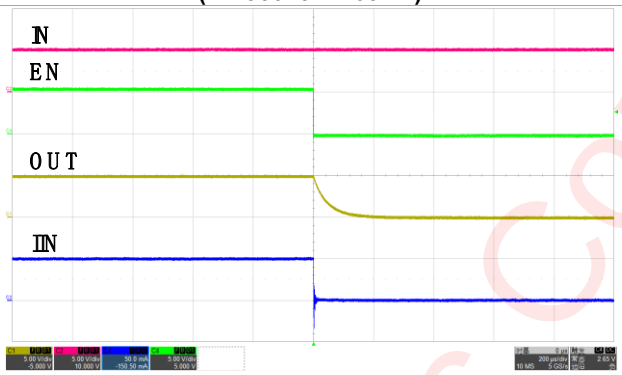
Figure 12 Turn On Response (AW35015CD/65CD)



C1: 5.00V/div C2: 5.00V/div t=1ms/div
C3: 50mA/div C4: 5.00V/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=10μF，Set I_{LIMIT}=1.0A，R_L=100Ω

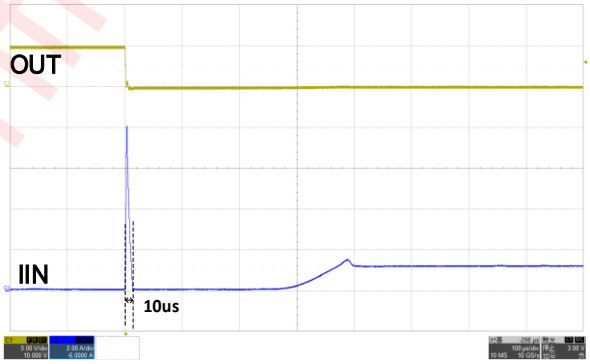
Figure 13 Turn On Response (AW35015CD/65CD)



C1: 5.00V/div C2: 5.00V/div t=200μs/div
C3: 50mA/div C4: 5.00V/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=1μF，Set I_{LIMIT}=1.0A，R_L=100Ω

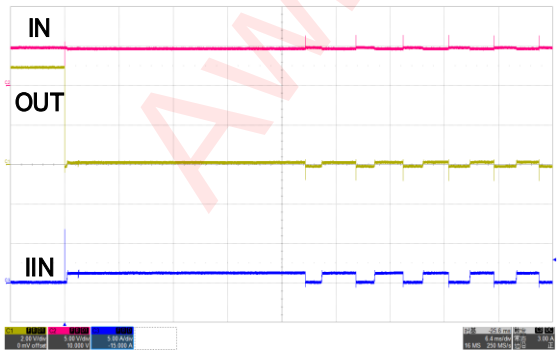
Figure 14 Turn Off Response (AW35015CD/65CD)



C1: 5.00V/div C3: 2A/div t=100μs/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=1μF，Set I_{LIMIT}=1.0A

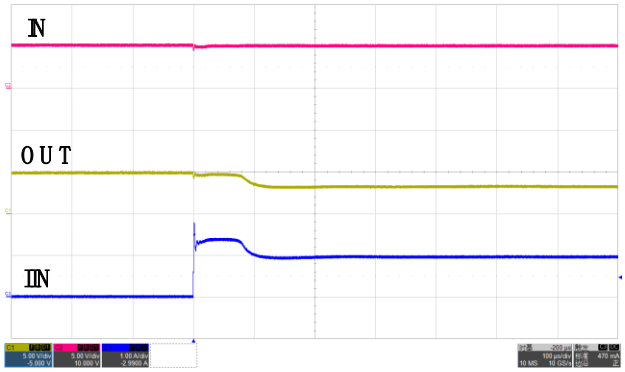
Figure 15 Short Circuit Response



C1: 2.00V/div C2: 5.00V/div t=6.4ms/div
C3: 5A/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=1μF，Set I_{LIMIT}=1.0A

Figure 16 Continuous Short Response



C1: 5.00V/div C2: 5.00V/div t=100μs/div
C3: 1A/div

V_{IN}=5V，C_{IN}=1μF，C_{OUT}=1μF，Set I_{LIMIT}=1.0A

Figure 17 Current Limit Response

Functional Description

The AW35015CD/15C/65CD/65C is a P channel MOSFET power distribution switch with current limit function. In addition, the switch also features fast short-circuit response, under voltage lockout, over temperature protection and reverse current protection.

Current Limit Threshold Setting

The AW35015CD/15C/65CD/65C provides adjustable current limit threshold which implemented by an external resistor from ISET to ground. The current limit function can prevent the switch from over current condition. The adjustable current limit value can be calculated using the following equations:

AW35015CD/AW35015C	$I_{LIMIT}=6800/R_{SET}$
AW35065CD/AW35065C	$I_{LIMIT}=26000/R_{SET}$

The minimum current limit is 400mA，beyond 2.5A is forbidden.

Fast Short Circuit Protection

The AW35015CD/15C/65CD/65C provides short circuit protection function which can limit the output current to a safe level without damaging the switch.

Under Voltage Lockout (UVLO)

The AW35015CD/15C/65CD/65C has under voltage lockout function which can disable the switch until the input voltage reaches the UVLO threshold (typical 2.3V). The UVLO threshold has a 95mV hysteresis voltage which can prevent the unwanted on/off cycling when there is noise on the input voltage.

Over Temperature Protection (OTP)

When the junction temperature exceeds 155°C, the internal OTP circuit turn off the power switch. There is a temperature hysteresis 25°C, in other words, the OTP circuit can turn on the switch only if the junction temperature is below 130°C.

Quick Output Discharge(QOD)

The AW35015CD/AW35065CD include the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is set to low level, a discharge resistance with a typical value of 75Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

Reverse Current Protection (RCP)

The AW35015CD/15C/65CD/65C includes the Reverse Current Protection(RCP) function, which can prevent the current to flowing through the P-FET or the body diode when V_{OUT} greater than V_{IN}. Whatever the switch is on or off, the AW35015CD/15C/65CD/65C always has this function. When V_{OUT}-V_{IN} greater than V_{REV}, the internal comparator quickly turns off the switch, in order to prevent large reverse current from V_{OUT} to V_{IN}. The switch will return to normal operation once the reverse voltage scenario disappeared.

The I_{REV_ACT} parameter in the figure 18 can be calculated by the following formula: $I_{REV\_ACT} = \frac{V_{REV}}{R_{dson}}$

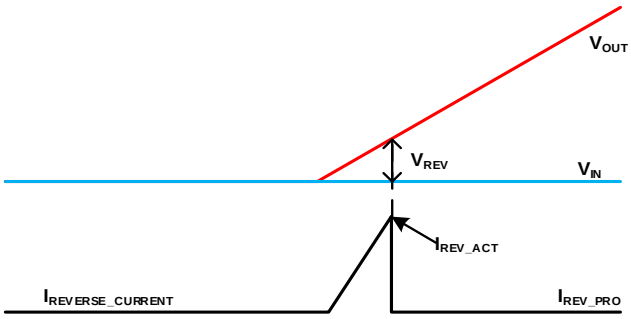


Figure 18 RCP parameter diagram

Application Information

Input and Output Capacitor Selection

Input and output capacitance improves the performance of the device, the actual capacitance should be optimized for the particular application. For all applications, a 1μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions.

Placing a 1μF or greater ceramic capacitor on the output pin is recommended when large transient currents are expected on the output.

Programming the Current-Limit Threshold

The current limit threshold is user programmable via an external resistor. The AW35015CD/15C/65CD/65C uses an internal regulation loop to provide a regulated voltage on the ISET pin. The current limit threshold is proportional to the current sourced out of ISET. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{SET}. The traces routing the R_{SET} resistor to the AW35015CD/15C/65CD/65C should be as short as possible to reduce parasitic effects on the current limit accuracy.

The following equations can be used to calculate the resulting current limit threshold for a given external resistor value (R_{SET}):

AW35015CD/AW35015C: $I_{LIMIT}=6800/R_{SET}$, where $2.72k\Omega \le R_{SET} \le 17k\Omega$.

AW35065CD/AW35065C: $I_{LIMIT}=26000/R_{SET}$, where $10.4k\Omega \le R_{SET} \le 65k\Omega$.

PCB Layout Consideration

AW35015CD/15C/65CD/65C is a low ON-Resistance power switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW35015CD/15C/65CD/65C) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35015CD/15C/65CD/65C) and close to OUT pin.

2. The AW35015CD/15C/65CD/65C integrates an up to 2.5A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths on figure 19 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

3. Use rounded corners on the power trace from the power supply connector to AW35015CD/15C/65CD/65C to decrease EMI coupling.

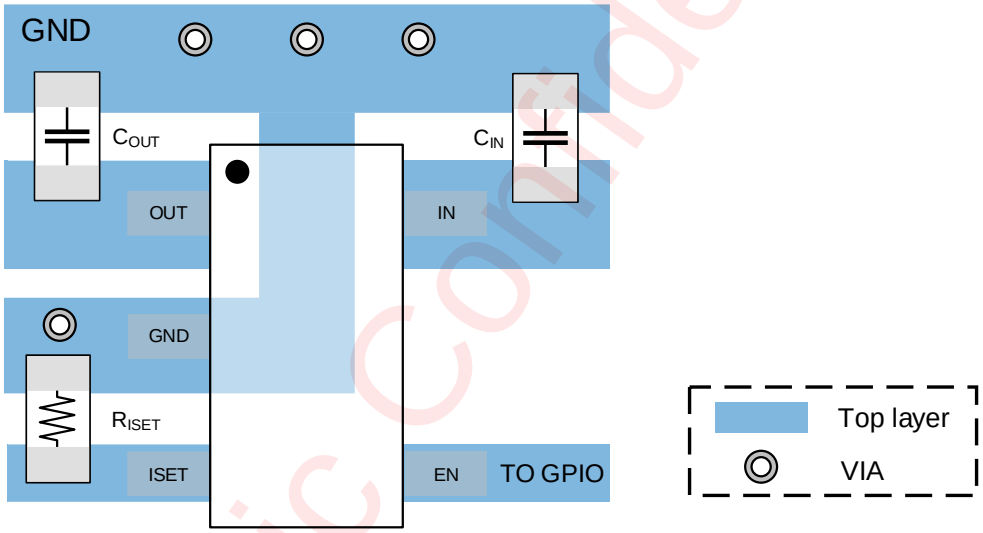
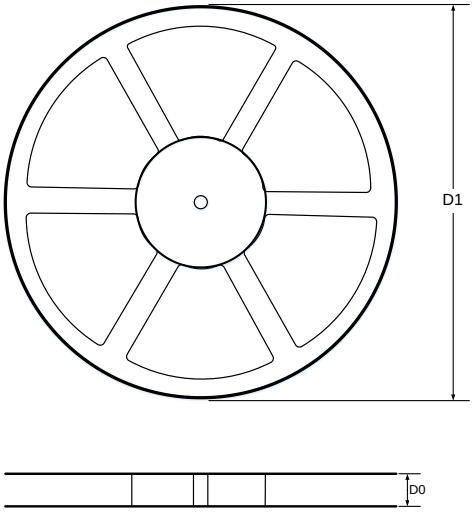


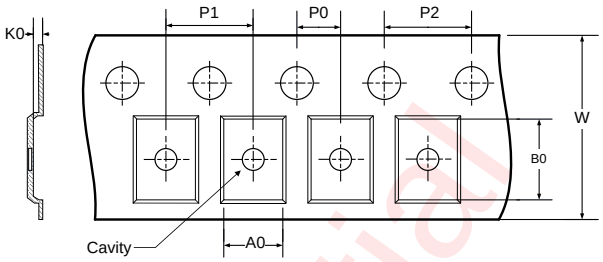
Figure 19 PCB layout example

Tape And Reel Information

REEL DIMENSIONS

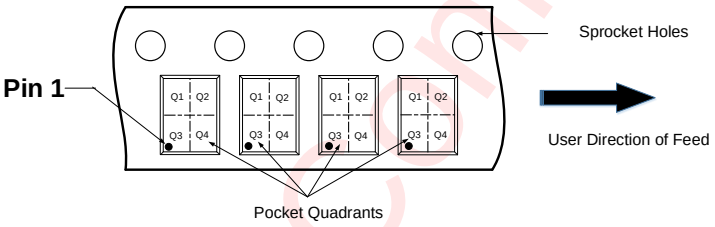


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



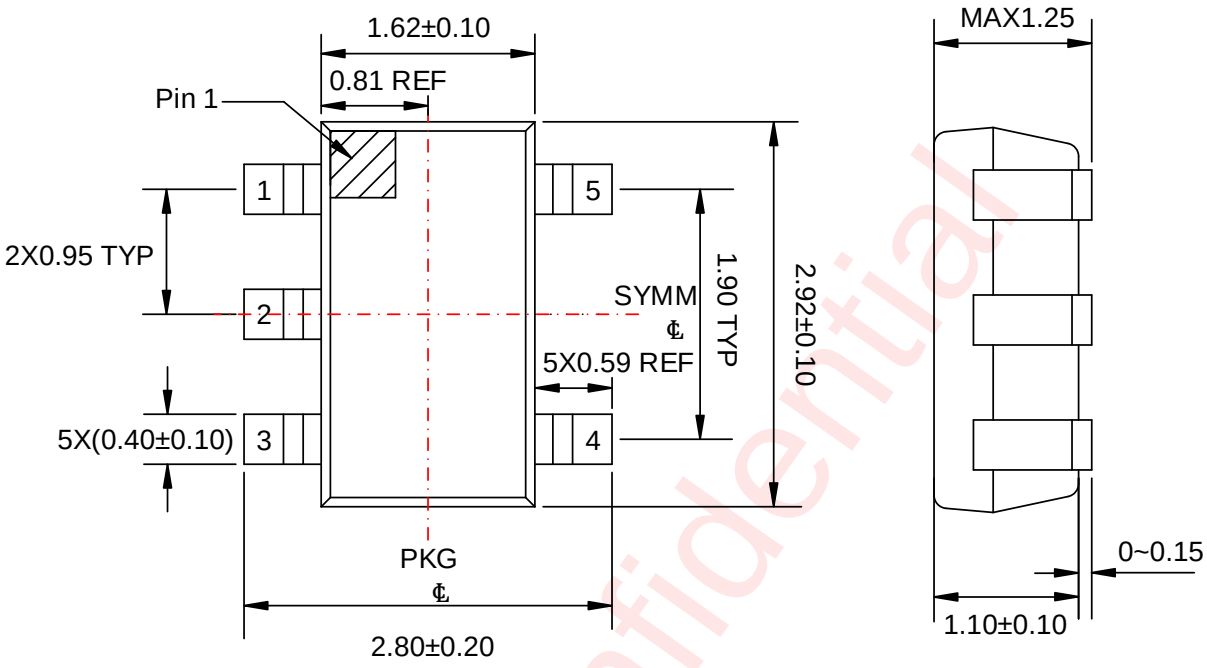
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

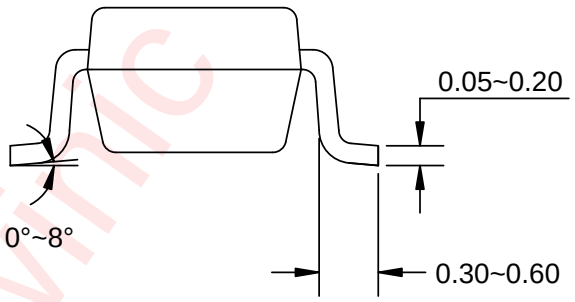
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.5	3.3	3.2	1.4	2	4	4	8	Q3

All dimensions are nominal

Package Description



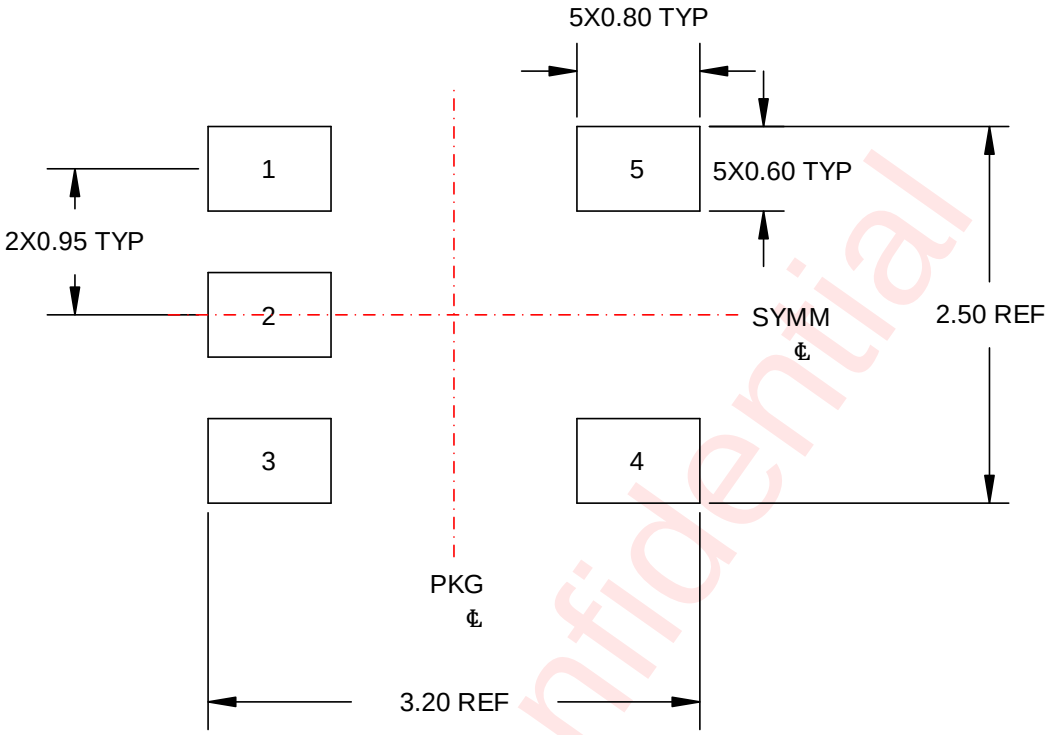
Top View **Side View**

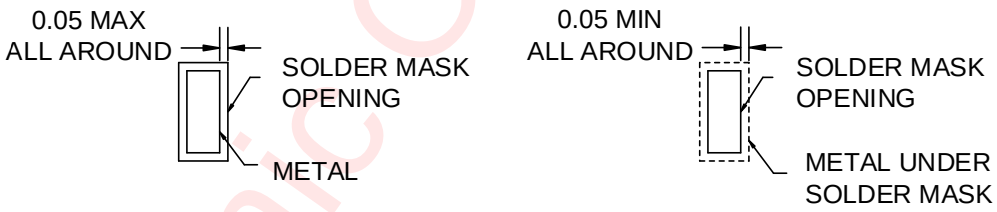


Side View

Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	May 2024	Officially released
V1.1	Dec. 2024	1. Add UL certificate file number(P1) 2. Add the parameter of θ_{JC} (P5)

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.