I²S/TDM Input, High Efficiency, 10.25V BOOST Digital Smart K Audio Amplifier with SKTune Algorithm

FEATURES

- **Integrates SKTune Algorithm**
  - **Bass Booster**
  - **Parametric Audio Path Equalizer (EQ)**
  - **Automatic Gain Control (AGC)**
  - **Dynamic Equalizer Enhancement (DEE)**
  - **Multi-Band Dynamic Range Compressor (MBDRC)**
  - **Anti-clip Voltage Limiter**
  - **Speaker Protection**
- **Speaker Current and Voltage Sense**
- **Smart BOOST with total efficiency up to 84%**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 9.3μV**
- **THD+N: 0.01%**
- Extensive Pop-Click Suppression
- Volume control (from -96dB to 0dB)
- I²S/TDM interface:
  - I²S, Left-Justified and Right-Justified
  - Supports 1/2/4/6/8 slots TDM
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16, 20, 24, 32 Bits
- Ultrasonic support via TDM/I²S running at 96kHz
- I²C-bus control interface(1MHz)
- Power Supplies:
  - VDD: 3V~5.5V
  - DVDD: 1.65V~1.95V
  - VDDIO: 1.65V~3.6V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- Support PVDD external power supply application
- FOWLP 2.75mmX3.25mmX0.543mm-42B package

DESCRIPTION

The AW88396FOR is an I²S/TDM input, high efficiency digital Smart K audio amplifier with an integrated 10.25V smart boost converter and SKTune speaker protection algorithms. Due to its 9.3μV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 5.7W output power into an 8Ω speaker at 1% THD+N.

The AW88396FOR integrates SKTune algorithm that includes parametric audio path equalizer, multi-band dynamic range control, anti-clip voltage limiter and speaker protection. The SKTune algorithm maximizes speaker performance while maintaining safe speaker conditions.

The AW88396FOR integrates a high-efficiency smart boost converter as the Class-D amplifier supply rail. The output voltage of boost converter can be adjusted smartly according to the amplitude of input signal, which extremely improves the efficiency without clipping distortion.

The AW88396FOR features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I²C-bus interface, and the device address is configurable.

The AW88396FOR offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

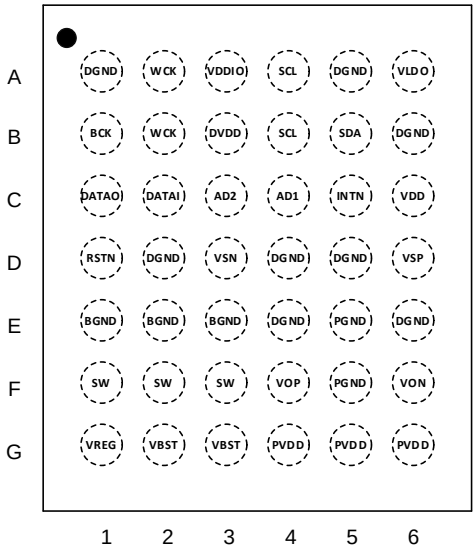
AW88396FOR is available in a FOWLP 2.75mmX3.25mmX0.543mm-42B package.

APPLICATIONS

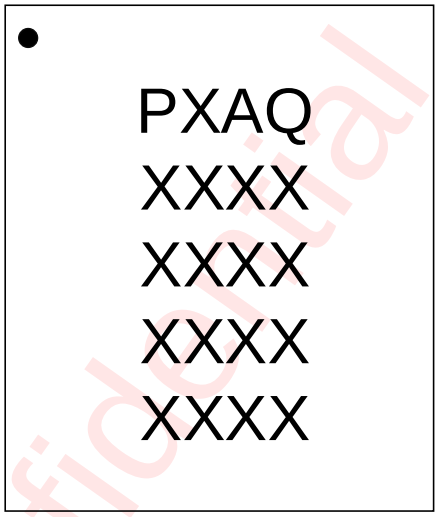
- Mobile phones
- Tablets
- Portable Audio Devices

PIN CONFIGURATION AND TOP MARK

AW88396FOR
(Top View)



AW88396FOR Marking
(Top View)



PXAQ - AW88396FOR
XXXX/XXXX/XXXX/XXXX - Production Tracing Code

Figure 1 AW88396FOR pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
A3	VDDIO	Digital I/O supply voltage
A6	VLDO	Digital core voltage regulator output
A2,B2	WCK	I2S word select input / TDM frame sync signal
B3	DVDD	Digital power supply
A4,B4	SCL	I2C clock input
B1	BCK	I2S/TDM bit clock input
B5	SDA	I2C data I/O
C1	DATAO	I2S/TDM data out
C2	DATAI	I2S/TDM data input
C3	AD2	I2C address select input
C4	AD1	I2C address select input
C5	INTN	Interrupt output
C6	VDD	Battery power supply

Pin No	Pin Name	Description
D1	RSTN	Active low hardware reset
E1,E2,E3	BGND	Boost GND
A1,A5,B6,D2,D4,D5,E4,E6	DGND	Digital GND
E5,F5	PGND	Power GND
F1,F2,F3	SW	Boost switch pin
F4	VOP	Non-inverting Class-D output
F6	VON	Inverting Class-D output
G1	VREG	Voltage output of regulator
G2,G3	VBST	Boost output
G4,G5,G6	PVDD	Class-D power supply
D6	VSP	Voltage sense non-inverting
D3	VSN	Voltage sense inverting

FUNCTIONAL BLOCK DIAGRAM

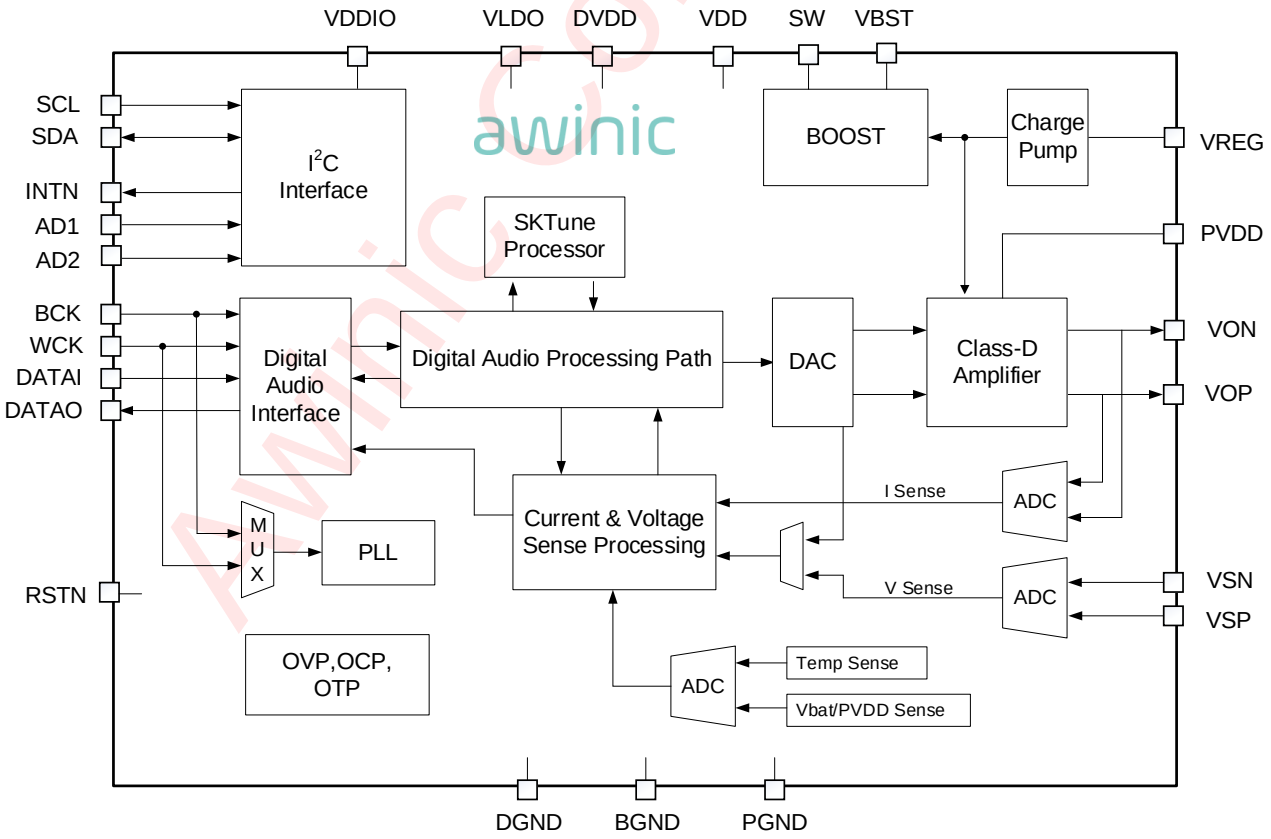


Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

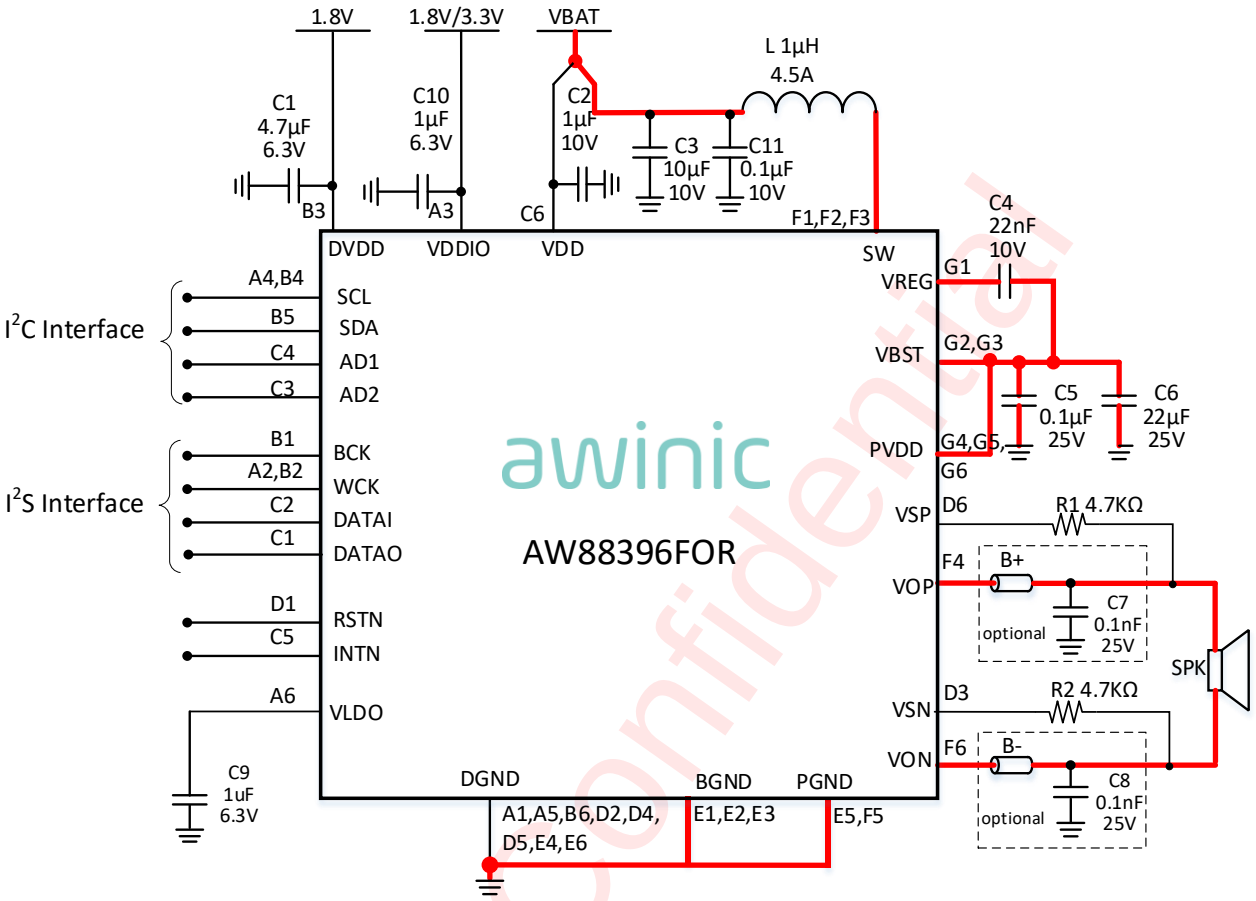


Figure 3 AW88396FOR Application Circuit

Note: Traces carry high current are marked in red in the above figure

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EXTERNAL PVDD POWER SUPPLY APPLICATION DIAGRAM

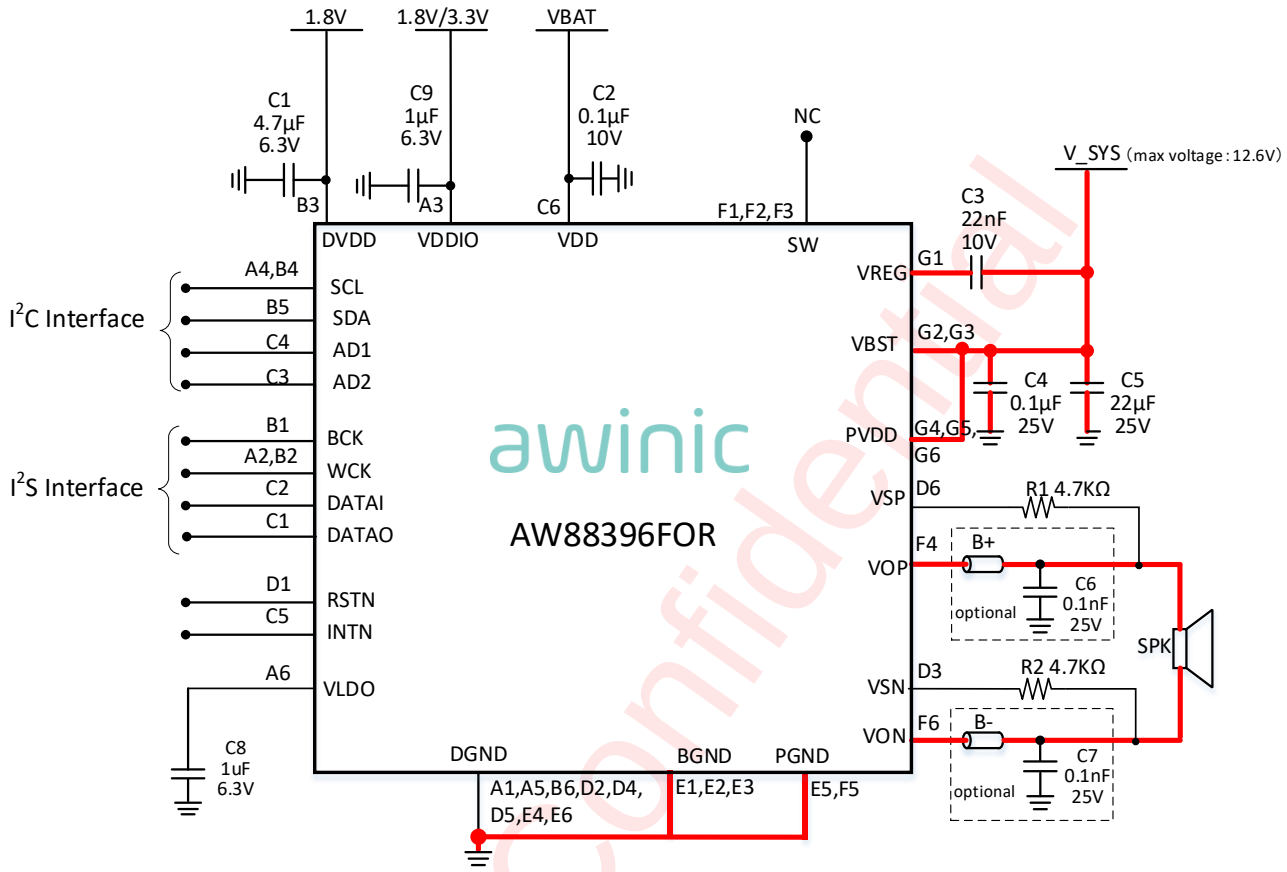


Figure 4 AW88396FOR External Pvdd Power Supply Application Circuit

Note: Traces carry high current are marked in red in the above figure

ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88396FOR	-40℃ ~ 85℃	FOWLP 2.75mmX3.25mm X0.543mm-42B	PXAQ	MSL1	RoHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING (NOTE1)

Parameter	Range
Battery Supply Voltage V_{VDD}	-0.3V to 6V
Digital Supply Voltage V_{DVDD}	-0.3V to 2V
Digital I/O supply voltage V_{VDDIO}	-0.3V to 3.9V
Boost output voltage V_{PVDD}	-0.3 to 13.2V(Note 6)
Boost SW pin voltage	-0.3 to 12V (Note 2)
VOP/VON pin voltage	-0.3 to 13.2V (Note 2,6)
VREG pin voltage	-0.3 to V_{PVDD}+6V
Minimum load resistance R_L	3.2Ω(Note 3)
Package Thermal Resistance θ_{JA}	48°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (Note 4,5)	
HBM（Human Body Model）	±2000V
CDM(Charge Device Model)	±1500V
Latch-up	
Test Condition：JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT: 200mA -IT: -200mA

Note 1: *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2: *SW/VOP/VON pin can handle 16V transients for less than 5ns*

Note 3: *When the load resistance R_L is less than 5Ω, please refer to the corresponding application notes and the maximum boost output voltage V_{PVDD} should be less than 9V.*

Note 4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017*

Note 5: *Test method: ESDA/JEDEC JS-002-2018*

Note 6: *PVDD/VOP/VON pin Maximum voltage is 12V when Built-in boost mode, PVDD external power supply is 13.2V.*

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition: T_A=25°C, V_{VDD}=3.6V, V_{DVDD}=1.8V, V_{VDDIO}=1.8V, V_{PVDD}=10.25V, R_L=8Ω+33μH, f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VDD}	Battery supply voltage	On pin VDD	3.0		5.5	V
V_{DVDD}	Digital supply voltage	On pin DVDD	1.65	1.8	1.95	V
V_{VDDIO}	Digital IO supply voltage	On pin VDDIO	1.65	1.8	3.6	V
V_{PVDD_EXTER}	Pvdd external voltage	On pin PVDD	3.0	12	12.6	V
I_{VDD}	Battery supply current	Operating mode (Noise-Gate Off, I²S signal input 0)		5.5		mA
		Operating mode (Noise-Gate On, I²S signal input 0)		4.3		mA
		Standby mode		5.0		μA
		Power down mode		0.5	2	μA
I_{PVDD}	Pvdd external power supply ($V_{PVDD\_EXTERNAL}$=12V)	Operating mode (Noise-Gate Off, I²S signal input 0)		8.5		mA
		Standby mode		2		μA
		Power down mode		2		μA
I_{DVDD}	Digital supply current	Operating mode, SKTune Algorithm activated, running full enhancement (I²S signal input 0dB)		8.6		mA
		Operating mode, SKTune Algorithm activated, (I²S signal input 0)		4.0		mA
		Operating mode, SKTune Algorithm bypassed (I²S signal input 0dB)		3.2		mA
		Operating mode, SKTune Algorithm bypassed (I²S signal input 0)		2.8		mA
		Standby mode		5.5		μA
		Power down mode		0.8		μA
Boost						

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{PVDD}	Boost output voltage			10.25		V
V_{OVP}	Over-voltage threshold			V_{PVDD} +0.75		V
	OVP hysteresis voltage			400		mV
I_{L_PEAK}	Inductor peak current limit			4.1(Note1)		A
F_{BST}	Operating Frequency	fs = 48KHz		2		MHz
Class-D						
R_{dson}	Drain-Source on-state resistance	High side MOS + Low side MOS		269		mΩ
Po	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, V_{VDD}=4.2V, V_{PVDD}=10.25V		5.7		W
		THD+N=10%, R_L=8Ω+33μH, V_{VDD}=4.2V, V_{PVDD} =10.25V		7.2		W
		THD+N=1%, R_L=6Ω+33μH, V_{VDD}=4.2V, V_{PVDD} =10.25V		5.8		W
		THD+N=10%, R_L=6Ω+33μH, V_{VDD}=4.2V, V_{PVDD} =10.25V		7.3		W
		THD+N=1%, R_L=4Ω, V_{VDD}=4.2V, V_{PVDD} =8V		6.2		W
	Speaker Output Power (Pvdd external power supply)	R_L=4Ω+33μH, V_{VDD}=5V, $V_{PVDD\_EXTERNAL}$=12V		14		W
V_{OS}	Output offset voltage	I^2S signal input 0	-10	0	10	mV
η	Total efficiency (Class-D)	V_{VDD}=4.2V, Po=0.45W, R_L=8Ω+33μH		89		%
	Total efficiency (Boost+Class-D)	V_{VDD}=4.2V, Po=2W, R_L=8Ω+33μH		84		%
	Total efficiency (Pvdd external power supply +Class-D)	VVDD=5V, Po=2W, RL=4Ω+33μH VPVDD_EXTERNAL =12V		88		%
		V_{VDD}=5V, Po=14W, R_L=4Ω+33μH, $V_{PVDD\_EXTERNAL}$=12V		92		%
THD+N	Total harmonic distortion plus noise	V_{VDD}=4.2V, Po=1W, R_L=8Ω+33μH, f=1kHz , V_{PVDD} =10.25V		0.01		%
E_N	Speaker Mode Output noise(Noise-Gate Off)	A-weighting		15.8		μV

Symbol	Description	Test Conditions		Min	Typ.	Max	Units
	Speaker Mode Output noise(Noise-Gate On)	A-weighting			1		μV
	Receiver Mode Output noise(Noise-Gate Off)	A-weighting			9.3		μV
	Receiver Mode Output noise(Noise-Gate On)	A-weighting			1		μV
FR_{amp}	Frequency response flatness (Note2)	SPK(20Hz-20kHz) , Po=1W			0.3		dB
		SPK(20Hz-40kHz) , Po=1W			1		dB
		RCV(20Hz-20kHz) , Po=0.5W			0.2		dB
		RCV(20Hz-40kHz) , Po=0.5W			0.2		dB
SNR	Signal-to-noise ratio	V_{VDD}=4.2V, V_{PVDD}=10.25V, Po=5.7W, R_L=8Ω+33μH, A-weighting			112		dB
DNR	Dynamic Range	-60dBFS Method, A-weighting			110		dB
PSRR	Power supply rejection ratio	Receiver Mode V_{VDD}=4.2V, V_{p-p_sin}=200mV	217Hz		87		dB
			1kHz		89		dB
Current Sense							
I_{SNS_FS}	Current sense full scale				3.125		A
SNR	Signal-to-noise ratio	Ipeak=1A, R_L=8Ω+33μH, A-weighting			65		dB
THD+N	Total harmonic distortion plus noise	Po=1W, R_L=8Ω+33μH			0.25		%
ΔI_{SNS}	Current sense accuracy	Po=1W, R_L=8Ω+33μH			2		%
Voltage Sense							
V_{SNS_FS}	Voltage sense full scale				18.875		V
SNR	Signal-to-noise ratio	Ipeak=1A, R_L=8Ω+33μH, A-weighting			65		dB
THD+N	Total harmonic distortion plus noise	Po=1W, R_L=8Ω+33μH			0.1		%
ΔV_{SNS}	Voltage sense accuracy	Po=1W, R_L=8Ω+33μH			2		%
Digital Logical Interface							
V_{IL}	Logic input low level	BCK, WCK, DATAI Pin				0.3 x V_{VDDIO}	V

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{IH}	Logic input high level		0.7 x V_{VDDIO}		V_{VDDIO}	V
V_{IL}	Logic input low level	RSTN, SCL, SDA, AD1, AD2 Pin			0.3 x V_{VDDIO}	V
V_{IH}	Logic input high level		0.7 x V_{VDDIO}		3.6	V
V_{OL}	Logic output low level	I_{OUT}=2mA			0.45	V
V_{OH}	Logic output high level	I_{OUT}=-2mA	V_{VDDIO} - 0.45		V_{VDDIO}	V
Protection						
T_{SD}	Over temperature protection threshold			150		°C
T_{SDR}	Over temperature protection recovery threshold			130		°C
UVP	Under-voltage protection voltage			2.6		V
	Under-voltage protection hysteresis voltage			200		mV

Note 1: IL_PEAK *registers are adjustable; Refer to the list of registers.*
Note 2: *FS=96kHz when the amplitude response variation is 20Hz-40kHz.*

I²C INTERFACE TIMING

Parameter			Fast mode			Fast mode plus			Units
No.	Sym	Name	Min	Typ.	Max	Min	Typ.	Max	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

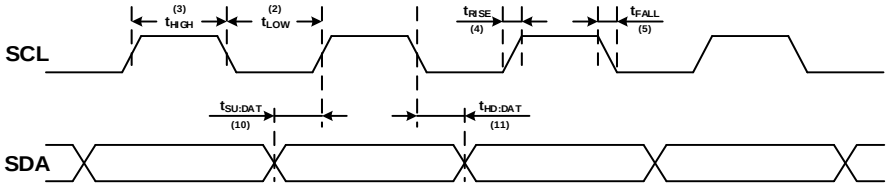


Figure 5 SCL and SDA timing relationships in the data transmission process

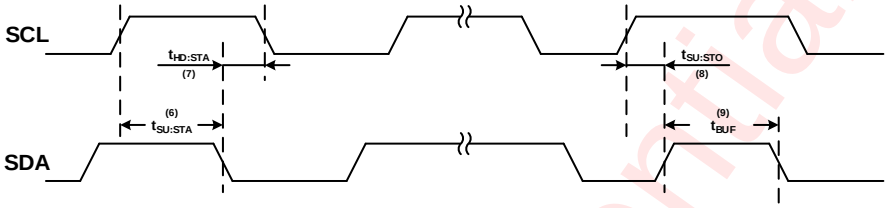


Figure 6 The timing relationship between START and STOP state

DIGITAL AUDIO INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8		96	kHz
f_{bck}	Bit clock frequency, on pin BCK	16*fs		12.288(NOTE)	MHz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			40	ns

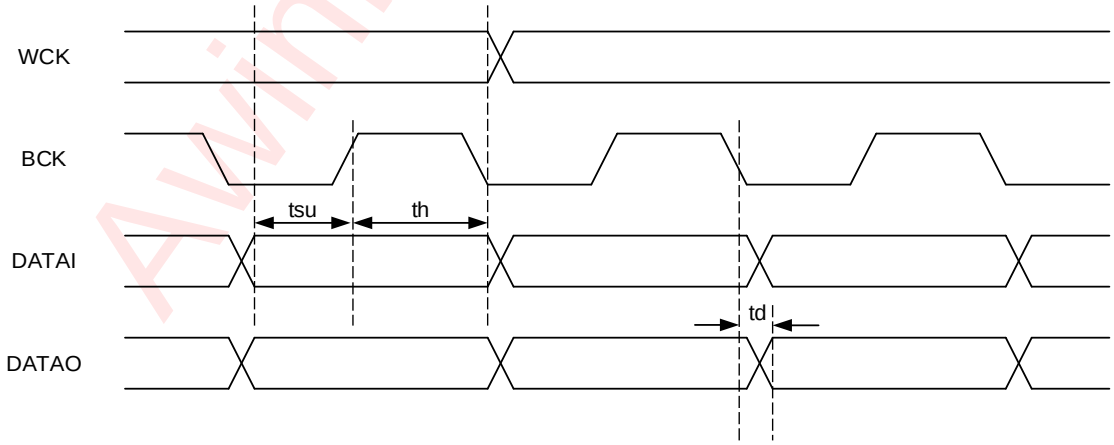


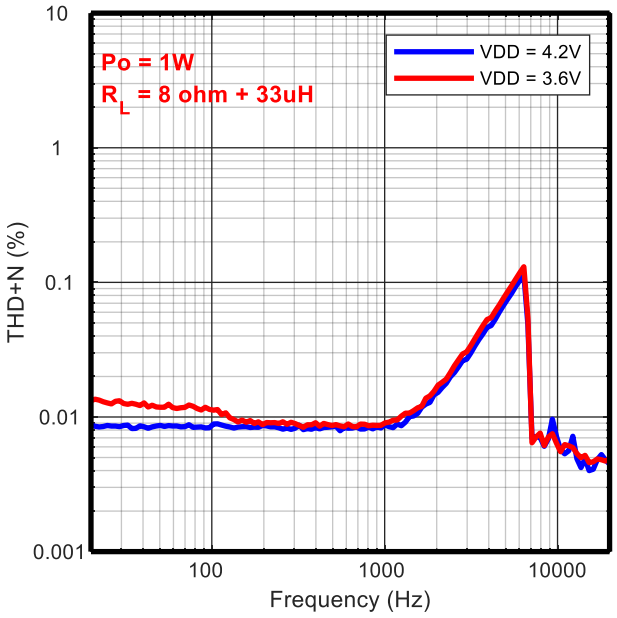
Figure 7 Digital Audio Interface Timing

NOTES: *The digital audio interface supports up to 8 slots (32-bit) at a 32/44.1/48 kHz sample rate, and 4 slots (32-bit) at a 96 kHz sample rate.*

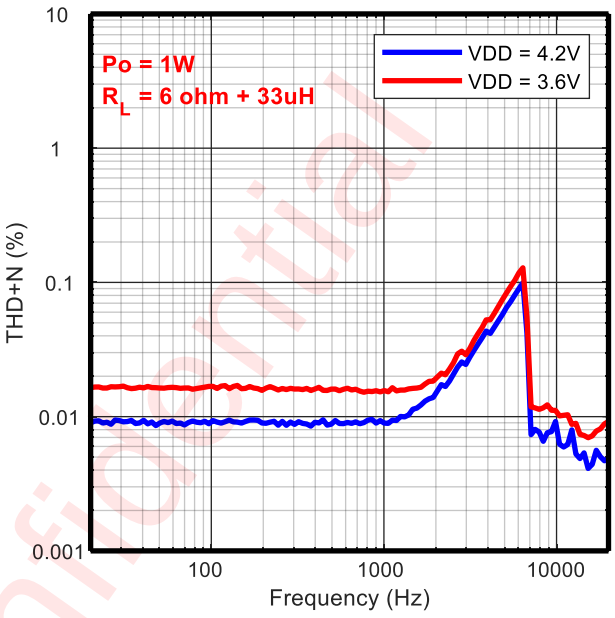
TYPICAL CHARACTERISTIC CURVES

PVDD INTERNAL POWER SUPPLY APPLICATION

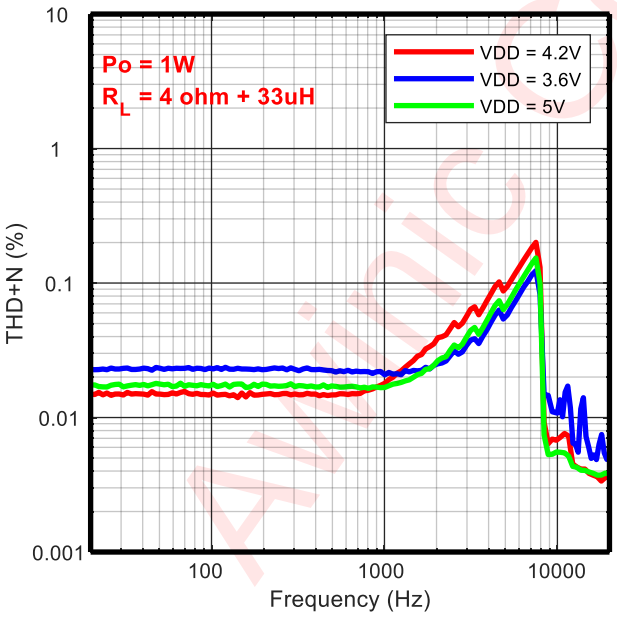
THD+N VS. FREQUENCY



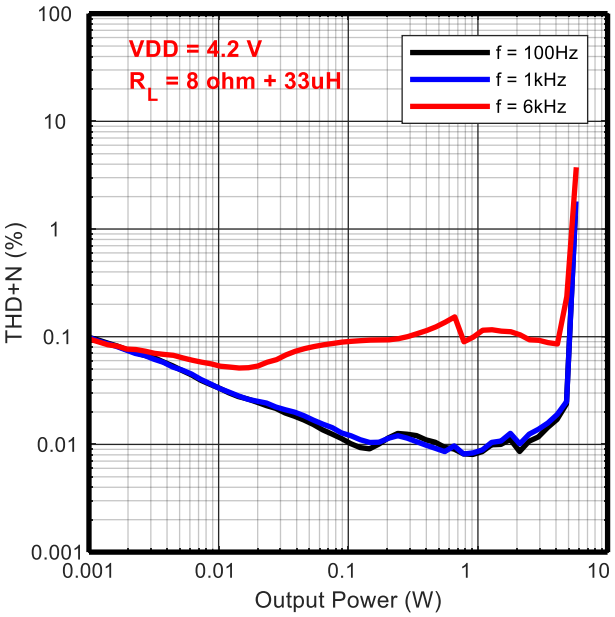
THD+N VS. FREQUENCY



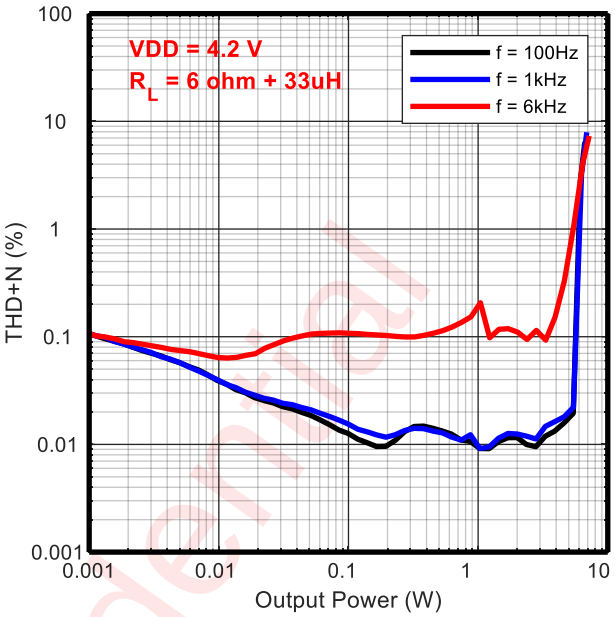
THD+N VS. FREQUENCY



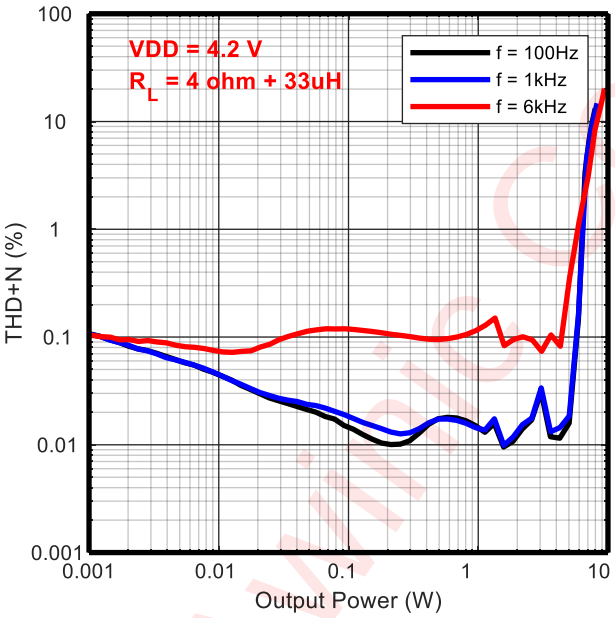
THD+N VS. OUTPUT POWER



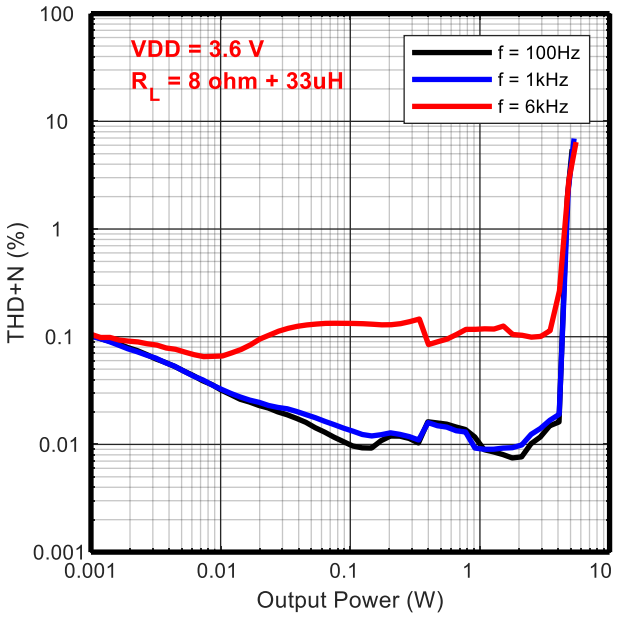
THD+N VS. OUTPUT POWER



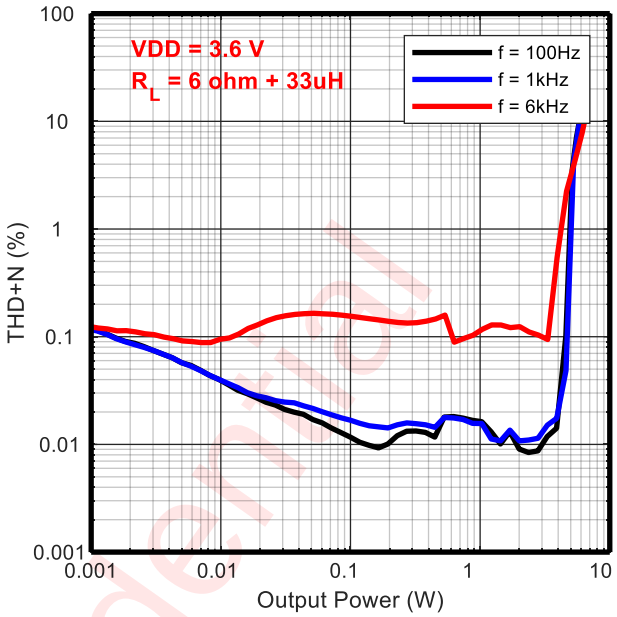
THD+N VS. OUTPUT POWER



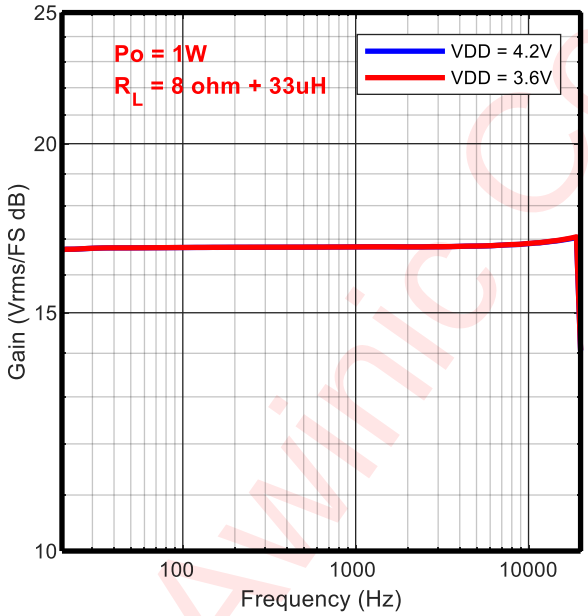
THD+N VS. OUTPUT POWER



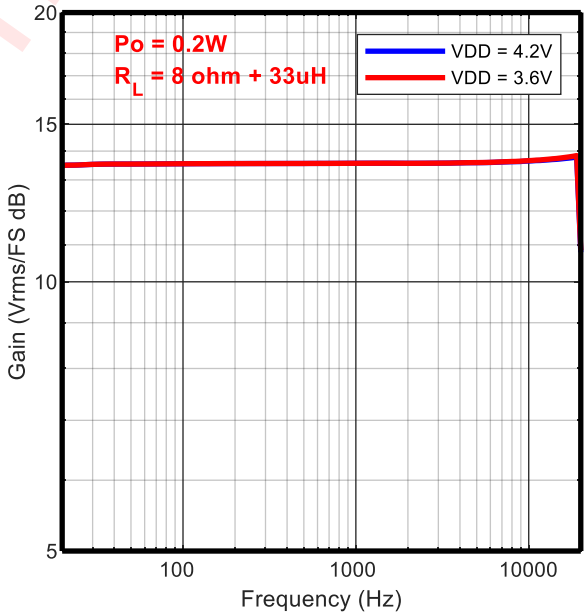
THD+N VS. OUTPUT POWER



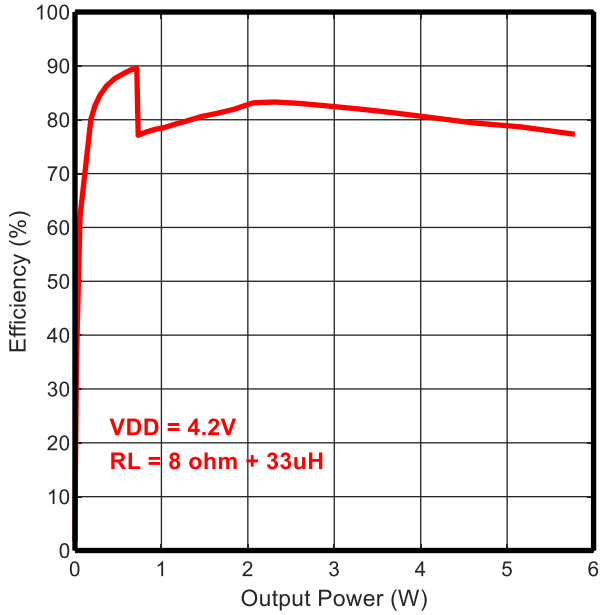
SPEAKER GAIN VS. FREQUENCY



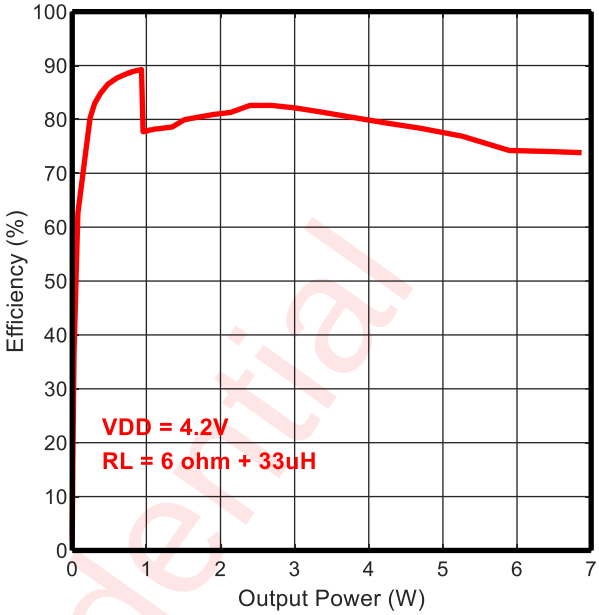
RECEIVER GAIN VS. FREQUENCY



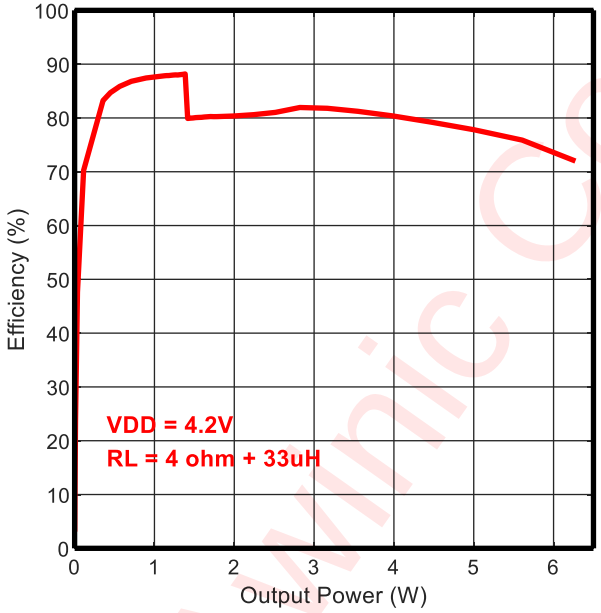
EFFICIENCY VS. OUTPUT POWER



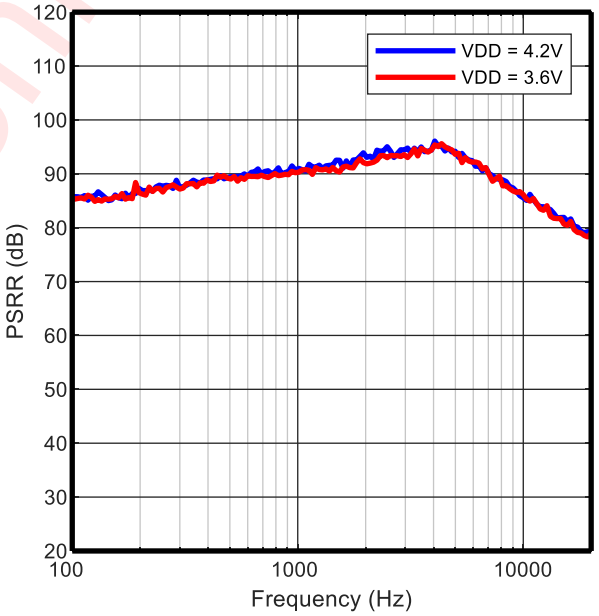
EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER

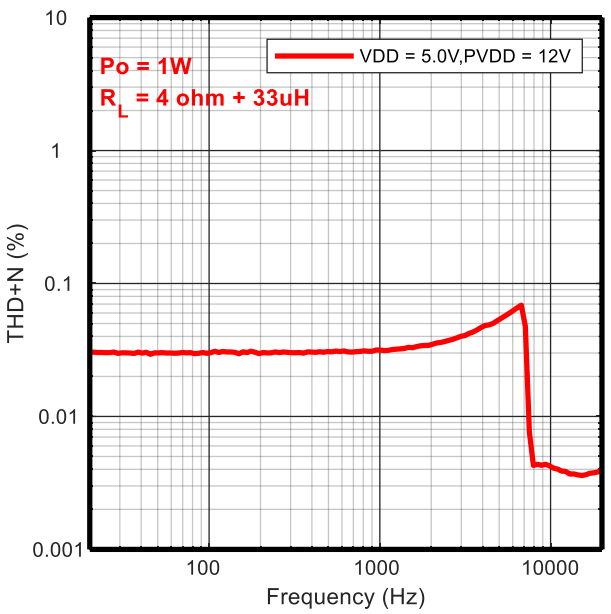


RECEIVER PSRR VS. FREQUENCY

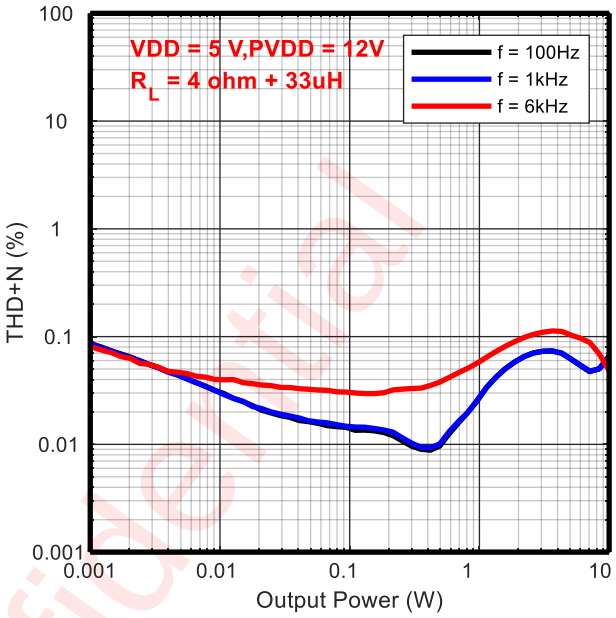


PVDD EXTERNAL POWER SUPPLY APPLICATION

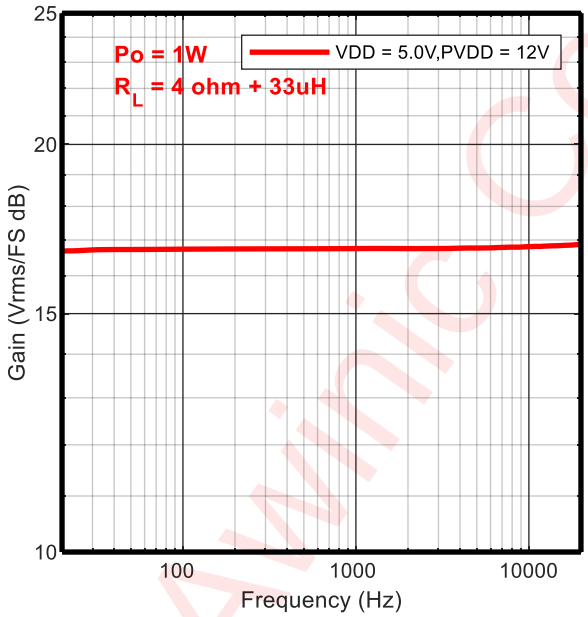
THD+N VS. FREQUENCY



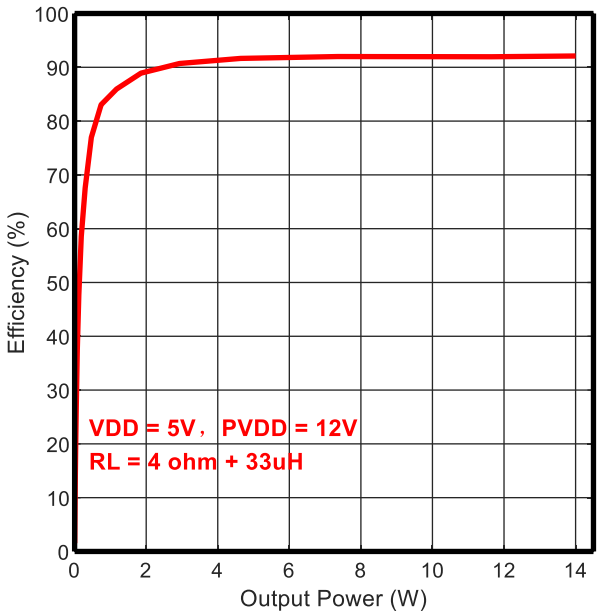
THD+N VS. OUTPUT POWER



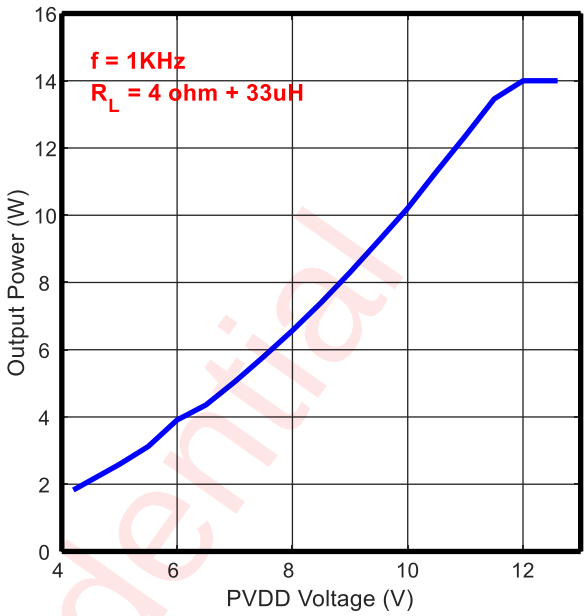
SPEAKER GAIN VS. FREQUENCY



EFFICIENCY VS. OUTPUT POWER



OUTPUT POWER VS. PVDD



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD and DVDD supply voltage. When the VDD supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{VDD} < 2.1V V_{DVDD} < 1.1V	Power supply is not ready, chipset is power down.
Stand-By	V_{VDD} > 3.0V V_{DVDD} > 1.65V	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Configuring	PWDN = 0	Device is biased while boost and class-D output is floating. System configuration carried out in this mode
Operating	AMPPD = 0	Amplifier is fully operating

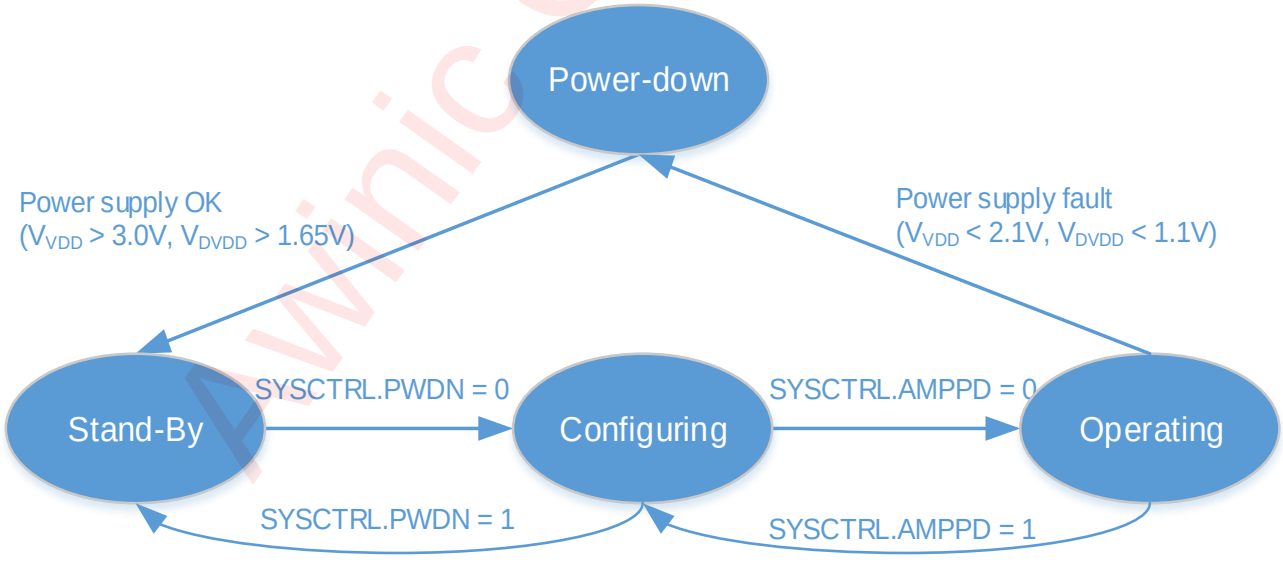


Figure 8 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{DVDD} < 1.1 V
- V_{VDD} < 2.1 V
- RSTN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.
The device will jump out of the power-down mode automatically when all of the supply voltages are OK (V_{DVDD} > 1.65 V and V_{VDD} > 3.0 V) and RSTN goes HIGH.

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK and RSTN pin is HIGH. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to stand-by mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 1;

In this mode the internal bias, OSC and PLL modules will start to work.

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.
This device power up sequence is illustrated in the following figure:

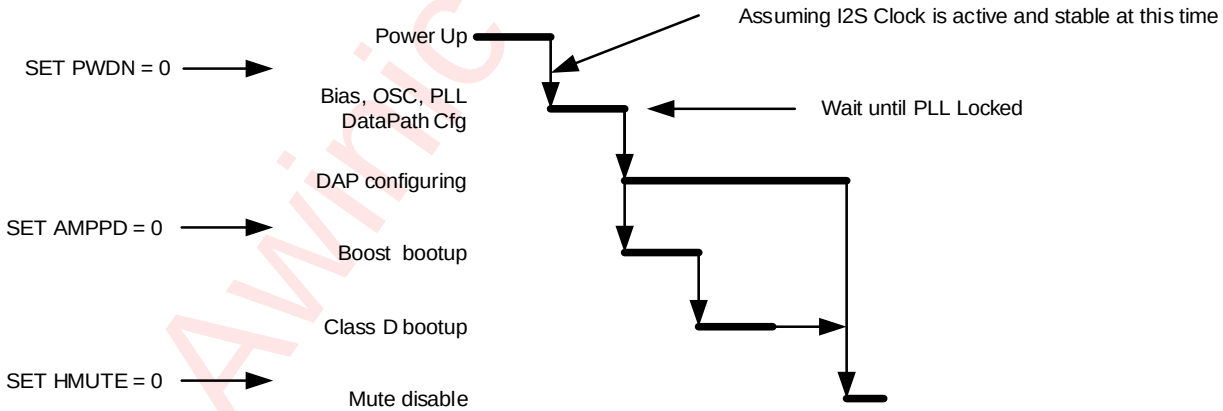


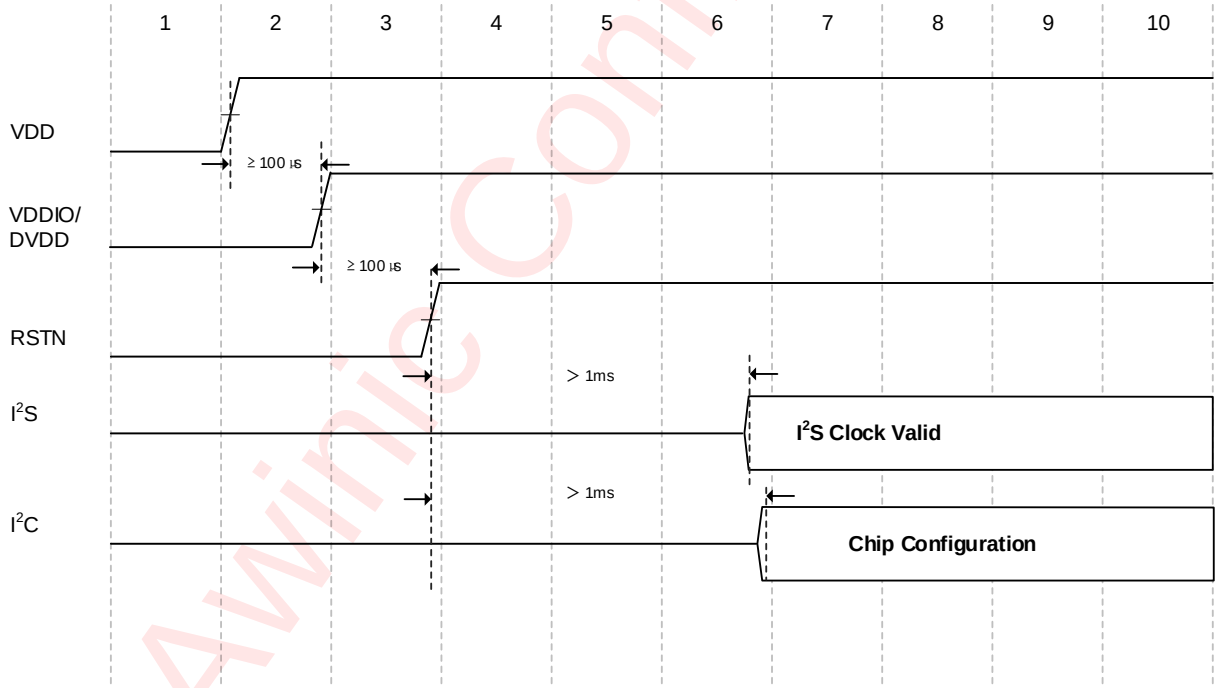
Figure 9 Power up sequence

Detail description for each step is listed in the following table.

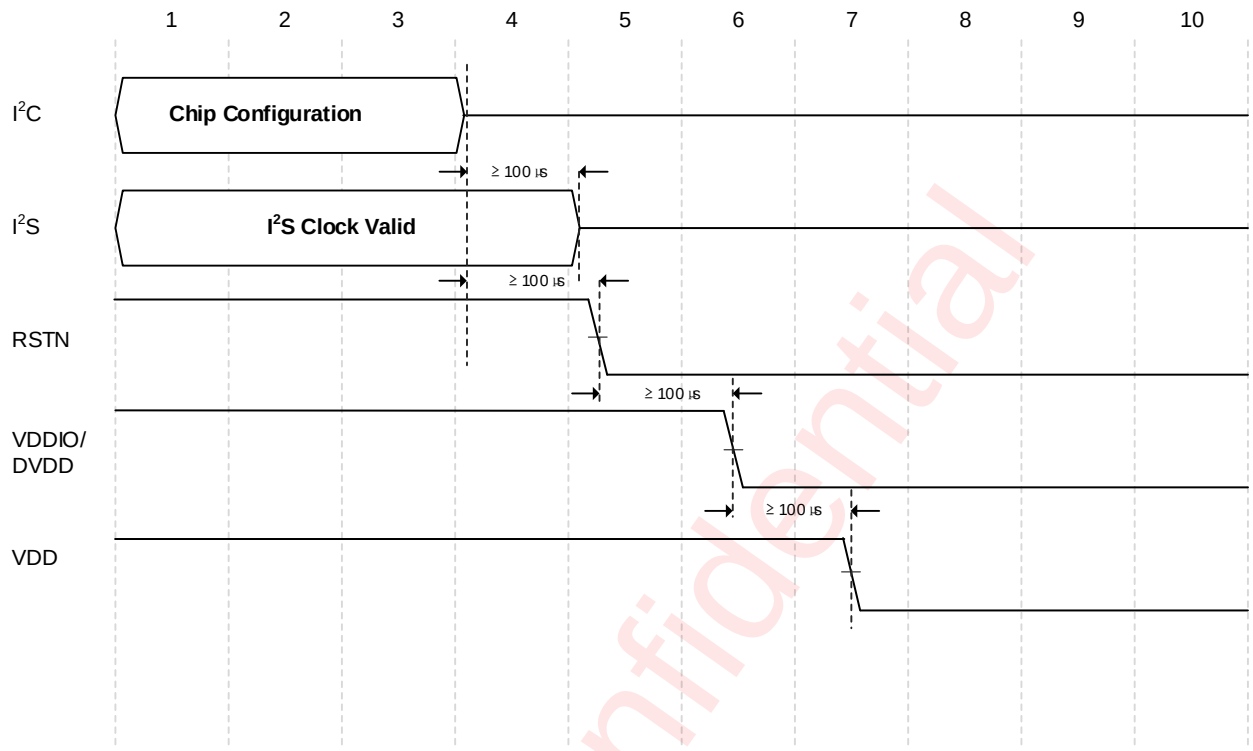
Table 2 Detail Description of Power up sequence

Index	Description	Mode
1	Wait for VDD, VDDIO, DVDD supply power up	Power-Down
2	I²S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Bias, OSC, PLL active	
3.3	Waiting for PLL locked	
4.1	Enable Boost and amplifier (SYSCTRL.AMPPD =0) Boost and Amplifier boot up	Operating
4.2	Waiting for SYSST.SWS =1	
5	Release Hard-Mute Data Path active	

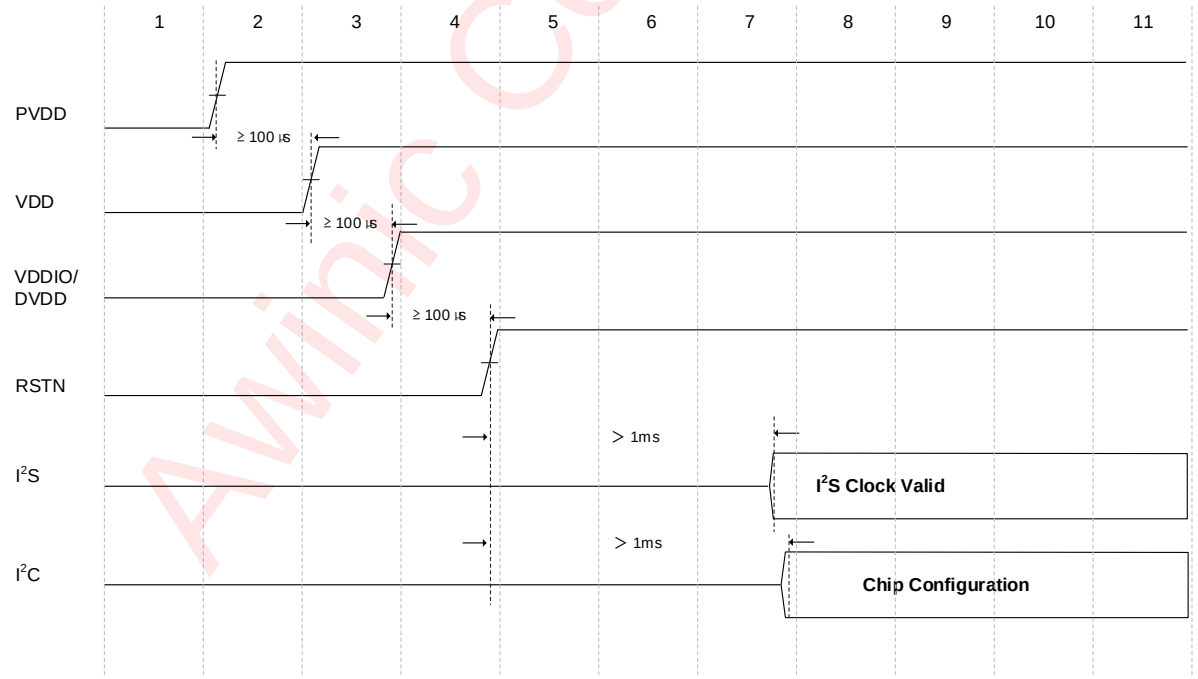
Power up sequence (PVDD internal power supply) considering I²S, I²C timing shows as below:



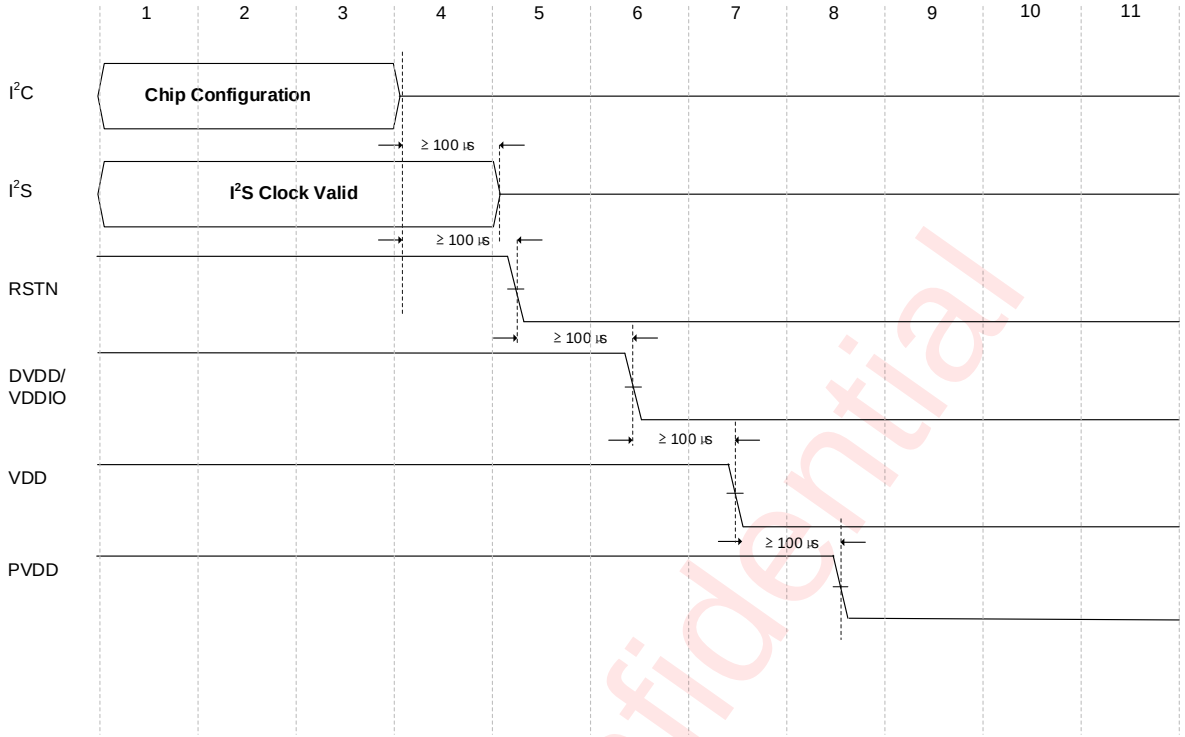
Power down sequence (PVDD internal power supply) considering I²S, I²C timing shows as below:



Power up sequence (PVDD external power supply) considering I²S, I²C timing shows as below:



Power down sequence (PVDD external power supply) considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers are cleared.

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The interface is compliant with all TDM/I²S interface configurations and supports a wide range of TDM/I²S interface configurations. It also offers the possibility of providing an ultrasonic path to the speaker. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO

Two-slot I²S and 1/2/4/6/8-slot TDM are supported in this device. The digital audio interface supports up to 8 slots (32-bit) at a 32/44.1/48 kHz sample rate, and 4 slots (32-bit) at a 96 kHz sample rate. The digital audio Interface on this device is slaver only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL.I2SBCK. The frequency of BCK can be calculated according to the following equation:

*BCK frequency = SampleRate * SlotLength * SlotNumber*

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface, both WCK and BCK could be used as the reference clock of internal Phased Locked Loop (PLL).

The input audio data can be attenuated -6dB in this module, by setting bit I2SCFG2.INPLEV. The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL.CHSEL.

Table 3 Supported I²S interface parameters

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs/64fs
Left-justified	16b/20b/24b/32b	32fs/48fs/64fs
Right-justified	16b/20b/24b/32b	32fs /48fs/64fs

The output port DATAO, can be enabled or disabled via bit I2SCFG1.I2STXEN. The unused slots can be set to Hi-z or active, which is controlled by I2SCFG2.DOHZ. When the unused slots are active, the data could be zeros or same data of used slot, which can be configured via I2SCFG2.I2SDOSEL.

STANDARD I²S MODE

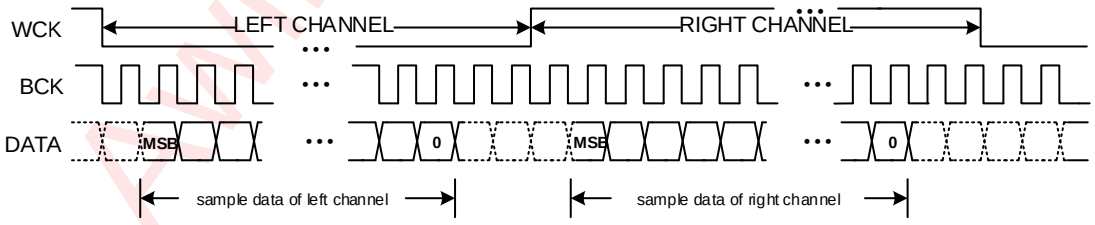


Figure 10 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

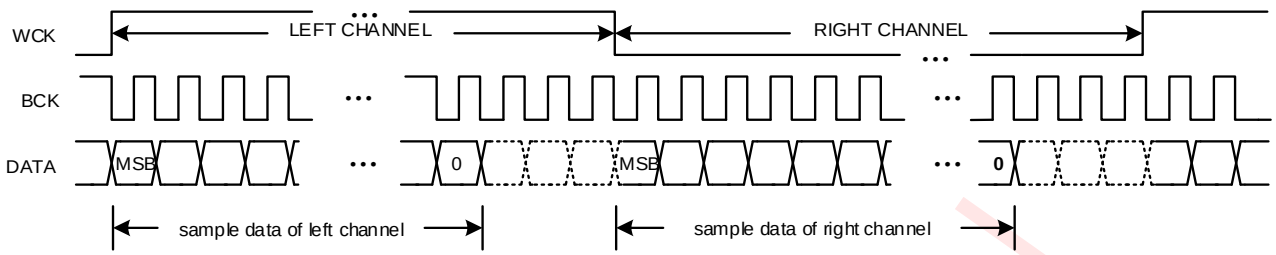


Figure 11 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

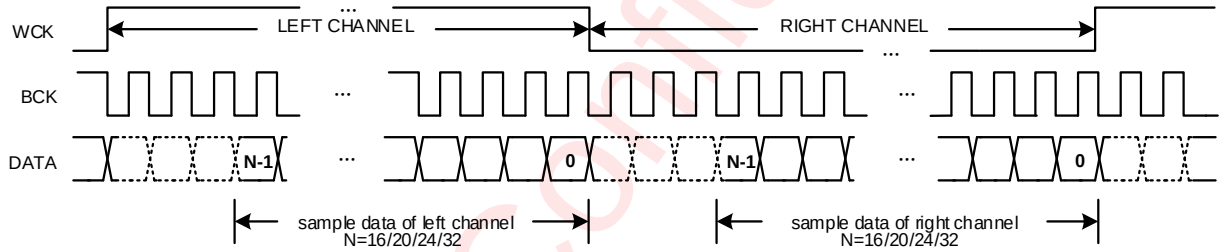


Figure 12 I²S Timing for Right-Justified Mode

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kinds of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the supported slot-number. 1/2/4/6/8-slot is supported in TDM mode, while 2-slot is supported in I²S mode. In TDM mode, the high level pulse width of WCK signal can be one slot time or one period of BCK.

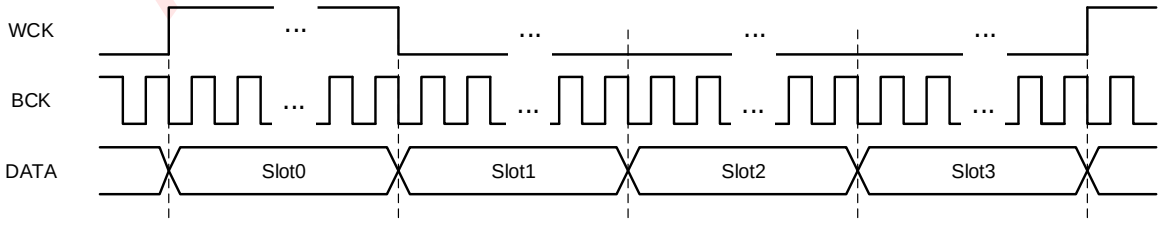


Figure 13 TDM Timing

ULTRASONIC APPLICATION

The device offers two modes for ultrasonic application via TDM/I²S running at 96kHz:
TDM Mode: Ultrasonic signal and audio signal could be sent into different slots of TDM/I²S separately, and then be mixed in the device.
Mixed Mode: Ultrasonic signal could be mixed with audio signal, and then be sent into one slot of TDM/I²S. In this mode, the frequency of ultrasonic signal should be larger than 25kHz.

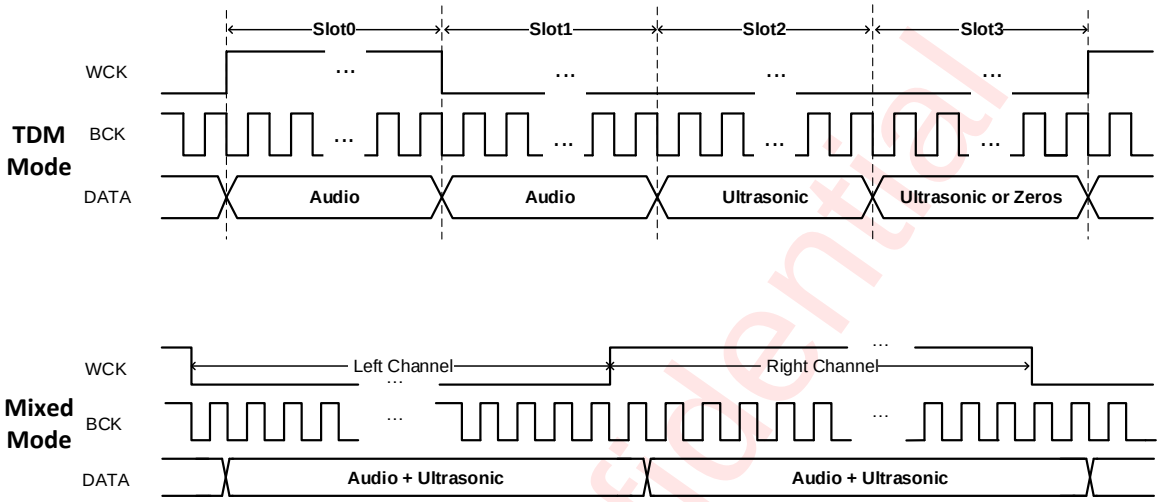


Figure 14 Ultrasonic Application for Two PA

DIGITAL AUDIO PROCESSING

This device incorporates one programmable Digital Audio Processor (DAP) block. It provides the algorithm for audio signal processing and speaker protection. The following functions are available in this module:

- SKTune
- HDCC
- Hardware AGC
- Volume control
- HMute

The signal processing flow in the DAP is illustrated in the following figure.

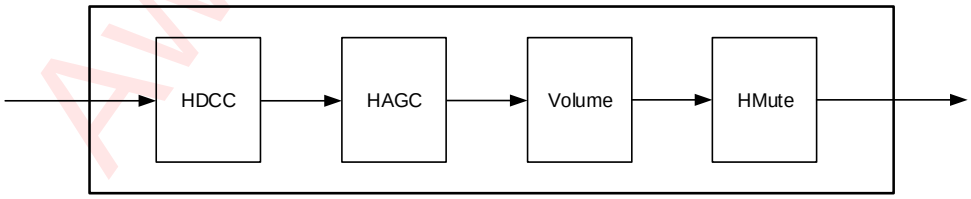


Figure 15 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker in the actual audio application, such as the maximum undistorted power is about 5.7W in the 10.25V power supply for 8Ω speaker. However, many speakers' rated power is about 1W, the overload signal can cause damage to the speaker if there is no output power control. The audio power amplifier with HAGC can protect the speaker effectively. When the output power doesn't exceed the setting threshold, the HAGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the HAGC module will reduce the internal gain of amplifier and restrict the output power under the setting threshold.

VOLUME CONTROL

The volume controller attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0dB to -96dB with 0.094dB/step.

MUTE

This module performs mute control for the audio stream.

SKTUNE ALOGRITHM

This device integrates SKTune algorithm that maximizes the speaker performance while maintaining safe speaker conditions. The following functions are available in this module.

- Bass Booster
- Parametric Audio Path Equalizer (EQ)
- Automatic Gain Control (AGC)
- Dynamic Equalizer Enhancement (DEE)
- Multi-Band Dynamic Range Compressor (MBDRC)
- Anti-clip Voltage Limiter
- Speaker Protection

The signal processing flow in the SKTune algorithm is illustrated in the following figure:

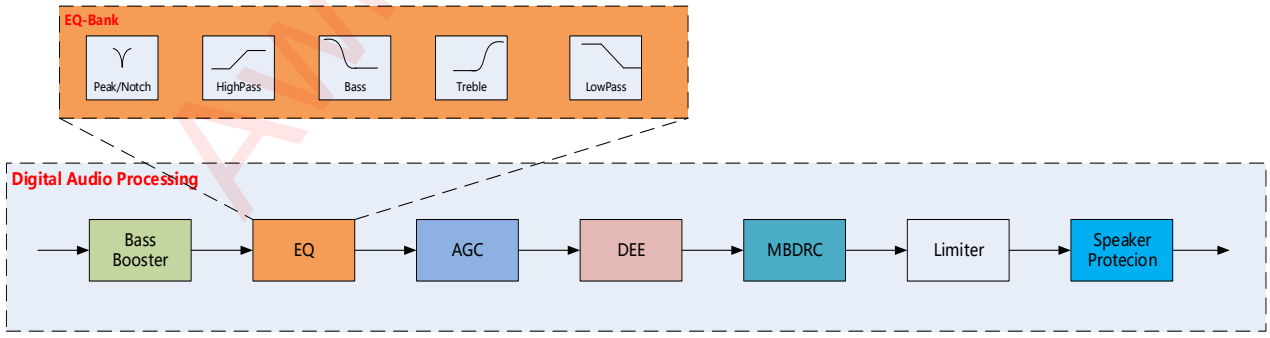


Figure 16 Block Diagram of SKTune algorithm

BASS BOOSTER

Small loudspeakers have poor performance in display low frequency audio signal, which can't meet people's demand for high quality sound. BASS BOOSTER uses psychoacoustic technology to highly elevate the low frequency performance in small loudspeaks.

PARAMETRIC AUDIO PATH EQUALIZER

Sixteen Parametric Audio Path Equalizers (EQ) are available and each of the equalizer can be fully programmable. It's possible to be implemented as any type of filter (high-pass, low-pass, peak, notch, bass, treble etc.) with different design methodologies to achieve the required frequency response.

AUTOMATIC GAIN CONTROL

Automatic Gain Control (AGC) adjust the signal to an appropriate range by applying different gain to achieve the best output effect of the speaker. As the input signal amplitude changes, gain changes automatically. It attenuate big signals and amplify small signals.

DYNAMIC EQUALIZER ENHANCEMENT

Dynamic Equalizer Enhancement (DEE) operate signals in one frequency band without affecting other frequency bands. Like a precise surgery, different amplitude signals may have different effects which depend on the type of the equalizer and parameter you set.

MULTI-BAND DYNAMIC RANGE CONTROL

A highly configurable and scalable MBDRC is available to improve audio performance. A block diagram of the MBDRC is illustrated in the following figure:

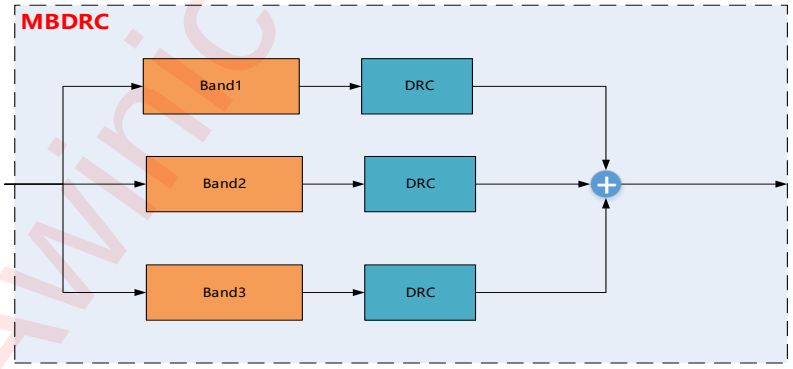


Figure 17 Simplified MBDRC block diagram

Three sub-band DRCs are supported. The audio input can be processed with individually configurable band-limited DRCs.

ANTI-CLIP VOLTAGE LIMITER

The anti-clip voltage limiter is used to protect the output signal from exceeding the amplifier clip level. When

signal is over the amplifier clip level it will be attenuated automatically and limited below the threshold without clipping.

SPEAKER PROTECTION

This device has integrated three protection schemes for the speaker.

- **Membrane excursion control:** avoiding speaker membrane over-excursion
- **Programmable Power Control**: avoiding speaker voice coil over-power
- **Coil temperature control**: avoiding speaker voice coil over-temperature

Membrane excursion control

The speaker membrane excursion is proportional to the amplitude of input signal. This device controls the membrane excursion by control the signal amplitude. It predicted the speaker membrane excursion according to the input signal at first. Then it'll attenuate the amplitude of the input signal automatically once the predicted excursion over the threshold.

Programmable Power Control

The power controller limits the maximum output power in amplifier mode when necessary. The power of output signal will be attenuated and limited below the programmable threshold in given attack time when the amplitude of input signal is above the threshold. While the attenuation will be released in given release time when the amplitude of input signal is below the threshold

Coil temperature control

Speaker voice coil temperature is proportional to its impedance in general. This device continuously monitors the impedance of speaker voice coil with integrated ADCs, and the coil temperature could be calculated according to its impedance. When the coil temperature is near the threshold, it controls the amplitude of signal sending to speaker.

DC-DC CONVERTER

This device using smart boost converter generates the amplifier supply rail. The DC-DC converter can work in different mode via BSTCTRL2.BST_MODE:

- **Pass-through mode**: the voltage of VDD is transparently passed to output of converter PVDD
- **Smart boost 1 mode**: the output voltage can be switch between VDD and programmed output voltage according to the amplifier output's signal swing requirements.
- **Smart boost 2 mode**: the output voltage can be dynamically adjusted according to the amplifier output's signal swing requirements in order to maximize efficiency.

PASS-THROUGH MODE

The internal boost circuit is not working; the voltage of VDD is passed to PVDD directly.

SMART BOOST 1 MODE

Smart boost 1 mode can dynamically turn on or off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

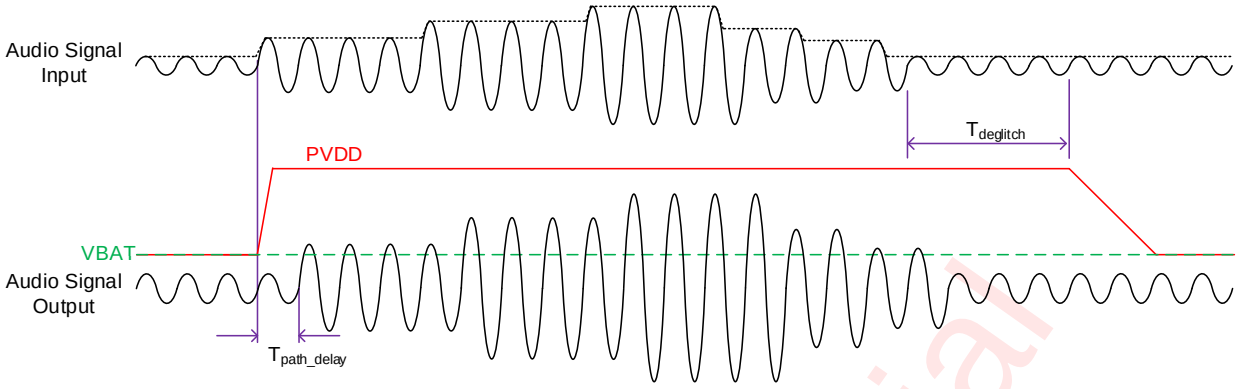


Figure 18 Boost Circuit Behavior in Smart Boost 1 Mode

SMART BOOST 2 MODE

The boost circuit works dynamically according to the output audio level. When the level of output audio signal is below the setting threshold, the boost circuit will not be activated. Till the level of output audio signal is above the threshold, the boost circuit starts to work before the audio stream arriving at amplifier power stage. The output voltage PVDD is dynamically adjusted to meet the requirement of output audio signal.

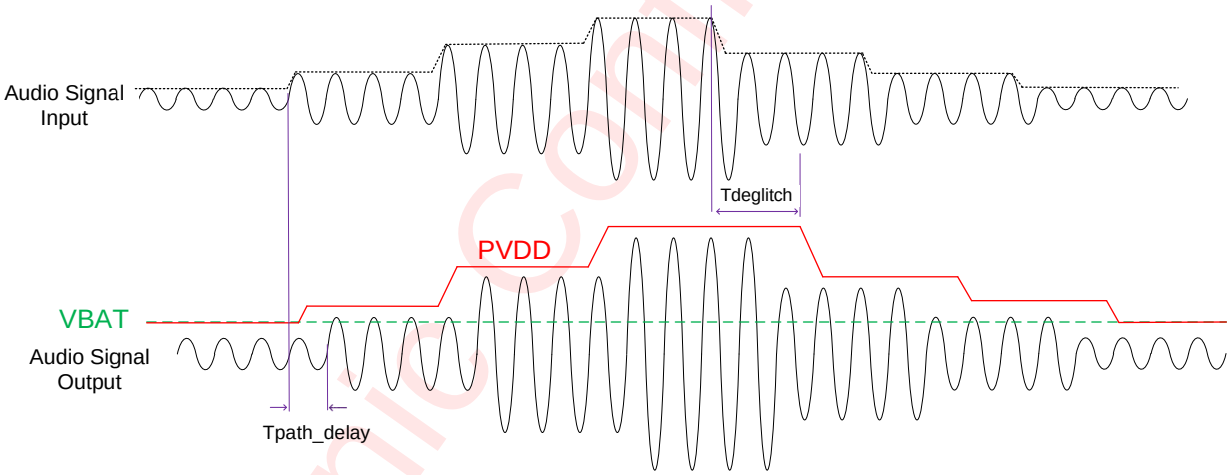


Figure 19 Boost Circuit Behavior in Smart Boost 2 Mode

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (Short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when under voltage occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place or not.

BATTERY VOLTAGE MONITORING

The device monitors the voltage on the VDD pin, which is most commonly the battery for the system. The battery voltage level is available via bits VBAT_DET in the Battery Supply Voltage register VBAT. Status bits VBAT_DET can be used to calculate the battery voltage. The battery voltage level V_{BAT} is:

$$V_{BAT} = \frac{VBAT\_DET}{2^{10} - 1} \times 6.025V$$

For example, if VBAT_DET = 1001100011, the battery voltage level V_{BAT} is equal to 3.6V.

DIE TEMPERATURE MONITORING

The device monitors the die temperature and the result is available via bits TEMP_DET in the Temperature register TEMP. The TEMP_DET is a two's complement value. For example, if TEMP_DET = 00011001, the die temperature is 25℃.

CURRENT SENSING

The device provides speaker current sense for real time monitoring of loudspeaker behavior. Current sensing is not disturbed by capacitance (<1nF) on the output lines or on the long speaker tracks. The current sensing transfer function I_{SNS} is:

$$I_{SNS} = \frac{D_{OUT}}{2^{15} - 1} \times 3.125A$$

D_{OUT}: the current sense I²S output stream

VOLTAGE SENSING

In the device, the speaker voltage sensing is done either internally before signal is being output to speaker or externally at speaker pads. This function is for real time monitoring of loudspeaker behavior. The voltage sensing transfer function V_{SNS} is:

$$V_{SNS} = \frac{D_{OUT}}{2^{15} - 1} \times V_{fs}$$

The V_{fs} of internally and externally voltage sensor is 12.6V and 18.875V respectively.

AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP\_NORM\_V \times D_{in}$$

D_{in}: the level of input signal with a range from -1 to +1.

AMP_NORM_V: the equivalent amplifier output voltage when D_{in} is 1. In receiver mode the AMP_NORM_V is 4.5V, in speaker mode it's 12V.

RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 9.3μV. Speaker and Receiver combo applications can be realized without changing any hardware.

When the device is set to receiver mode, the power supply of Class D driver stage is from VDD directly without boost.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode plus at 1 MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

Table 4 Address Selection

AD2	AD1	Address(7-bit)
GND	GND	0x34
GND	VDDIO	0x35
VDDIO	GND	0x36
VDDIO	VDDIO	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

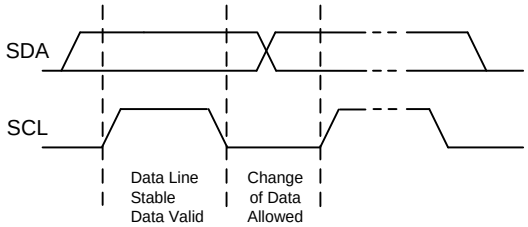


Figure 20 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

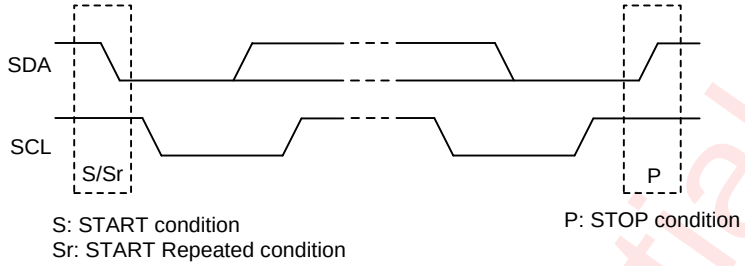


Figure 21 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

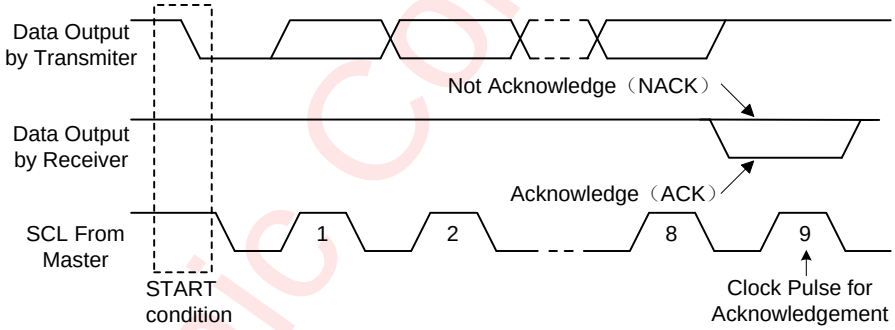


Figure 22 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

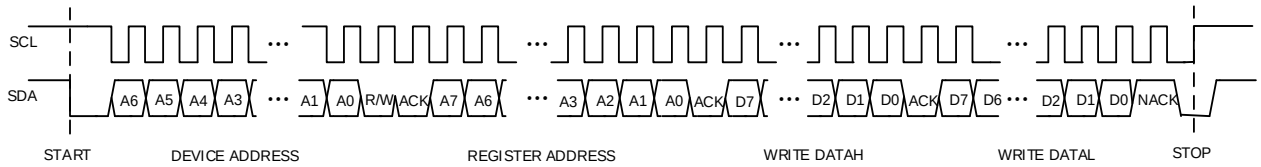


Figure 23 I²C Write Byte Cycle

In a write process, the following steps should be followed:

a) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends high data byte of 16-bit data to be written to the addressed register.

g) Slave sends acknowledge signal.

h) Master sends low data byte of 16-bit data to be written to the addressed register.

i) Slave sends acknowledge signal.

j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g).

k) Master generates STOP condition to indicate write cycle end.

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

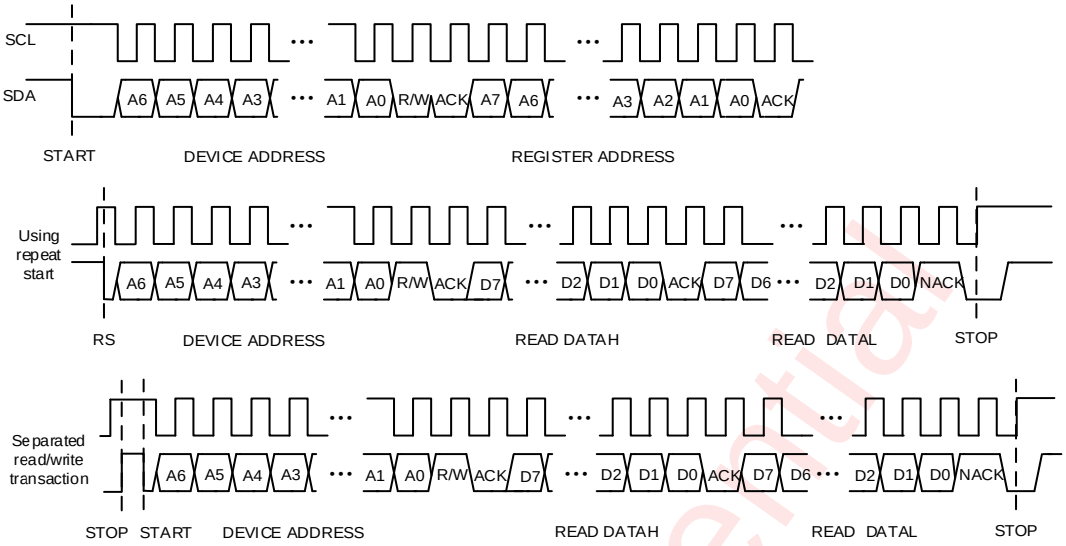


Figure 24 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	RO	IDCODE																0x2183
0x01	SYSST	RO		UVLS	ADPS	DSPS	BSTOCS	OVPS	BSTS	SWS		WDS	NOCLKS	CLKS	OCDS		OTHS	PLLS	0x0000
0x02	SYSINT	RC		UVLI	ADPI	DSPI	BSTOCI	OVPI	BSTI	SWI		WDI	NOCLKI	CLKI	OCDI		OTHI	PLLI	0x0000
0x03	SYSINTM	RW		UVLM	ADPM	DSPM	BSTOCM	OVPM	BSTM	SWM		WDM	NOCLKM	CLKM	OCDM		OTHM	PLLM	0xFFFB
0x04	SYSCTRL	RW		SPK_GAIN	RCV_GAIN		RMSE	HAGCE	HDCCE	HMUTE	RCV_MODE	I2SEN	WSINV	BCKINV	IPLL	DSPBY	AMPPD	PWDN	0xE307
0x05	SYSCTRL2	RW	EN_MPD				INTMODE	INTN	VOL										0x8000
0x06	I2SCTRL1	RW	INPLEV	CFSEL			CHSEL		I2SMD		I2SFS		I2SBCK		I2SSR				0x04E8
0x07	I2SCTRL2	RW	FSYNC_TYPE	SLOT_NUM			I2S_TX_SLOTVLD				I2S_RXR_SLOTVLD				I2S_RXL_SLOTVLD				0x0010
0x08	I2SCTRL3	RW	IV2CH	I2SDOSEL	DOHZ	I2SCHS	DRVSTREN	I2SRXEN	I2STXEN	I2S_TXEDGE	ULS_MODE	ULS_EN	LPBK		I2S_RXULS_SLOTVLD				0x2C01
0x09	DACCFG1	RW	RVTH								AVTH								0x3940
0x0a	DACCFG2	RW	ATTH																0x0030
0x0b	DACCFG3	RW	RTTH																0x01E0
0x0C	DACCFG4	RW									HOLDTH								0x1C64
0x16	PWMCTRL3	RW			NOISE_GATE_EN														0x82BA
0x21	VBAT	RO					VBAT_DET												0x02EB
0x22	TEMP	RO					TEMP_DET												0x0019
0x23	PVDD	RO					PVDD_DET												0x02A0
0x42	WDT	RO									WDT_CNT								0x0000
0x60	BSTCTRL1	RW	BST_MODE				BST_RTH					BST_ATH							0xC404
0x61	BSTCTRL2	RW	BST_IPEAK				BST_TDEG					BST_VOUT_SET							0x5B58

DETAILED REGISTER DESCRIPTION

ID: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	IDCODE	RO	Chip ID (2183h) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x2183

SYSST: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RO	Not used	0
14	UVLS	RO	VDD under voltage indicator 0: Normal 1: UVLO	0
13	ADPS	RO	Boost Adaptive status. 0: Pass Through 1: Boost	0
12	DSPS	RO	Set when at least one DSP acknowledge request flag is set 0: Normal 1: DSP request	0
11	BSTOCS	RO	Boost over current indicator 0: Normal 1: Over Current	0
10	OVPS	RO	Boost OVP status indicator 0: Normal 1: OVP	0
9	BSTS	RO	Boost start up status. 0: Not finished 1: Finished	0
8	SWS	RO	Amplifier switching status. 0: Not switching 1: Switching	0
7	Reserved	RO	Not used	0
6	WDS	RO	DSP watch-dog status 0: Normal 1: Abnormal	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Normal 1: OC	0
2	Reserved	RO	Not used	0

1	OTHS	RO	Die Temperature is higher than 150℃ 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RC	Not used	0
14	UVLI	RC	Interrupt indicator for Power On and UVLS	0
13	ADPI	RC	Interrupt indicator for ADPS	0
12	DSPI	RC	Interrupt indicator for DSPS.	0
11	BSTOCI	RC	Interrupt indicator for BSTOCS.	0
10	OVPI	RC	Interrupt indicator for OVPS.	0
9	BSTI	RC	Interrupt indicator for BSTS.	0
8	SWI	RC	Interrupt indicator for SWS.	0
7	Reserved	RC	Not used	0
6	WDI	RC	Interrupt indicator for WDS	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	Reserved	RC	Not used	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

Note: It will be set to '1' once corresponding status bit changed, and all the interrupt bits will be cleared after reading 0x02 via IIC bus.

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	1
14	UVLM	RW	Interrupt mask for UVLI.	1
13	ADPM	RW	Interrupt mask for ADPI	1
12	DSPM	RW	Interrupt mask for DSPI.	1
11	BSTOCM	RW	Interrupt mask for BSTOCI.	1
10	OVPM	RW	Interrupt mask for OVPI	1
9	BSTM	RW	Interrupt mask for BSTI.	1
8	SWM	RW	Interrupt indicator for SWI.	1
7	Reserved	RW	Not used	1
6	WDM	RW	Interrupt mask for WDI.	1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	Reserved	RW	Not used	0
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

Note: All the mask bits are high-active. The interrupt will be masked when its corresponding mask bit is set to “1”, then this interrupt will not be sent to INTN pin.

SYSCTRL: (Address 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RW	Not used	1
14	SPK_GAIN	RW	Speaker Mode gain setting 0: 6.31 AV 1: 12.62 AV	1
13:12	RCV_GAIN	RW	Configuration for gain in Receiver Mode 00: 3.4 AV 01: 4.53 AV 10: 6.8 AV 11: Reserved	2
11	RMSE	RW	Hardware AGC mode selection 0: Peak AGC 1: RMS AGC	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: Disable 1: Enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: Disable 1: Enable	1
8	HMUTE	RW	Disable/Enable Hardware mute module 0: Disable 1: Enable	1
7	RCV_MODE	RW	Receiver mode enable, active "1". VCOM is 1/3*PVDD for speaker, and 1/2*PVDD for receiver. 0: Speaker 1: Receiver	0
6	I2SEN	RW	Disable/Enable whole I2S interface module 0: Disable 1: Enable	0
5	WSINV	RW	I2S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I2S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: WCK	0
2	DSPBY	RW	DSP bypass control bit 0: Working 1: Bypass	1
1	AMPPD	RW	Amplifier power down control bit, PowerDown until system configuration finished 0: Working 1: Power Down	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 05h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	EN_MPD	RW	Disable/Enable MPD multi stage power mode, Gain will be automatically adjusted only when EN_MPD is high. It can enable the small-signal detection or not, based on the audio input, so that the quiescent current could be reduced and the noise level will be smaller. 0: Disable 1: Enable	1
14:12	Reserved	RW	Not used	0
11	INTMODE	RW	Interrupt pad INTN output mode selection 0: Open-drain 1: Push&Pull	0
10	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
9:0	VOL	RW	Volume control, from 0 to -96dB, in unit of -0.094dB	0

I2SCTRL1: (Address 06h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	INPLEV	RW	Input level selection bit, i2s input signal will be attenuated by -6dB at first when this register is set to 1. 0: 0dB 1: -6dB	0
14:12	CFSEL	RW	I2S legacy path output data selection 000: HAGC 001: DFIFO 010: ULS 011: SAR_test 100: IV 101: IVBT 110: Fast IVBT Others: Reserved	0
11:10	CHSEL	RW	Left/right channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:8	I2SMD	RW	I2S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0
7:6	I2SFS	RW	I2S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SBCK	RW	I2S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Reserved	2

3:0	I2SSR	RW	I2S interface sample rate configuration 0000: 8 KHz 0001: 11 KHz 0010: 12 KHz 0011: 16 KHz 0100: 22 KHz 0101: 24 KHz 0110: 32 KHz 0111: 44 KHz 1000: 48 KHz 1001: 96 KHz 1010: 192KHz Others: Reserved	8

I2SCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
15	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-bck	0
14:12	SLOT_NUM	RW	I2S TDM mode control. 000: I2S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: Reserved	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …... 1111: Slot 15	0
7:4	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …... 1111: Slot 15	1
3:0	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …... 1111: Slot 15	0

I2SCTRL3: (Address 08h)

Bit	Symbol	R/W	Description	Default
15	IV2CH	RW	I2S TX channel data packing mode control. When I2SBCK is set to 32*fs mode, Current & Voltage data could be transmitted to I2S Left & Right channels	0

			by Using Special Mode. 0: Legacy 1: Special	
14	I2SDOSEL	RW	I2S unused channel data selection 0: Zeros 1: TXData	0
13	DOHZ	RW	Unused channel Data control, When it is set to 0, all Channels are available. Otherwise Unused channel is set to be HiZ. 0: All 1: HiZ	1
12	I2SCHS	RW	I2S Tx Channel selection 0: Left 1: Right	0
11	DRVSTREN	RW	I2S_DATAO PAD driving strength setting 0: 4mA 1: 12mA	1
10	I2SRXEN	RW	Disable/Enable I2S receiver module 0: Disable 1: Enable	1
9	I2STXEN	RW	Disable/Enable I2S transmitter module 0: Disable 1: Enable	0
8	I2S_TXEDGE	RW	I2S TX clock edge selection 0: negedge 1: posedge	0
7	ULS_MODE	RW	Ultrasonic mode control 0: LowPass 1: TDM	0
6	ULS_EN	RW	Ultrasonic mode enable 0: Disable 1: Enable	0
5:4	LPBK	RW	I2S data Loopback control bits 00: Disable 01: Far-Back 10: Near-Back 11: Reserved	0
3:0	I2S_RXULS_SLOTVLD	RW	RX ultrasonic channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 …… 1111: Slot 15	1

DACCFG1: (Address 09h)

Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x39

7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC) : P0= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC) : P0=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Speaker Gain configured by SYSCTRL.SPK_GAIN and SYSCTRL2.VOL . RLoad is 8ohm	0x40

DACCFG2: (Address 0ah)

Bit	Symbol	R/W	Description	Default
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x0030

DACCFG3: (Address 0bh)

Bit	Symbol	R/W	Description	Default
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0ch)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RW	Not used	0x1C
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x64

PWMCTRL3: (Address 16h)

Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	0x2
13	NOISE_GATE_EN	RW	Enable/Disable of noise gate function 0: Disable 1: Enable	0x0
12:0	Reserved	RW	Not used	0x02ba

VBAT: (Address 21h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	VBAT_DET	RO	Detected Voltage of battery, and the full scale is 6.025V VBAT=(VBAT_DET)/1023×6.025	0x2EB

TEMP: (Address 22h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0

9:0	TEMP_DET	RO	Detected Die Temperature (Two's Complement), typical values are as follows. 0x3D8 : -40 degree 0x00 : 0 degree 0x01 : 1 degree 0x19 : 25 degree 0x37 : 55 degree	0x019

PVDD: (Address 23h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	PVDD_DET	RO	Detected Voltage of PVDD, and the full scale is 12.05V PVDD=(PVDD_DET)/1023×12.05	0x2A0

WDT: (Address 42h)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RO	Not used	0
7:0	WDT_CNT	RO	Watch dog timer count	0

BSTCTRL1: (Address 60h)

Bit	Symbol	R/W	Description	Default
15:14	BST_MODE	RW	BOOST mode selection, Initialize to 3 . 00: Pass Through 01: Power Exter 10: Smart Boost 1 11: Smart Boost 2	0x3
13:7	BST_RTH	RW	Smart boost release threshold setting, When signal is above over the threshold, the voltage of PVDD will be raised up higher than VDD in smart boost mode Release threshold = ((BST_RTH /128 * SET_GAIN)**2)/2/Rload, which SET_GAIN represents actual gain of Class-D, and is determined by SYSCTRL.SPK_GAIN or SYSCTRL.RCV_GAIN	8
6:0	BST_ATH	RW	Smart boost attack threshold setting. When signal is below the threshold, the voltage of PVDD will be equal to VDD in smart boost mode. Attack threshold = ((BST_ATH/128 * SET_GAIN)**2)/2/Rload, which SET_GAIN represents actual gain of Class-D, and is determined by SYSCTRL.SPK_GAIN or SYSCTRL.RCV_GAIN	4

BSTCTRL2: (Address 61h)

Bit	Symbol	R/W	Description	Default
15:12	BST_IPEAK	RW	Boost peak current limiter threshold 0000: 1.5A 0001: 1.75A 0010: 2.0A 0011: 2.25A 0100: 2.5A 0101: 2.75A 0110: 3.0A 0111: 3.25A	5

			1000: 3.5A 1001: 3.75A 1010: 4A 1011: 4.25A 1100: 4.50A Others: Reserved	
11:8	BST_TDEG	RW	Smart Boost small signal level detection deglitch time 0000: 0.50 ms 0001: 1.00 ms 0010: 2.00 ms 0011: 4.00 ms 0100: 8.00 ms 0101: 10.7 ms 0110: 13.3 ms 0111: 16.0 ms 1000: 18.6 ms 1001: 21.3 ms 1010: 24.0 ms 1011: 32.0 ms 1100: 64.0 ms 1101: 128 ms 1110: 256 ms 1111: 1200 ms	11
7	Reserved	RW	Not used	0
6:0	BST_VOUT_SET	RW	BOOST max output Voltage control bits (62.5mV/Step) 0000000~0010111: reserved 0011000: 5V …… 1101100: 10.25V others: reserved	0x58

APPLICATION INFORMATION

EXTERNAL COMPONENTS

BOOST INDUCTOR SELECTION

Inductance value is limited by the boost converter's internal loop compensation, a large L_{SW} will reduce the phase margin of the DC-to-DC converter. Also, the inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency under all operating conditions, the recommended value of inductor is 1μH.

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, inductance value will decline since the magnetic core begins to saturate; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. The inductor saturation current rating could to be considered with the following equation:

$$I_{L\_PEAK} = \frac{2 * P_{OUT}}{\eta * VDD} + \frac{VDD * (PVDD - VDD)}{2 * L_{SW} * F_{BST} * PVDD}$$

Following is the inductor selection reference for typical speaker impedances.

VDD (V)	PVDD (V)	R_L (Ω)	Efficiency (%)	P_{OUT} (W)	I_{L_PEAK} (A)	I_{SAT_min} (A)
4.2	10.25	8	77	5.7	4.1	4.5
4.2	10.25	6	75	5.8	4.3	4.5

BOOST CAPACITOR SELECTION

Boost output capacitor is usually within the range 0.1μF~47μF. The ceramic capacitors with low ESR are recommended for low ripple voltage which is determined as following equation:

$$\Delta PVDD = \frac{(PVDD - VDD) * I_{OUT}}{\eta * PVDD * F_{BST} * C_{OUT}} + \left(\frac{I_{OUT} * PVDD}{VDD} + \frac{VDD * (PVDD - VDD)}{2 * L_{SW} * F_{BST} * PVDD}\right) * R_{C\_ESR}$$

Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the material, size, capacitor voltage, and capacitance values. It is suggested to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance.

Please notice the DC bias characteristics when selecting capacitors. For typical applications, it is necessary to ensure that the residual capacitance is higher than **3.6μF.** Take the following capacitances as the output capacitor of boost for example:

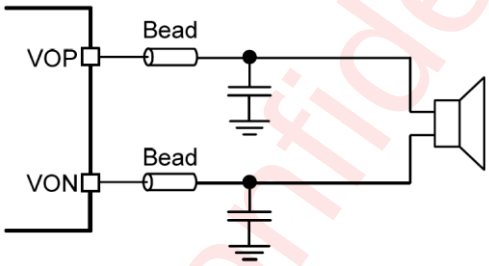
Value	Material	Size (mm^3)	Rated Voltage	Quantity	Value@10.25V
10μF	X5R	1.60×0.80×0.40 (0603)	25V	2	3.8μF
22μF	X5R	2.00×1.25×0.50 (0805)	25V	1	4.2μF

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 1μF low equivalent-series-resistance (ESR) ceramic capacitor is recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 1μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 25V.

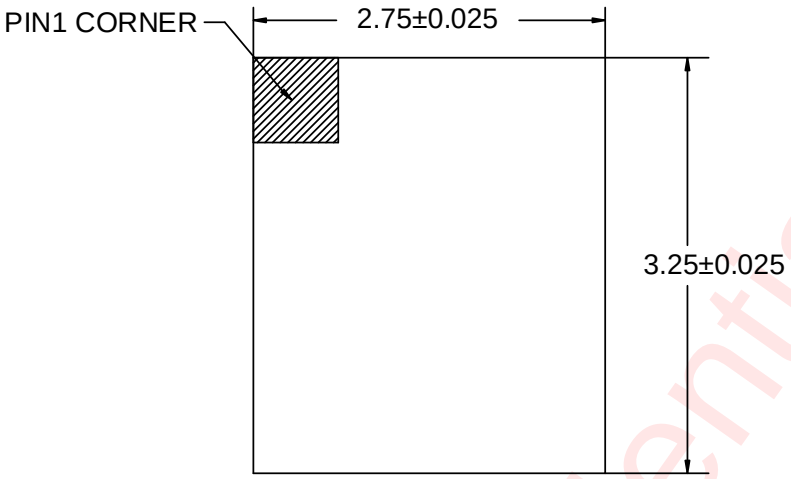


LAYOUT CONSIDERATION

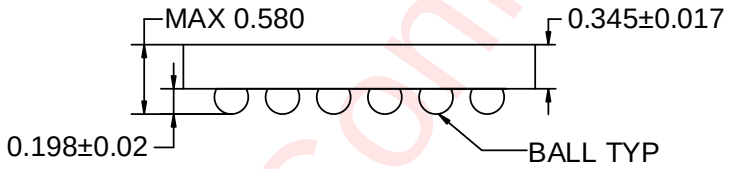
In order to obtain excellent performance of the PA, the below PCB layout guidelines should be followed:

1. All the filter capacitors should be placed close to the corresponding pins of the PA, including VBST, VDD, DVDD, VDDIO.
2. The traces of SW pin should support currents up to the device over-current limit (peak current 4.5A), and the input line from the battery to the SW pin should be traced above 4A current drive.
3. For the case of speaker impedance equal to 8Ω, try to provide a separate, short and thick power line to the PA, the copper width is recommended to be larger than 4mm.
4. The beads and capacitor should be placed close to the VON and VOP pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 1.2mm.
5. The via numbers determine the current capability. Typically, the boost converter trace need four via to handle the current requirement around 4A.
6. The capacitance on the output lines or on the long speaker tracks should be less than 1nF.

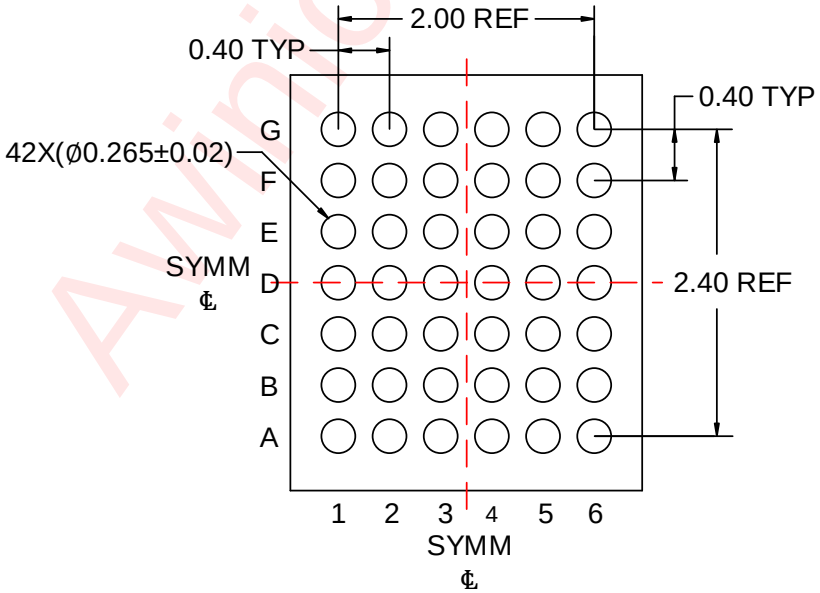
PACKAGE DESCRIPTION



TOP VIEW



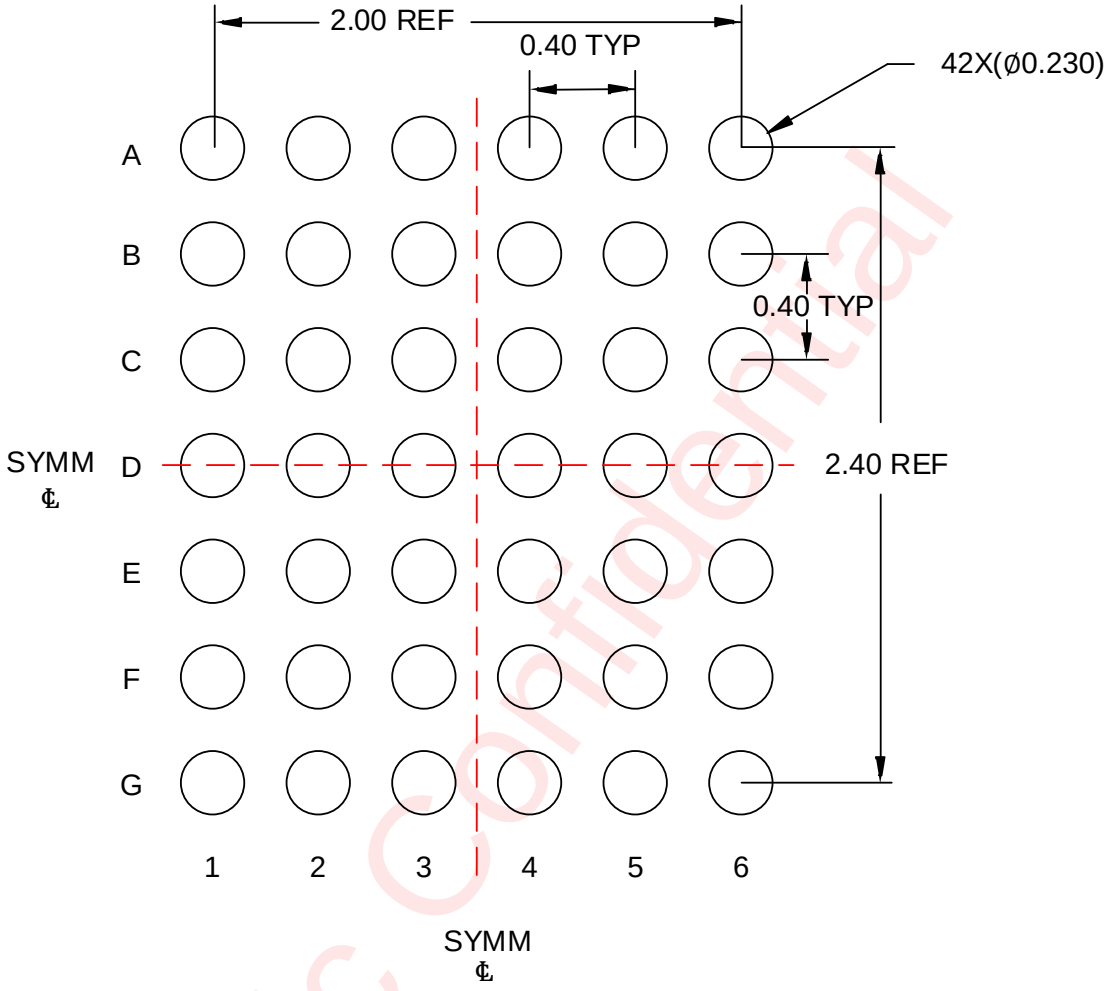
SIDE VIEW

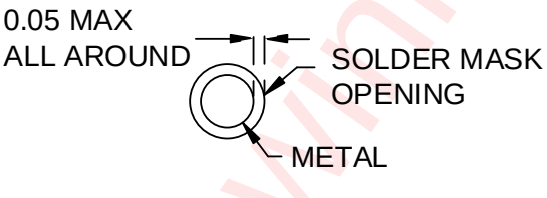


BOTTOM VIEW

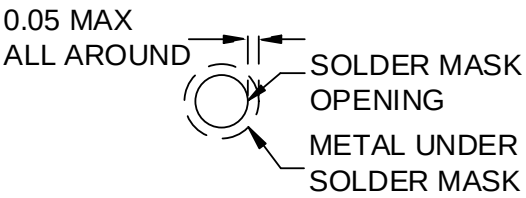
Unit:mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED

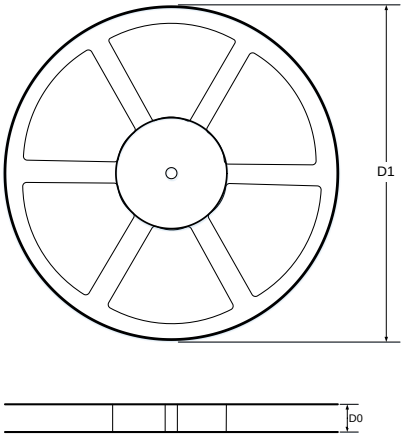


SOLDER MASK DEFINED

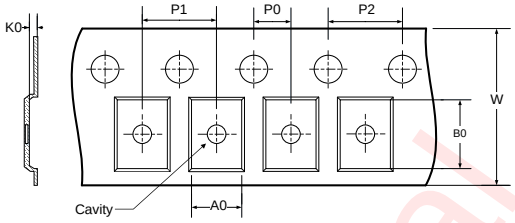
Unit: mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

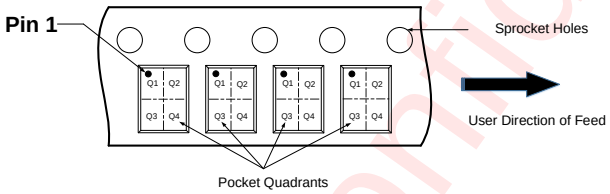


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3	3.35	0.75	2	8	4	12	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Sep. 2023	Officially Released
V1.1	Sep. 2024	Update 4ohm application and PVDD external power supply application description
V1.2	Aug. 2025	EC table add PVDD external power supply operating voltage range EC table add I_{PVDD} Operating mode test condition

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