

FM Low-Noise-Amplifier with differential output

FEATURES

- Without any earphone or telescopic antenna, receive FM-radio signal through re-using normal antenna
- Differential output
- Internal 4-bit tunable capacitor-array using One-Line-Logic unit
- Ultra-low noise-figure: 1.7dB
- Standard CMOS process technology
- High power gain of 21dB under 2.8V supply
- High linearity
- Supply voltage: 1.5V~3.6V
- Shut-down current: <math><0.1\mu\text{A}</math>
- Slim 1.1x0.7x0.405 mm³ ECP-6L package

GENERAL DESCRIPTION

AW5027 is a Low-Noise-Amplifier (LNA) with differential output, without earphone or telescopic antenna, re-using normal antenna to receive FM-radio signal

AW5027 adopt differential outputs, enhance the level of anti interference capability

AW5027 is characterized with low noise, high gain and high linearity. Typical noise figure is 1.7dB and power gain is 21dB

AW5027 integrates RF radio switch inside, implementing high impedance under shut-down condition. Shut-down current is less than 0.1 μA

AW5027 is available in slim 1.1mmx0.7mm x0.405mm ECP-6L package. The specified operating free-air temperature ranges from -40 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$.

APPLICATIONS

- Feature or Smart mobile phone
- Mobile audio device

TYPICAL APPLICATION CIRCUIT

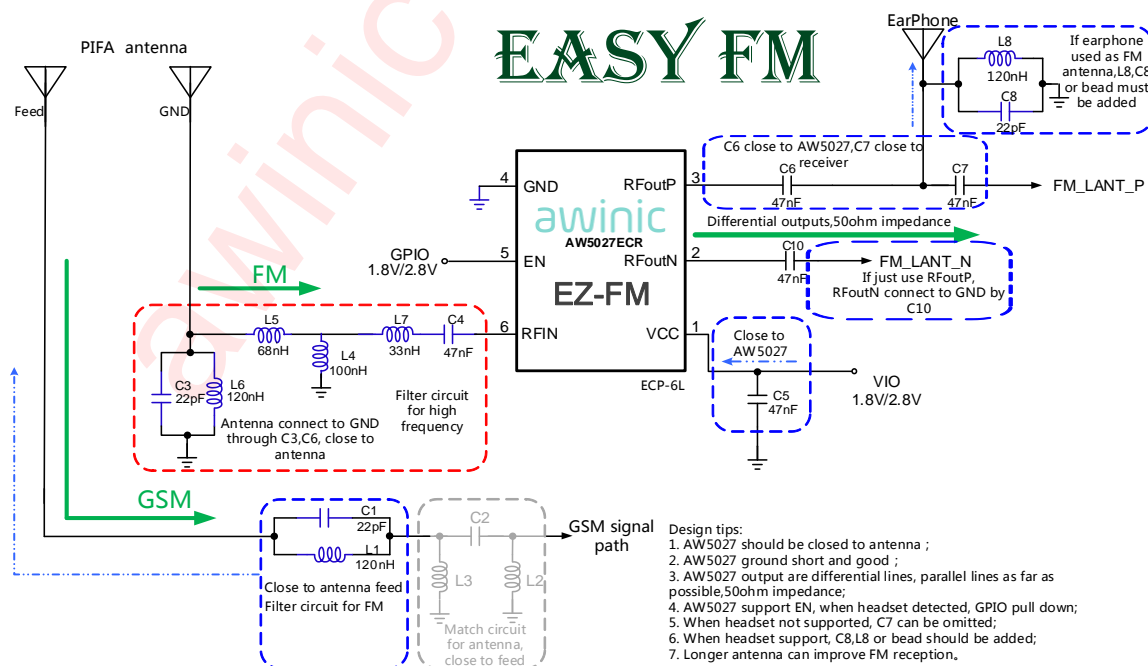


Figure 1 Typical Application Circuit of AW5027

PIN CONFIGURATION AND TOP MARK

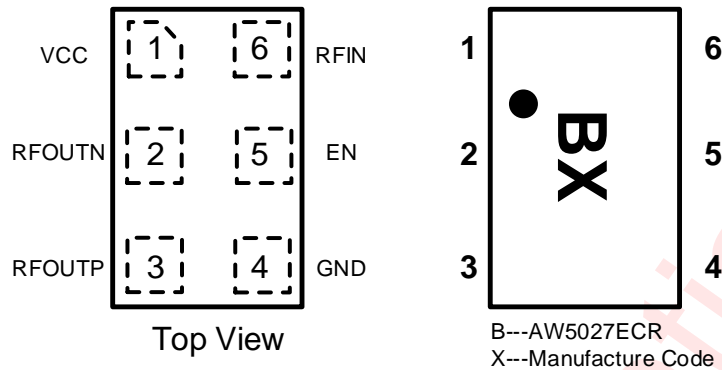


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	VCC	Supply connection.
2	RFOUTN	RF output N.
3	RFOUTP	RF output P.
4	GND	Ground.
5	EN	EN (high level) supports 1.8V/2.8V IO with internal 150Kohm pull-down resistor.
6	RFIN	RF input.

FUNCTIONAL BLOCK DIAGRAM

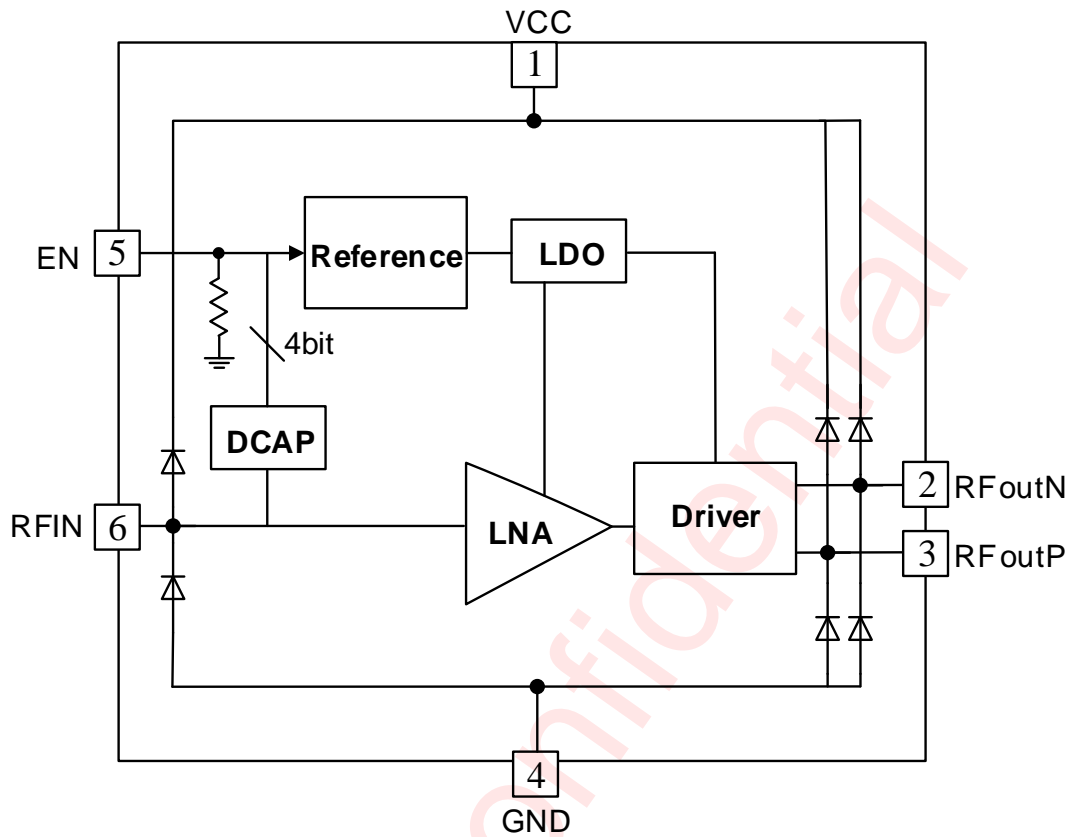
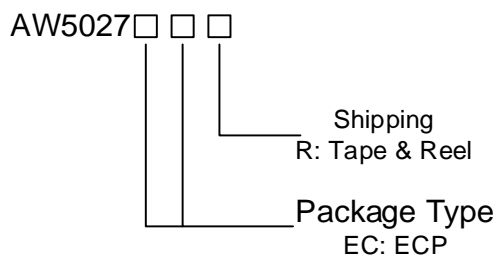


Figure 3 FUNCTION BLOCK DIAGRAM

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW5027ECR	-40°C ~ 85°C	ECP 1.1mm*0.7mm - 6L	B	MSL1	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATINGS (NOTE1)

PARAMETERS	RANGE
Supply Voltage VCC	-0.3 V to 4.2 V
EN pin voltage	-0.3 V to 4.2 V
Supply maximum current ICC	30 mA
RFIN input power Pin	20 dBm
Maximum Junction temperature T _{JMAX}	125 °C
Storage temperature T _{STG}	-65 °C to 150 °C
Operating free-air temperature range	-40 °C to 85 °C
Lead Temperature (Soldering 10 Seconds)	260 °C
ESD ^(NOTE 2)	
HBM	±2kV
CDM	±1kV
Latch-up	
JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT: +200mA -IT: -200mA

ELECTRICAL CHARACTERISTICS

TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ISD	Shut-down Current	EN=0V		0.1	1	μA
IQ	Static Current	EN=1.8V		7.5		mA
NF	Noise Figure	Input/Output 50ohm		1.8		dB
S11	Input Return Loss	Input/Output 50ohm		-3.5		dB
Kf	Stability Factor	Input/Output 50ohm		>1		
IIP3	Input 3rd-order intercept point	(NOTE 3)		-13.5		dBm
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-22.6		dBm
OOB P-1dB	Output-Of-Band 1dB- compression point	(NOTE 4)		-8.7		dBm
RFoutP						
S12	Reverse Isolation	Input/Output 50ohm		-36.0		dB
S21	Power Gain	Input/Output 50ohm		20.5		dB
S22	Output Return Loss	Input/Output 50ohm		-20.0		dB
RFoutN						
S12	Reverse Isolation	Input/Output 50ohm		-49.5		dB
S21	Power Gain	Input/Output 50ohm		19.4		dB
S22	Output Return Loss	Input/Output 50ohm		-22.8		dB

TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ISD	Shut-down Current	EN=0V		0.1	1	μA
IQ	Static Current	EN=2.8V		10.0		mA
NF	Noise Figure	Input/Output 50ohm		1.7		dB
S11	Input Return Loss	Input/Output 50ohm		-3.2		dB
Kf	Stability Factor	Input/Output 50ohm		>1		
IIP3	Input 3rd-order intercept point	(NOTE 3)		-11.2		dBm
IB P-1dB	In-Band 1dB-compression point	Input/Output 50ohm		-21.4		dBm
OOB P-1dB	Output-Of-Band 1dB- compression point	(NOTE 4)		-7.9		dBm
RFoutP						
S12	Reverse Isolation	Input/Output 50ohm		-38.2		dB
S21	Power Gain	Input/Output 50ohm		21.2		dB
S22	Output Return Loss	Input/Output 50ohm		-22.3		dB
RFoutN						
S12	Reverse Isolation	Input/Output 50ohm		-48.9		dB
S21	Power Gain	Input/Output 50ohm		20.7		dB
S22	Output Return Loss	Input/Output 50ohm		-23.3		dB

ELECTRICAL CHARACTERISTICS OF TUNABLE CAPACITOR

TA=25 °C, VCC=1.5~3.6V, EN=VCC, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).

PARAMETER		MIN	TYP	MAX	UNIT
V _{cc}	Supply Voltage	1.5	2.8	3.6	V
T _H	EN High Level Duration Time	0.4		50	μs
T _L	EN Low Level Duration Time	0.4		50	μs
T _{LATCH}	EN State Latch Time ^(NOTE 5)	150		500	μs
T _{OFF}	EN Off Delay Time ^(NOTE 6)	150		500	μs
n	Tunable Stage Number		16		
C _{min}	Minimum Tunable Capacitor		15		pF
C _{max}	Maximum Tunable Capacitor		45		pF
C _{step}	Minimum Stage		2		pF

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

NOTE3: Measure IIP3 parameter through two tones of -40dBm/tone with the frequency of 97M and 98MHz

NOTE4: Input/Output are both 50-ohm; Input signal is composed of in-band 90-MHz signal and out-of-band 900MHz signal. Signal of 90-MHz is fixed to -40-dBm; signal of 900MHz varies and power level is measured when power gain of 90MHz signal drops 1dB.

NOTE5: Latch mechanism is already designed inside. When pulse width of high-level is wider than state latch time, chip will keep latch state inside unchanged and won't accept any new pulses, until off state.

NOTE6: Latch mechanism is already designed inside. When EN is changed from high-level to low-level, state inside will be changed to off after off delay time.

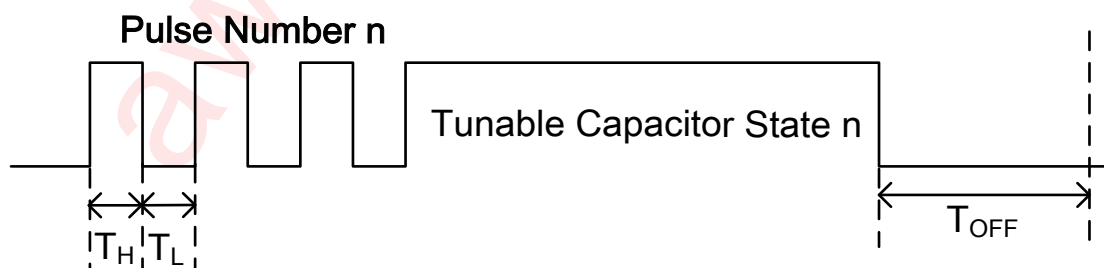
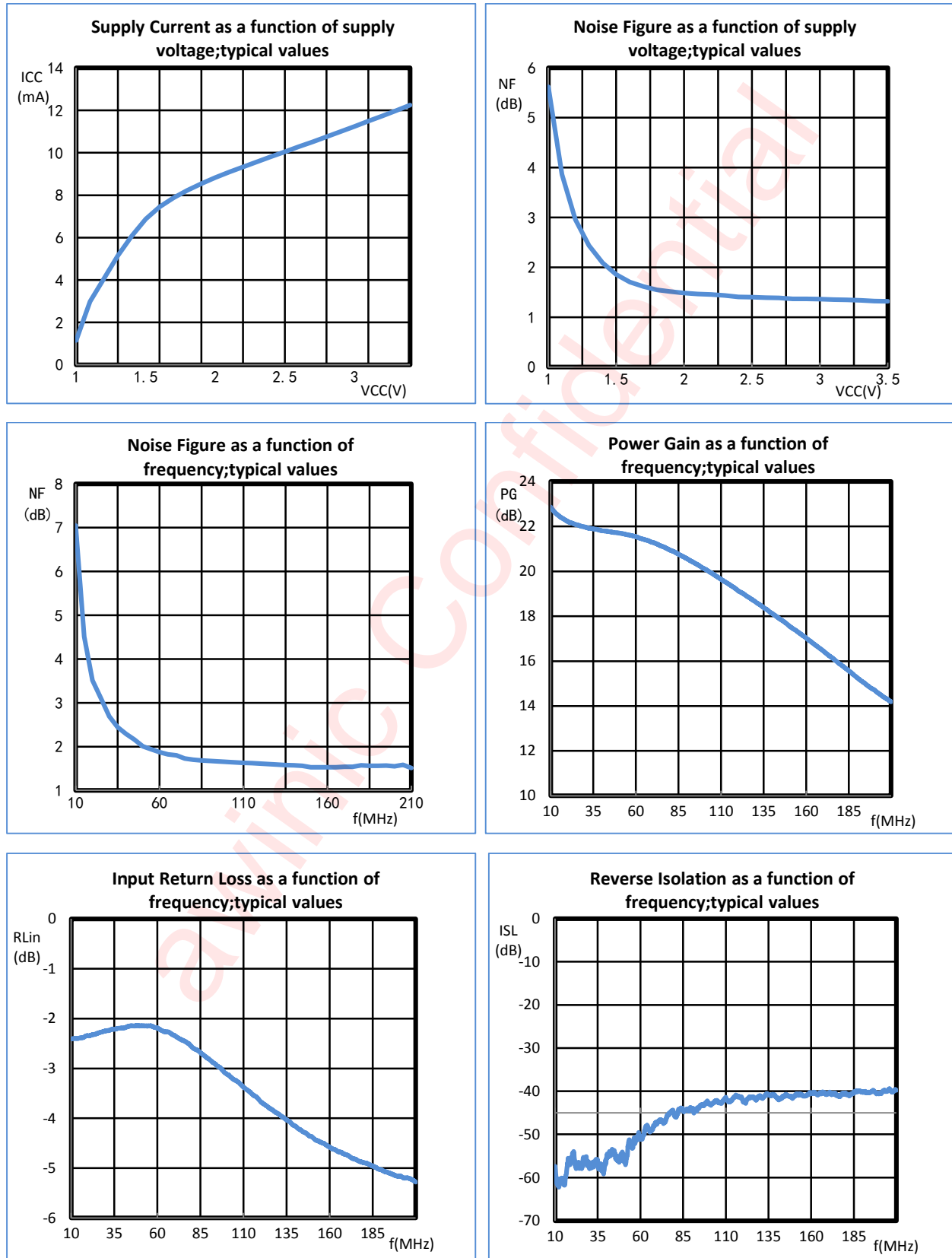
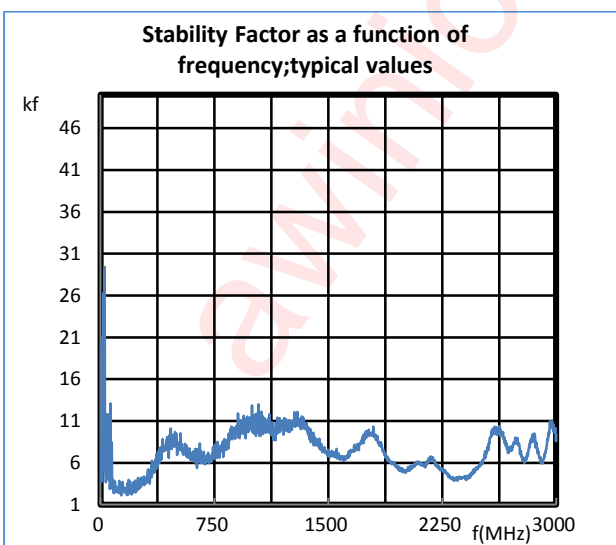
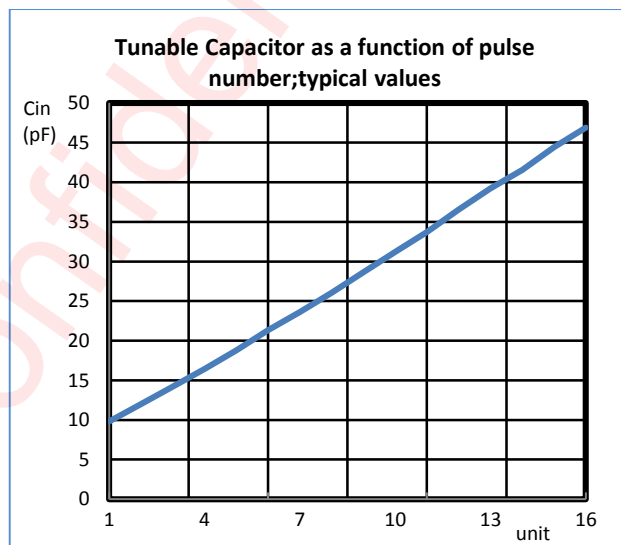
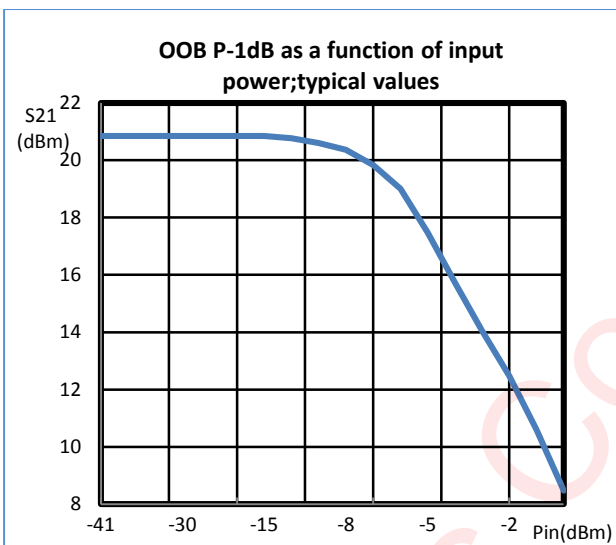
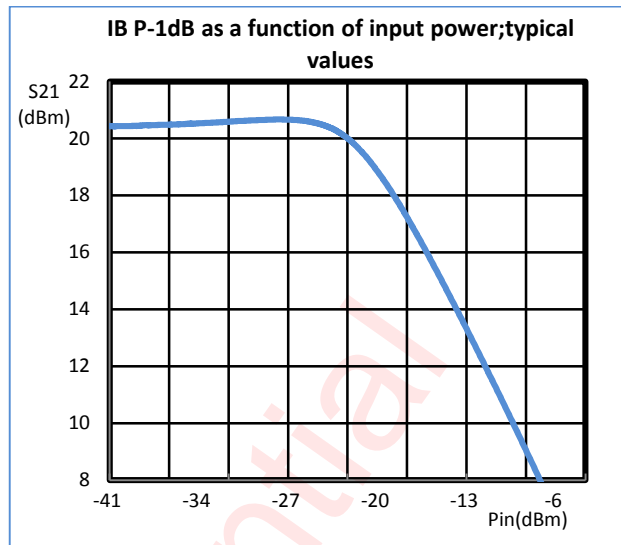
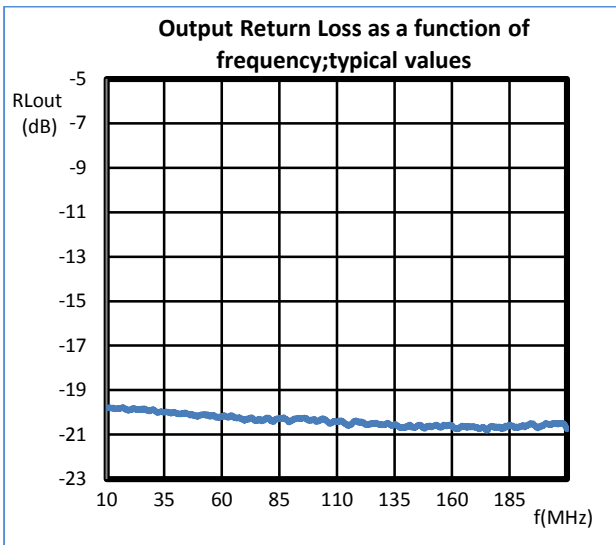


Figure 4 One-Line-Logic Timing Diagram

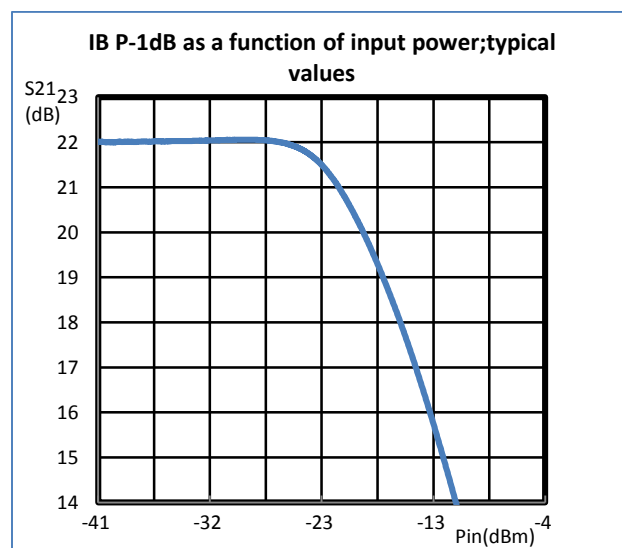
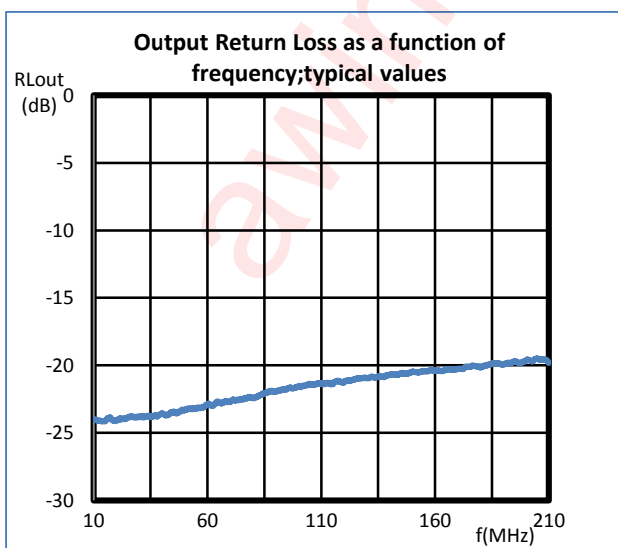
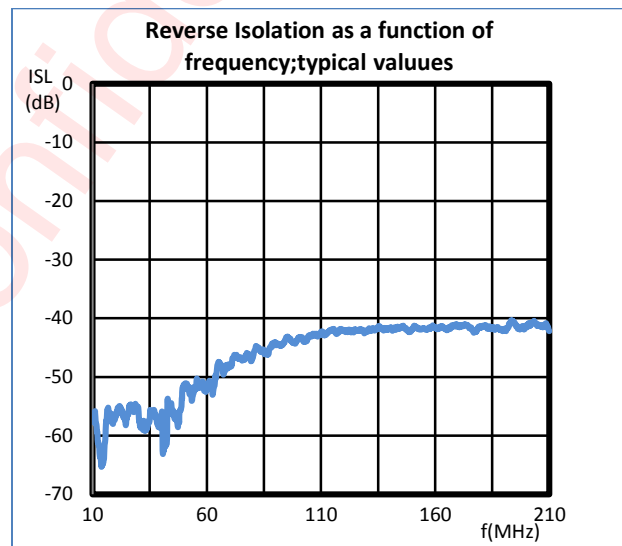
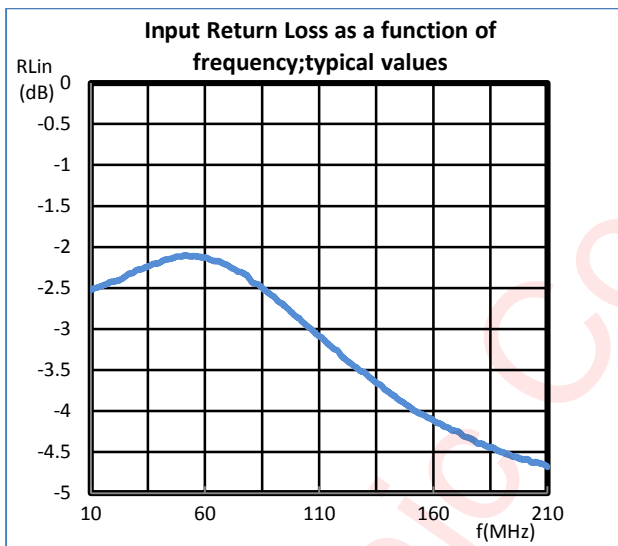
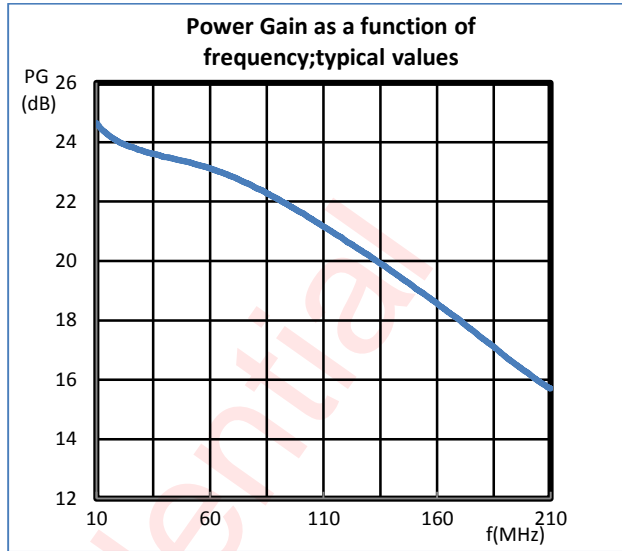
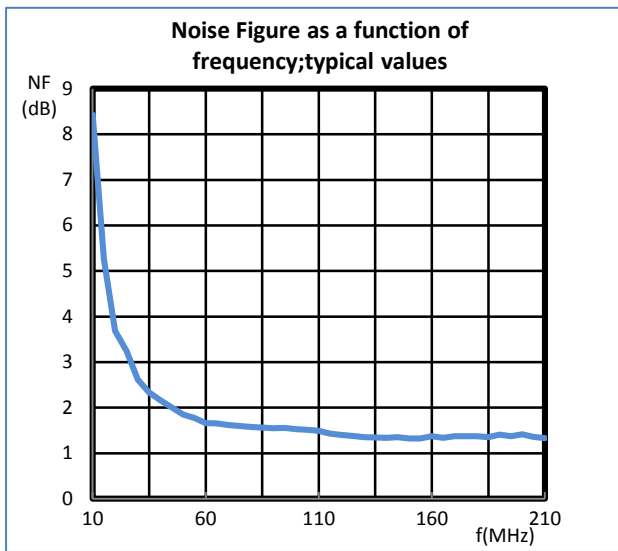
TYPICAL CHARACTERISTICS

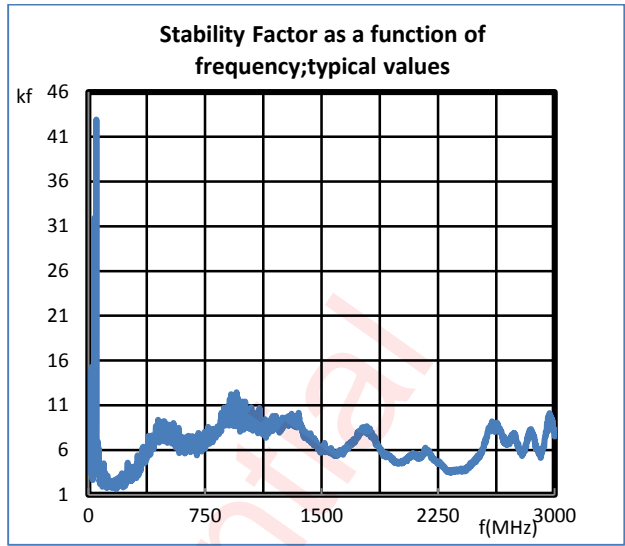
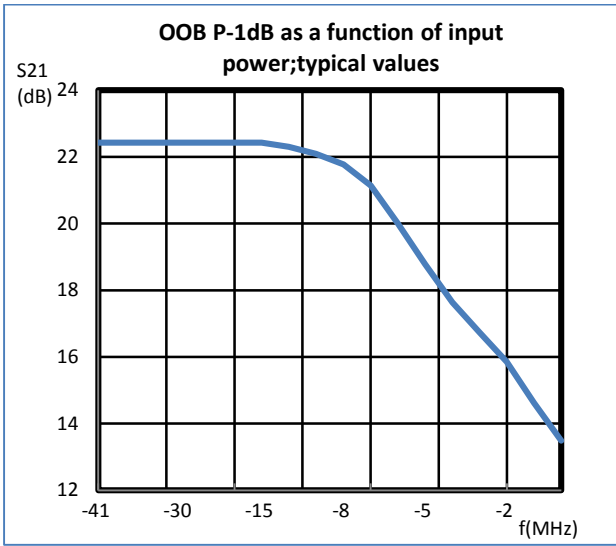
TA=25 °C, VCC=1.8 V, EN=1.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).



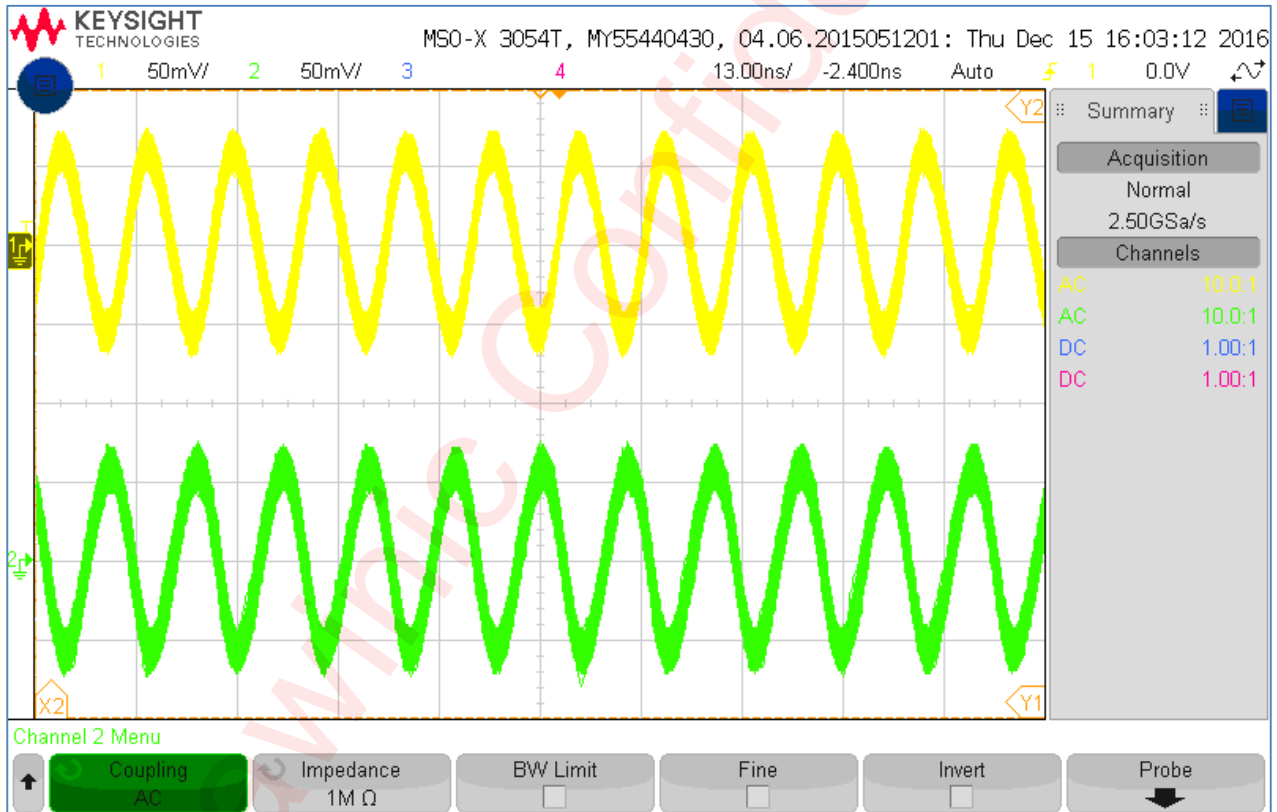


TA=25 °C, VCC=2.8 V, EN=2.8 V, Rs=Ro=50 ohm, frequency=90 MHz for typical values (unless otherwise noted).





Differential Outputs



AW5027 APPLICATION BOARD

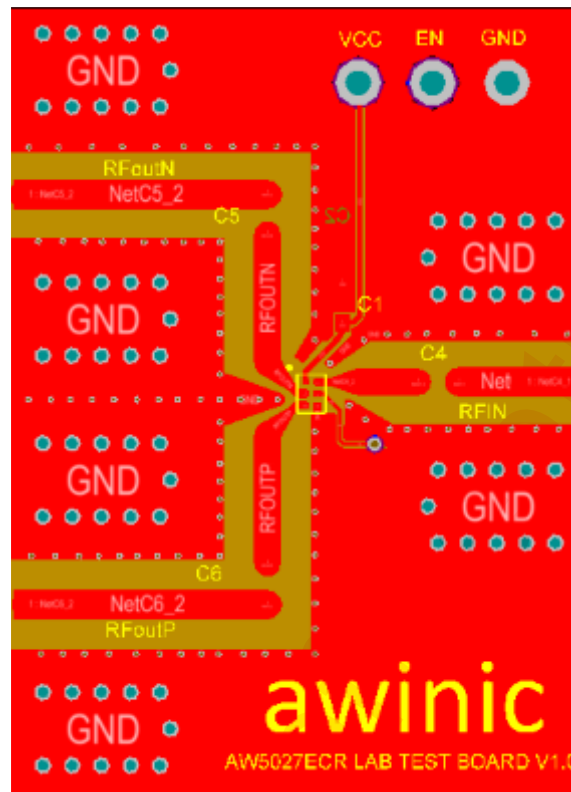


Figure 5 AW5027EVB

MEASUREMENT DIAGRAM

Test DC Characteristics (Current&Power)

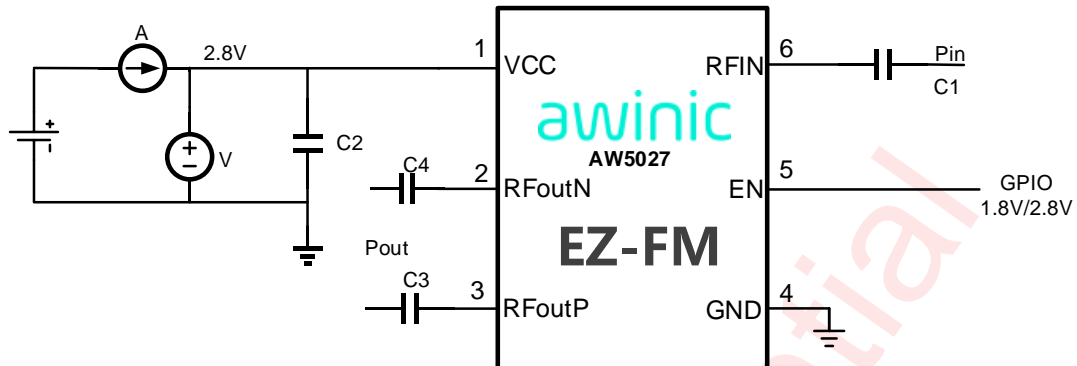


Figure 6 AW5027 DC Test diagram

Test S-parameter

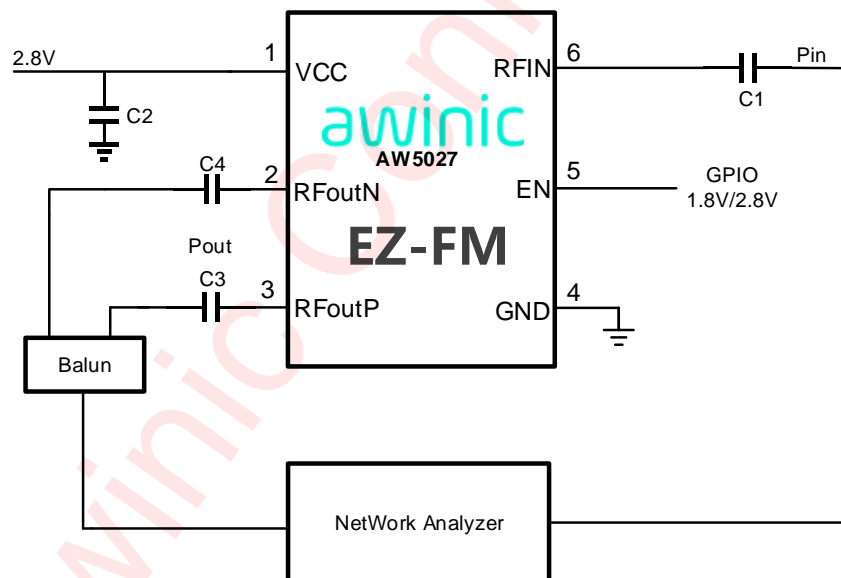


Figure 7 AW5027 S-parameter measurement Diagram

Test Noise-Figure

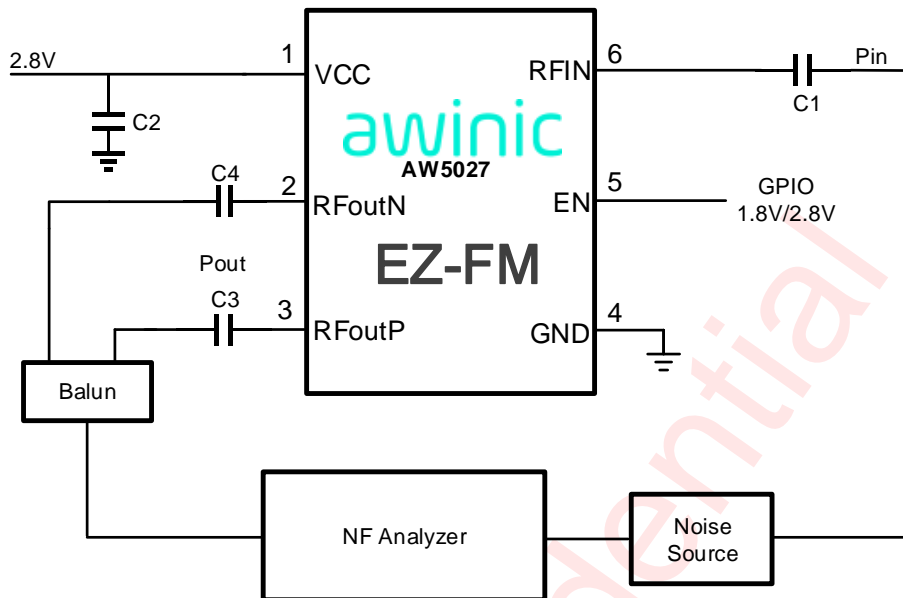


Figure 8 AW5027 Noise Figure Measurement Diagram

Test IIP3

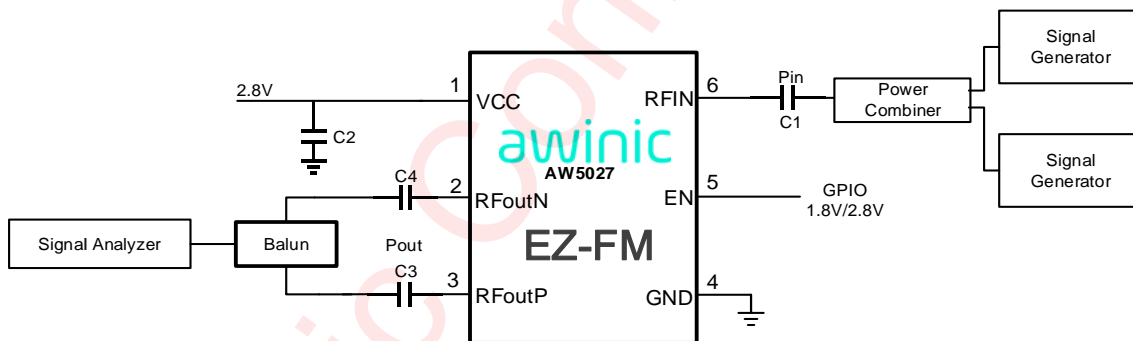


Figure 9 AW5027 IIP3 Measurement Diagram

Test Tunable Capacitor

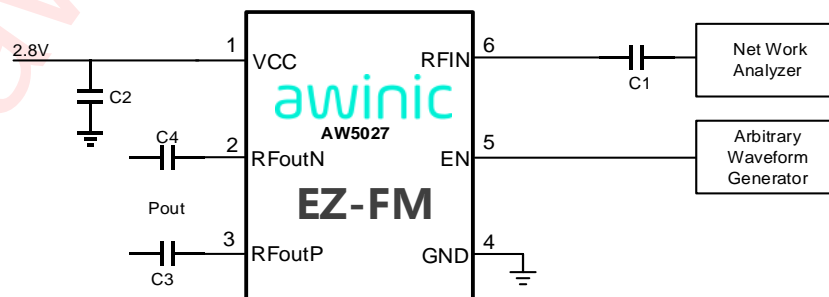


Figure 10 AW5027 Tunable Capacitor Measurement Diagram

APPLICATION INFORMATION

Choice of components

Take Figure 1 for example:

Filter block near PIFA antenna is composed of L6 and C3. These two components can be removed for Dipole antenna. Typical value of L6 is 120 nH and C3 is 22 pF.

Filter block of FM signal is composed of C1 and L1. GSM signal could go through and FM signal will be blocked. GSM antenna π -type matching circuit is composed of C2, L3 and L2, adjustable based on GSM antenna characteristics. Typically C1 is 22 pF and L1 is 120 nH.

Matching circuit of FM signal path is composed of C4, L4, L5 and L7. FM signal could go through and GSM signal will be blocked. Typically L4 is 100 nH, L5 is 68 nH and L7 is 33 nH.

C5 is supply filtering capacitor. C6 ,C10 are DC-blocking capacitor. Both are 47 nF typically.

Only when supporting earphone antenna application, C7 is added with the value of 47 nF.

Following tables show recommended inductor/capacitor types and values.

CHOICE OF INDUCTOR

PART No.	TYP.	Q(min)	Frequency	MFR	SIZE
LQG15HS33NJ02	33nH	8	100MHz	Murata	0402
LQG15HS68NJ02	68nH	8	100MHz		0402
LQG15HSR12J02	120nH	8	100MHz		0402
LQG15HSR10J02	100nH	8	100MHz		0402
SDCL1005C33NJTDF	33nH	8	100MHz	Sunlord	0402
SDCL1005C68NJTDF	68nH	8	100MHz		0402
SDCL1005CR12JTDF	120nH	8	100MHz		0402
SDCL1005CR10JTDF	100nH	8	100MHz		0402

CHOICE OF CAPACITOR

PART No.	TYP.	Voltage	MFR	SIZE
GRM1555C1H220JA01	22pF	25V	Murata	0402
GRM1555C1H390JA01	39pF	25V		0402
GRM155R71C473KA01	47nF	16V		0402

EN Control

AW5027 supports earphone. When baseband detects earphone inserting, GPIO will pull down, cutting off AW5027 to avoid unnecessary power consumption.

When One-Line-Logic is enabled to change the capacitance of tunable capacitor to improve the voltage gain at the input port, based equivalent diagram is shown as figure 11.

In operation frequency band of FM, short antenna can be approximated to series of open induced voltage and equivalent inductor. Therefore, through tuning capacitance value in input port, the voltage gain can be achieved in specified frequency. Meanwhile the receiver performance will be improved.



Figure 11 AW5027 Frequency Tuning Equivalent Schematic

In schematic, the value of tunable capacitor will be derived as following. f_{boost} is FM operation frequency, L_{eqq} is equivalent inductance of input port towards antenna side, which depends on the type and size of short antenna, C_{in} is tunable capacitance of input port.

$$f_{boost} = \frac{1}{2 * \pi * \sqrt{L_{eqq} * C_{in}}} \text{ (Hz)}$$

Figure 12 shows an example of voltage gain influenced by tunable capacitor. Blue and red curves are voltage gain (equal to input voltage / open induced voltage) with maximum and minimum tunable capacitor, respectively. The equivalent inductance of short antenna is 150nH.

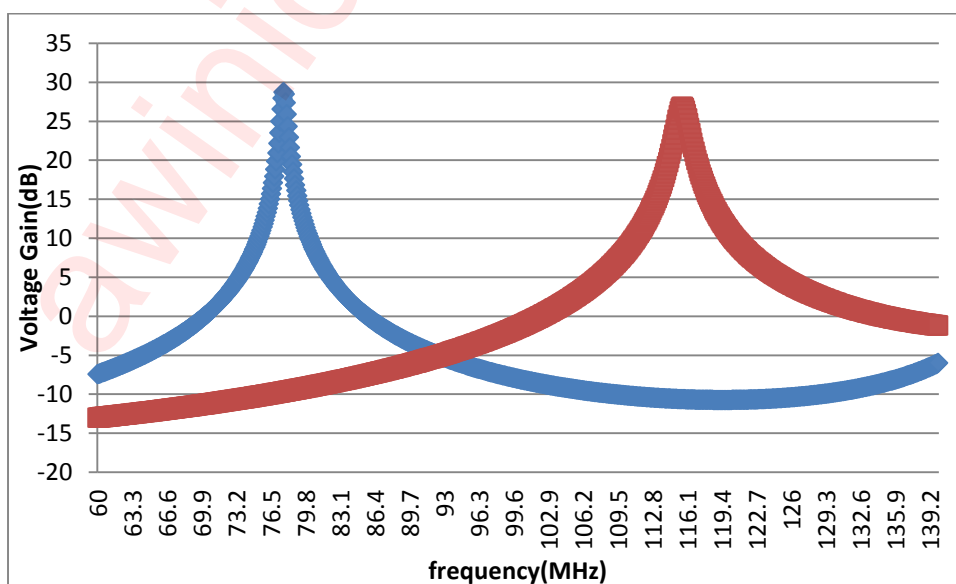


Figure 12 Voltage Gain with Different Tunable Capacitor

PACKAGE DESCRIPTION

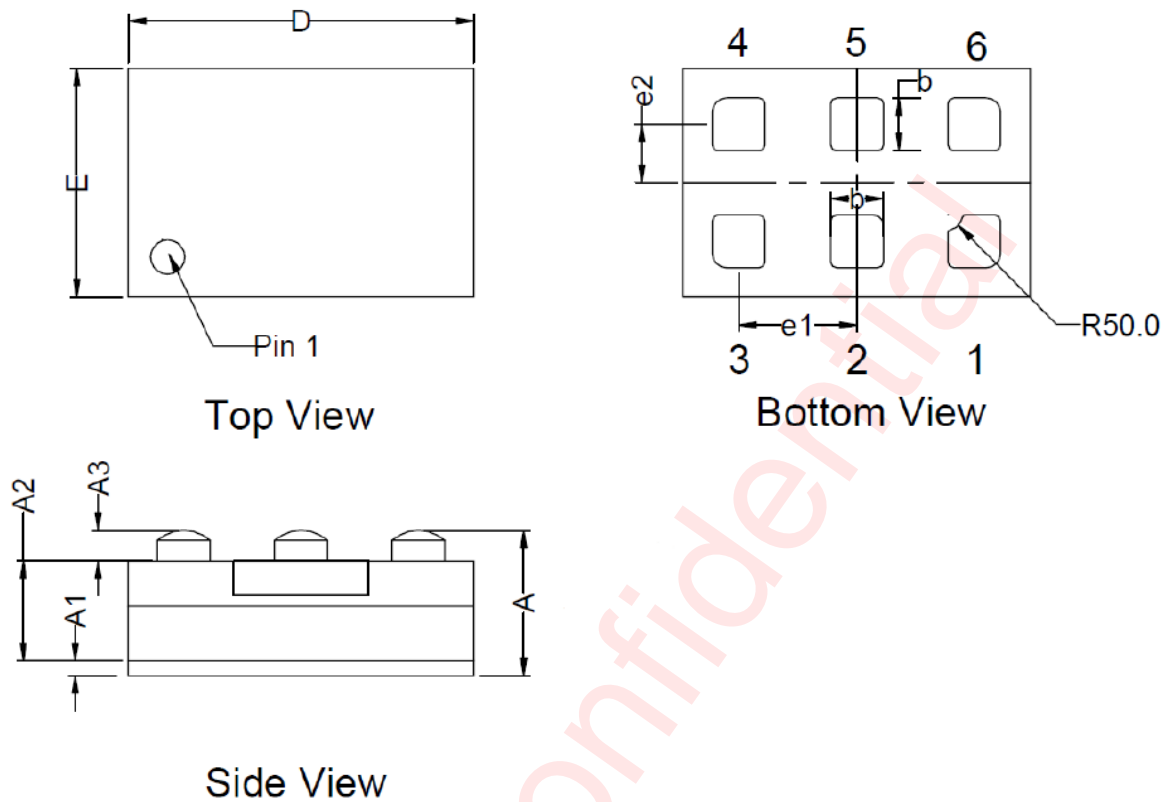


Figure 13 Package outline

AW5027 OUTLINE DIMENSIONS

Symbol	NOM	Tolerance
A	0.405	± 0.0215
A1	0.025	± 0.005
A2	0.360	± 0.0125
A3	0.020	± 0.004
D	1.100	± 0.025
E	0.700	± 0.025
b	0.180	± 0.010
e1	0.400	± 0.050
e2	0.200	± 0.050

All Dimensions are in Millimeters

LAND PATTERN DATA

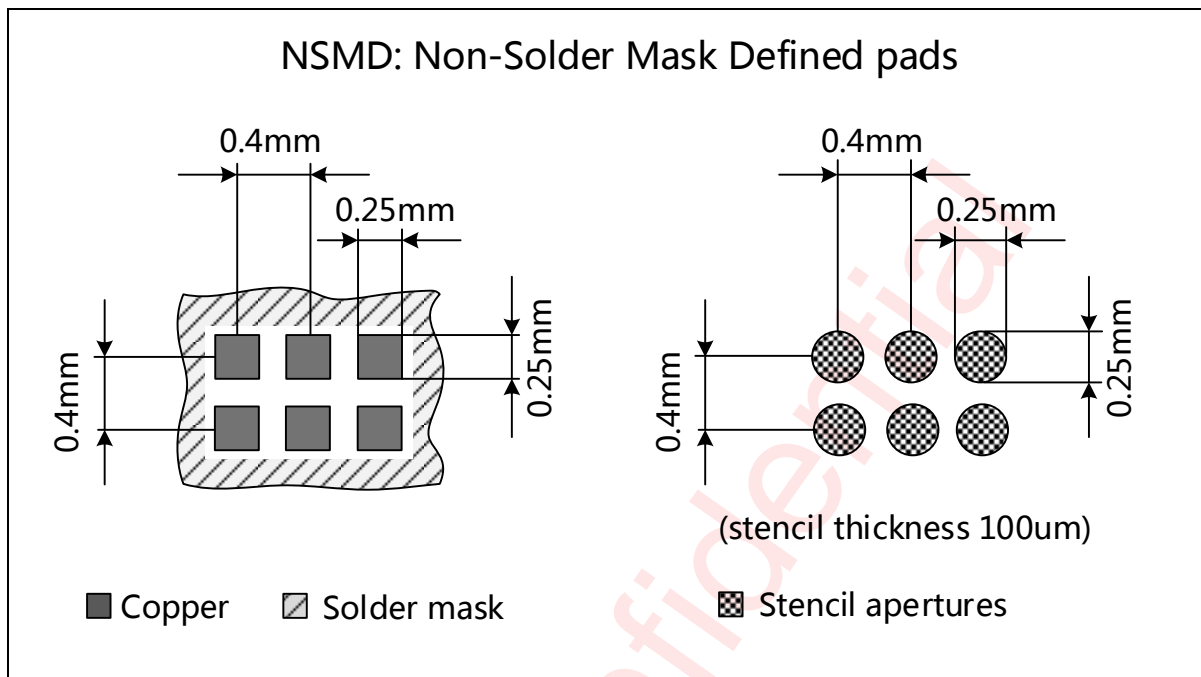
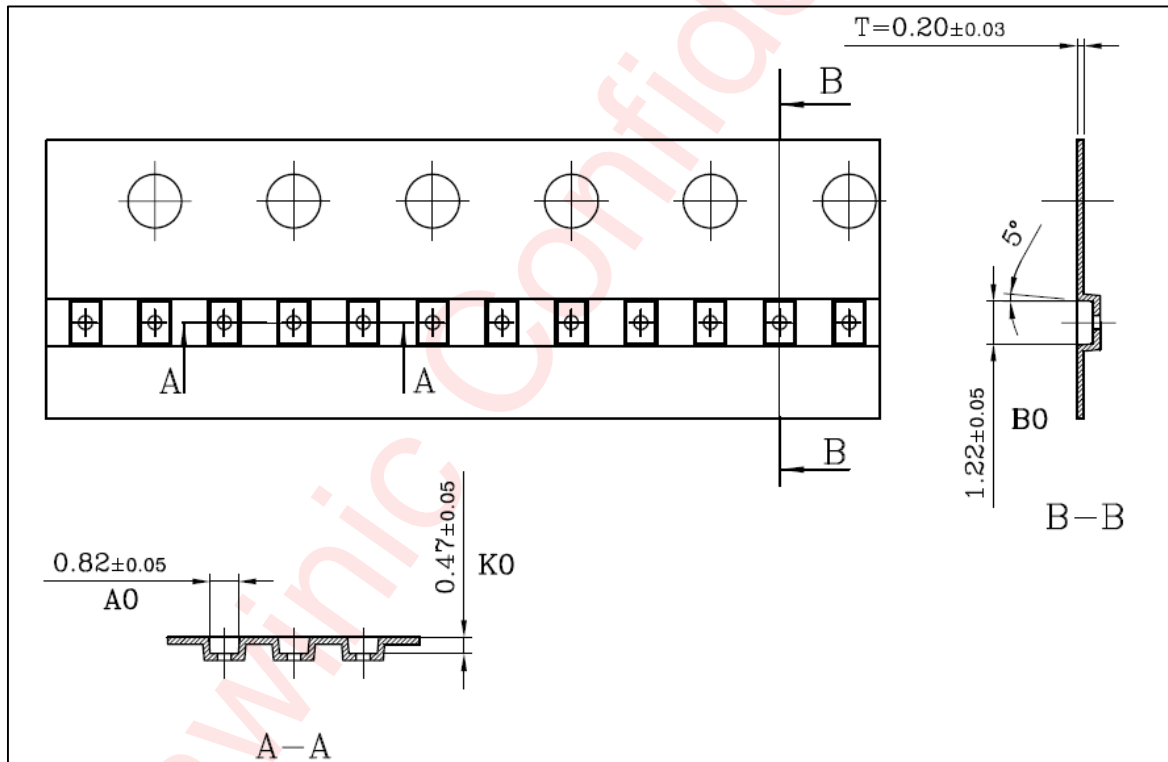
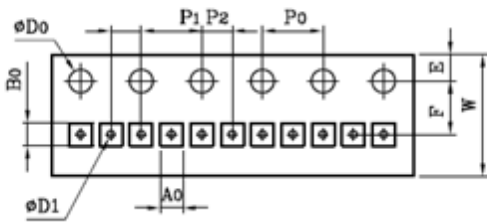


Figure 14 Land Pattern

TAPE DESCRIPTION

SPECIFICATION					(UNIT:mm)				
SPEC	W	P1	E	F	D0	D1	P0	P2	10P0
SIZE	8.00 ±0.30	2.00±0.10	1.75±0.1	3.5±0.05	1.5 ^{+0.10} ₀	0.40±0.05	4.00±0.10	2.00±0.05	40.0 ±0.2
SPEC	A0	A1	B0	B1	K0	K1	T		
SIZE	0.82±0.05		1.22±0.05		0.47±0.05		0.20±0.03		



Pin 1 direction

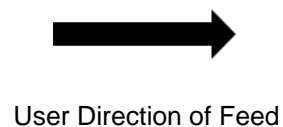
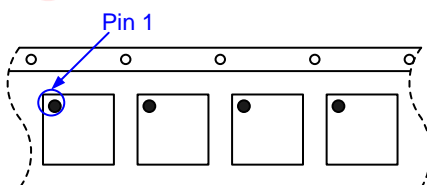
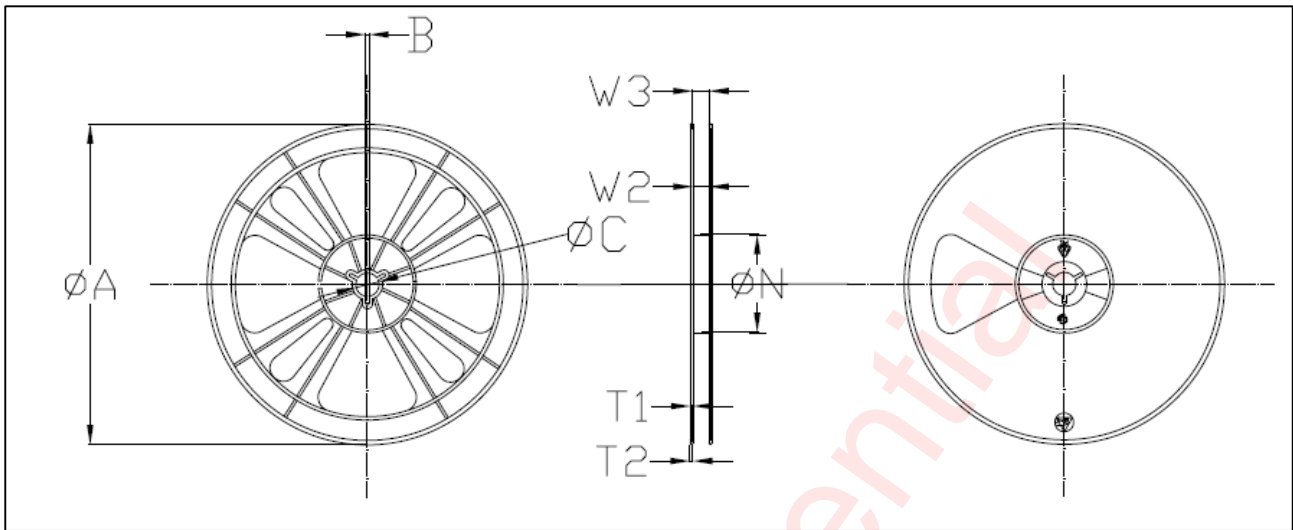


Figure 15 Tape Description

REEL DESCRIPTION



Note:

1. surface resistivity: 10^5 to 10^{11} ohm/sq.
2. Restriction criterion of hazardous substance for packing material follow GP-M001

Figure 16 Reel Description

Item	Value&Tolerance
A	179 ± 1.0
B	2.0 ± 0.1
C	13.5 ± 0.2
N	54.8 ± 0.2
W2	9.0 ± 0.2
W3	9.2 ± 1.0
T1	1.2 ± 0.2
T2	1.5 ± 0.2

All Dimensions are in Millimeters

REFLOW

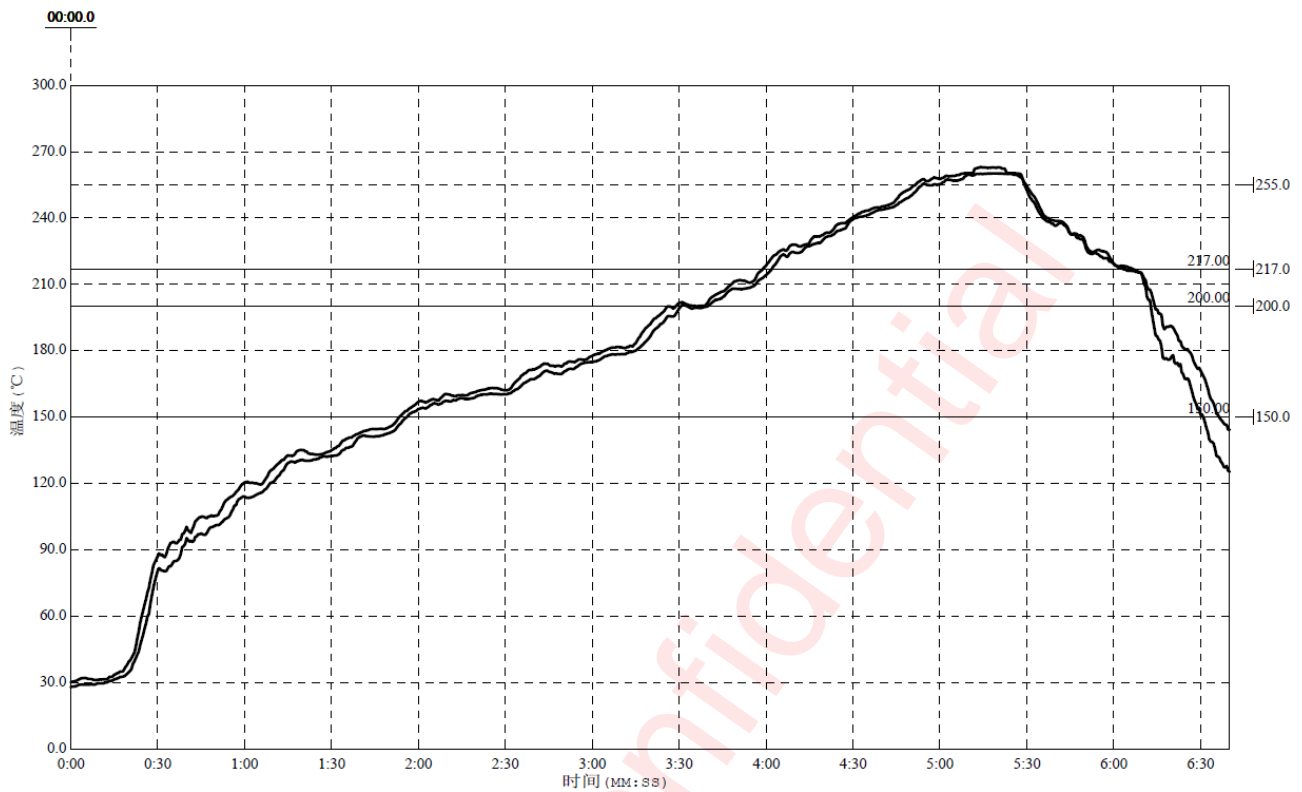


Figure 17 Package Reflow Oven Thermal Profile

Reflow Note	Spec
Average ramp-up rate (217°C to Peak)	Max. 3°C/sec
Time of Preheat temp.(from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec.
Ramp-down rate	Max. 6°C/sec
Time from 25°C to peak temp	Max. 8min.

NOTES

- All data are compared with the package-top temperature, measured on the package surface
- AW5027 adopted the Pb-Free assembly.

REVISION HISTORY

Document ID	Release date	Change notice	Supersedes
AW5027_V0.9	2016-09	Preliminary data sheet	-
AW5027_V1.0	2017-10	Update description in diagram	AW5027_V0.9
AW5027_V1.1	2018-02	Update MSL, Application Note Pi-network inductor number L2 and format	AW5027_V1.0
AW5027_V1.2	2018-08	Update Latch up info and package dimension unit	AW5027_V1.1

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