High Efficiency, 6-Channel WLED Driver

Features

- Wide Operating Input Voltage: 2.7V ~ 24V
- High Output Voltage: Up to 40V
- Channel Current Programmable: 5mA to 50mA
- Channel Current Regulation:
  - Accuracy ±2%
  - Matching ±1%
- PWM and/or I²C Control
- Dimming Controls
  - Direct PWM Dimming up to 25kHz with Minimum 1% Duty (400ns)
  - Up to 12-bit Resolution with 2kHz input PWM signal
  - Up to 11-bit Resolution with 4kHz input PWM signal
  - Up to 10-bit Resolution with 8kHz input PWM signal
  - Up to 12-bit Dimming Resolution with I²C Control Mode
- I²C Programs LED Current, Switching Frequency 300kHz to 1.7MHz
- Embedded Memory by MTP
- Protections
  - Input Undervoltage Lockout(UVLO)
  - LED Strings Open and Short Detection
  - Current Limit Protection
  - Over Voltage Protection
  - Over-Temperature Protection
- WBQFN 3.5mmX3.5mmX0.75mm-20L Package

Applications

Table and Notebook Backlight

Wearable Device

General Description

AW99706A is a highly accurate, highly matching six-string LCD backlighting power solution for notebook. It is a highly integrated step-up DC-DC converter operating with a wide input voltage for 2.7V to 24V and a temperature range from -40°C to 85°C.

AW99706A integrates a high voltage MOSFET and six high accuracy, high voltage current sinks. Each current sink can be regulated up to 50mA. The LED current can be adjusted via an I²C interface and/or through a PWM signal. The PWM dimming resolution is up to 12-bit.

AW99706A supports 300kHz to 1.7MHz switching frequency. Flexible selection of switching frequency according to efficiency and component size.

AW99706A provides 3 ramp control modes for smooth transform of backlight brightness. Soft start mode can only be chose during the process of turning on and off backlight. Fade in/out mode and slope mode can be chose during both turning on/off backlight and dimming transition.

Thorough protection features include over voltage limit, over temperature, over current protection, input undervoltage lockout, LED open and short detection. The protection status will be showed in register.

Typical Application Circuit

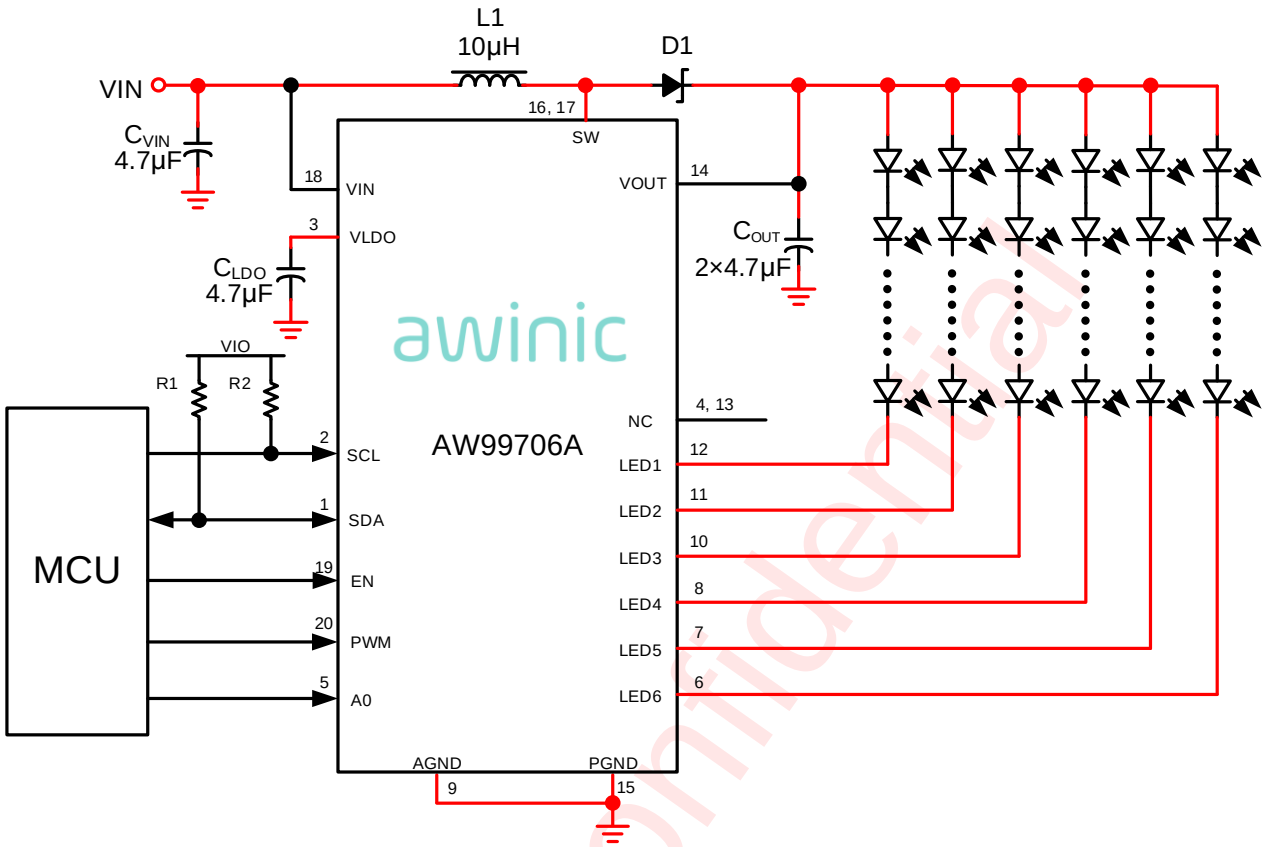
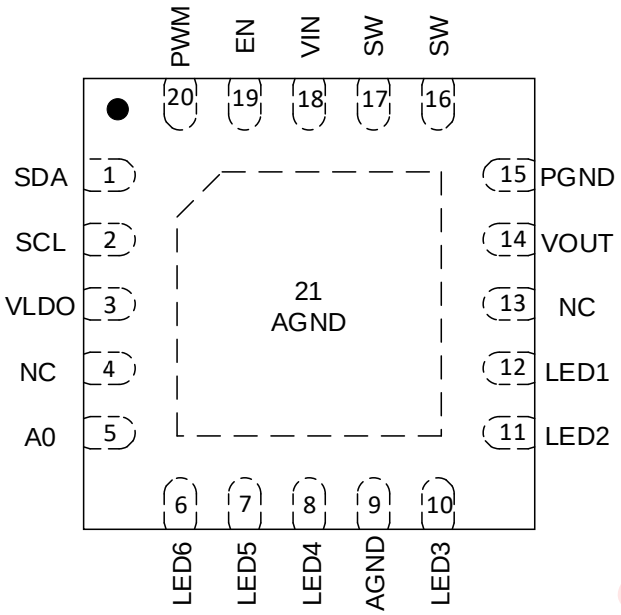


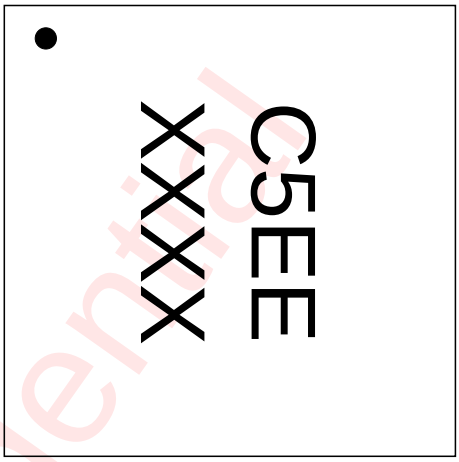
Figure 1 Typical Application Circuit of AW99706A

Pin Configuration And Top Mark

AW99706AQNR (Top View)



AW99706AQNR Marking (Top View)



C5EE – AW99706AQNR
XXXX – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	SDA	Serial data connection of the I²C interface.
2	SCL	Serial clock connection of the I²C interface.
3	VLDO	Output of internal regulator. Connect a capacitor between this pin and the ground reference.
4, 13	NC	No connect pin. Suggest floating or connecting to GND.
5	A0	Device Address Select (7bits), when A0 = 0, the device address is 0x76, when A0 = 1, the device address is 0x77.
6	LED6	Current sink for LED6.
7	LED5	Current sink for LED5.
8	LED4	Current sink for LED4.
9, 21 (Exposed Pad)	AGND	Analog Ground.
10	LED3	Current sink for LED3.
11	LED2	Current sink for LED2.
12	LED1	Current sink for LED1.
14	VOUT	Output of boost converter. The internal feedback and over voltage protection circuitry monitors the voltage on this pin.
15	PGND	Power ground.
16, 17	SW	Switch node of boost converter.
18	VIN	Power supply input.

19	EN	Enable control input .Logic high input to enable the device.
20	PWM	PWM dimming input. With an internal pull-down resister to GND.

Functional Block Diagram

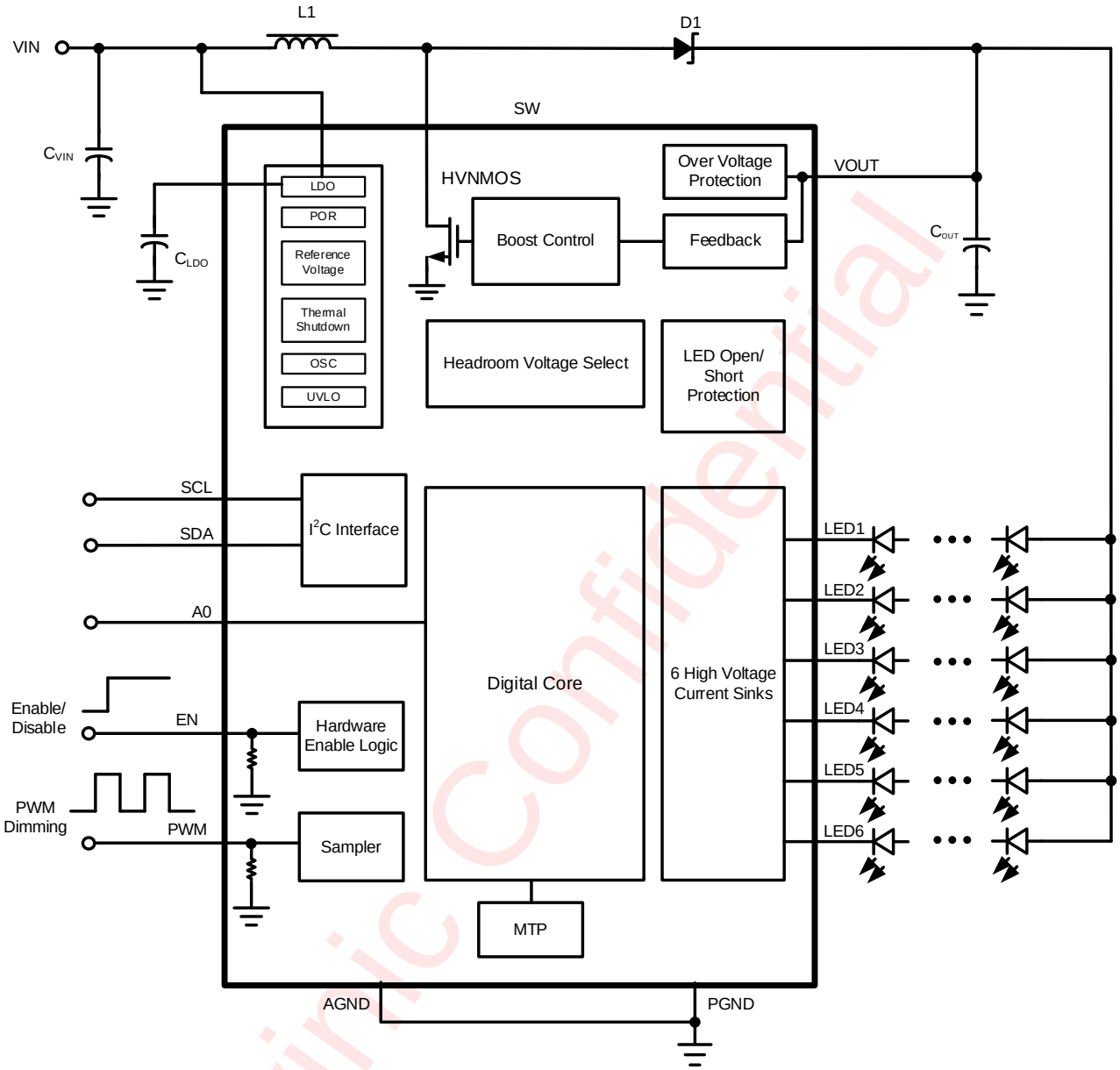


Figure 3 Functional Block Diagram

Typical Application Circuits

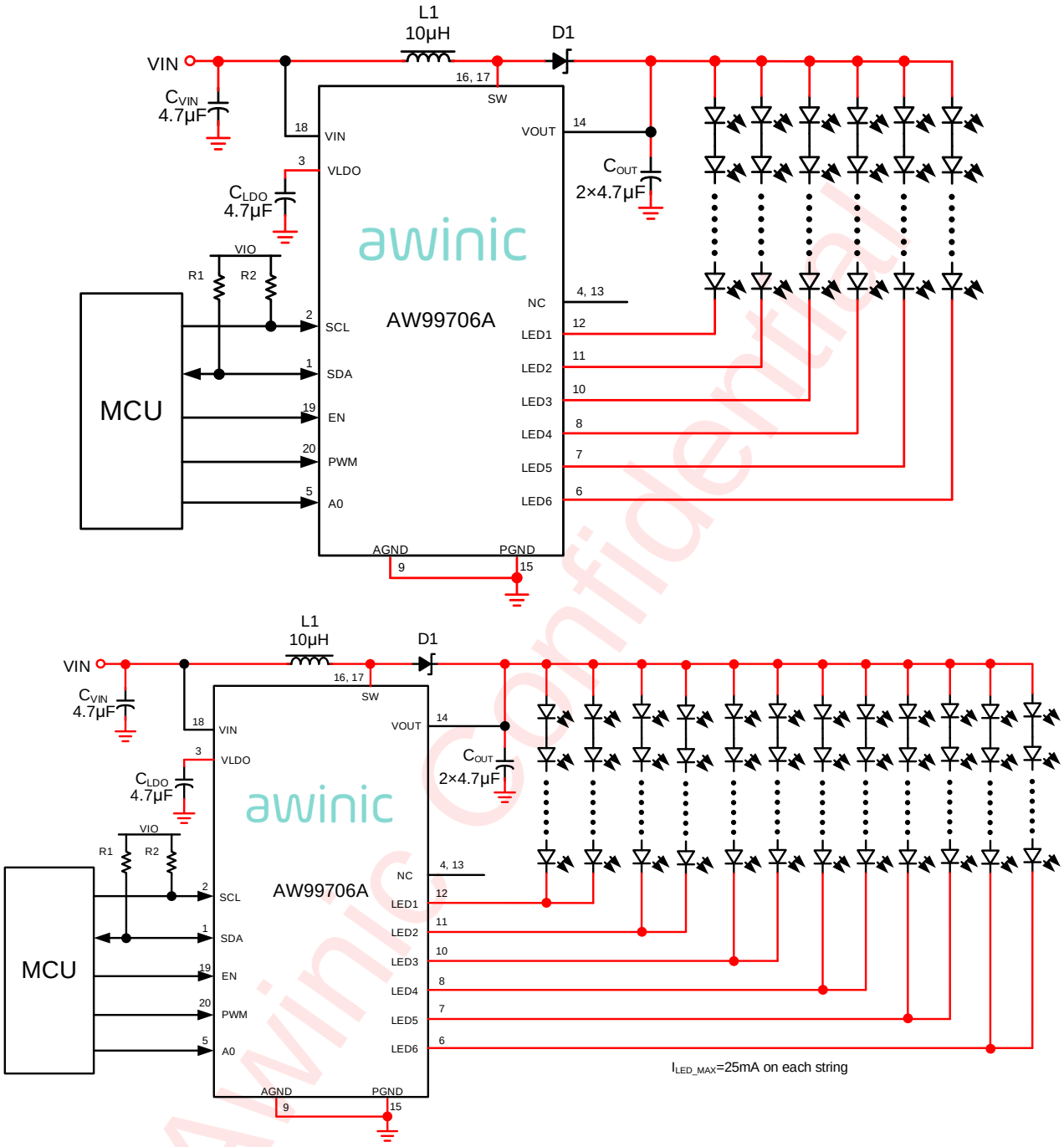


Figure 4 Typical Application Circuit of AW99706A

Notice for typical application circuits:

1：Please place C_{IN}, C_{LDO}, L1, D1 as close to the chip as possible.

2：C_{OUT} should be place as close to the Schottky diode

3：For the sake of driving capability, the power lines, output lines, and the connection lines of SW, C_{LDO}, and LED channel lines should be short and wide as possible. The power path marked in red as shown in the figures above, please traces according to 3A power line alignment rules, of which the proposed width is about 120mil. (outputs current of 300mA, route the path with width of 25mil)

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW99706AQNR	-40°C～85°C	WBQFN 3.5mmx3.5mmx 0.75mm-20L	C5EE	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Supply voltage range VIN(NOTE 1)	-0.3V to 26V
Voltage on PWM, EN (NOTE 1)	-0.3V to 26V
Voltage on VLDO,SDA, SCL, A0 (NOTE 1)	-0.3V to 6V
Voltage on SW, VOUT, LED1, LED2, LED3, LED4, LED5, LED6(NOTE 1)	-0.3V to 40V
Junction-to-ambient thermal resistance θ_{JA}	55.39°C/W
Operating free-air temperature range T_A	-40°C to 85°C
Operating Junction temperature T_J	-40°C to 150°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(Including CDM HBM)(NOTE 2)	
VBUS PIN HBM (Test condition: ESDA/JEDEC JS-001-2017)	±2kV
Other PINS HBM (Test condition: ESDA/JEDEC JS-001-2017)	±2kV
CDM (Test condition: ESDA/JEDEC JS-002-2018)	±1.5kV
Latch-Up	
Test condition: JEDEC78E	+IT：+200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	2.7	12	24	V
C_{VLDO}	LDO capacitance	1	4.7	10	μF
C_{IN}	Input capacitance	2.2	4.7	/	μF
C_{OUT}	Output capacitance	4.7	10	/	μF
L	Inductance		10		μH
T_A	Operating free-air temperature range	-40	25	85	°C

NOTE: The detailed recommended value of C_{IN}, C_{OUT} and L is shown in Application Information

Electrical Characteristics

Minimum and maximum limits apply over the operating ambient temperature, typical values are at T_A = 25°C, and VIN = 12V (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply						
V_{IN}	Input operating range		2.7		24	V
I_{SD}	Shutdown current	V_{IN}=24V, EN=L			2	μA
I_{STB}	Standby supply current	LDO enabled, boost disabled		0.7		mA
I_Q	Quiescent current	LDO enabled, boost enabled, no load		2.1		mA
UVLO	Input under voltage lockout	UVLOSEL=0		2.2		V
		UVLOSEL=1		5		V
$UVLO_{HYS}$	UVLO hysteresis			0.2		V
T_{OTP}	Over temperature protection threshold			150		°C
T_{OTP_HYS}	Over temperature protection threshold			20		°C
V_{LDO}	Internal LDO voltage	LDO_SEL=0		3.3		V
		LDO_SEL=1		5		V
Boost Converter						
F_{SW_ACC}	Switching frequency accuracy	Boost operates at PWM mode, f_{SW}=750kHz	-15		15	%
F_{SW_RG}	Switching frequency setting range	Boost operates at PWM mode	0.3		1.7	MHz
V_{BOOST_MIN}	Boost minimum output voltage range	VBT_MIN=0		7		V
		VBT_MIN=1		16		V
V_{BOOST_MAX}	Boost maximum output voltage range	VBT_MIN=0: VBT_MAX=000~010 VBT_MAX=011 VBT_MAX=100 VBT_MAX=101 VBT_MAX=110 VBT_MAX=111		 21 23 25 28 30 32.5		V
		VBT_MIN=1: VBT_MAX=000 VBT_MAX=001 VBT_MAX=010 VBT_MAX=011 VBT_MAX=100 VBT_MAX=101 VBT_MAX=110		 25 28 30 32.5 36 38 40		V
D_{MAX}	Maximum duty cycle	f_{SW}=300kHz		95		%
		f_{SW}=750kHz		93		
R_{DSON}	Boost switch R_{DSON}			150		mΩ

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LIM}	Switching current limitation setting	SW_ILMT=00		1.5		A
		SW_ILMT=01		2		A
		SW_ILMT=10		2.5		A
		SW_ILMT=11		3		A
T_{MIN_ON}	Boost minimum on time			50		ns
V_{OVP}(1)	Vout over voltage protection			V_{BOOST} +1.5		V
LED Current						
I_{LK_LEDx}	Leakage current of LEDx	V_{LEDx}=36V, I_{LEDx}=0mA			2	uA
I_{LED_MAX}	Maximum LED current setting		5	20	50	mA
I_{LED_ACC}	LED DC current accuracy	PWM Duty = 1-5%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-5		5	%
		PWM Duty = 5-15%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-4		4	%
		PWM Duty = 15-100%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-2		2	%
I_{LED_MAT}	LED DC current matching	PWM Duty = 1-5%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-5		5	%
		PWM Duty = 5-15%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-2		2	%
		PWM Duty = 15-100%, I_{LEDx} = 20mA, PWM Freq = 1kHz	-1		1	%
S_{res_2k}	DC dimming resolution with PWM input	PWM Freq<2kHz		4096		steps
S_{res_4k}		PWM Freq=2k to 4kHz		2048		steps
S_{res_8k}		PWM Freq=4k to 8kHz		1024		steps
S_{res_25k}		PWM Freq=8k to 25kHz		512		steps
T_{PWM_MIN}	PWM Minimum On Time	PWM Dimming Freq = 25kHz		400		ns
MTP Memory Characteristics						
Data Write Time	T_{WR}	Timing of write all configure into MTP		600		ms
Logic Interface(A0,EN,PWM,SCL,SDA)						
V_{IH}	High level input voltage		1.3			V
V_{IL}	Low level input voltage				0.4	V

(1) V_{BOOST} is set by the internal logic according to the real-time number of LEDs.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I²C Interface, see Figure 5						
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
F_{SCL}	Interface Clock frequency				400	kHz
T_{HD}: STA	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
T_{SU}: STA	(Repeat-start) Start condition setup time		0.6			μs
T_{HD}: DAT	Data hold time		0			μs
T_{SU}: DAT	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
T_{SU}:STO	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

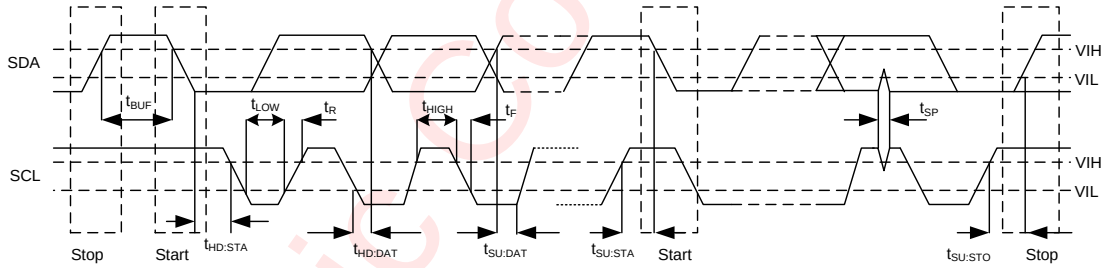
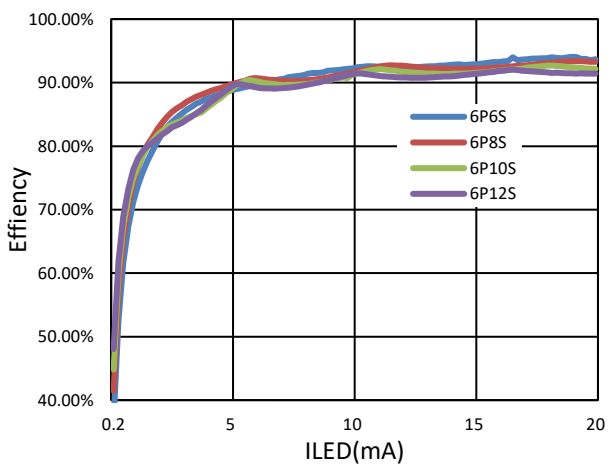


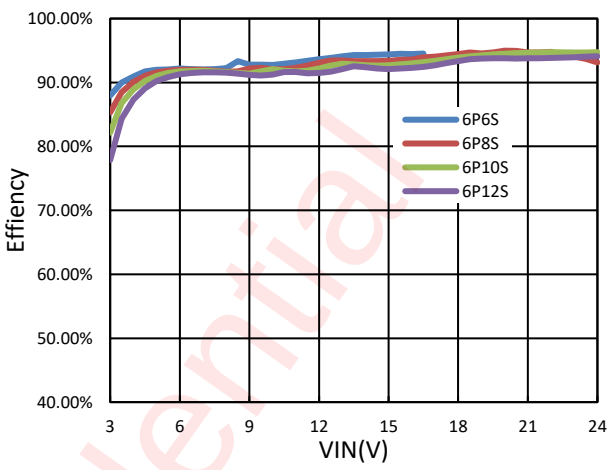
Figure 5 I²C Interface Timing

Typical Characteristics

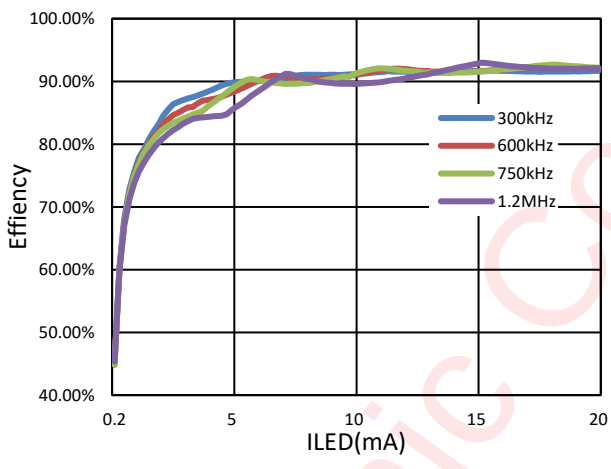
VIN=12V, T_A = 25°C, EN = 1.8V, C_{IN} = 4.7 μF, C_{OUT} = 2×4.7 μF and L=10μH, 6P10S, ILED = 20mA, unless otherwise noted .



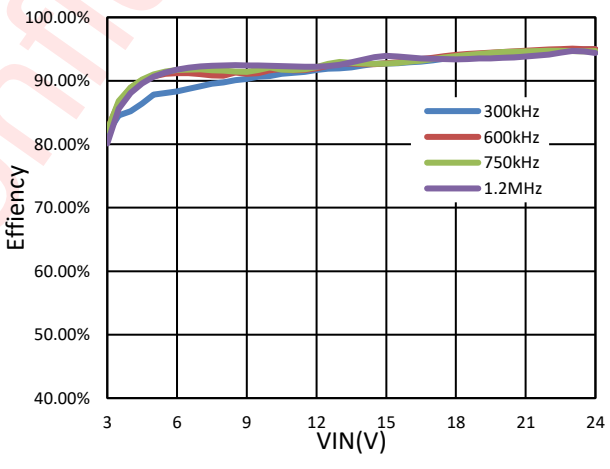
Boost Efficiency vs ILED in 6 Strings



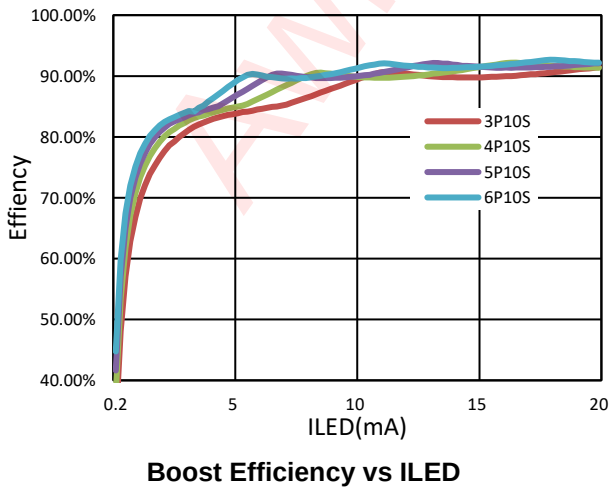
Boost Efficiency vs VIN in 6 Strings



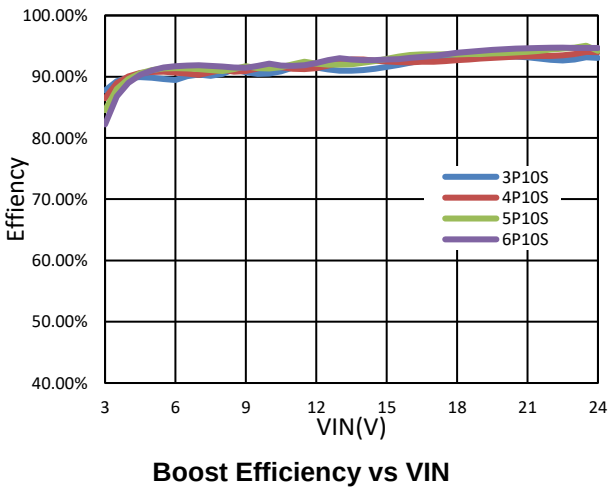
Boost Efficiency vs ILED in 6P10S



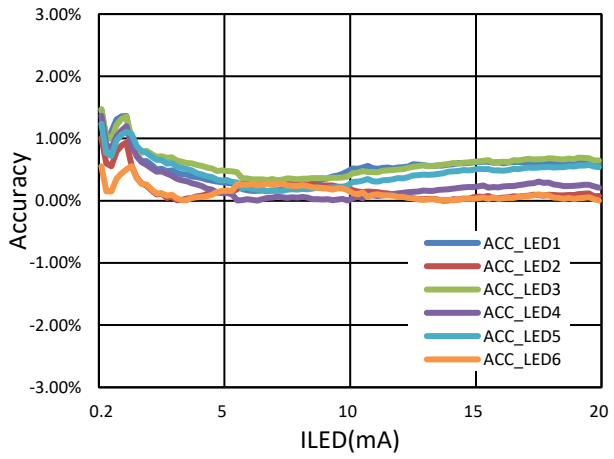
Boost Efficiency vs VIN in 6P10S



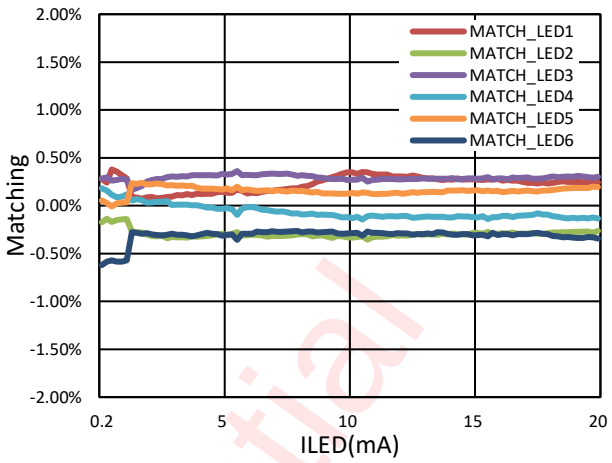
Boost Efficiency vs ILED



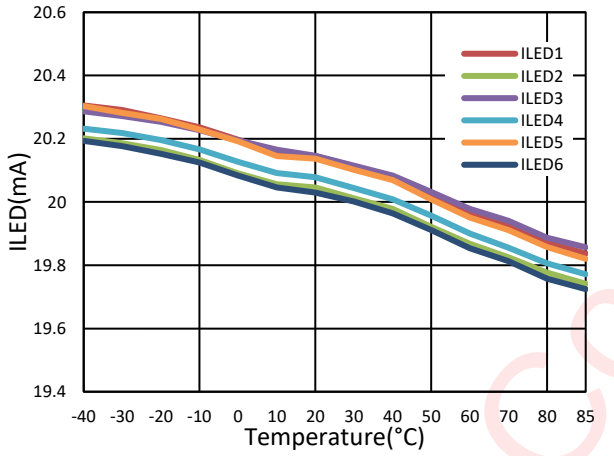
Boost Efficiency vs VIN



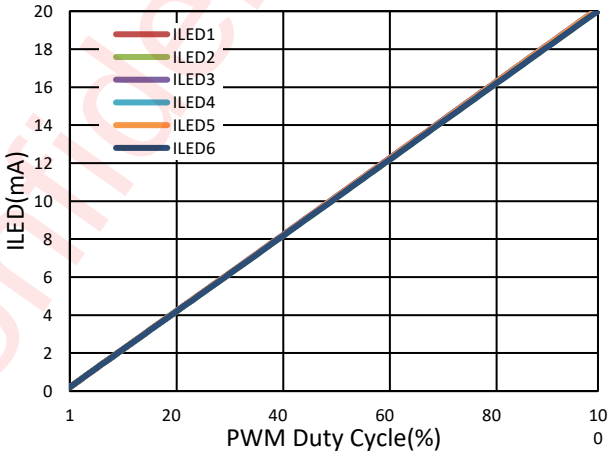
LED Current Accuracy in DC Mode



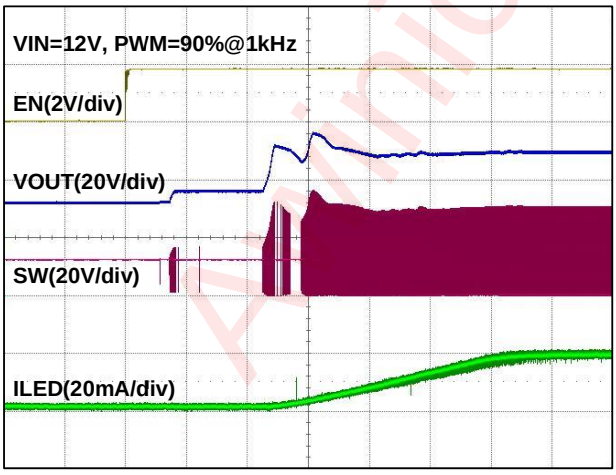
LED Current Matching in DC Mode



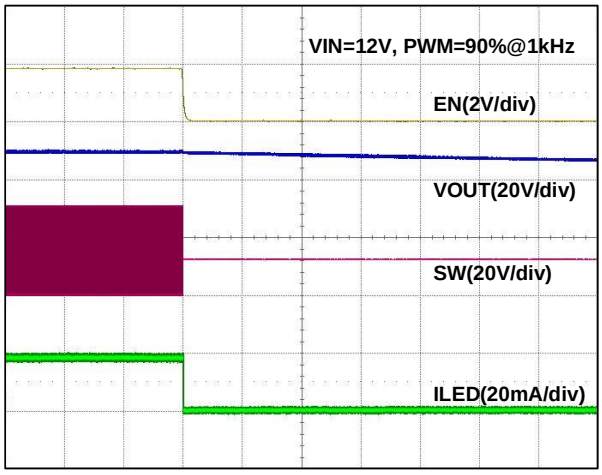
LED Current vs Temperature



LED Current vs PWM Duty Cycle



Start up Sequence



Shut Down

Detailed Functional Description

AW99706A is an inductive boost convert for WLED backlight display. AW99706A have six high-voltage LED channels with high current accuracy and high channel-to-channel matching. AW99706A can be controlled by I²C interface and PWM duty cycle.

The boost converter can adaptively adjust the output voltage to the optimal LED driver voltage up to 40V. This function reduces power consumption by adjusting the output voltage to the lowest under all conditions. The boost converter can operate at frequencies ranging from 300kHz to 1.7MHz through registers. Programmable SW edge rate can reduce switching noise and improve EMI performance.

The current sink of AW99706A has an up to 12-bit dimming resolution. AW99706A supports multiple current transition modes for smooth brightness transition. In addition, phase shift in LED PWM dimming can reduce audible noise and boost output capacitors.

AW99706A has full protection functions to ensure stable operation of device and external components. The device includes input under voltage lock-out, thermal shutdown, over current protection, adaptive over voltage protection, LED open and short circuit detection.

Timing Diagram

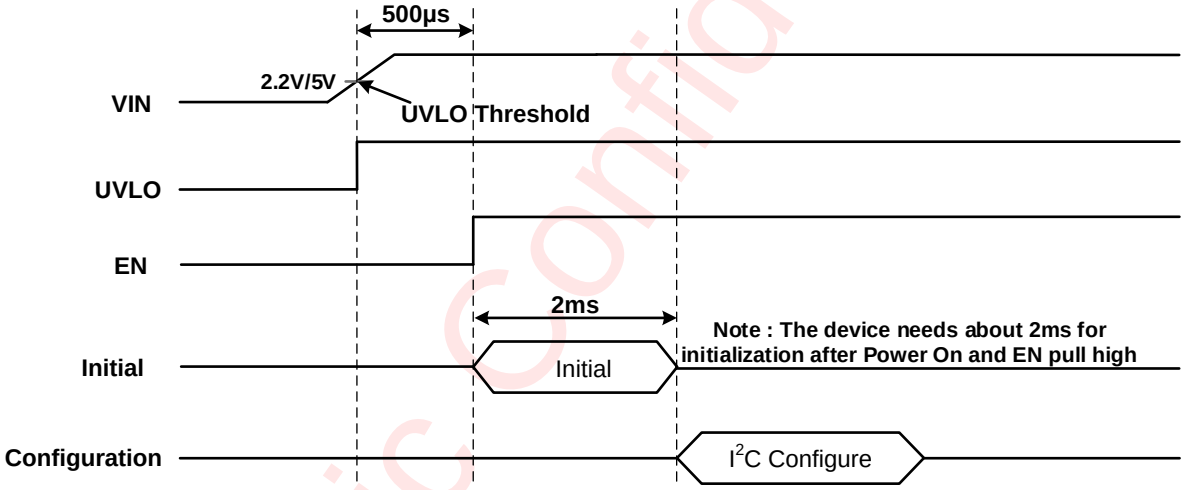


Figure 6 Power Up Timing

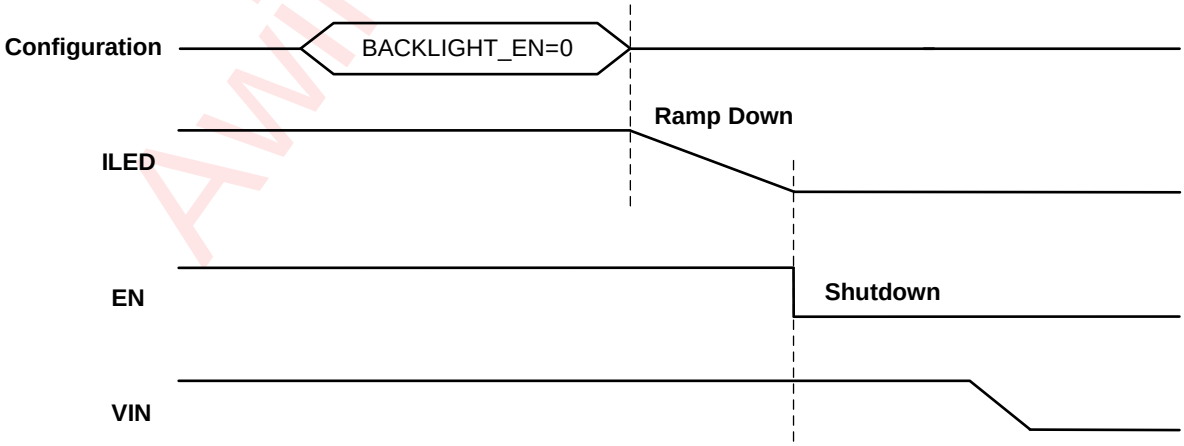


Figure 7 Power Down Timing

Hardware Enable & Standby Mode

When EN is pulled low, AW99706A enters Shutdown mode, all registers are reset to default state, and I²C

interface is disabled, the device will not respond to any I²C command.

When EN is pulled high, the device goes into Standby mode, and the device can respond to I²C command for at least $t_{start-up}$=2ms.

Both EN and I²C command can be used to turn off the LED current, but there are some differences:

If pulling EN low and write 1'b0 into BACKLIGHT_EN (CFG 0x0D), the LED current will be turned off immediately without any ramp.

If EN is keeping high, the LED current will ramp down with a fixed time by writing 1'b0 into BACKLIGHT_EN (CFG 0x0D), or writing 0 into BRT (CFG 0x04, 0x05) or pulling PWM low to turn off backlight.

Adaptive Output Voltage Control

Write 1'b1 into BACKLIGHT_EN (CFG 0x0D) to activate the boost converter, and AW99706A enters Active mode from Standby mode. The initial boost output voltage can be configured as 7V or 16V through VBT_MIN (CFG 0x0C).

AW99706A can adaptively adjust boost output voltage according to the number of LED strings. The range of adjustment is set by VBT_MIN and VBT_MAX (CFG 0x0C). The boost output voltage consists of the headroom voltage and the forward voltage of the LED string shown in Figure 8. The headroom voltage of AW99706A can be set through HR_OFFSET and DRV_HR (CFG 0x09).

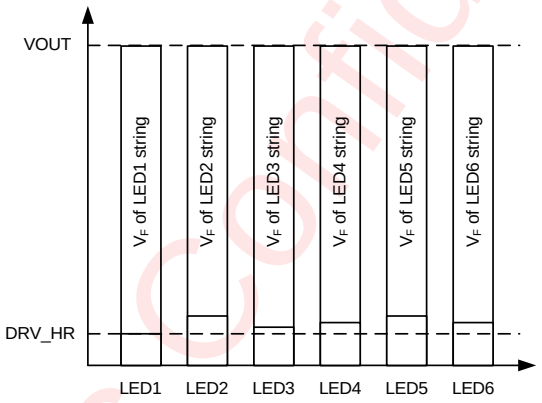


Figure 8 Adaptive VOUT Control Scheme

When turning on the backlight, AW99706A will adaptively adjust the boost output voltage to the most suitable value. AW99706A will continuously monitor the boost output voltage and headroom voltage. When all headroom voltages are above the set value, the converter will reduce the boost output voltage to reduce power consumption. When the headroom voltage is lower than the set value, the converter will increase the boost output voltage to ensure that all headroom voltages meet the set value.

Adjustable Switching Frequency

The boost switching frequency of AW99706A can be set by SW_FREQ (CFG 0x01) from 300kHz to 1.7MHz, up to 12 switching frequencies are available for selection. Higher switching frequency can bring lower output voltage ripple, and lower switching frequency can improve boost efficiency.

EMI Reduction

Programmable Slew Rate Control uses a combinational drivers for boost switch. Enabling all drivers allows boost switch on/off transition time to be the shortest, enabling just one driver allows boost switch on/off transition time to be the longest. The longer the transition time, the lower the switching noise on the SW pin. Note that the shortest transition time brings the best efficiency as the switching losses are the lowest.

Figure 9 shows the EMI programmable steps, and the Programmable Slew Rate Control operates at the SW_EDGE_RATE (CFG 0x00).

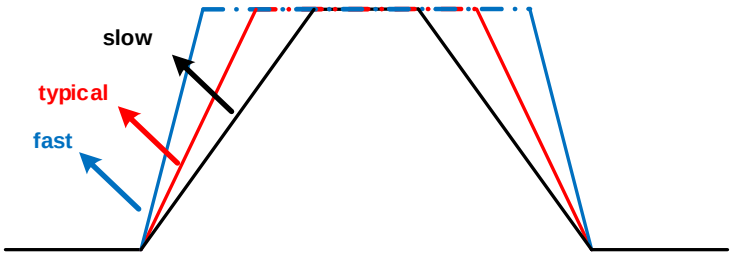


Figure 9 EMI Reduction Operation

Brightness Control

By setting BRT_MODE (CFG 0x07) shown in Table 1, AW99706A support 4 methods to control backlight brightness. The brightness can be set by the registers via I²C interface and input PWM signal. AW99706A also supports that the brightness is controlled directly by input PWM signal.

Table 1 Brightness Control Mode Selection

BRT_MODE	Brightness Control Mode
2'b00	PWM
2'b01	I²C
2'b10	PWM×I²C
2'b11	PWM×I²C (PRAMP)

PWM Mode

Writing 2'b00 into BRT_MODE (CFG 0x07) allows AW99706A to enter PWM mode, in which the brightness of the backlight is only determined by the duty cycle of the input PWM signal. The PWM sampling module will encode the PWM duty cycle to brightness code according to the PWM sampling rate set in PWM_SRATE (CFG 0x07) after detecting the input PWM signal. The AW99706A supports a high sampling accuracy that can encode the duty cycle of the PWM signal to an up to 12-bit brightness code. The minimum on time of PWM input signal that AW99706A can support is 400ns. The flow chart of PWM mode is shown in Figure 10.

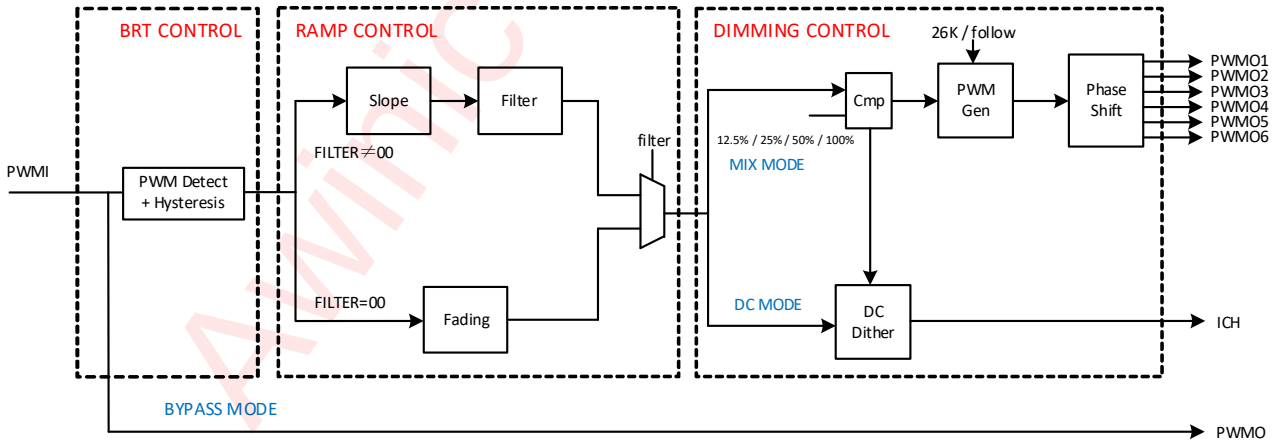


Figure 10 PWM Mode Scheme

AW99706A provides PWM code hysteresis function to eliminate the duty jitter of PWM signals. During the continuous upward adjustment process of backlight brightness, PWM code hysteresis can make the downward adjustment of low *n*-bit brightness code ineffective. Similarly, during the continuous downward adjustment process of backlight brightness, PWM code hysteresis can make the downward adjustment of low *n*-bit brightness code ineffective. Parameter *n* can be set in PWM_CODE_HYS (CFG 0x0B).

AW99706A also provides PWM polarity function. Writing 1'b1 into PWM_PO (CFG 0x00) enables PWM polarity, and AW99706A will encode the low level of PWM signal as brightness code.

I²C Mode

Writing 2'b01 into BRT_MODE allows AW99706A to enter I²C mode. In I²C mode, the backlight brightness code can be directly written to the register via I²C interface. Backlight brightness with a resolution of up to 12bit is set by BRT_MSB (CFG 0x04) and BRT_LSB (CFG 0x05). AW99706A supports 8~12-bit brightness adjustment set by BRT_WIDTH (CFG 0x03). When *BRT_WIDTH = 8-bit*, the brightness written to BRT_MSB will not be effective. When *BRT_WIDTH > 8-bit*, continuously write BRT_MSB and BRT_LSB to set the backlight brightness, and take effect after writing BRT_LSB. The flow chart of I²C mode is shown in Figure 11.

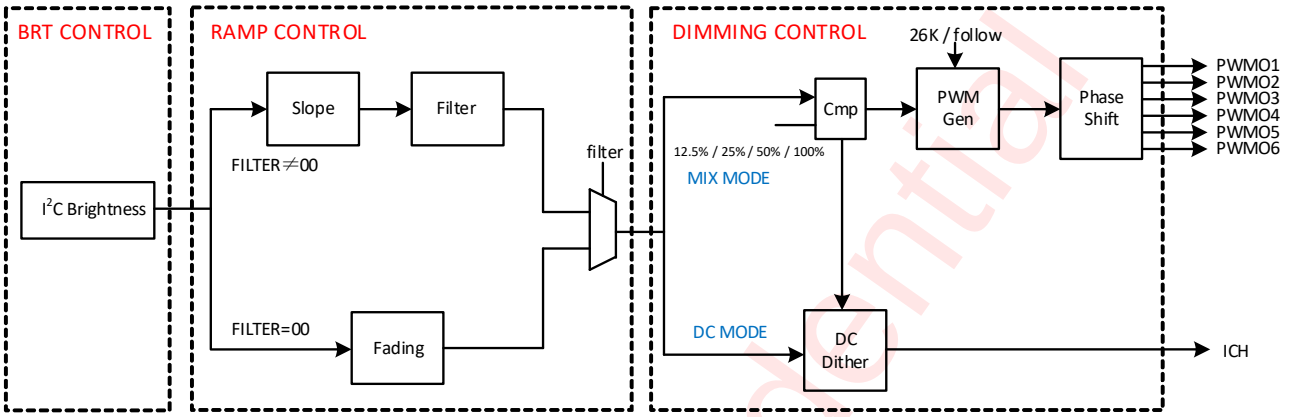


Figure 11 I²C Mode Scheme

I²C×PWM Mode

Writing 2'b10 in BRT_MODE allows AW99706A to enter I²C×PWM mode. In this mode, the backlight brightness code is calculated by:

$$BRT_{BL} = BRT_{REG} \times BRT_{PWM}$$

Where BRT_{BL} is backlight brightness, BRT_{REG} is the value writing into registers via I²C interface, and BRT_{PWM} is the brightness code encoding by input PWM signal duty cycle. Modifying both the duty of input PWM signal and the value in the registers can change the backlight brightness. And the backlight brightness conversion time will comply with the RAMP setting in the registers. The flow chart of I²C×PWM mode is shown in Figure 12.

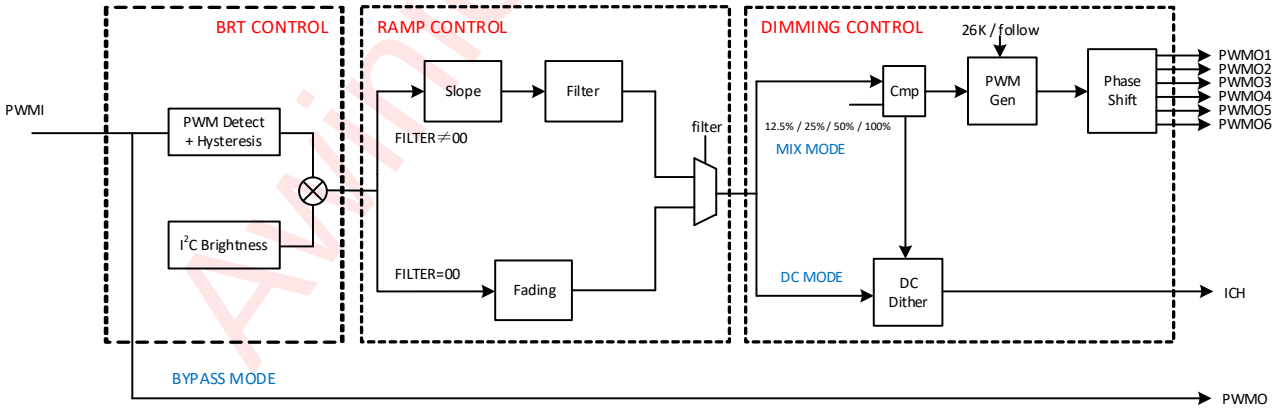


Figure 12 I²C×PWM Mode Scheme

I²C×PWM (P-ramp) Mode

Writing 2'b10 in BRT_MODE allows AW99706A to enter I²C×PWM (P-ramp) mode. In this mode, the calculation of brightness code is the same as the I²C×PWM mode. Differently, only modifying the value in registers by I²C interface will make the backlight brightness transition follow the time setting in the registers in ***RAMP CONTROL***. When modifying the PWM duty, the backlight brightness transition time is 1/4 of FADE

in/out mode. The flow chart of I²C×PWM (PRAMP) mode is shown in Figure 13.

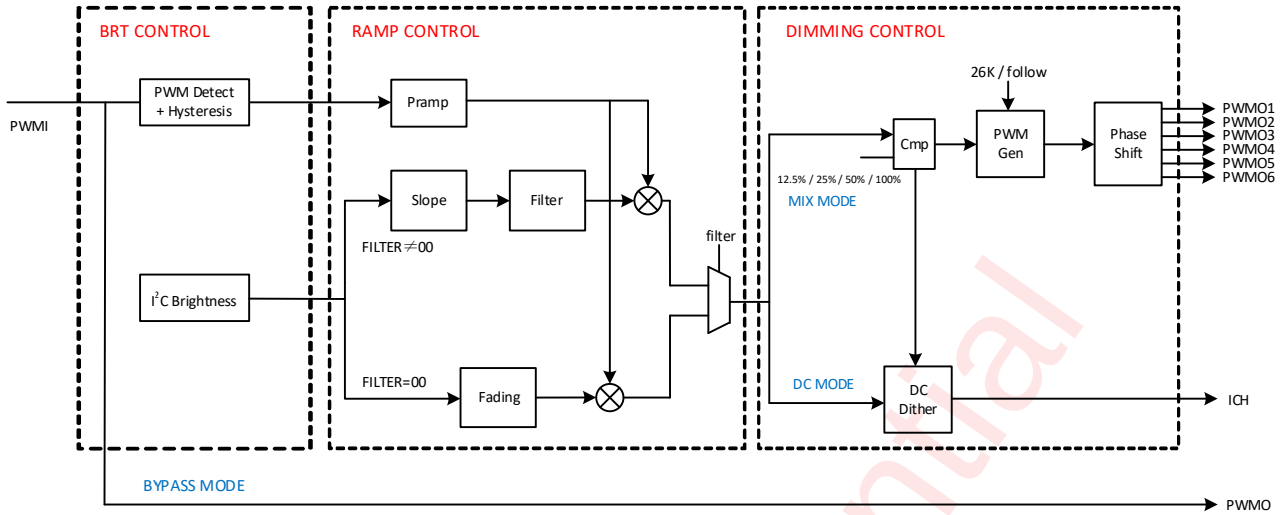


Figure 13 I²C×PWM (PRAMP) Mode Scheme

Dimming Mode

There are 6 output channels on AW99706A, each of which can be individually controlled to enable or disable through LEDx_EN (CFG 0x0D). AW99706A will generate a 12-bit dimming code by internal logic according to the brightness code, ramp control, dimming modes and functions. The dimming code and maximum current decide the actual current on each output channel.

The maximum current is set by ILED_MAX (CFG 0x02), and can be calculated by:

$$I_{LED\_MAX} = 5 + 0.5 \times code_{ILED\_MAX} \quad (code_{ILED_{MAX}} = 0\sim90)$$

The minimum value is 5mA and the maximum value is 50mA. When the value written to ILED_MAX is greater than 0x5A, the maximum current will be kept at 50mA.

AW99706A supports 4 dimming modes: bypass mode, DC mode, MIX mode and MIX-26k mode. The dimming mode can be configured by DIM_MODE(CFG 0x00):

Table 3 Dimming Mode Selection

DIM_MODE	Dimming Mode
2'b00	Bypass
2'b01	DC
2'b10	MIX
2'b11	MIX-26k

Bypass Mode

In bypass mode, all LED current waves will follow the input PWM signal. AW99706A operates in ON/OFF dimming mode. The maximum LED current is set in ILED_MAX (CFG 0x02). The frequency and duty cycle of the LED current are the same as the input PWM signal. The dimming curve wave of bypass mode is shown in Figure 14.

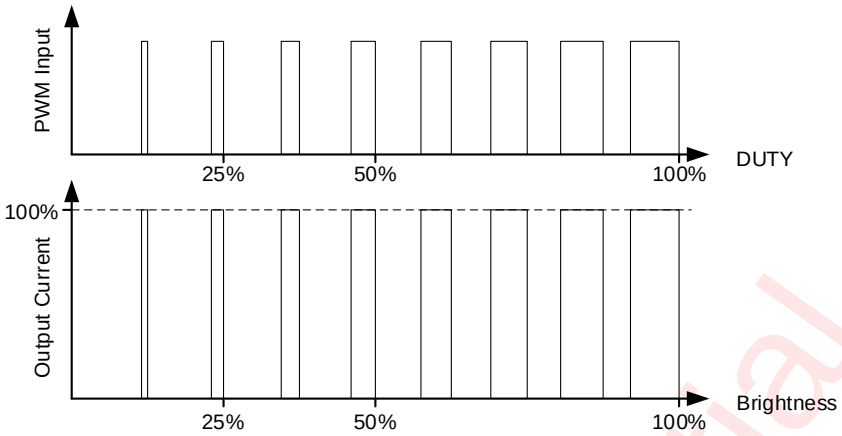


Figure 14 LED current in Bypass Mode

DC Mode

In DC mode, AW99706A outputs DC current. The LED current is determined by the registers or the input PWM duty. The maximum current is set by ILED_MAX (CFG 0x02). The dimming curve of DC mode is shown in Figure 15.

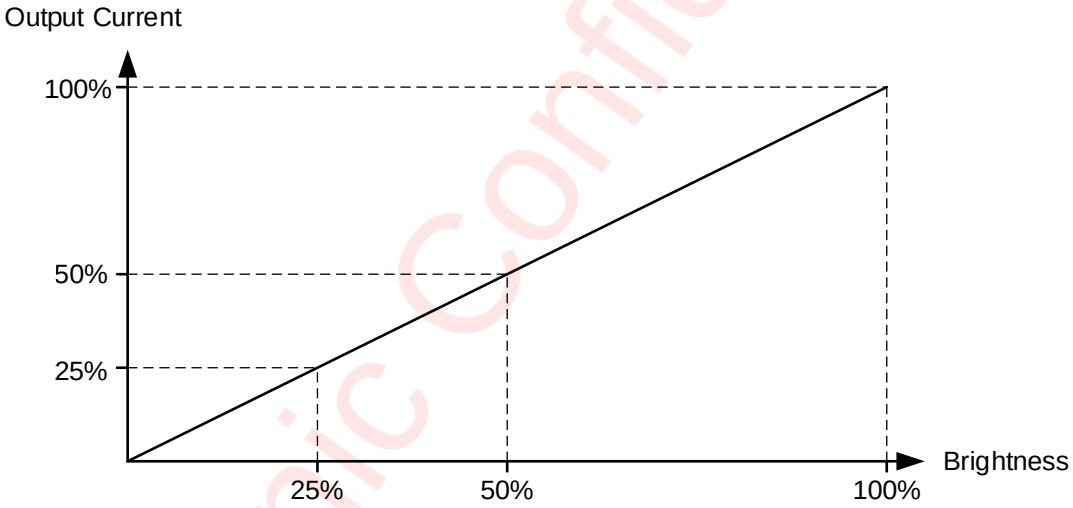


Figure 15 LED current in DC Mode

MIX Mode

AW99706A supports MIX mode, which combines the advantages of PWM dimming and DC dimming. Output current in MIX mode is PWM at low brightness and DC at high brightness. PWM dimming provides higher linearity and accuracy at low brightness, and DC dimming provides higher efficiency at high brightness. The dimming curve of MIX mode is shown in Figure 16.

Switching point between PWM mode and DC mode is set by PWM_TO_DC_THRESHOLD (CFG 0x00). There are 2 switching points can be chosen in 12.5% and 25%. The high level of PWM output current is controlled by the maximum current and the switching point: ILED_MAX×PWM_TO_DC_THRESHOLD.

If there is PWM in the brightness control, the frequency of the PWM output current follows the input signal. When the brightness is controlled by only I^2C, the frequency of the PWM output current is determined by ILED_FREQ (CFG 0x08).

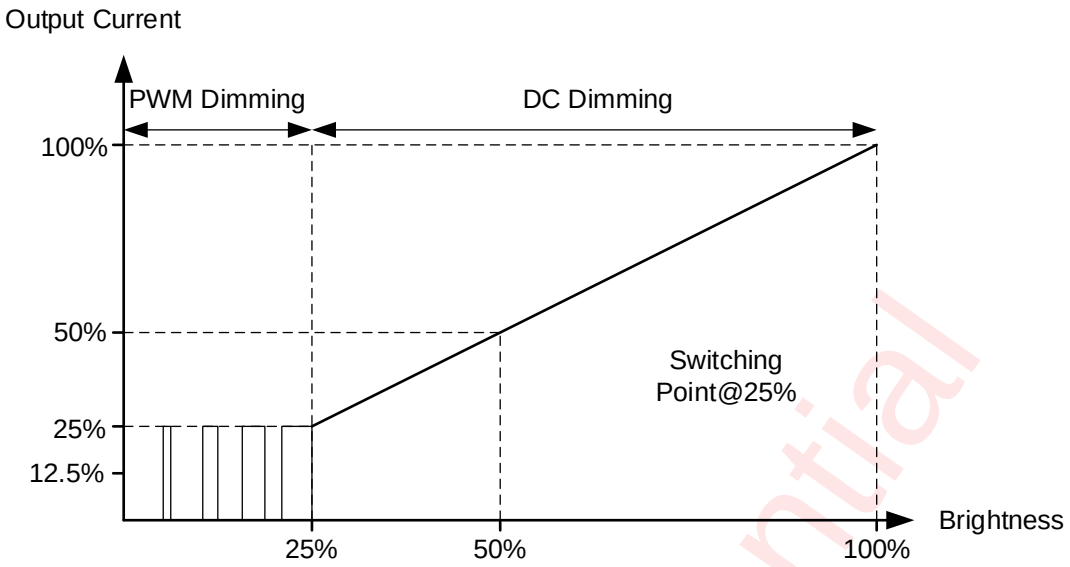


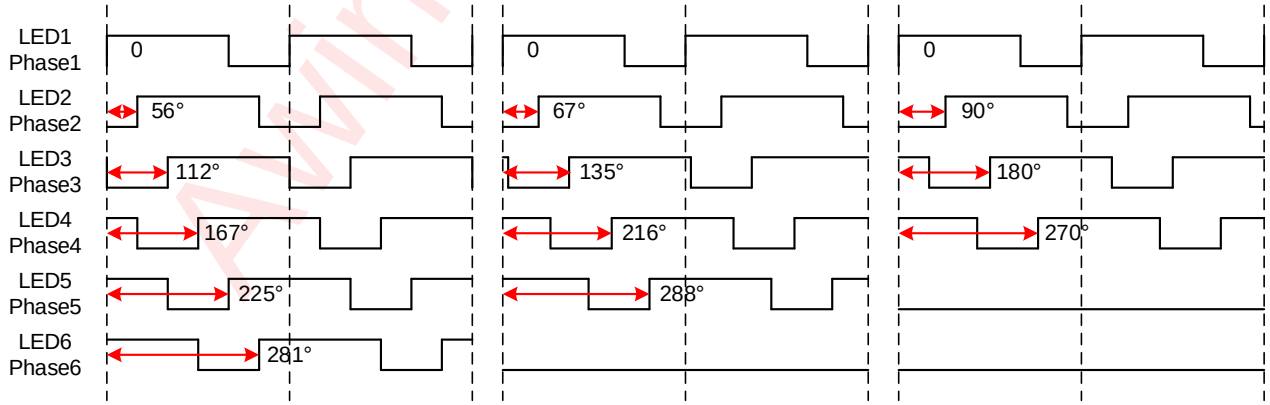
Figure 16 LED current in MIX Mode

MIX-26k Mode

The MIX-26k mode of AW99706A is similar to the MIX mode, but the frequency of the PWM output current is only determined by the ILED_FREQ (CFG 0x08). Lower frequencies can provide higher current accuracy at ultra-low brightness, but may cause audio noise.

Phase Shift

To reduce the peak load current and ceramic-capacitor audible ringing, AW99706A supports 8 PWM phase shift modes. When setting PS_EN (CFG 0x0B) to “1’b1”, the phase shifting scheme is enabled. Phase shift mode is set by PS_MODE (CFG 0x0B). The degrees of phase shift and open channels can be set in phase shift mode. For example, ‘6-phase, 6 drivers’ means that all 6 LED channels are open and none of the 6 channels will open synchronously. ‘3-phase, 3 drivers’ means that only LED1~3 will be open and these LED channels will work in 3 different phases. ‘2-phase, 6 drivers’ means than all LED channels are open, LED1~3 work synchronously and LED4~6 work synchronously in another phase. The current wave of phase shift is shown in Figure 17.



(a) 6-phase, 6 drivers (b) 5-phase, 5 drivers (c) 4-phase, 4 drivers

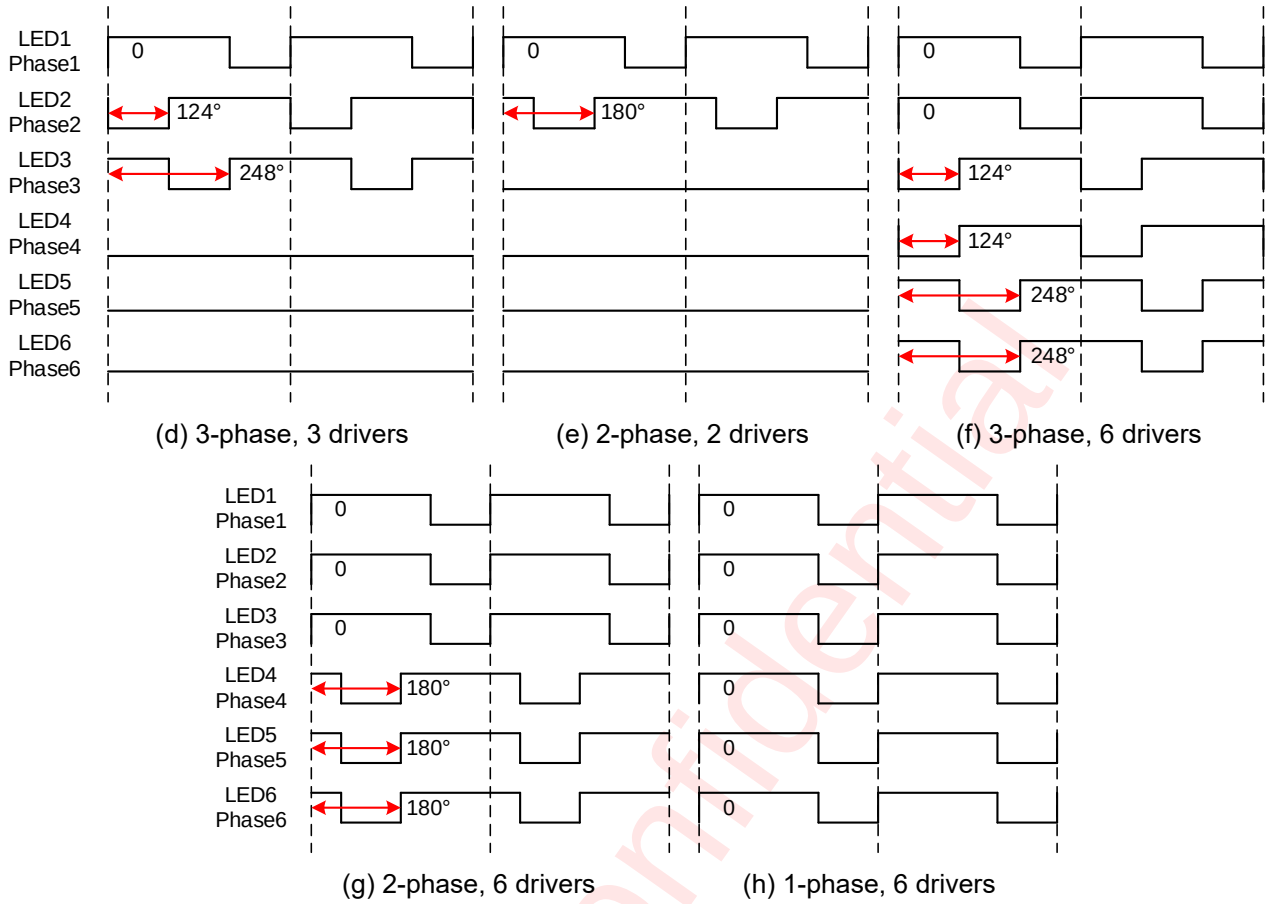


Figure 17 Phase Shift Scheme

Dithering

AW99706A supports an up to 3-bit dithering function to raise dimming accuracy in MIX mode or MIX-26k mode. Dithering can raise dimming accuracy when the dimming resolution is lower than input brightness resolution. Write “0” in DITHER_MODE (CFG 0x0A) enable dithering only during brightness transitions. Write “1” in DITHER_MODE at all times. By modify the value in DITHER (CFG 0x0A) can set dithering level. The highest resolution that dither can raise to is 12-bit. The example of 2-bit dithering with 11-bit input brightness resolution and 9-bit dimming resolution is shown in Figure 18.

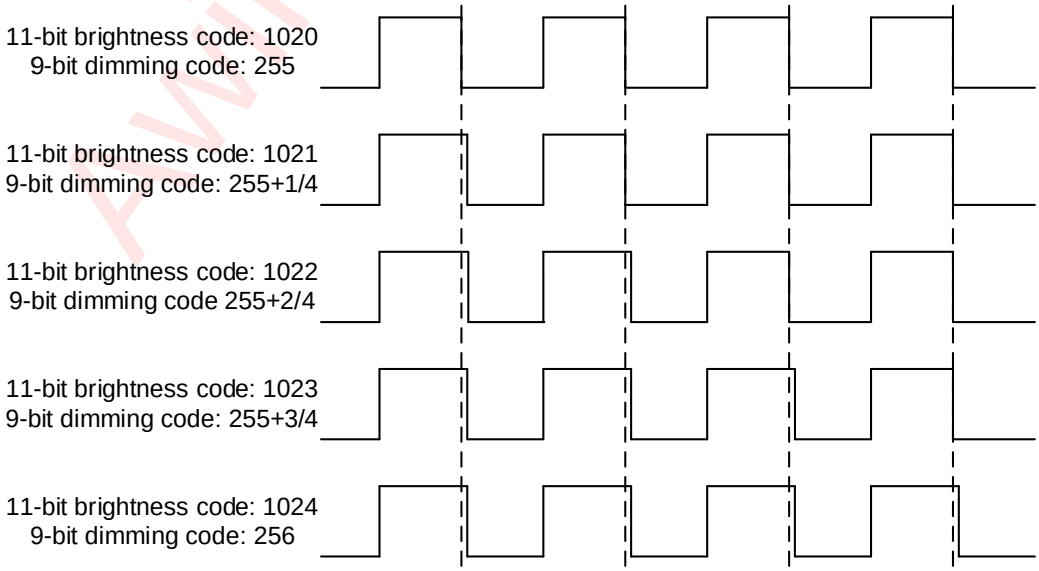


Figure 18 2-bit Dither with 11-bit Brightness Resolution and 9-bit Dimming Resolution

Ramp Control

AW99706A provides 3 ramp control modes for smooth transform of backlight brightness. It can be set by ONOFF_CTR (CFG 0x08) and RAMP_CTR (CFG 0x06). Turning on/off ramp is set by ONOFF_CTR, and dimming transition ramp is set by RAMP_CTR.

Soft Start

If the value in ONOFF_CTR is 2'b00, the turning on/off ramp of AW99706A is soft start and fast end. In this mode, the ramp time can be programmed by ONOFF_TIME (CFG 0x08). If the LED current is changed from zero to any other by I²C brightness code or PWM duty cycle, the current ramp time will follow the value of the ONOFF_TIME (CFG 0x08) programmed.

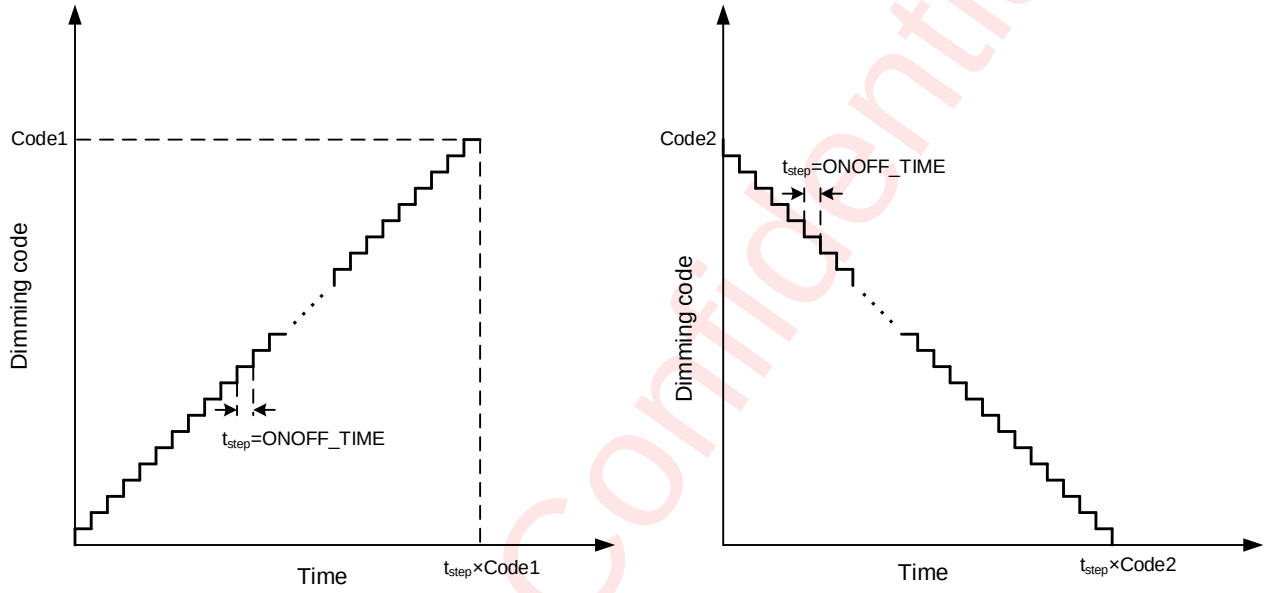


Figure 19 LED current ramp in soft start and soft end mode

As is shown in Figure 19, the slope of current ramp time t_{step} is set by ONOFF_TIME, the total current ramp time is

$$T_{tot\_on} = Code \times t_{step}$$

The 12-bit dimming code is calculated by the set current:

$$Code = \frac{I_{LED}}{I_{LED\_MAX}} \times 4096$$

where I_{LED} is the current set by I²C brightness code or PWM duty cycle, I_{LED_MAX} is the current set in ILED_MAX. The fast end means that the LED current will turn off immediately when turning off the backlight.

If the value in ONOFF_CTR is 2'b01, AW99706A enters soft start/end mode. The step time of turning on and turning off can be programmed by ONOFF_TIME.

If the value in ONOFF_CTR is 2'b1x, the turning on/off ramp mode can be set as Fade in/out mode or Slope mode.

Fade in/out Mode

AW99706A provides Fade in/out mode to transform backlight from one brightness to another or turn on/off backlight with a fixed slope. Writing 2'b00 into RAMP_CTR (CFG 0x06) to enter Fade in/out mode, and the sloe of current transition can be set in FADE_TIME (CFG 0x06). In this mode, the total ramp time of LED current transition can be calculated by:

$$t_{tot} = |Code2 - Code1| \times t_{step}$$

Where t_{step} is the current transition step time that could be set in FADE_TIME, $Code2$ is the 12-bit dimming code of target brightness, and $Code1$ is the 12-bit dimming code of initial brightness.

In I²C×PWM(P-ramp) control mode, if the PWM duty cycle has changed, the total ramp time is equal to 1/4 ramp time of PWM control mode. If the I²C code has changed, the total ramp time is equal to the time of I²C control mode.

The LED current ramp in Fade in/out mode is shown in Figure 20.

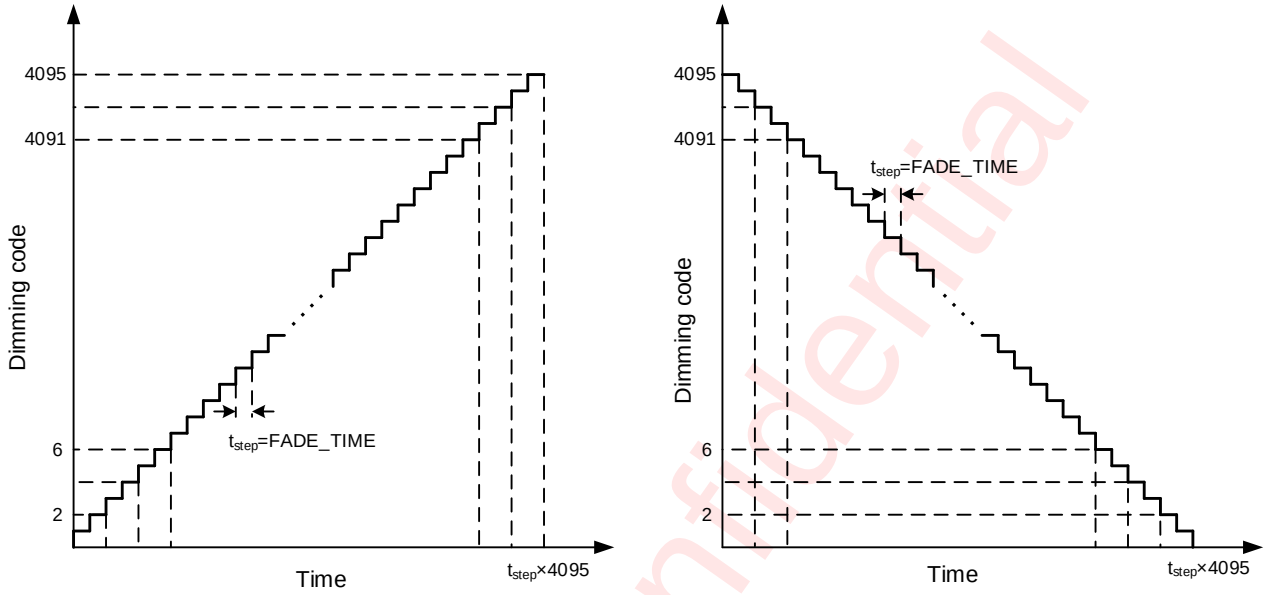


Figure 20 LED current ramp in Fade in/out mode

Slope Mode

AW99706A also provides Slope mode for a fixed LED current ramp time. If the value in FILTER is not 2'b00, AW99706A will enter Slope mode. In this mode, the total ramp time is independent from the dimming code change. AW99706A supports 8 programmable options of ramp time in Slope mode from 8ms to 504ms by setting SLOPE_TIME (CFG 0x06).

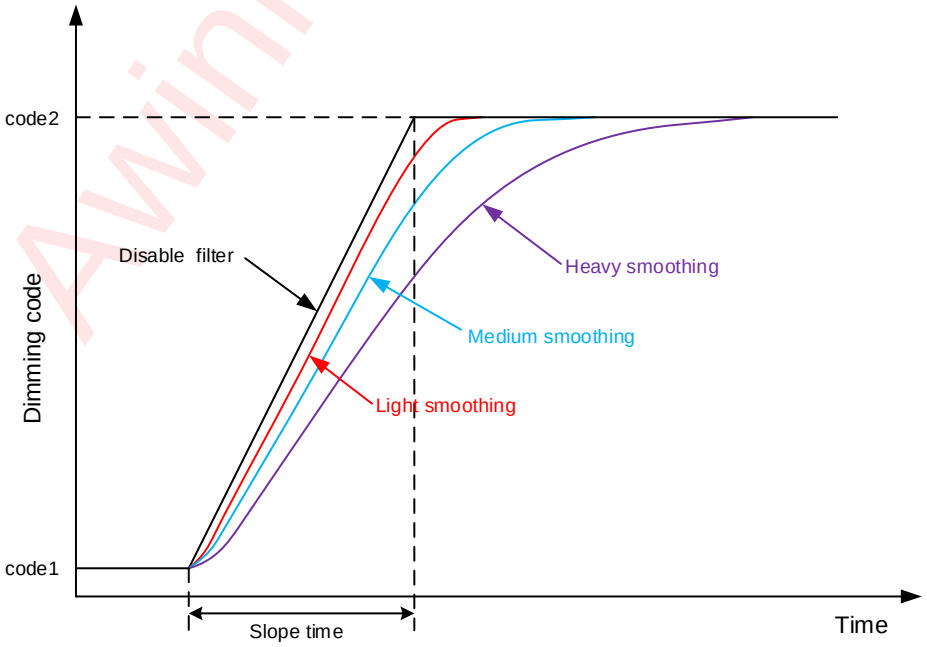


Figure 21 Different Levels of Slope Filter

In Slope mode, writing 1'b0 into FLT_DIS (CFG 0x03) enable slope filter which makes the LED current ramp more smoothly in the beginning and end of ramp time. Changing the value in FILTER can set the level of slope filter. Different levels of slope filter for LED current ramp is shown in Figure 21.

LED Fault Detection

AW99706A is equipped with LED open/short protection function. There are three voltage thresholds for each LED pin for LED open/short detection. The low threshold is the headroom voltage which can be set in HR_OFFSET and DRV_HR (CFG 0x09). The mid threshold is the sum of the headroom voltage and VREF_HYS (CFG 0x0A). The high threshold can be set by VREF_HI (CFG 0x0A).

LED Open Detection

The criterion of LED open is that one of the headroom voltages drops below the low threshold and one of the headroom voltages raises above the high threshold. AW99706A will raise the output voltage when detecting that one of headroom voltages drops below the low threshold. After one of the headroom voltages raises above the high threshold and the open channel is still below the low threshold, AW99706A will determine that this LED channel has open. AW99706A will report LED open status to the host through LED_OPEN_FLAG (CFG 0x12).

LED Short Detection

When an LED short occurs, the headroom voltage on this channel will suddenly increase. When the headroom voltage on this short channel is above the high threshold, and there is at least one headroom voltage still between the low and mid thresholds, the LED short is detected. AW99706A will report LED short status to the host through LED_SHORT_FLAG (CFG 0x13). With writing 1'b1 into LED_SHORT_PROTECTION (CFG 0x03), AW99706A will close the LED channel when LED short is detected.

Over Voltage Protection (OVP)

The OVP function can protect IC and system from excessive voltage. The OVP module monitors the boost output voltage on VOUT pin and limits the VOUT and SW from exceeding safe operating voltages. AW99706A provides an adaptive OVP threshold calculated by V_{BOOST}+1.5V, where V_{BOOST} is the adaptive output voltage . Once VOUT exceeds the threshold, the NFET will be turned off immediately. After the output voltage drops below the OVP threshold, the switch on NFET will restart. AW99706A will report OVP status to the host through FLAG (CFG 0x10).

Over Current Protection (OCP)

The OCP (over current protection) protects device from high current density by a cycle-by-cycle current limit of internal high voltage NFET. Once inductor peak current exceeds the threshold, the NFET will be turn off immediately. AW99706A will report OCP status to the host through FLAG (CFG 0x10). The AW99703 has four selectable OCP thresholds (1.5A, 2A, 2.5A and 3A). These are programmable in SW_ILMT (CFG 0x01).

Over Temperature Protection (OTP)

OTP (Over temperature protection) function monitors the AW99706A's junction temperature in real-time. If it reaches 150℃, the boost converter stops switching and current sinks are all disabled. Once it drops by 20℃, the chip will resume to its previous settings. If temperature goes above 150℃, AW99706A will report OTP status to the host through FLAG (CFG 0x10).

Under Voltage Lock-out (UVLO)

Under voltage lock-out (UVLO) is integrated to detect the input voltage VIN. Once VIN drops below UVLO falling threshold, the current sinks are disabled and the boost converter stops switching. AW99706A will report UVLO status to the host through FLAG (CFG 0x10). If VIN increases above UVLO rising threshold, the boost converter and the current sinks will resume to their previous settings. AW99706A has two selectable UVLO thresholds (2.2V, 5V). These are programmable in UVLOSEL (CFG 0x02).

Multi-time Programmable (MTP)

AW99706A provides multi-time programmable function to modify default configuration of registers. Writing 1'b1 into MTP_LDO_SEL (CFG 0x1E) to set LDO voltage to 5V can enable MTP function. The MTP function requires that VIN should be above 5V. Writing 0x80 into MTPRUN (CFG 0x1F) after set new default values in all registers can make MTP effective. Writing 1'b0 into MTP_LDO_SEL or power AW99706A up again to set LDO voltage to 3.3V after MTP setup is completed.

General I²C Operation

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the A0 pin according to the following table 2:

The A0 pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 111011x. The permitted I²C addresses are 0x76(7-bit) and 0x77(7-bit).

Table 2 Address Selection

A0	Address(7-bit)
GND	0x76
VDD	0x77

DATA VALIDATION

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

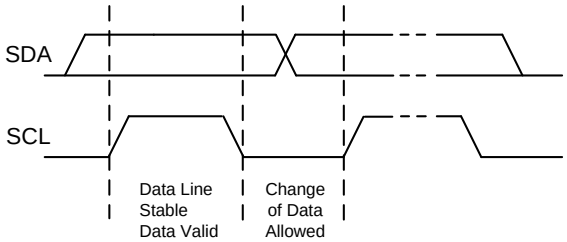


Figure 22 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

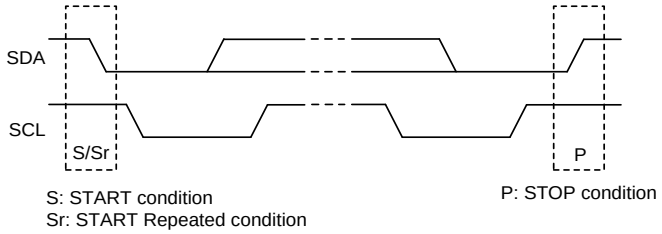


Figure 23 I²C Start/Stop Condition Timing

ACKNOWLEDGE(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

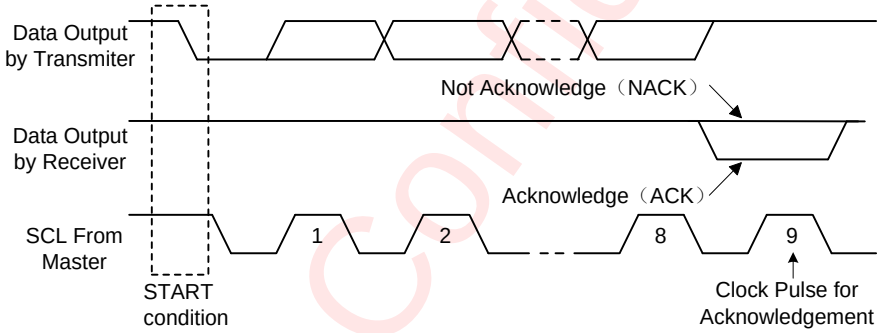


Figure 24 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal

h) If master will send further data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g)

i) Master generates STOP condition to indicate write cycle end

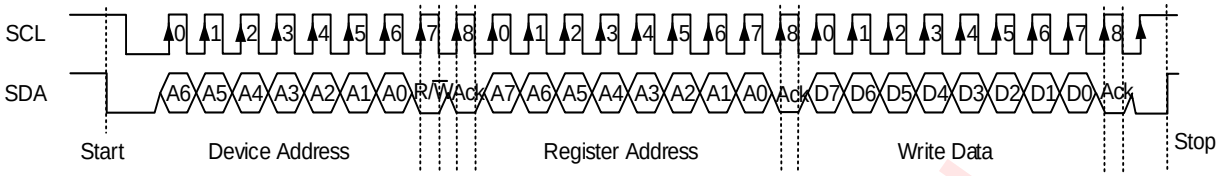


Figure 25 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

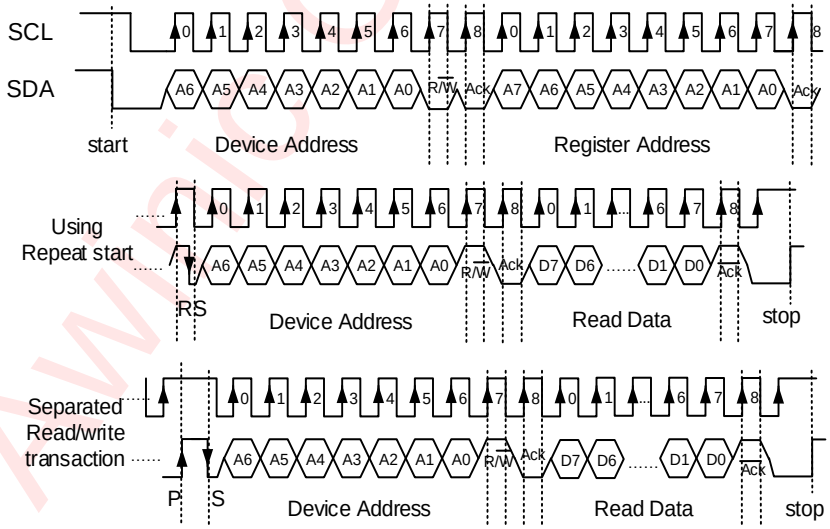


Figure 26 I²C Read Byte Cycle

Register Configuration

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	CFG0	*RW*	PWM_PO	SW_EDGE_RATE				PWM_TO_DC_THRESHOLD	DIM_MODE		0x65
0x01	CFG1	*RW*			SW_ILMT		SW_FREQ				0x39
0x02	CFG2	*RW*	UVLOSEL	ILED_MAX							0x1E
0x03	CFG3	*RW*	LED_SHORT_PROTECTION	FLT_DIS				BRT_WIDTH			0x04
0x04	CFG4	*RW*					BRT_MSB				0x00
0x05	CFG5	*RW*	BRT_LSB								0x00
0x06	CFG6	*RW*	RAMP_CTR		SLOPE_TIME			FADE_TIME			0xA9
0x07	CFG7	*RW*	PWM_SRATE						BRT_MODE		0x04
0x08	CFG8	*RW*	ILED_FREQ			ONOFF_CTR		ONOFF_TIME			0x0C
0x09	CFG9	*RW*	HR_OFFSET				DRV_HR			EN_PFM	0x4B
0x0A	CFGA	*RW*	VREF_HI		VREF_HYS			DITHER_MODE	DITHER		0x72
0x0B	CFGB	*RW*	PS_EN	PS_MODE				PWM_CODE_HYS			0x01
0x0C	CFGC	*RW*		VBT_MIN	VBT_MAX						0x6C
0x0D	CFGD	*RW*	BACKLIGHT_EN	LED1_EN	LED2_EN	LED3_EN	LED4_EN	LED5_EN	LED6_EN		0XFE
0x10	FLAG	*RO*					OVL_FLAG	OCP_FLAG	OTP_FLAG	UVLO_FLAG	0x00
0x11	CHIPID	*RO*	CHIP_ID								0x07
0x12	LED_OPEN_FLAG	*RO*			LED1_OPEN_FLAG	LED2_OPEN_FLAG	LED3_OPEN_FLAG	LED4_OPEN_FLAG	LED5_OPEN_FLAG	LED6_OPEN_FLAG	0x00
0x13	LED_SHORT_FLAG	*RO*			LED1_SHORT_FLAG	LED2_SHORT_FLAG	LED3_SHORT_FLAG	LED4_SHORT_FLAG	LED5_SHORT_FLAG	LED6_SHORT_FLAG	0x00
0x1E	MTPLDOSEL	*RW*								MTP_LDO_SEL	0x00
0x1F	MTPRUN	*WO*	MTPRUN_EN								0x00

NOTE7: *The default value refers to the set value of the registers when the chip is manufactured, which is the recommendation setting to maintain the overall function and good performance of the chip as well.*

Register Detailed Description

CFG0：PWM Control Register (Address 00H)

Bit	Symbol	R/W	Description	Default
7	PWM_PO	RW	PWM polarity enable: 0: disable (default) 1: enable	0x65
6:5	SW_EDGE_RATE	RW	SW Edge Rate Control: 00: slow 01-10: typical 11: fast (default)	
4:3	Reserved	RW	Not used	
2	PWM_TO_DC_THRESHOLD	RW	Mixed mode duty change: 0: 12.5% 1: 25% (default)	

1:0	DIM_MODE	RW	Dimming Mode Selection: 00: BYPASS 01: DC (default) 10: MIX 11: MIX_26k	

CFG1：Boost Control Register (Address 01H)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0x39
5:4	SW_ILMT	RW	Switching Current Limitation Selection: 00: 1.5A 01: 2A 10: 2.5A 11: 3A (default)	
3:0	SW_FREQ	RW	Boost Switching Frequency(300kHz-1.7MHz): 0100: 300k 0101: 400k 0110: 500k 0111: 600k 1000: 660k 1001: 750k (default) 1010: 850k 1011: 1M 1100: 1.2M 1101: 1.33M 1110: 1.5M 1111: 1.7M	

CFG2： (Address 02H)

Bit	Symbol	R/W	Description	Default
7	UVLOSEL	RW	UVLO Threshold: 0: 2.2V (default) 1: 5.0V	0x1E
6:0	ILED_MAX	RW	ILED Current Setting: 000 0000: 5mA 000 0001: 5.5mA 000 0010: 6mA … 001 1110: 20mA (default) 001 1111: 20.5mA … 101 1010: 50mA	

CFG3： (Address 03H)

Bit	Symbol	R/W	Description	Default
7	LED_SHORT_ PROTECTION	RW	When SHORT fault happened, Enable Close LEDx: 0: OFF (default) 1: ON	0x04
6	FLT_DIS	RW	Slope filter function enable: 0: Enable filter (default) 1: Disable filter	
5:3	Reserved	RW	Not used	
2:0	BRT_WIDTH	RW	Bit selection (Brightness Control by I2C Register,8-12bit): 000: 8bit 001: 9bit 010: 10bit 011: 11bit 100-111: 12bit (default)	

CFG4： Brightness Control1 Register (Address 04H)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0x00
3:0	BRT_MSB	RW	Led Brightness Msb Register	

CFG5： Brightness Control2 Register (Address 05H)

Bit	Symbol	R/W	Description	Default
7:0	BRT_LSB	RW	Led Brightness Lsb Register	0x00

CFG6： (Address 06H)

Bit	Symbol	R/W	Description	Default
7:6	RAMP_CTR	RW	Ramp Control and Filter Selection: 00: Fade in/fade out 01: Light filter 10: Medium filter (default) 11: Heavy filter	0xA9
5:3	SLOPE_TIME	RW	Slope Time Control: 000: 8ms 001: 24ms 010: 48ms 011: 96ms 100: 200ms 101: 300ms (default) 110: 400ms 111: 500ms	

2:0	FADE_TIME	RW	Fade In/Out Time Control(per step): 000: 8us 001: 16us (default) 010: 32us 011: 64us 100: 128us 101: 256us 110: 512us 111: 1024us	

CFG7： (Address 07H)

Bit	Symbol	R/W	Description	Default
7:5	PWM_SRATE	RW	PWM Sample Rate: 000: auto detection (default) 001: 0.5MHz 010: 1MHz 011: 2MHz 100: 4MHz 101: 8MHz 110-111: 24MHz	0x04
4:2	Reserved	RW	Not used	
1:0	BRT_MODE	RW	Advanced Brightness Mode Control: 00: PWM (default) 01: I^2C 10: I^2C×PWM 11: I^2C×PWM(PWM ramp)	

CFG8： (Address 08H)

Bit	Symbol	R/W	Description	Default
7:5	ILED_FREQ	RW	PWM frequency of LED current in MIX_26k: 000: 26KHz (default) 001: 26/2KHz 010: 26/4KHz 011: 26/8KHz 100-111: 26/16KHz	0x0C
4:3	ONOFF_CTR	RW	Turn on/off Mode Control: 00: Soft_start + fast_end 01: Soft_start + soft_end (default) 10-11: RAMP_CTR = 00 fade RAMP_CTR = 01/10/11 slope	
2:0	ONOFF_TIME	RW	Turn on/off Time Control(per step): 001: 0.25us 010: 0.5us 011: 1us 100: 2us (default) 101: 4us 110: 8us 111: 16us	

CFG9： (Address 09H)

Bit	Symbol	R/W	Description	Default
7:4	HR_OFFSET	RW	Headroom voltage offset: 0000: 460mV 0001: 390mV 0010-0011: 320mV 0100-0111: 250mV (default) 1000-1111: 180mV	0x4B
3:1	DRV_HR	RW	Headroom voltage offset and LOW comparator threshold: 000: HR_OFFSET+875mV 001: HR_OFFSET+750mV 010: HR_OFFSET+625mV 011: HR_OFFSET+500mV 100: HR_OFFSET+375mV 101: HR_OFFSET+250mV (default) 110: HR_OFFSET+125mV 111: HR_OFFSET	
0	EN_PFM	RW	PFM function enable: 0: Disable PFM 1: Enable PFM (default)	

CFGA： (Address 0AH)

Bit	Symbol	R/W	Description	Default
7:6	VREF_HI	RW	High Comparator threshold: 00: 5V 01: 4V (default) 10: 3V 11: 2V	0x72
5:4	VREF_HYS	RW	Mid Comparator threshold: 00: DRV_HR+1000mV 01: DRV_HR+750mV 10: DRV_HR+500mV 11: DRV_HR+250mV (default)	
3	Reserved	RW	Not used	
2	DITHER_MODE	RW	Dither function method select: 0: Dither only on transitions (default) 1: Dither at all times	
1:0	DITHER	RW	Dither(1-3bit): 00: Dithering disabled 01: 1-bit dithering 10: 2-bit dithering (default) 11: 3-bit dithering	

CFGB： (Address 0BH)

Bit	Symbol	R/W	Description	Default
7	PS_EN	RW	PWM out phase shift enable: 0: Disable (default) 1: Enable	0x01

6:4	PS_MODE	RW	Select PWM output phase configuration: 000: 6-phase, 6 drivers (0°, 56°, 112°, 167°, 225°, 281°) (default) 001: 5-phase, 5 drivers (0°, 67°, 135°, 216°, 288°, OFF) 010: 4-phase, 4 drivers (0°, 90°, 180°, 270°, OFF, OFF) 011: 3-phase, 3 drivers (0°, 124°, 248°, OFF, OFF, OFF) 100: 2-phase, 2 drivers (0°, 180°, OFF, OFF, OFF, OFF) 101: 3-phase, 6 drivers (0°, 0°, 124°, 124°, 248°, 248°) 110: 2-phase, 6 drivers (0°, 0°, 0°, 180°, 180°, 180°) 111: 1-phase, 6 drivers (0°, 0°, 0°, 0°, 0°, 0°)	
3	Reserved	RW	Not used	
2:0	PWM_CODE_HYS	RW	PWM code Hysteresis: 000: 0LSB 001: 1LSB (default) 010: 2LSB 011: 3LSB 100: 4LSB 101-111: 5LSB	

CFGC： (Address 0CH)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0x6C
6	VBT_MIN	RW	Boost min voltage control: 0: BOOST_MIN=7V; 1: BOOST_MIN=16V; (default)	
5:3	VBT_MAX	RW	Boost max voltage control: VBT_MIN=0 000-010: 21V 011: 23V 100: 25V 101: 28V 110: 30V 111: 32.5V VBT_MIN=1 000: 25V 001: 28V 010: 30V 011: 32.5V 100: 36V 101: 38.5V (default) 110: 40V	
2:0	Reserved	RW	Not used	

CFGD： (Address 0DH)

Bit	Symbol	R/W	Description	Default
7	BACKLIGHT_EN	RW	Backlight Enable	0xFE
6	LED1_EN	RW	Led Chanel 1 Enable	
5	LED2_EN	RW	Led Chanel 2 Enable	
4	LED3_EN	RW	Led Chanel 3 Enable	
3	LED4_EN	RW	Led Chanel 4 Enable	
2	LED5_EN	RW	Led Chanel 5 Enable	
1	LED6_EN	RW	Led Chanel 6 Enable	
0	Reserved	RW	Not used	

FLAG： (Address 10H)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0x00
3	OVL_FLAG	RO	OVL Flag	
2	OCP_FLAG	RO	OCP Flag	
1	OTP_FLAG	RO	OTP Flag	
0	UVLO_FLAG	RO	UVLO Flag	

CHIPID： (Address 11H)

Bit	Symbol	R/W	Description	Default
7:0	CHIP_ID	RO	Chip Id	0x07

OPENFLAG： (Address 12H)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0x00
5	LED1_OPEN_FLAG	RO	LED1_OPEN_FLAG	
4	LED2_OPEN_FLAG	RO	LED2_OPEN_FLAG	
3	LED3_OPEN_FLAG	RO	LED3_OPEN_FLAG	
2	LED4_OPEN_FLAG	RO	LED4_OPEN_FLAG	
1	LED5_OPEN_FLAG	RO	LED5_OPEN_FLAG	
0	LED6_OPEN_FLAG	RO	LED6_OPEN_FLAG	

SHORTFLAG： (Address 13H)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0x00
5	LED1_SHORT_FLAG	RO	LED1_SHORT_FLAG	
4	LED2_SHORT_FLAG	RO	LED2_SHORT_FLAG	
3	LED3_SHORT_FLAG	RO	LED3_SHORT_FLAG	
2	LED4_SHORT_FLAG	RO	LED4_SHORT_FLAG	
1	LED5_SHORT_FLAG	RO	LED5_SHORT_FLAG	
0	LED6_SHORT_FLAG	RO	LED6_SHORT_FLAG	

MTPLDOSEL： (Address 1EH)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RO	Not used	

0	MTP_LDO_SEL	RW	LDO Voltage Select: 0: 3.3V (default) 1: 5V	0x00

MTPRUN： (Address 1FH)

Bit	Symbol	R/W	Description	Default
7:0	MTPRUN_EN	WO	MTP Process Run Enbale: 01: Read Mode 80: Write Mode	0x00

Application Information

Inductor Selection

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current.

The inductor DC current can be calculated as:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (1)$$

The inductor current peak to peak ripple can be calculated as

$$I_{PP} = \frac{1}{L \times F_S \times \left(\frac{1}{V_{OUT}+V_F-V_{IN}} + \frac{1}{V_{IN}}\right)} \quad (2)$$

The F_S is the operating frequency, the V_F is the schottky diode's forward voltage.

Therefore, the peak current I_P seen by the inductor is calculated as

$$I_P = I_{IN\_DC} + \frac{I_{PP}}{2} \quad (3)$$

The inductor saturation current rating should be considered to cover the inductor peak current. Smaller size and better efficiency are the major concerns for portable devices. The inductor should have low core loss at the switching frequency and low DCR for better efficiency. For these reasons, a 10μH to 47μH inductor value range for different switching frequency is recommended.

Table 4 lists the recommended inductor for the AW99706A. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

Table 4 Recommended Inductors for AW99706A

LED Strings	VIN(V)	Recommended Inductor		
		300k~500kHz	600k~660kHz	750k~1.7MHz
6P6S	2.7~4.4	10 μH - 22 μH	10 μH - 22 μH	10 μH - 22 μH
	5.4~8.8	10 μH - 22 μH	10 μH - 22 μH	10 μH - 22 μH
5P8S	2.7~4.4	15 μH - 33 μH	15 μH - 33 μH	10 μH - 22 μH
	5.4~8.8	10 μH - 22 μH	10 μH - 33 μH	10 μH - 22 μH
6P8S	2.7~4.4	15 μH - 33 μH	15 μH - 33 μH	10 μH - 22 μH
	5.4~8.8	10 μH - 33 μH	10 μH - 33 μH	10 μH - 22 μH
4P10S	5.4~8.8	15 μH - 47 μH	10 μH - 33 μH	10 μH - 22 μH
6P10S	5.4~8.8	15 μH - 47 μH	10 μH - 33 μH	10 μH - 22 μH
6P12S	8.1~13.2	15 μH - 47 μH	10 μH - 33 μH	10 μH - 22 μH

Schottky Diode Selection

To optimize the efficiency, a high-speed and low reverse-recovery current Schottky diode are recommended. Make sure the diode's average and peak current ratings exceed the output average current and the peak inductor current. In addition, the diode's break-down voltage rating must exceed the maximum voltage across the diode. Usually, unexpected high-frequency voltage spikes can be seen across the diode when the diode

turns off. Therefore, leaving some voltage rating margin is always needed to guarantee normal long-term operation when selecting a diode.

Input and Output Capacitors Selection

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming ESR of a capacitor is zero, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (4)$$

Where, V_{ripple} represents peak-to-peak output ripple. The additional output ripple caused by ESR can be calculated as:

$$V_{ripple\_ESR} = I_{OUT} \times R_{ESR} \quad (5)$$

V_{ripple_ESR} can be neglected for ceramic capacitors due to its low ESR, but must be considered if tantalum or electrolytic capacitors are used.

Note that the ceramic capacitance is dependent on the voltage rating. With a DC bias voltage, the capacitance can lose as much as 50% of its value at its rated voltage rating. Leave a large enough voltage rating margin when selecting the component. Therefore, leave enough margin on the voltage rating to ensure adequate capacitance at the required output voltage.

An X5R or X7R capacitor of 4.7μF is recommended for input side. The recommended capacitances of output side is two X5R or X7R capacitors of 4.7μF. The VLDO requires an X5R or X7R capacitor in the range of 1μF to 10μF.

The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

Table 5 Recommended Capacitances for the Boost and LDO Power Stages

Switch Frequency	C_{IN}(μF)	C_{OUT}(μF)	C_{VLDO}(μF)
300kHz~660kHz	4.7	4.7x2	4.7
750kHz~1.7MHz	2.2	4.7x2	4.7

Power Dissipation

The maximum IC junction temperature should not be exceed 125°C under normal operating conditions. This restriction limits the power dissipation of the AW99706A. It is recommended to keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined by using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{ja}} \quad (6)$$

Where, T_{Jmax} is the Maximum Junction Temperature, T_A is the maximum ambient temperature for the application. θ_{ja} is the thermal resistance junction-to-ambient given in Power Dissipation Table.

PCB Layout Consideration

PCB layout is an important design step for those high frequency, high current switching power regulators in order to minimize noise and keep loop stable.

1. To reduce switching losses, it is better to make the SW pin rise and fall times as short as possible. Minimizing the length and area of all traces connected to the SW pin and using a ground plane under the switching regulator are strongly recommended to minimize inter-plane coupling.

2. The input bypass capacitors should be placed as close to the IC as possible to get the best decoupling. The input capacitor must not only be close to the VIN pin, but also to the AGND pin in order to reduce the device supply ripple and keep loop stable.

3. The output capacitors should be placed as close to the schottky diode as possible.

4. Recommended to place IC, inductor, schottky diode, the input and output capacitor on the same layer.

5. The path of the inductor, schottky diode, the input and output capacitor should be kept as short as possible to minimize noise and ringing. Minimize trace lengths between the IC and the inductor, the diode, the input and the output capacitor; keep these traces short, direct, and wide.

6. Connect the exposed paddle to the PCB ground plane using at least four vias.

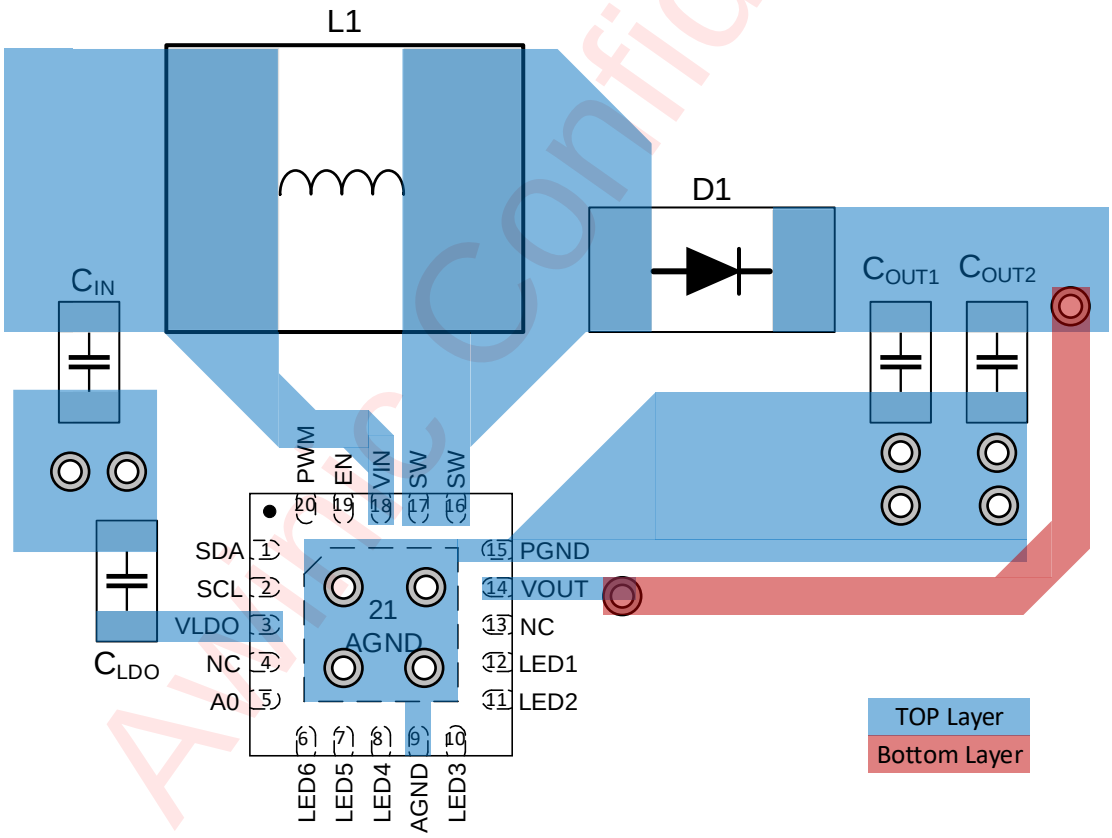
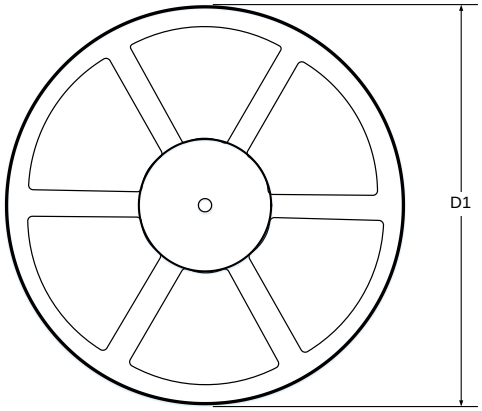
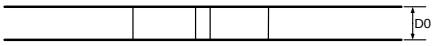


Figure 27 AW99706A LAYOUT Reference

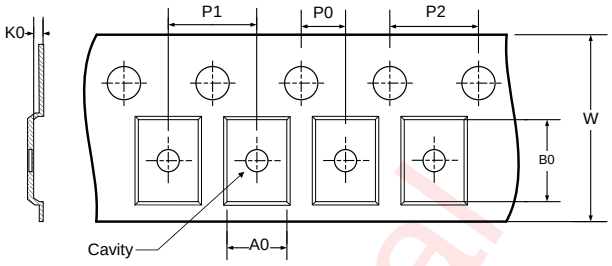
Tape And Reel Information

REEL DIMENSIONS



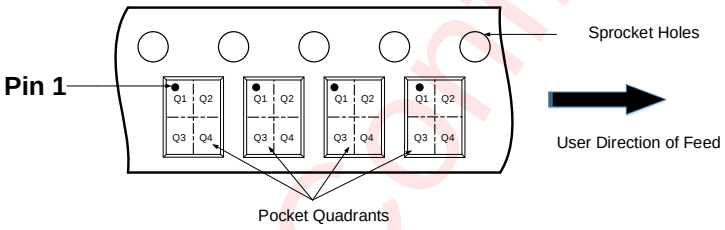


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



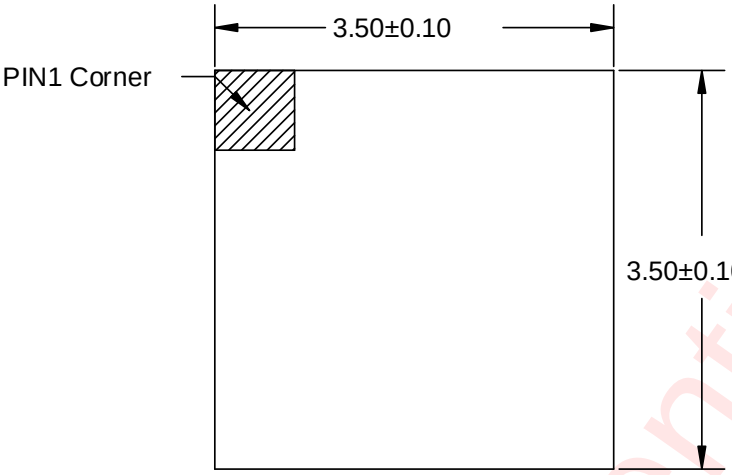
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

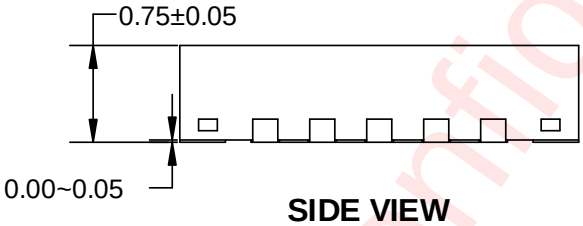
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.75	3.75	1.05	2	8	4	12	Q1

All dimensions are nominal

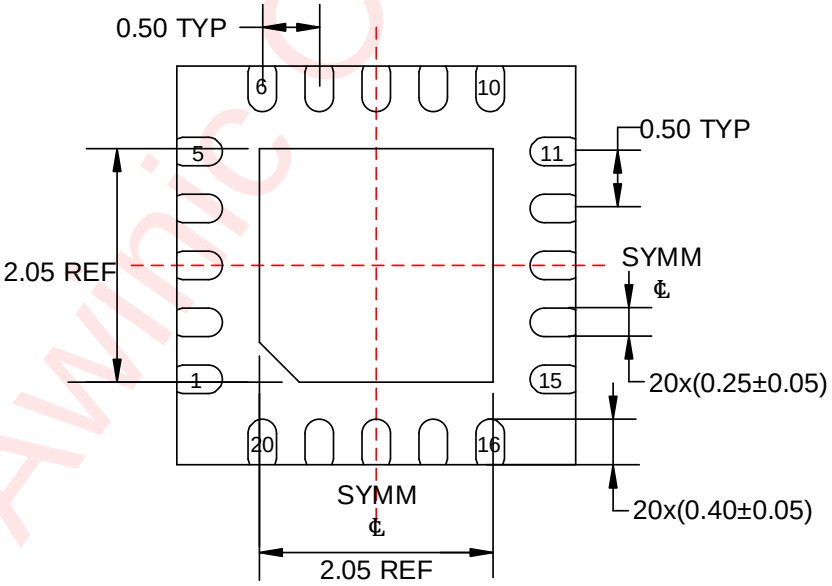
Package Description



TOP VIEW



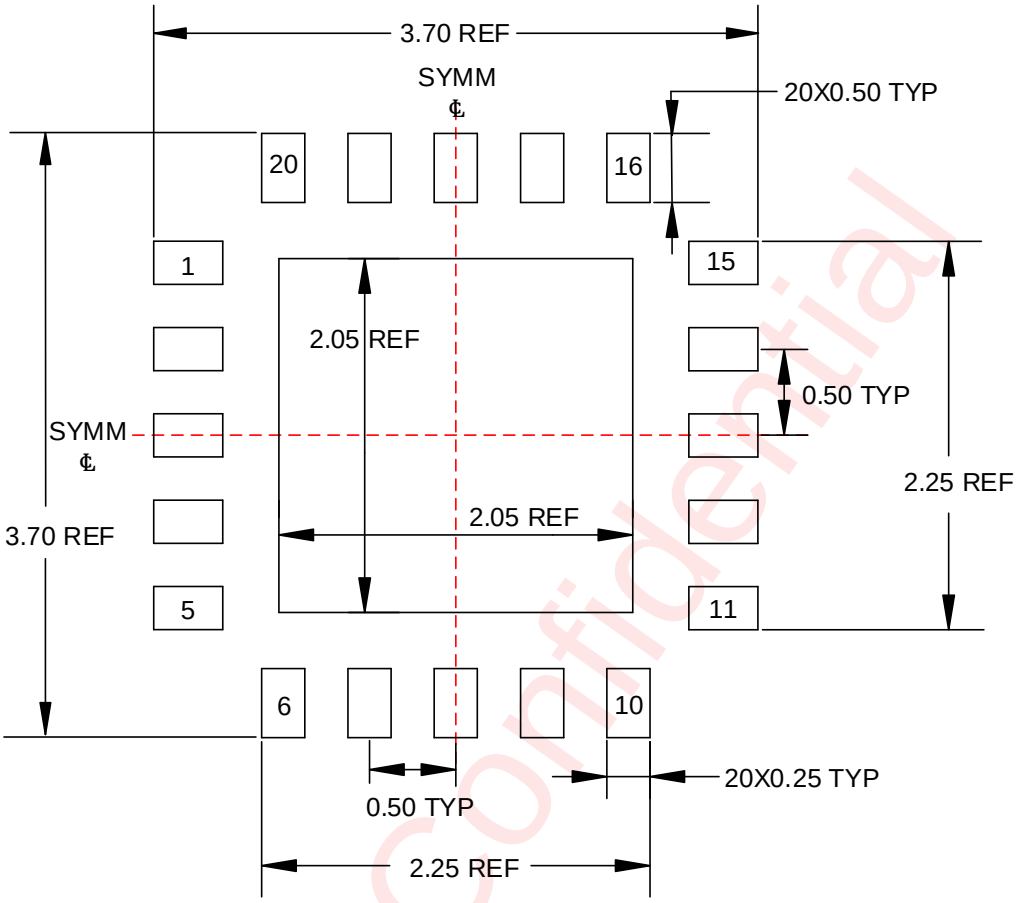
SIDE VIEW

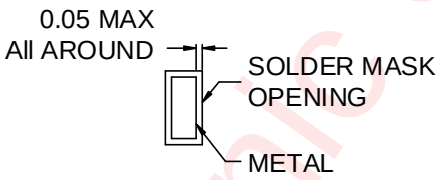


BOTTOM VIEW

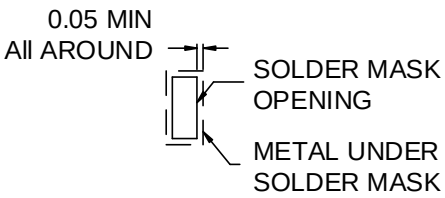
Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Apr. 2024	Officially released
V1.1	Feb. 2025	1. Update the LED current accuracy.(P1&P10) 2. Add the timing diagram.(P14) 3. Update the register configuration.(P28&P34)
V1.2	Oct. 2025	1. Update the title.(P1) 2. Update the max duty cycle of the EC table.(P9)

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