XPL51200

Sink and Source DDR Termination Regulator

FEATURES

- VIN Input Voltage Range: 2.9V to 5.5V
- VLDOIN Voltage Range: 1.1V to 3.5V
- Support DDR I (1.25 VTT), DDR II (0.9 VTT), DDR III (0.75 VTT), DDR IIIL (0.675VTT) and DDR IV (0.6 VTT) Requirements
- Requires Minimum Output Capacitance of 20uF
- PGOOD to Monitor Output Regulation
- EN Input
- Remote Sensing (VOSNS)
- Built-In Soft-Start and UVLO
- Over Current Protection
- Thermal Shutdown Protection
- Lead free and halogen free

APPLICATIONS

- Memory Termination Regulator for DDR I, DDR II, DDR III, DDR IIIL, Low-Power DDR III and DDR IV
- Notebooks, Desktops and Servers
- Telecom, Datacom and Base Stations

DESCRIPTION

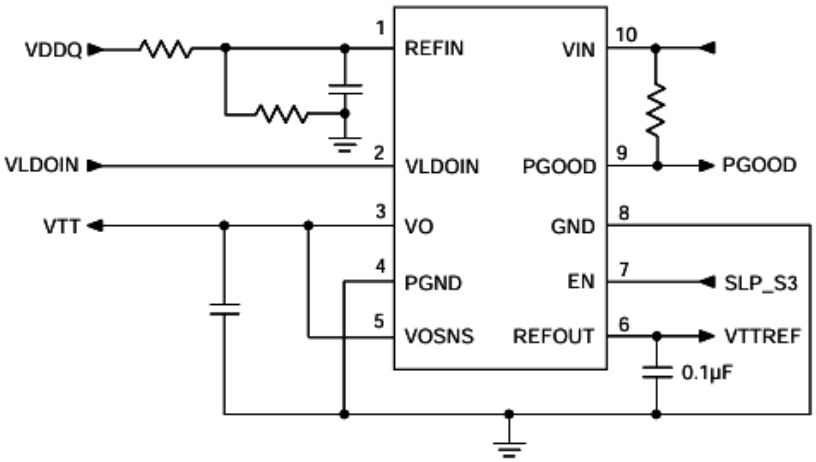
The XPL51200 device is a sink and source DDR termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is key consideration.

The XPL51200 maintains a fast transient response and requires a minimum output capacitance of only 20 µF. The XPL51200 supports a remote sensing function and all power requirements for DDR, DDR II, DDR III, DDR IIIL, Low-Power DDR III and DDR IV VTT bus termination.

In addition, the XPL51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The XPL51200 is available in the thermally efficient 10-pin 3x3 DFN package with thermal pad, and supports the operating temperature range from –40°C to +125°C.

SIMPLIFIED APPLICATION CIRCUIT



REVISION HISTORY

Release	Rev	Changes	Date
Released		First release	6/30/2025

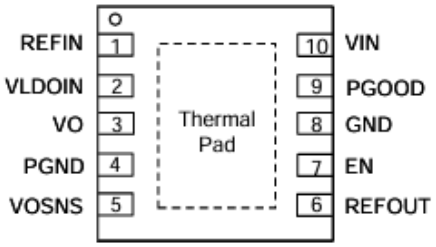
ORDERING INFORMATION

Part Number	Output Current (A)	Package	Top Marking	MPQ
XPL51200	3	3×3 DFN-10	51200	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION

(Top View)



Pin Configuration

Pin	Name	Description
1	REFIN	Reference input.
2	VLDOIN	Power input of the regulator.
3	VO	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	VOSNS	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	EN	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN directly.
8	GND	Analog ground. Connect to negative terminal of the output capacitor.
9	PGOOD	Open-drain, power-good indicator.
10	VIN	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A ceramic decoupling capacitor with a value 4.7μF is required.
11	Exposed Pad	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

ABSOLUTE MAXIMUM RATINGS(1)

Parameter	Min	Max	Units
VIN, VLDOIN	-0.3	6	V
EN, REFIN, VOSNS	-0.3	6	V
VOUT, REFOUT, PGOOD	-0.3	6	V
PGND to GND	-0.3	0.3	V
Power Dissipation, PD @ TA = 25°C		2.5	W
Operating junction temperature, TJ	-40	+150	°C
Storage temperature	-55	+150	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	V_{IN}	2.9		5.5	V
LDO input voltage	V_{LDOIN}	1.1		3.5	V
Junction Temperature Range	T_{OJ}	-40		125	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on two-layer XPL51200 EVB in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	24.68	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	12.99	°C/W

ELECTRICAL SPECIFICATIONS

TJ = –40°C to +125°C (typical value at TJ = +25°C), VIN = VEN = 3.3 V; VLDOIN = 1.5 V, REFIN =VOSNS = 0.75 V, COUT = 3 x 10 µF; unless otherwise specified

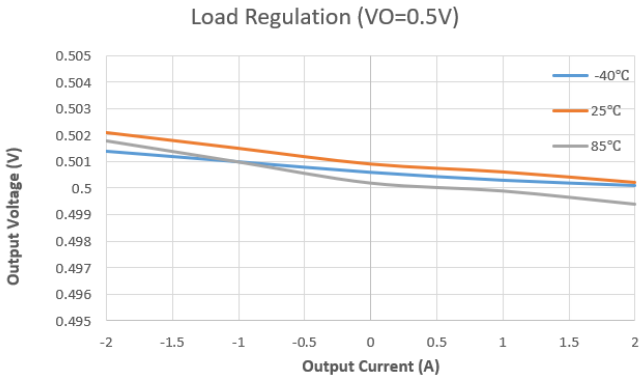
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
VIN supply current	I_{VIN}	V_{VIN}=3.3V, no load, V_{EN}=3.3V		0.55		mA
VIN standby current	I_{VINSTB}	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}>0.4V		150		uA
VIN shutdown current	I_{VINSDN}	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}=0V		75		uA
VLDOIN supply current	I_{VLDOIN}	V_{VIN}=3.3V, no load		10		uA
VLDOIN standby current	$I_{VLDOINSTB}$	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}>0.4V		0.5		uA
VLDOIN shutdown current	$I_{VLDOINSDN}$	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}=0V		0.3		uA
REFIN input current	I_{REFIN}	V_{EN}=3.3V		0.1		uA
VOSNS input current	I_{VOSNS}	V_{VIN}=3.3V, no load, V_{EN}=3.3V		12		uA
VTT output voltage	V_{VTT}	DDR I		1.25		V
		DDR II		0.9		
		DDR III		0.75		
		DDR IIIL		0.675		
		DDR IV		0.6		
VTT output voltage tolerance refer to REOUT	V_{VTTOS}	I_{VTT}=0		1		mV
VTT output voltage tolerance refer to REFOUT	ΔV_{VTT}	|IVTT|<2A		1		mV
VTT source current limit	$I_{VOCLSRC}$	VTT=REFIN *0.90, PGOOD=HI		5		A
VTT sink current limit	$I_{VOCLSNK}$	VTT=REFIN *1.1, PGOOD=HI		5		A
VO discharge current	$I_{DISCHARGE}$	V_{REFIN}=0V, V_{VTT}=0.3V, V_{EN}=0V		12		Ω
PGOOD threshold	V_{PGTH}	PGOOD lower threshold refer to REFOUT		-20		%
		PGOOD upper threshold refer to REFOUT		20		
		PGOOD hysteresis		5		
PGOOD startup delay	$T_{PGSTUPDLY}$	VOSNS is within 15% of REFOUT		2		ms
PGOOD bad delay	$T_{PGBADDLY}$	VOSNS is outside 20% of		15		us
PGOOD output low voltage	$V_{PGOODLOW}$	I_{SINK}=4mA		0.37		V
PGOOD leakage current	$I_{PGOODLK}$	VOSNS is inside of PGOOD		5		uA
REFIN UVLO threshold	$V_{REFINUVLO}$	REFIN rising		0.39		V
REFIN UVLO threshold	$V_{REFINUVLO}$	Hysteresis		20		mV

TJ = –40°C to +125°C (typical value at TJ = +25°C), VIN = VEN = 3.3 V; VLDOIN = 1.5 V, REFIN =VOSNS = 0.75 V, COUT = 3 x 10 µF; unless otherwise specified

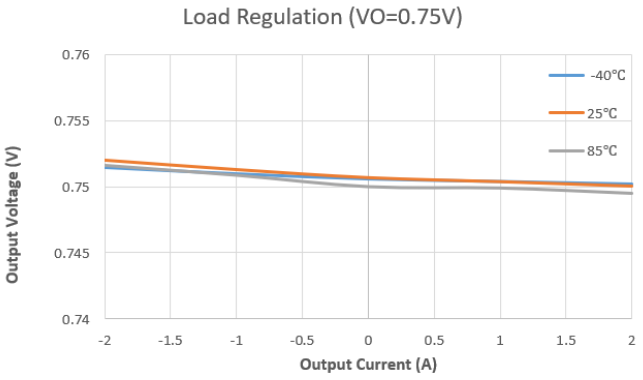
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
REFOUT output voltage	V_{REFOUT}	DDR I		1.25		V
		DDR II		0.9		
		DDR III		0.75		
		DDR IIIL		0.675		
		DDR IV		0.6		
REFOUT output voltage tolerance refer to REFIN	ΔV_{REFOUT}	-1mA < I_{REFOUT}< 1mA		1		mV
REFOUT source current limit	$I_{REFOUTSRCL}$	V_{REFOUT}=0V		50		mA
REFOUT sink current limit	$I_{REFOUTSNCL}$	V_{REFOUT}=VIN		80		mA
VIN UVLO threshold	$V_{VINUVLO}$	VIN rising		2.6		V
		Hysteresis		100		mV
EN input voltage threshold	V_{ENTH}	Enable rising		1.3		V
		Enable falling		0.8		
		Hysteresis		0.5		
Logic input leakage current	I_{ENLEAK}			0.01		uA
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SDHYS}			15		°C

TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

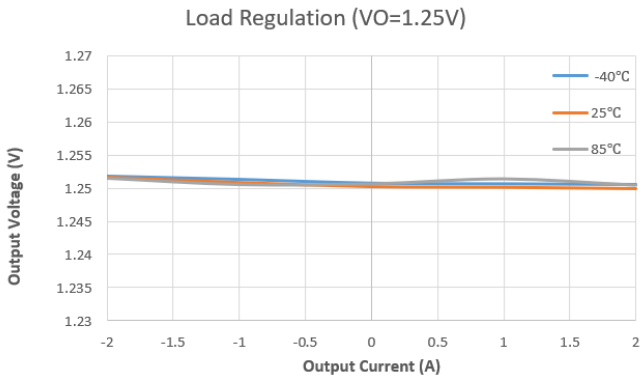
3 x 10uF MLCCs are used on the output.



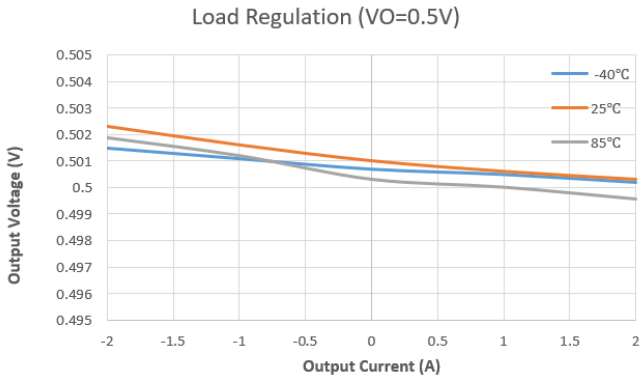
VIN=3.3V



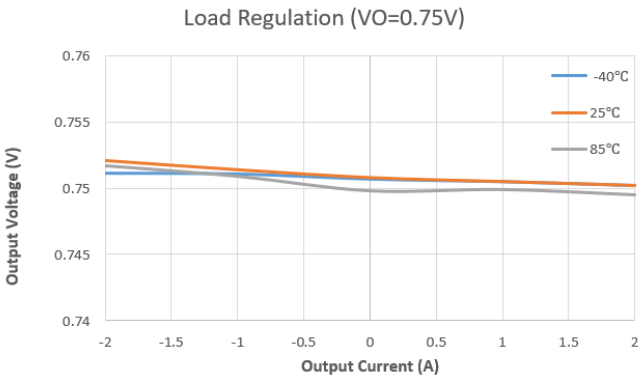
VIN=3.3V



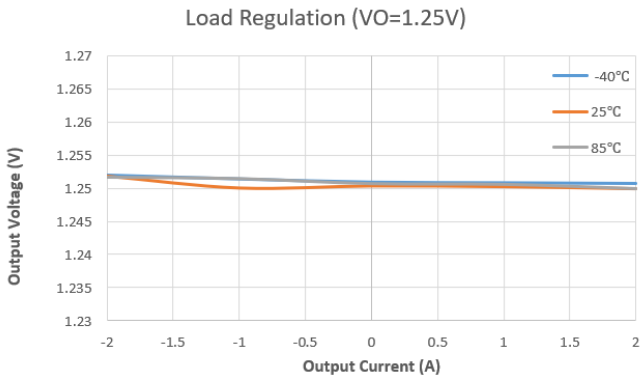
VIN=3.3V



VIN=5V

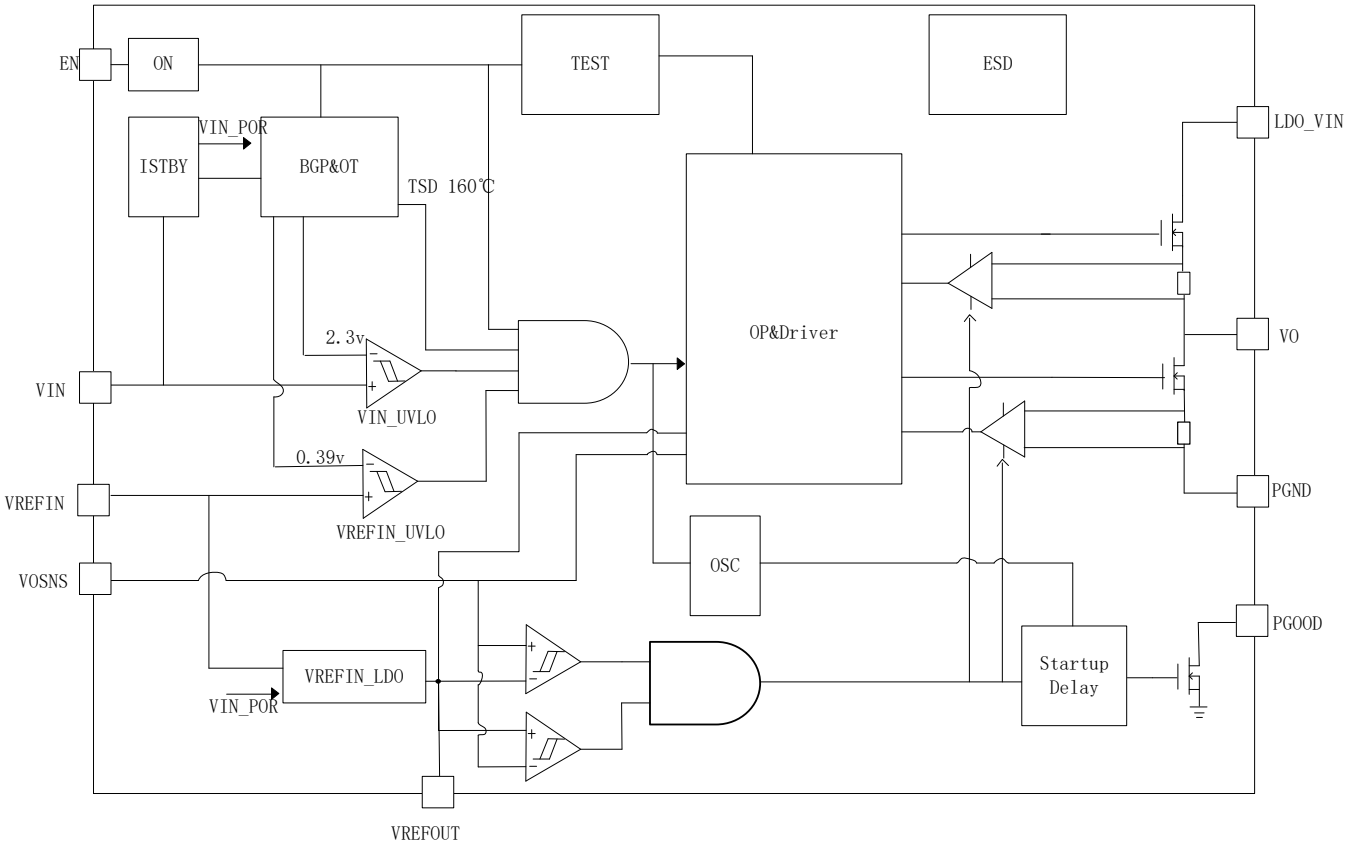


VIN=5V



VIN=5V

FUNCTIONAL DESCRIPTION



Block Diagram

Overview

The XPL51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The device maintains a fast transient response and only requires a minimum output capacitance of 20µF. The device supports a remote sensing function and all power requirements for DDR, DDR II, DDR III, DDR IIIL, Low-Power DDR III and DDR IV VTT bus termination.

VIN, VLDOIN

VIN and VLDOIN are two independent input supply pins for the XPL51200. VIN is used to supply all the internal analog circuits. VLDOIN is only used to supply the output stage to create the regulated VTT. To keep the regulation successfully, VIN should be equal to or larger than VLDOIN+1V. Using a higher VLDOIN voltage will produce a larger sourcing capability from VTT. But the internal power loss will also increase and then the heat increases.

If the junction temperature exceeds the thermal shutdown threshold, then the XPL51200 will enter the shutdown state that is the same as manual shutdown, where VTT is tri-state and VREF remains active.

Under-voltage Lockout (VIN UVLO)

The XPL51200 implements an under-voltage lockout circuit to keep the regulator shut off until VIN voltage exceeds the rising UVLO threshold.

REFIN

When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). Then, the XPL51200 generates REFOUT voltage by reference to REFIN. The REFIN voltage is supported from 0.5 V to 1.8 V for many types of low-power DDR applications.

REFOUT

REFOUT generates the VTT reference voltage. It has 10mA source and sink ability. REFOUT becomes active when REFIN voltage rises to 0.39 V and VIN is above the UVLO threshold. In contrast, it becomes deactivated and discharges to GND through an internal discharge resistance when REFIN is less than 0.37 V. REFOUT are independent of the EN pin state. For better performance, using an output bypass capacitor close this pin is more helpful for the noise. A ceramic capacitor in the range of 0.1µF to 0.01µF is recommended.

VOSNS

The VOSNS pin is the feedback sensing pin of the operation amplifier which regulates the VTT voltage. In most motherboard applications, the termination resistors will connect VTT in a long plane. If using the remote sensing pin – VOSNS to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the VOSNS pin must still be connected to VTT for correct regulation. Care should be taken when a long VOSNS trace is implemented in close proximity to the memory. Noise pickup in the VOSNS trace can cause problems with precise regulation of VTT. A small 0.1µF ceramic capacitor placed next to the VOSNS pin can help to filter any high frequency signals and preventing errors.

VO

VO is the regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the REFOUT voltage with large sinking and sourcing current capability. The maximum continuous current sourcing from VO is a function of VLDOIN. Using a higher VLDOIN will increase the source current, but it also increases the internal power dissipation and reduces the efficiency. Although the XPL51200 can deliver larger current, care should be taken for the thermal dissipation when larger current is required. Thus, an over current function is embedded for preventing overloading and short is occurred. Also, when the temperature exceeds the junction temperature, the thermal shutdown protection is activated. That will drive the VO output into tri-state until the temperature returns below the hysteretic trigger point.

IN Input Capacitor

It is recommended to place a 1-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to VIN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

LDOIN Input Capacitor

It is recommended to place a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel close to LDOIN pin to keep the voltage stable during transient.

Output Capacitor

To ensure stable operation, the XPL51200 requires output capacitance of 20µF or greater. It is recommended to select three 10-µF X5R-or X7R-type ceramic capacitors in parallel to minimize the equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must be placed as close to the OUT pin as possible.

Thermal Considerations

For continuous and reliable operation, the XPL51200 junction temperature should not exceed 125°C. The power dissipation can be calculated as:

$$P_D = (V_{LDOIN}-V_O)*I_{OUT} + V_{IN}*I_{VIN}$$

The junction temperature can be estimated as:

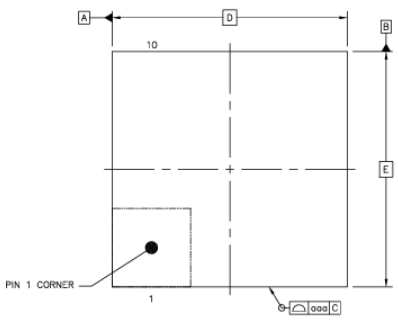
$$T_J = T_A + P_D * \theta_{JA}$$

Layout Considerations

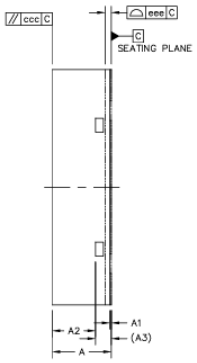
For the best performance of XPL51200, PCB layout suggestions as below are highly recommended:

- ✓ Use wide and short connection plane between capacitors and pins to minimize trace impedance.
- ✓ Connect the GND pin and PGND pin to the thermal pad directly. Use a large ground copper plane for good thermal dissipation, and add multiple vias to further reduce the GND loop trace.
- ✓ Place the input capacitors as close to VLDOIN pin as possible.
- ✓ Place the output capacitors as close to VO pin as possible.
- ✓ Connect the VOSNS pin to the positive node of output capacitors at VOUT terminal for output target level remote sensing.

PHYSICAL DIMENSIONS

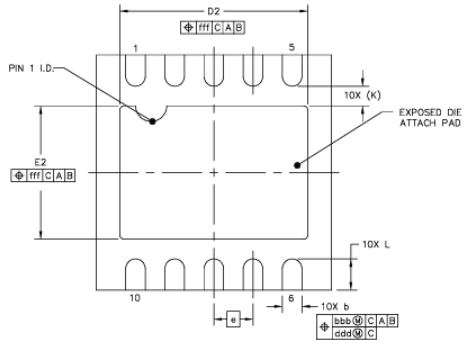


TOP VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.3	2.4	2.5
	Y	E2	1.6	1.7	1.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



BOTTOM VIEW

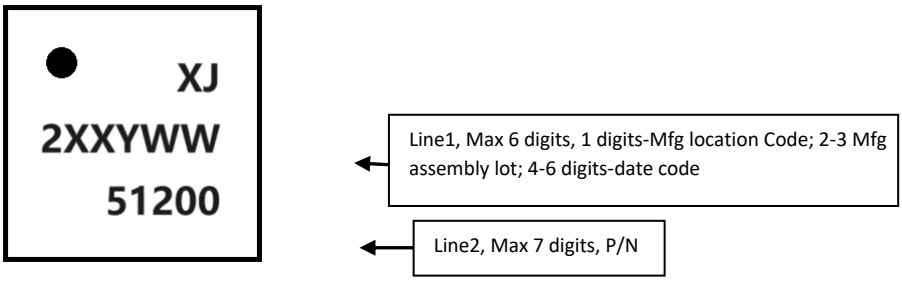
NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

MARKING AND REEL INFORMATION

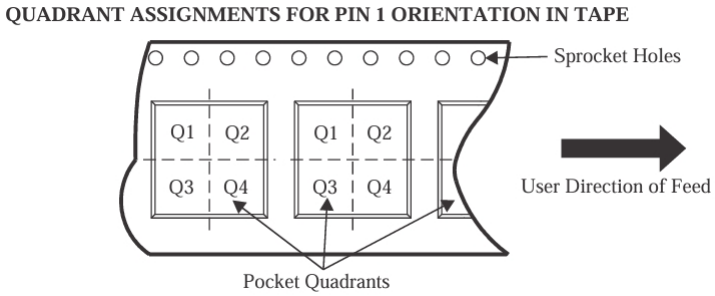
Package Marking & PQ information

XPL51200 Marking

Format:



Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Letter height of 0.5mm

Side pitch of 0.4mm

Line space of 0.25mm

LOGO

Right

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: Assembly location code: JCET: 2
b) 2nd & 3rd digit: Assembly lot number
c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

2. Product Number Code: Line 2

Product Name	P/N Code	Remark
XPL51200	51200	Max. 7 digitals are defined for the device type which are before "-"in general.

3. PQ Method:
   3000/reel in 13-inch