2A Ultra-small Load Switch with Slew Rate Control

Features

- Integrated P-channel MOSFET load switch
- Input voltage: 1V to 5.5V
- 2A maximum continuous switch current
- Switch on-resistance(typ.):
  Rdson=115mΩ at VIN=5.5V
  Rdson=119mΩ at VIN=4.2V
  Rdson=126mΩ at VIN=3.3V
  Rdson=142mΩ at VIN=2.5V
  Rdson=163mΩ at VIN=1.8V
  Rdson=235mΩ at VIN=1.2V
  Rdson=320mΩ at VIN=1V
- Controlled slew rate to limit inrush currents
- Ultra-low shutdown current
- Internal EN pull-down resistor
- Quick Output Discharge(QOD)
- SOT23-5L package

Applications

Smart IoT Devices
Low Power Subsystems
Portable Devices

General Description

The AWP35115 integrates a 126mΩ (typ.) P-channel MOSFET, which can operate over a wide input range of 1V to 5.5V. The AWP35115 features extremely low quiescent current (I_Q) and shutdown current (I_{SD}). Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The AWP35115 features output slew rate control, limiting inrush currents during turn-on to protect downstream devices.

In addition, AWP35115 has QOD function which can prevent the output from floating when the switch is disabled. A smart pull-down resistor is used to the EN pin during initial power-up and disconnects once the EN pin voltage reaches the V_{IH} level, then the standby current is very low and power loss can be reduced.

The AWP35115 is available in SOT23-5L package.

Typical Application Circuit

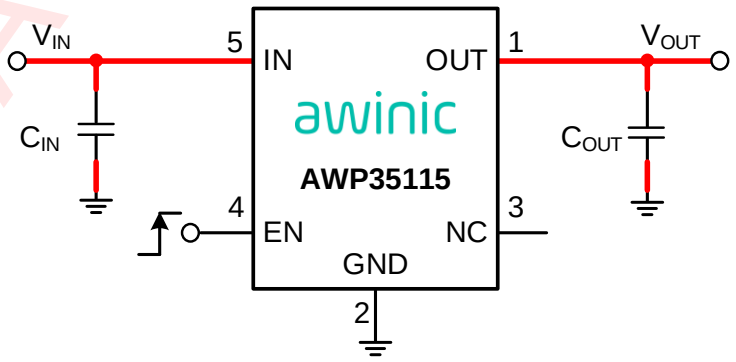


Figure 1 Typical Application Circuit of AWP35115

Pin Configuration And Top Mark

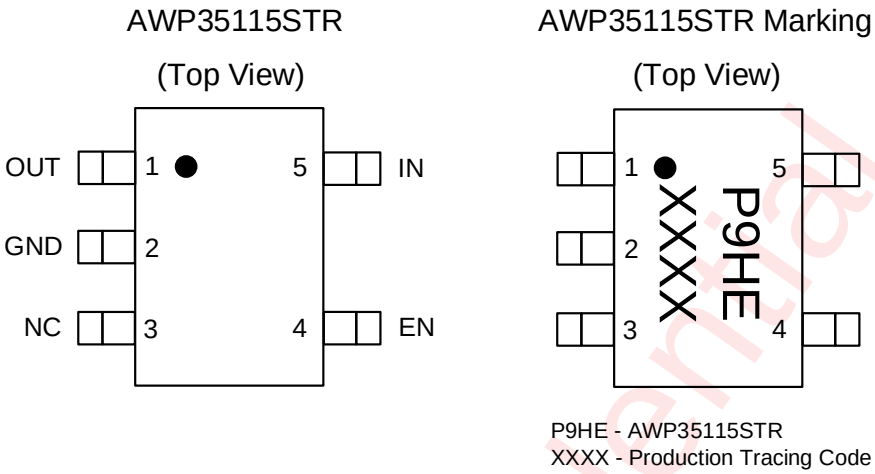


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
1	OUT	Output pin
2	GND	Ground
3	NC	Not connect
4	EN	Chip enable
5	IN	Power supply input

Functional Block Diagram

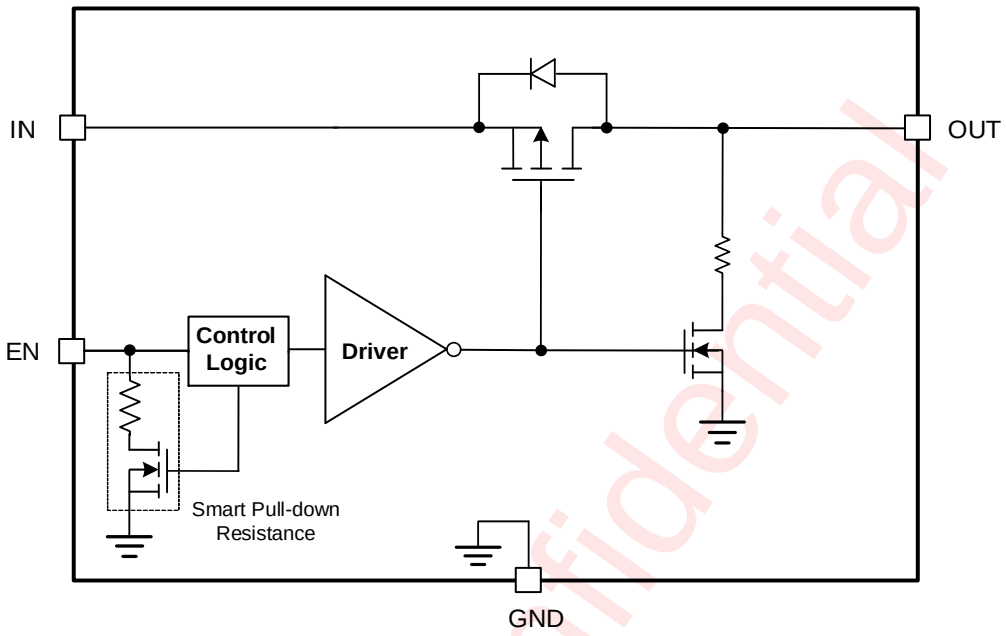


Figure 3 Functional Block Diagram

Typical Application Circuits

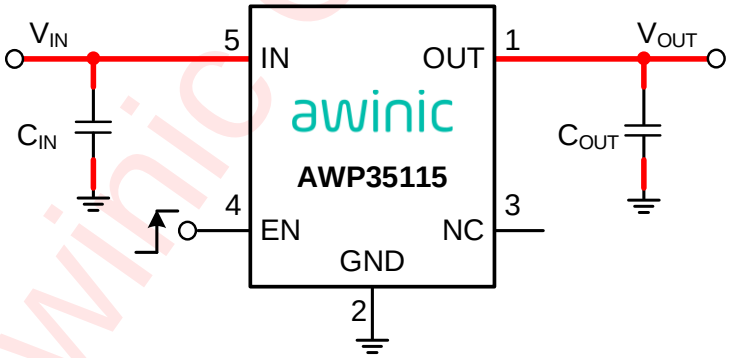


Figure 4 Typical Application Circuit of AWP35115

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP35115STR	-40°C ~ 105°C	SOT23-5L	P9HE	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
Enable Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current for V_{IN} ≥ 2.5V		2A
Maximum Continuous Switch Current for V_{IN} ≥ 2V		1.5A
Maximum Continuous Switch Current for 1.5V ≤ V_{IN} < 2V(NOTE 2)		1A
Maximum Continuous Switch Current for 1V ≤ V_{IN} < 1.5V(NOTE 2)		0.5A
Maximum Peak Switch Current for V_{IN} ≥ 2.5V(NOTE 3)		2.5A
Junction-to-ambient thermal resistance θ_{JA}(NOTE 4)		180°C/W
Operating Free-air Temperature Range		-40°C to 105°C
P_D (Power Dissipation) at T_A=25°C		0.81W
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) (NOTE 5)		±4kV
CDM(Charged Device Model) (NOTE 6)		±2kV
Latch-Up		
Latch-Up (NOTE 7)		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2025.

NOTE7: Test Condition: JESD78F.02.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	1		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output load capacitance(NOTE8)	0.1	1		μF

NOTE8: The Output load capacitance is the nominal value.

Electrical Characteristics

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 3.3V, C_{IN} = 1μF, I_{IN}≤ 2A.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_Q	Input quiescent current	V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=25°C		2		nA
		V_{IN}=V_{EN}=3.3V, I_{OUT}=0A, T_A=85°C		8		nA
		V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=25°C		3		nA
		V_{IN}=V_{EN}=5.5V, I_{OUT}=0A, T_A=85°C		15		nA
I_{SD}	Shutdown current from IN to GND	V_{IN}=3.3V, V_{EN}=0V, T_A=25°C		16		nA
		V_{IN}=3.3V, V_{EN}=0V, T_A=85°C		1000		nA
		V_{IN}=5.5V, V_{EN}=0V, T_A=25°C		35		nA
		V_{IN}=5.5V, V_{EN}=0V, T_A=85°C		1650		nA
POWER SWITCH						
I_{LEAKEN}	EN pin leakage current	V_{IH} < V_{EN} < V_{IN}+0.3V			10	nA
R_{EN}	Smart pull down resistor	V_{IN}=5V, V_{EN}=0.4V		7.2		MΩ
R_{DIS}	Output discharge resistance	V_{IN}=5.0V, EN disable, I_{OUT} Sinking 2mA		88		Ω
R_{dson}	Internal switch MOSFET on-state resistance	V_{IN}=5.5V, I_{OUT}=0.2A, T_A=25°C		115		mΩ
		V_{IN}=3.3V, I_{OUT}=0.2A, T_A=25°C		126		
		V_{IN}=1.8V, I_{OUT}=0.2A, T_A=25°C		163		
		V_{IN}=1.2V, I_{OUT}=0.2A, T_A=25°C		235		
		V_{IN}=1V, I_{OUT}=0.2A, T_A=25°C		320		
POWER SWITCH						
t_R	Output rise time	V_{IN}=3.3V, C_{OUT}=0.1μF, R_{OUT}=150Ω		470		μs
t_{ON}	Switch turn on time			520		μs
t_{EN}	Enable time			300		μs
t_F	Output fall time			15.5		μs
t_{OFF}	Switch turn off time			9.5		μs
V_{IH}	EN input high threshold level		1			V
V_{IL}	EN input low threshold level				0.4	V

Timing Diagram

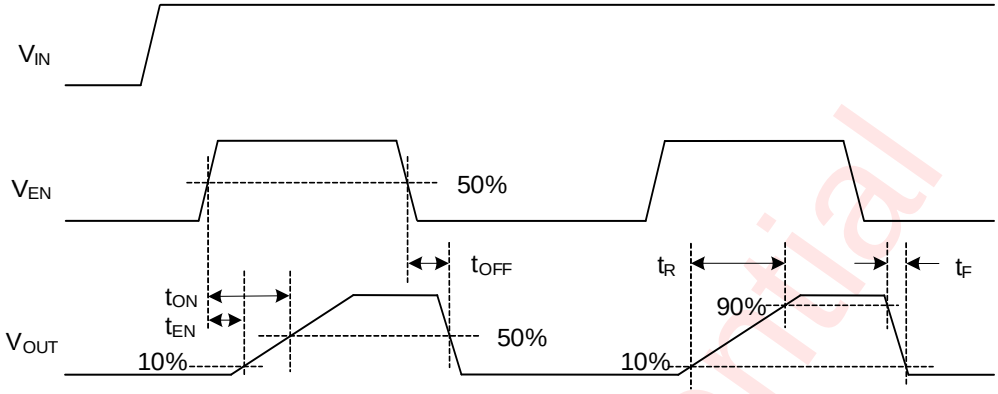


Figure 5 AWP35115 Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.

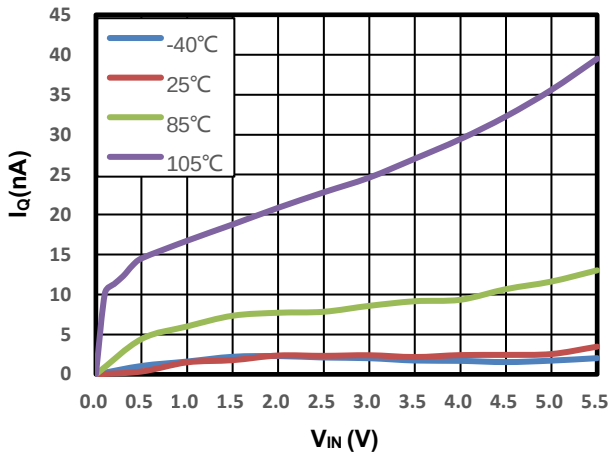


Figure 6 Quiescent Current vs. V_{IN}, No load

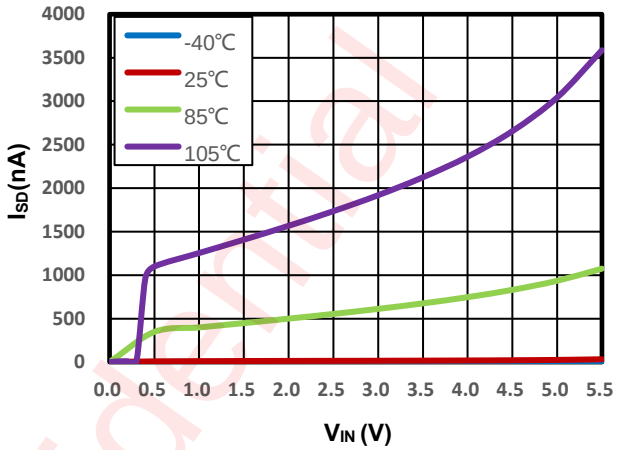


Figure 7 IN Shutdown Current vs. V_{IN}

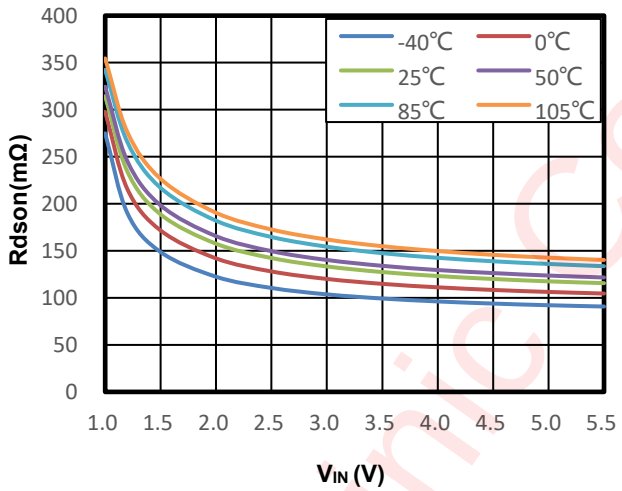


Figure 8 Rdson vs. V_{IN}(I_{OUT}=200mA)

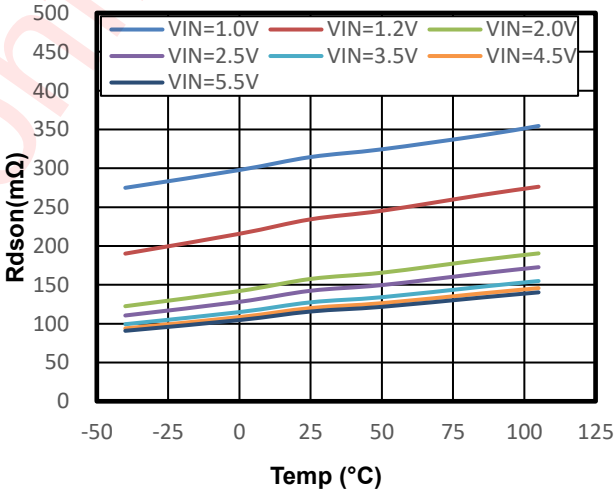


Figure 9 Rdson vs. Temperature(I_{OUT}=200mA)

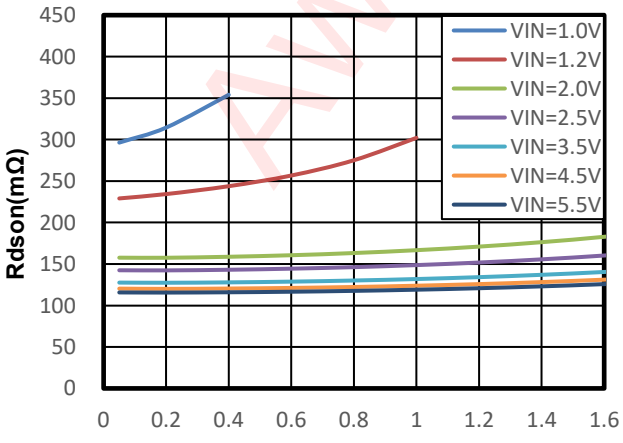
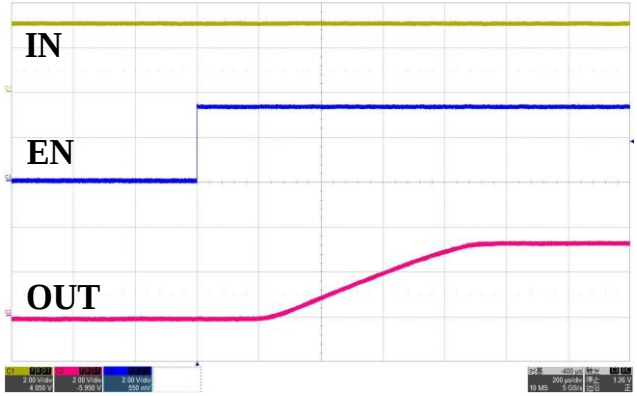


Figure 10 Rdson vs. I_{OUT}



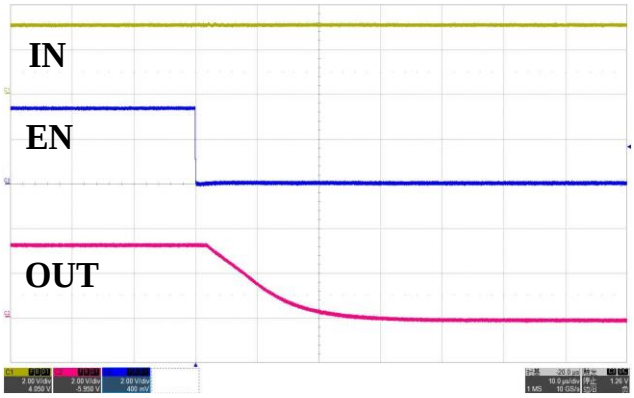
C1: 2.00V/div C2: 2.00V/div t=200μs/div
C3: 2.00V/div

V_{IN}=3.3V, C_{IN}=0.1μF, C_{OUT}=0.1μF, R_{load}=150Ω

Figure 11 Turn On Response

Typical Characteristics (continued)

Ambient temperature is 25°C, C_{IN} = C_{OUT}=1μF, unless otherwise noted.



C1: 2.00V/div C2: 2.00V/div t=10μs/div
C3: 2.00V/div

V_{IN}=3.3V, C_{IN}=0.1μF, C_{OUT}=0.1μF, R_{load}=150Ω

Figure 12 Inrush Current

Detailed Functional Description

The AWP35115 integrates a high side P channel MOSFET, and provides a low on-resistance for a low voltage drop across the device. A controlled slew rate is used in applications to limit the inrush current. The part can be turned on, with a supply voltage from 1V to 5.5V.

Turn On/Off Control

Enable pin is an active high port for AWP35115. The device is closed when EN pin is tied low or pulled down by internal 7.2MΩ resistor, forcing PMOS switch off. The IN/OUT path is activated with a minimum of V_{IN} of 1V and EN forced to high level.

Table 1. Functional Table

	EN	IN to OUT	OUT to GND
AWP35115	Low	OFF	ON
	High	ON	OFF

Slew Rate Control

When the switch is enabled, the device regulates the gate voltage of MOSFET, and controls the V_{OUT} slew rate during t_R to avoid a large input inrush current. The feature reduces the interference to the power supply.

Quick Output Discharge

The AWP35115 includes the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is disabled, a discharge resistance with a typical value of 88Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

Application Information

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device, the actual capacitance should be optimized for the particular application. For all applications, a 1μF or greater ceramic bypass capacitor between V_{IN} and GND is recommended as close to the device as possible. This precaution reduces ringing on the input due to power supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

PCB Layout Consideration

The AWP35115 is low ON-Resistance load switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AWP35115) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AWP35115) and close to OUT pin.

2. The AWP35115 integrates an up to 2A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R\theta_{JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths in Figure 13 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.

3. Use rounded corners on the power trace from the power supply connector to AWP35115 to decrease EMI coupling.

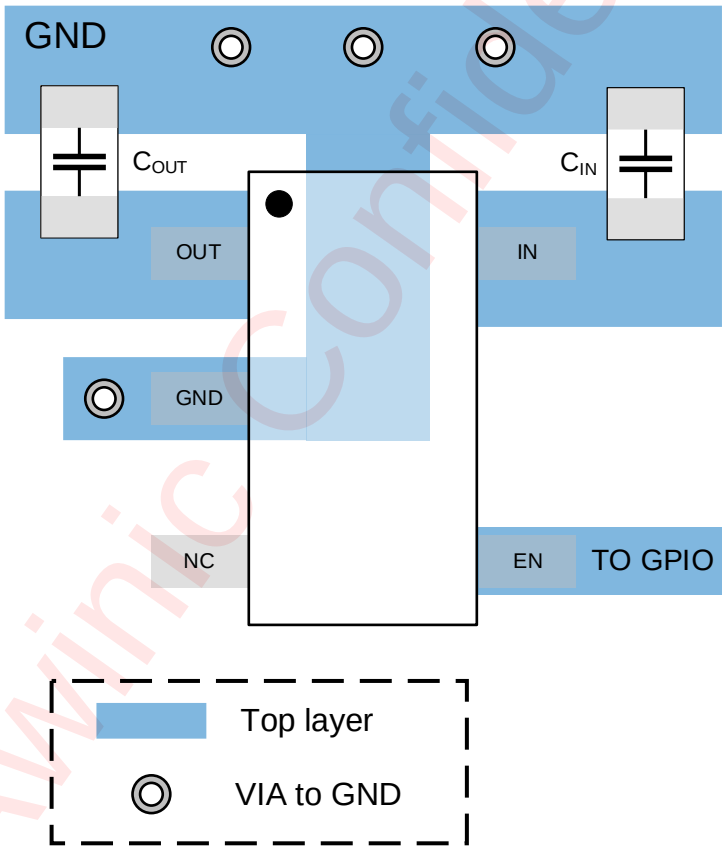
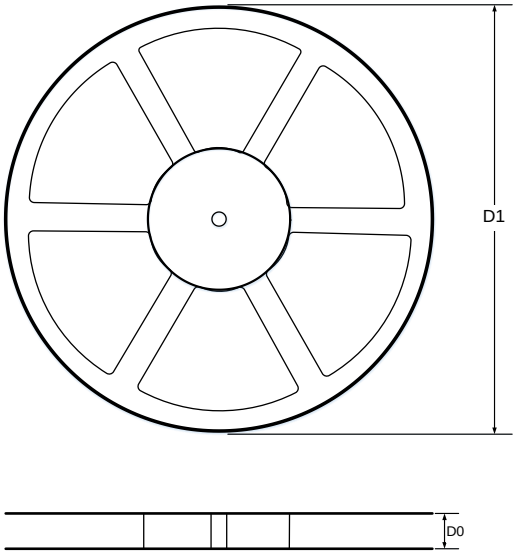


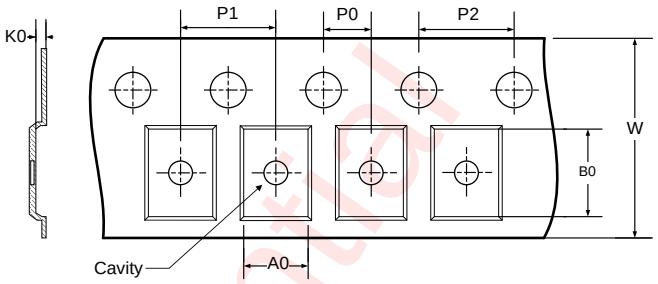
Figure 13 PCB layout example

Tape And Reel Information

REEL DIMENSIONS

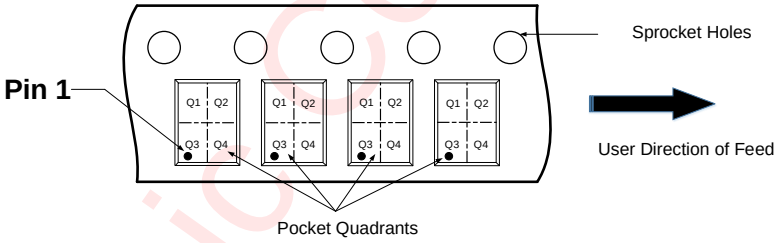


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



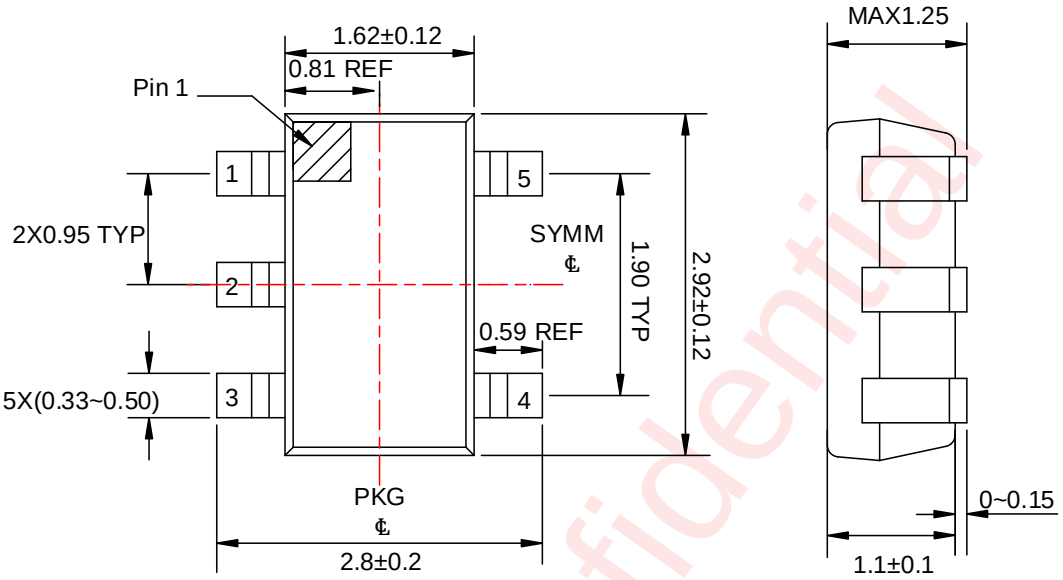
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

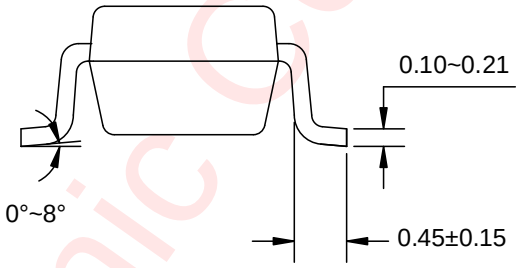
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

All dimensions are nominal

Package Description



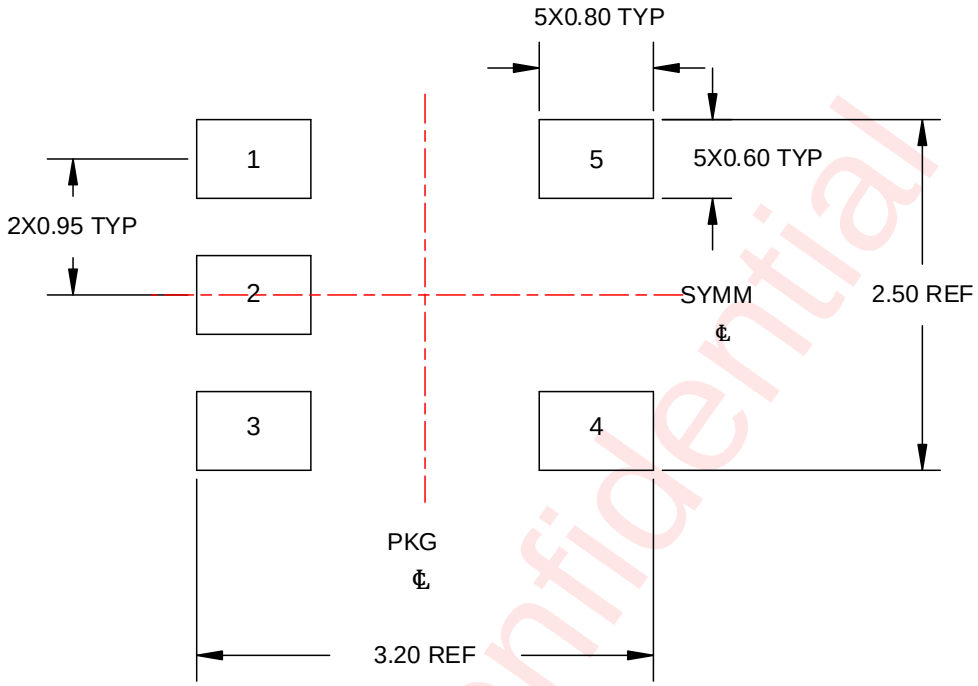
Top View **Side View**

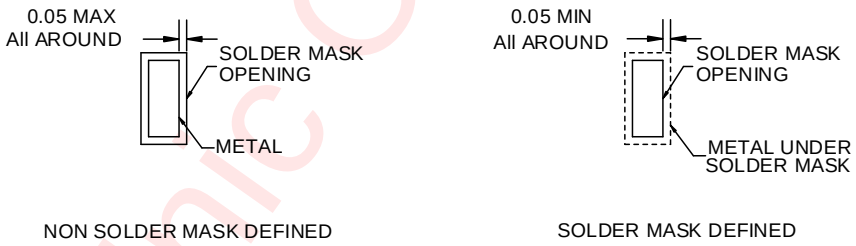


Side View

Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov. 2025	Officially released

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