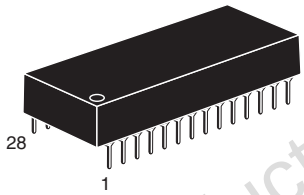
M48Z35AV

5.0 V or 3.3 V, 256 Kbit (32 Kbit x 8) ZEROPOWER® SRAM

Not recommended for new design

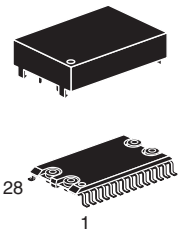
Features

- Integrated, ultra low power SRAM, power-fail control circuit, and battery
- READ cycle time equals WRITE cycle time
- Battery low flag ($\overline{BOK}$)
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltage:
  (V_{PFD} = power-fail deselect voltage)
  - M48Z35AV: 2.7 V ≤ V_{PFD} ≤ 3.0 V
- Self-contained battery in the CAPHAT™ DIP package
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- Pin and function compatible with JEDEC standard 32 Kbit x 8 SRAMs
- SOIC package provides direct connection for a SNAPHAT® top which contains the battery
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28
Battery CAPHAT™

SNAPHAT®
battery



SOH28

This is information on a product still in production but not recommended for new designs. www.st.com

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1 Description

The M48Z35AV ZEROPOWER® RAM is a 32 Kbit x 8, non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery-backed memory solution.

The M48Z35AV is a non-volatile pin and function equivalent to any JEDEC standard 32 K x8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed. The 28-pin 600 mil DIP CAPHAT™ houses the M48Z35AV silicon with a long life lithium button cell in a single package.

The 28-pin, 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in tape & reel form.

For the 28-lead SOIC, the battery package (e.g. SNAPHAT) part number is “M4Z28-BR00SH1.”

Figure 1. Logic diagram

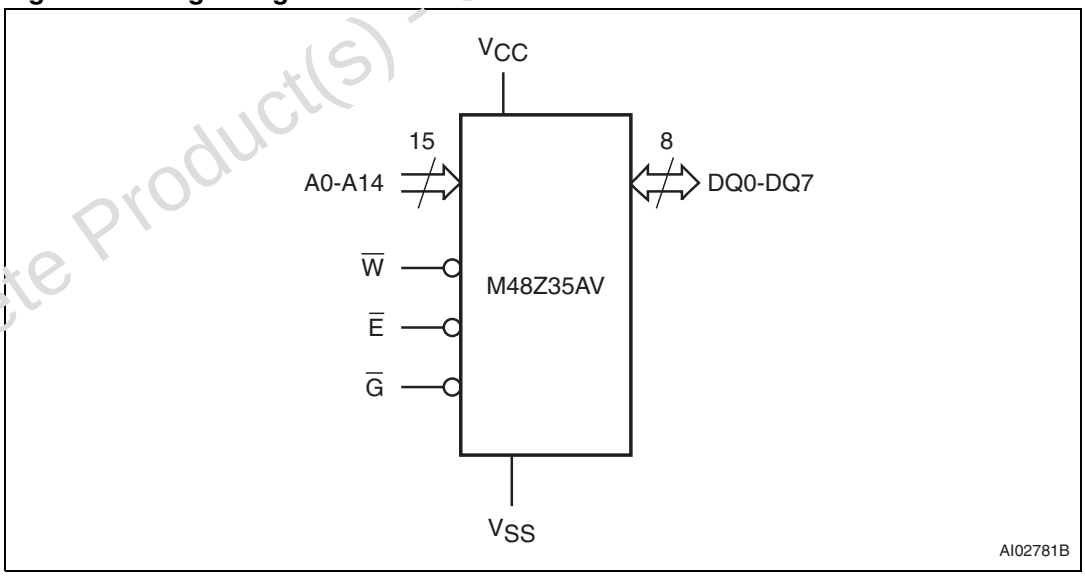


Table 1. Signal names

A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. DIP connections

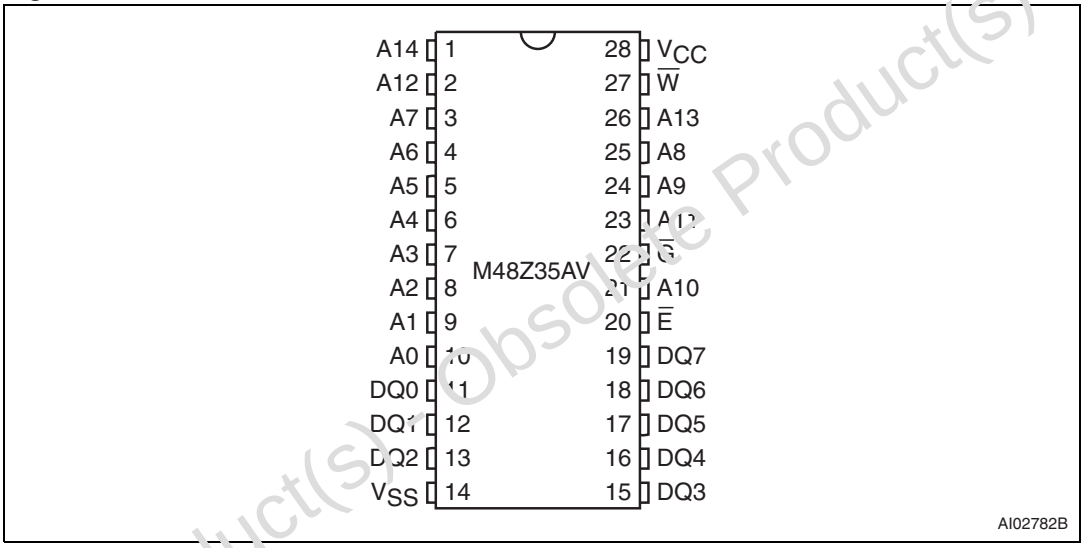


Figure 3. SOIC connections

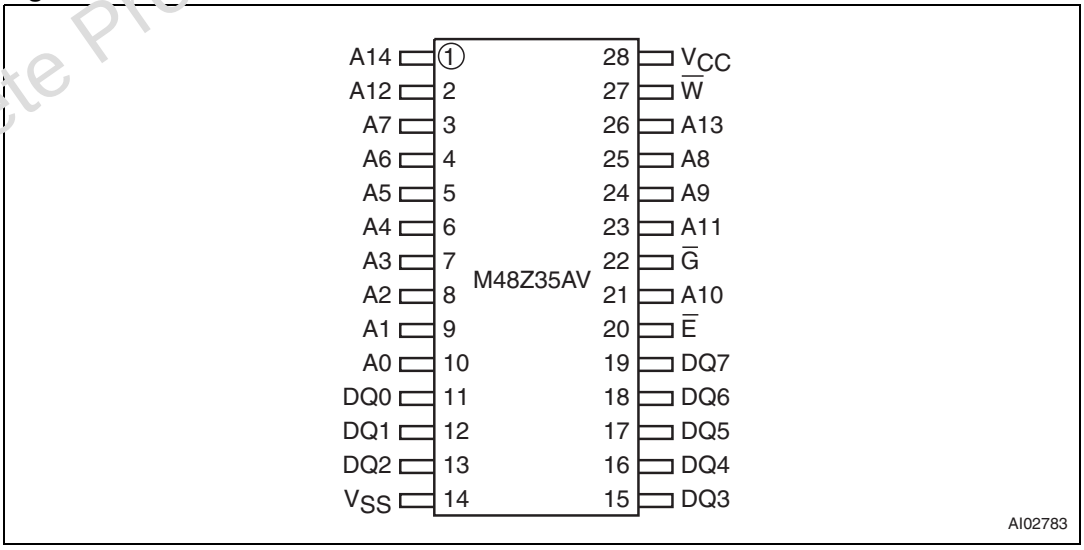
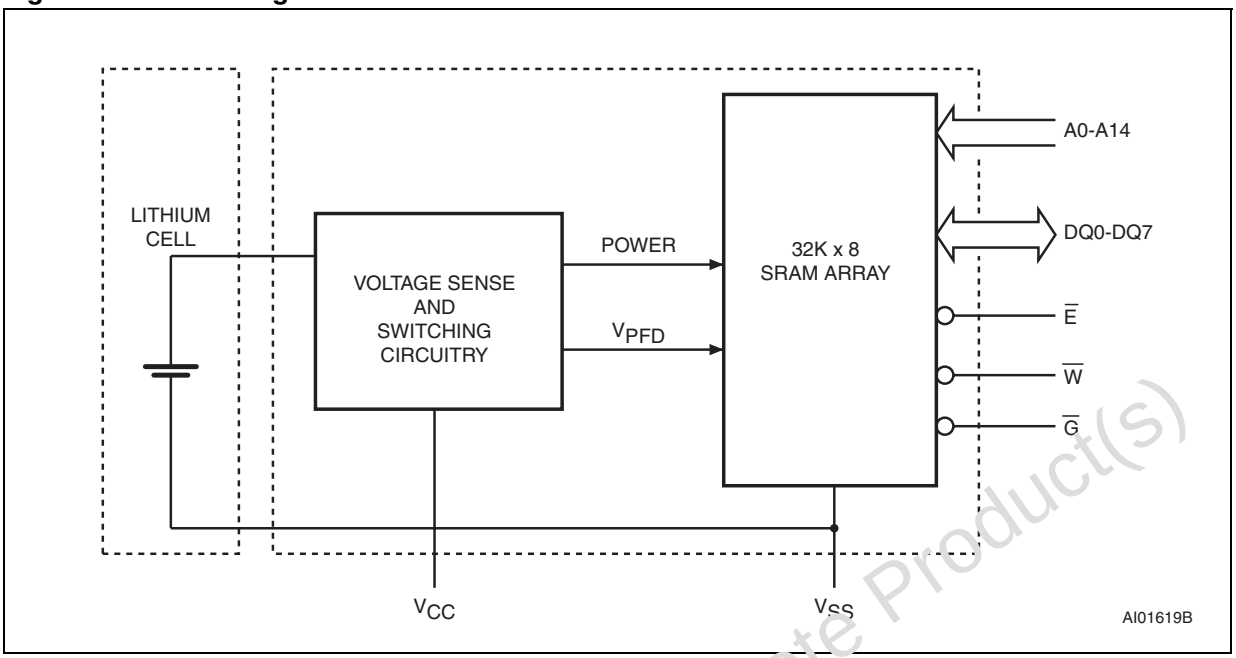


Figure 4. Block diagram



2 Operating modes

The M48Z35AV also has its own power-fail detect circuit. The control circuitry constantly monitors the single power supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately V_{SO}, the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. See *Table 10 on page 17* for details.

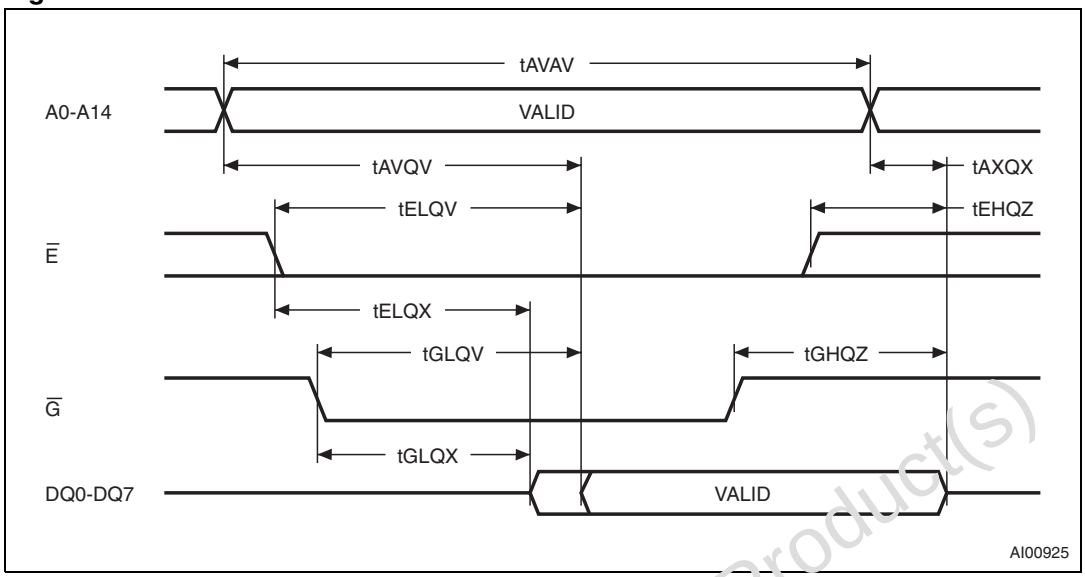
Note: X = V_{IH} or V_{IL}; V_{SO} = Battery backup switchover voltage.

2.1 READ mode

The M48Z35AV is in the READ mode whenever $\overline{W}$ (WRITE enable) is high, $\overline{E}$ (chip enable) is low. The device architecture allows ripple-through access of data from eight of 264,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 5. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = High.

Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48Z35AV –100		Unit
		Min	Max	
t_{AVAV}	READ cycle time	100		ns
t_{AVQV}	Address valid to output valid		100	ns
t_{ELQV}	Chip enable low to output valid		100	ns
t_{GLQV}	Output enable low to output valid		50	ns
t_{ELQX}[2]	Chip enable low to output transition	10		ns
t_{GLQX}[2]	Output enable low to output transition	5		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		50	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		40	ns
t_{AXQX}	Address transition to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF (see *Figure 10 on page 15*).

2.2 WRITE mode

The M48Z35AV is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. WRITE enable controlled, WRITE mode AC waveforms

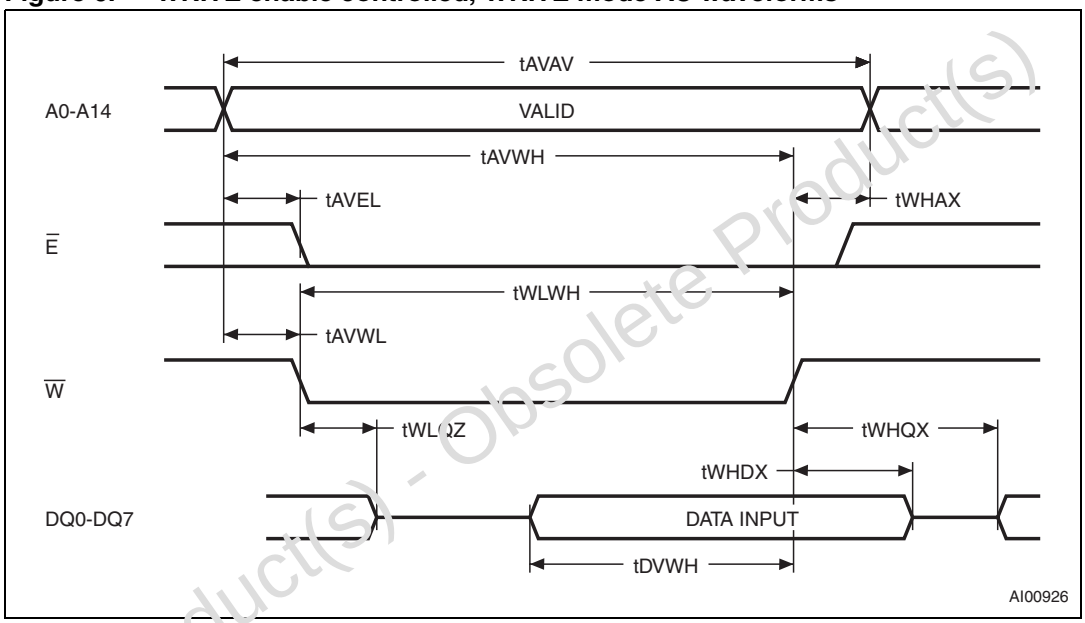


Figure 7. Chip enable controlled, WRITE mode AC waveforms

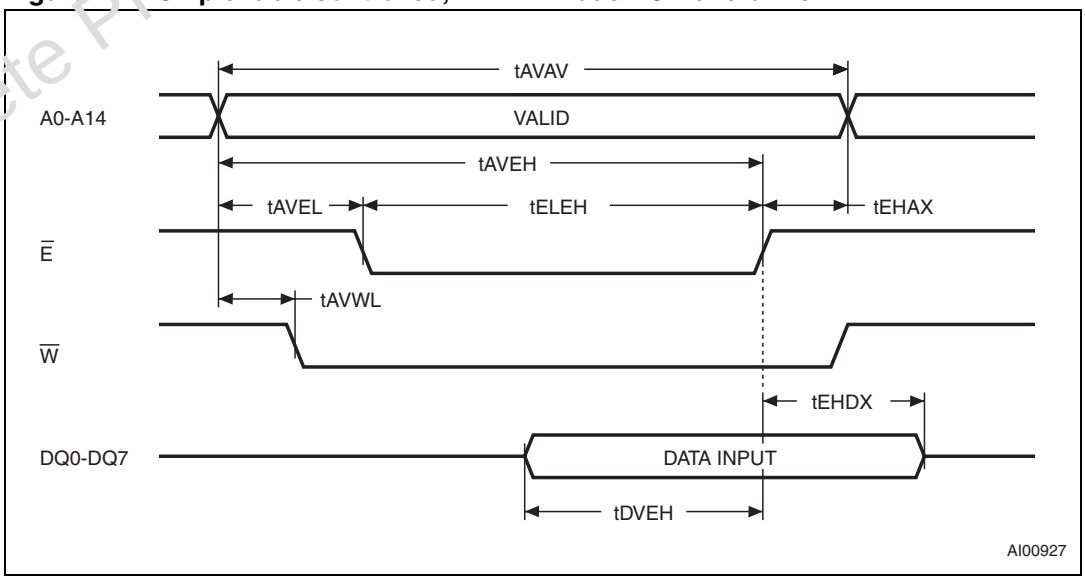


Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48Z35AV		Unit
		–100		
		Min	Max	
t_{AVAV}	WRITE cycle time	100		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	WRITE enable pulse width	80		ns
t_{ELEH}	Chip enable low to chip enable high	80		ns
t_{WHAX}	WRITE enable high to address transition	10		ns
t_{EHAX}	Chip enable high to address transition	10		ns
t_{DVWH}	Input valid to WRITE enable high	50		ns
t_{DVEH}	Input valid to chip enable high	50		ns
t_{WHDX}	WRITE enable high to input transition	5		ns
t_{EHDX}	Chip enable high to input transition	5		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		50	ns
t_{AVWH}	Address valid to WRITE enable high	80		ns
t_{AVEH}	Address valid to chip enable high	80		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF (see *Figure 10 on page 15*).
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48Z35AV operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z35AV may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

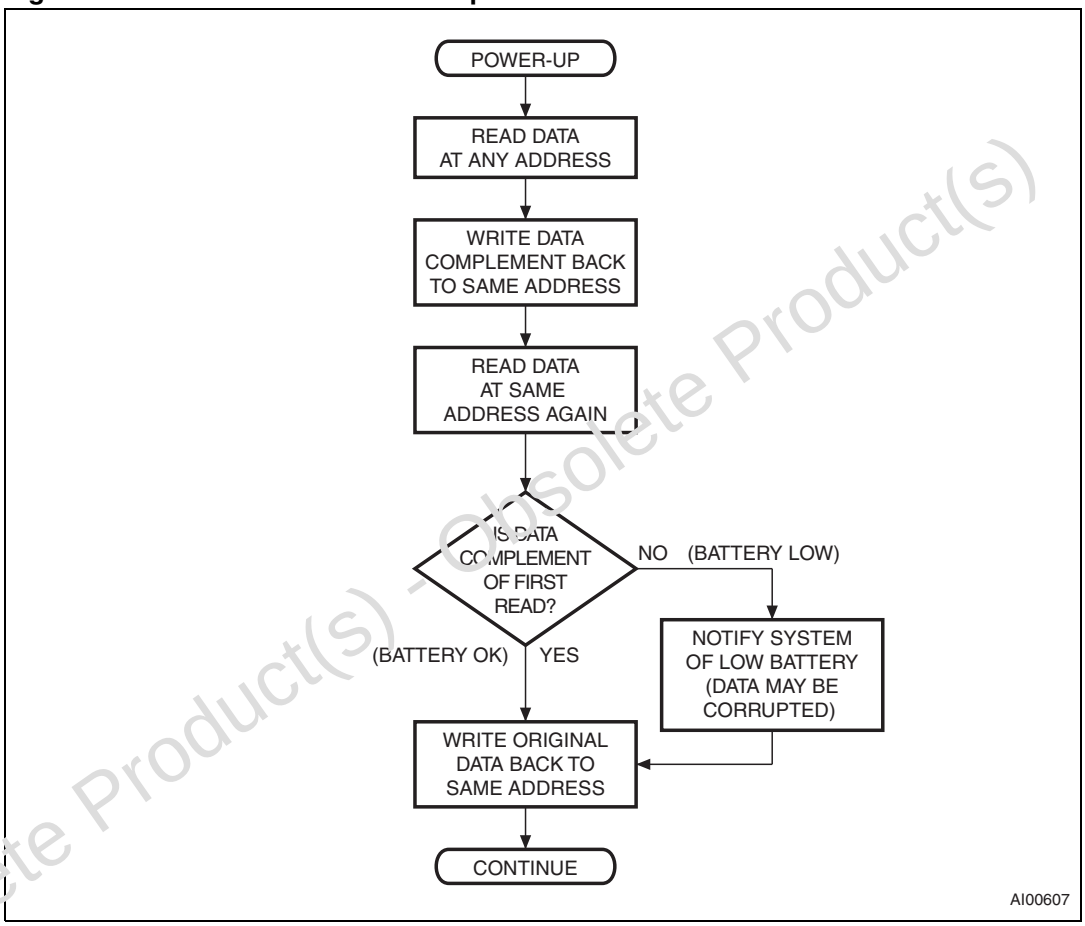
When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z35AV for an accumulated period of at least 10 years (at 25°C) when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min) plus t_{REC}(min). Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

Also, as V_{CC} rises, the battery voltage is checked. If the voltage is less than approximately 2.5 V, an internal battery not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first WRITE attempted will be blocked. The flag is automatically cleared after the first WRITE, and normal RAM operation resumes. *Figure 8* illustrates how a $\overline{BOK}$ check routine could be structured.

For more information on battery storage life refer to the application note AN1012.

Figure 8. $\overline{BOK}$ check routine example

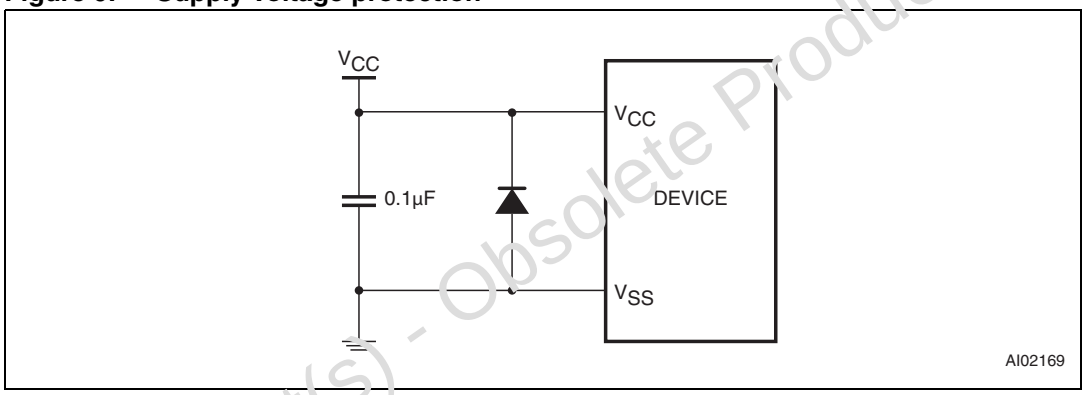


2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (see *Figure 9*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

Figure 9. Supply voltage protection



3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature		0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	SNAPHAT® top	–40 to 85	°C
		CAPHAT® DIP	–40 to 85	°C
		SOH28	–55 to 125	°C
T_{SLD} (1)(2)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to 4.6	V
V_{CC}	Supply voltage		–0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For DIP package, soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.
2. For SOH28 package, lead-free (Pb-free) lead finish: Reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

4 DC and AC parameters

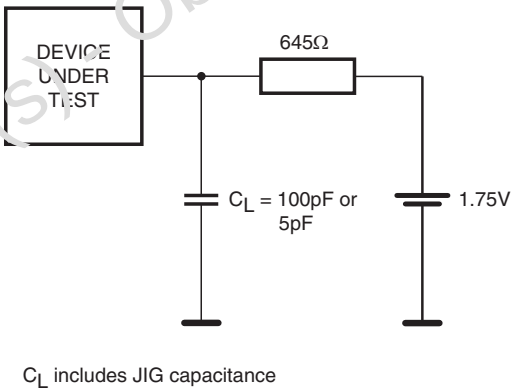
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in *Table 6: Operating and AC measurement conditions*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

Parameter	M48Z35AV	Unit
Supply voltage (V_{CC})	3.0 to 3.6	V
Ambient operating temperature (T_A)	0 to 70	°C
Load capacitance (C_L)	50	pF
Input rise and fall times	≤ 5	ns
Input pulse voltages	0 to 3	V
Input and output timing ref. voltages	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 10. AC measurement load circuit



Note: 50 pF for M48Z35AV.

Table 7. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance	-	10	pF
C_{IO}(3)	Input / output capacitance	-	10	pF

1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 8. DC characteristics

Symbol	Parameter	Test condition(1)	Min	Max	Unit
I_{LI}(2)	Input leakage current	0 V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}(2)	Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply current	Outputs open		50	mA
I_{CC1}	Supply current (TTL standby)	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply current (CMOS standby)	$\overline{E}$ = V_{CC} – 0.2 V		3	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1 mA	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. Outputs deselected.

Figure 11. Power down/up mode AC waveforms

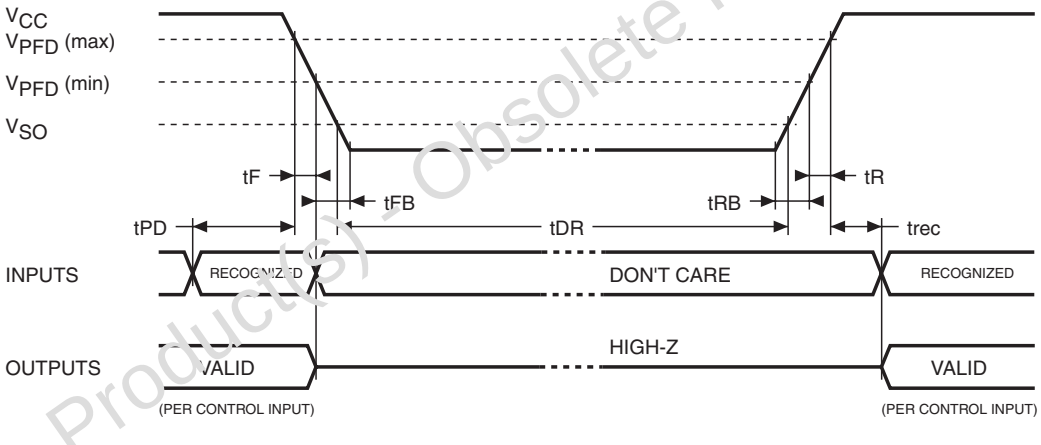


Table 9. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{rec}	V_{PFD} (max) to inputs recognized	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 10. Power down/up trip points DC characteristics

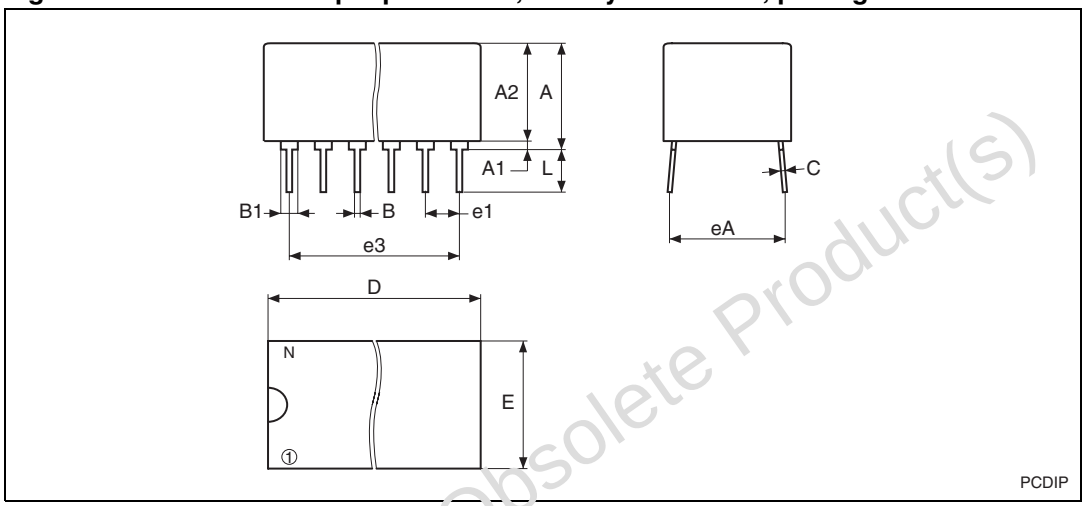
Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	2.7	2.9	3.0	V
V_{SO}	Battery backup switchover voltage		V_{PFD} – 100 mV		V
t_{DR}[3]	Expected data retention time	10			Years

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 3.0 to 3.6 V (except where noted).
3. At 25 °C, V_{CC} = 0 V.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 12. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline

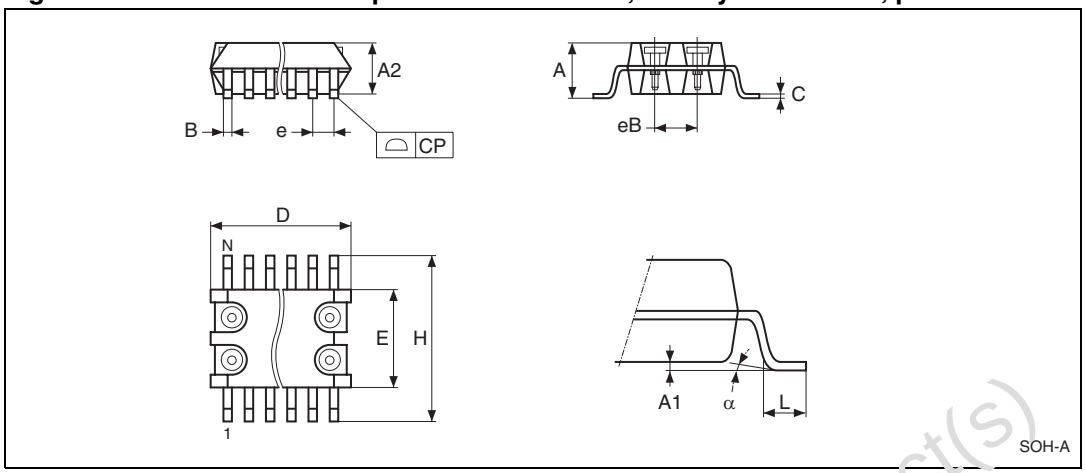


Note: Drawing is not to scale.

Table 11. PMDIP28 – 28-pin plastic DIP, battery CAPHAT™, pack. mech. data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3	33.02			1.3		
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

Figure 13. SOH28 – 28-lead plastic small outline, battery SNAPHAT®, pack. outline

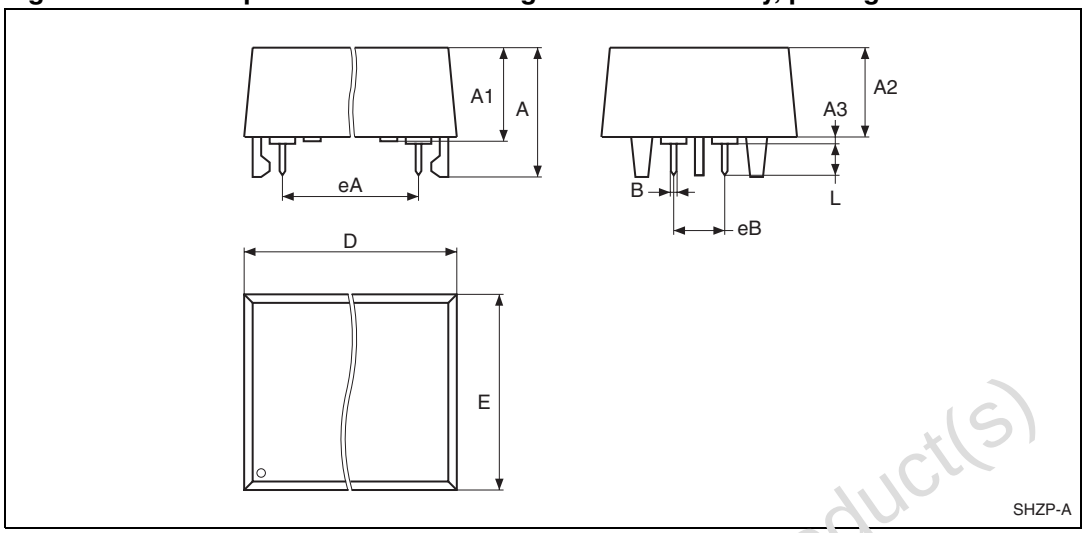


Note: Drawing is not to scale.

Table 12. SOH28 – 28-lead plastic small outline, battery SNAPHAT®, pack. mech. data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 14. SH – 4-pin SNAPHAT® housing for 48 mAh battery, package outline

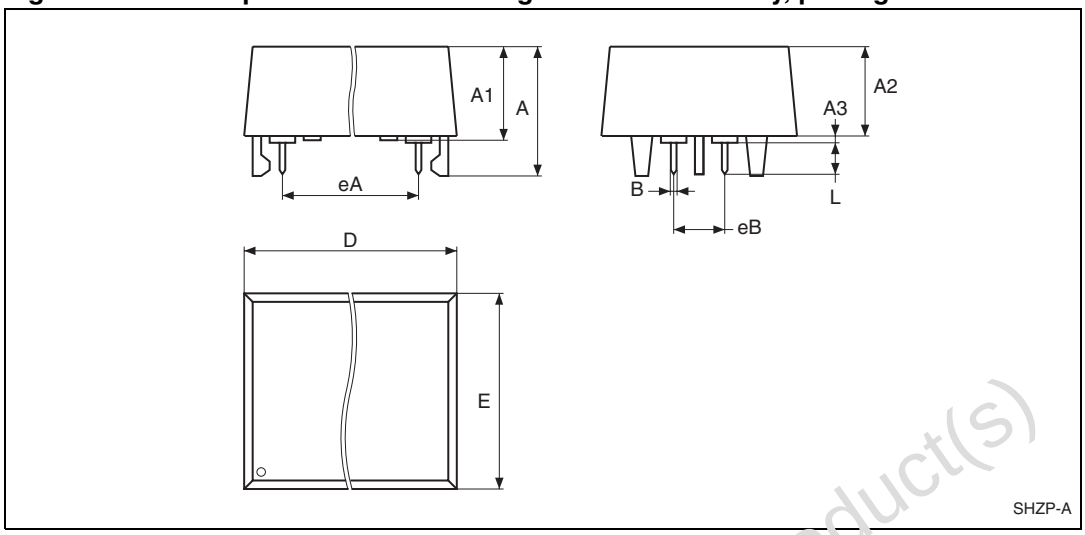


Note: Drawing is not to scale.

Table 13. SH – 4-pin SNAPHAT® housing for 48 mAh battery, pack. mech. data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 15. SH – 4-pin SNAPHAT® housing for 120 mAh battery, package outline



Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT® housing for 120 mAh battery, pack. mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

6 Part numbering

Table 15. Ordering information scheme

Example: M48Z 35AV –10 MH 1 E

Device type

M48Z

Supply voltage and write protect voltage

35AV(1) = V_{CC} = 3.0 to 3.6 V; V_{PFD} = 2.7 to 3.0 V

Speed

–10 = 100 ns (35AV)

Package

PC = PCDIP28
MH(2) = SOH28

Temperature range

1 = 0 to 70 °C

Shipping method

For SOH28:
E = Lead-free package (ECOPACK®), tubes
F = Lead-free package (ECOPACK®), tape & reel

For PCDIP28:
blank = tubes

1. Not recommended for new design. ST recommends the M48T35AV.
2. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number "M4Zxx-BR00SH1" in plastic tubes (see *Table 16*).

Caution: Do not place the SNAPHAT battery package "M4Zxx-BR00SH1" in conductive foam as it will drain the lithium button-cell battery.

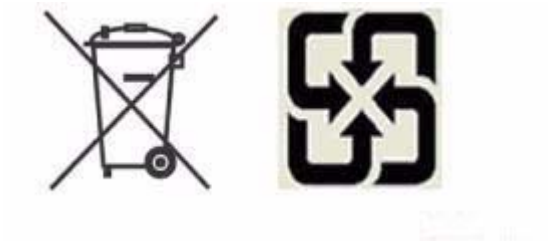
For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 16. SNAPHAT battery table®

Part number	Description	Package
M4Z28-BR00SH1	Lithium battery (48 mAh) SNAPHAT®	SH
M4Z32-BR00SH1	Lithium battery (120 mAh) SNAPHAT®	SH

7 Environmental information

Figure 16. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

8 Revision history

Table 17. Document revision history

Date	Revision	Changes
Sep-1999	1	First issue
20-Apr-2000	1.1	SH and SH28 packages for 2-pin and 2-socket removed
22-Jun-2001	2	Reformatted; added temperature information (*Table 7*, *8*, *3*, *4*, *9*, *10*)
05-Jul-2001	2.1	Removed reference to “Crystal” in Features Summary
17-Dec-2001	2.2	Changed speed grade designator to “–10” (*Table 15*)
29-May-2002	2.3	Modified reflow time and temperature footnotes (*Table 5*)
03-Oct-2002	2.4	Update V_{CC} for supply voltage (*Table 5*)
07-Nov-2002	2.5	Update absolute maximum ratings (*Table 5*)
02-Apr-2003	3	v2.2 template applied; test condition updated (*Table 10*)
24-Mar-2004	4	Reformatted; updated lead-free information (*Table 5*, *15*)
09-Jun-2005	5	Removal of SNAPHAT®, industrial temperature sales types (*Table 3*, *4*, *5*, *6*, *8*, *9*, *10*, *15*)
05-Nov-2007	6	Reformatted document; added lead-free second level interconnect information to cover page and *Section 5: Package mechanical data*; removed M48Z35AY and references throughout document; updated *Table 2*, *3*, *4*, *5*, *6*, *8*, *9*, *15* and *16*.
11-Mar-2009	7	Updated *Table 5* and text in *Section 5: Package mechanical data*; added *Section 7: Environmental information*; minor reformatting.
20-Oct-2010	8	Device is not recommended for new design; updated *Table 5*, *11*, *15*; reformatted document.
07-Jun-2011	9	Updated footnote *1* of *Table 5: Absolute maximum ratings*; updated *Section 7: Environmental information*.

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