

FEATURES

4 differential transmitters

4 differential receivers

2 observation receivers with 2 inputs each

Tunable range: ADRV9020: 650 MHz to 6000 MHz

Maximum receiver bandwidth: 200 MHz

Maximum transmitter bandwidth: 200 MHz

Maximum transmitter synthesis bandwidth: 450 MHz

Maximum observation receiver bandwidth: 450 MHz

Fully integrated independent fractional-N radio frequency synthesizers

Fully integrated clock synthesizer

Multichip phase synchronization for all local oscillators and baseband clocks

Support for Time-Division-Duplex applications

25 Gbps JESD204B/JESD204C digital interface

APPLICATIONS

3G/4G/5G TDD Massive MIMO and Macro Basestations

GENERAL DESCRIPTION

The ADRV9020 is a highly integrated, radio frequency (RF) agile transceiver offering four independently controlled transmitters, dedicated observation receiver inputs for monitoring each transmitter channel, four independently controlled receivers, integrated synthesizers, and digital signal processing functions to provide a complete transceiver solution. The device provides the high radio performance and low power consumption demanded by cellular infrastructure applications such as small cell base station radios, macro 3G/4G/5G systems, and massive multiple in/multiple out (MIMO) base stations.

The receiver subsystem consists of four independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The four independent transmitters use an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise. The device also includes two wide bandwidth, time shared observation path

receivers with two inputs each for monitoring transmitter outputs. The complete transceiver subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, eliminating the need for these functions in the digital baseband. Other auxiliary functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) that provide an array of digital control options are also integrated.

To achieve the high level of RF performance, the transceiver includes five fully integrated phase-locked loops (PLLs). Two PLLs provide high performance, low power fractional-N RF synthesis for the transmitter and receiver signal paths. One fully integrated PLL also supports an independent local oscillator (LO) mode for the observation receiver. Another PLL generates the clocks needed for the converters and digital circuits, and a fifth PLL provides the clock for the serial data interface. A multichip synchronization mechanism synchronizes the phase of all LOs and baseband clocks between multiple ADRV9020 chips. All voltage controlled oscillators (VCOs) and loop filter components are integrated and adjustable through the digital control interface.

The serial data interface consists of four serializer lanes and four deserializer lanes. The interface supports both the JESD204B and JESD204C standards, operating at data rates up to 24.33Gbps. The interface also supports interleaved mode for lower bandwidths, thus reducing the number of high speed data interface lanes to one. Both fixed and floating-point data formats are supported. The floating-point format allows internal automatic gain control (AGC) to be invisible to the demodulator device.

The ADRV9020 is powered directly from 1.0 V, 1.3 V, and 1.8 V regulators and is controlled via a standard SPI serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9020 is packaged in a 14mm × 14 mm, 289-ball chip scale ball grid array (CSP_BGA).

Rev. Pr1

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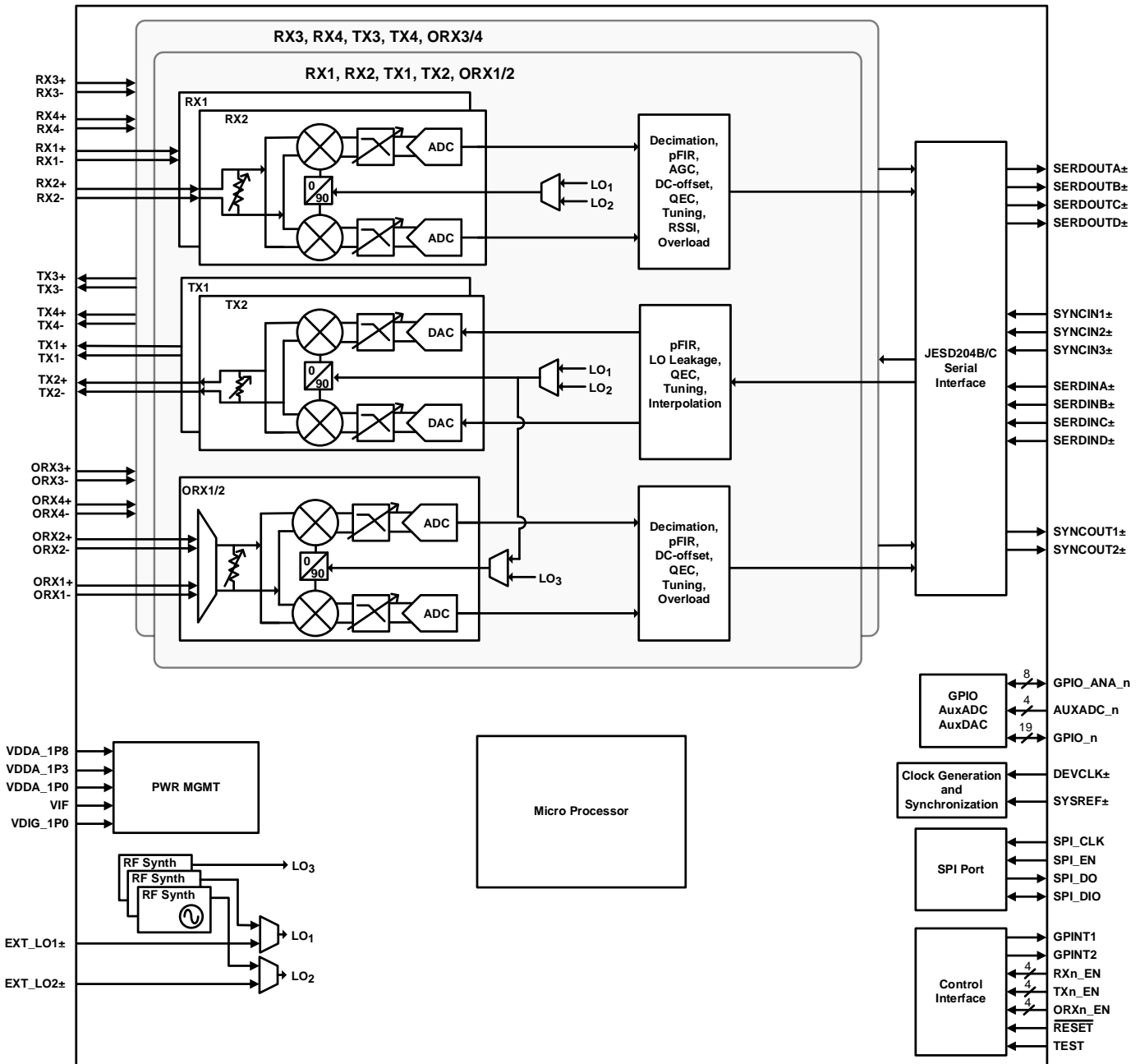


Figure 1 ADRV9020 Functional Block Diagram

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REVISION HISTORY

8/2019 — Rev PrI

Data graphs added.

SPECIFICATIONS

Electrical characteristics at ambient temperature range. Power supplies are as follows: VDDA_1P8 = 1.8 V, VIF = 1.8 V, VDDA_1P3 = 1.3 V, VDDA_1P0 = 1.0 V, and VDIG_1P0 = 1.0 V. VDDA_1P8 represents VCONV1_1P8, VCONV2_1P8, VANA1_1P8, VANA2_1P8, VANA3_1P8, VANA4_1P8, and VJVCO_1P8. VDDA_1P3 represents VANA1_1P3, VANA2_1P3, VCONV1_1P3, VCONV2_1P3, VRFVCO1_1P3, VRFVCO2_1P3, VAUXVCO_1P3, VCLKVCO_1P3, VRFSYN1_1P3, VRFSYN2_1P3, VCLKSYN_1P3, VAUXSYN_1P3, VRXLO_1P3, and VTXLO_1P3. VDDA_1P0 represents VJSYN_1P0, VDES_1P0, VTT_DES, and VSER_1P0. All RF specifications are based on measurements that include printed circuit board (PCB) and matching circuit losses unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS (Tx)						
Center Frequency		650		6000	MHz	ADRV9020
Tx Synthesis Bandwidth				450	MHz	Wider bandwidth for use in digital processing algorithms
Tx Large Signal Bandwidth				200	MHz	Zero-IF Mode
Peak-to-Peak Gain Deviation			1.0		dB	450 MHz BW, includes compensation by programmable finite impulse response (FIR) filter
			0.1		dB	Any 20 MHz BW span, includes compensation by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz BW
Maximum Output Power						0 dBFS, 1 MHz signal input, 50 Ω load, 0 dB Tx attenuation
800 MHz			6.7		dBm	
2600 MHz			6.3		dBm	
3800 MHz			6.4		dBm	
4800 MHz			6.1		dBm	
Power Control Range			32		dB	
Power Control Resolution			0.05		dB	
Attenuation Accuracy						
Integral Nonlinearity (Gain)	INL		0.1		dB	Valid over full power control range for any 4 dB step
Differential Nonlinearity (Gain)	DNL		±0.04		dB	Monotonic
Output Power Temperature Slope			-4.5		mdB/°C	Valid over full power control range
LO Delay Temperature Slope			1.05		ps/°C	Valid over full power control range
Adjacent Channel Leakage Power Ratio (ACLR) Long Term Evolution (LTE)						20 MHz LTE at -12 dBFS
800 MHz			-68		dB	
2600 MHz			-66		dB	
3800 MHz			-65		dB	
4800 MHz			-65		dB	
In-Band Noise Floor			-154.5		dBFS/Hz	0dB attenuation. In-band noise falls 1dB for each dB of attenuation for attenuation settings between 0 and 20dB.
Interpolation Images			-76		dBc	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Tx to Tx Isolation – All Tx Output Effects on all other Tx Outputs						
800 MHz			78		dB	
2600 MHz			77		dB	
3800 MHz			71		dB	
4800 MHz			70		dB	
Image Rejection						
Within Large Signal Bandwidth						QEC active up to 20 dB of attenuation, CW tone swept across the large signal BW
800 MHz			76		dB	
2600 MHz			73		dB	
3800 MHz			65		dB	
4800 MHz			64		dB	
Beyond Large Signal Bandwidth						Assumes that distortion power density is 25dB below desired power density
800 MHz			40		dB	
2600 MHz			34		dB	
3800 MHz			37		dB	
4800 MHz			37		dB	
Output Impedance	Z _{OUT}		50		Ω	Differential – nominal
Maximum Output Load Voltage Standing Wave Ratio (VSWR)				3		Maximum value to ensure adequate calibration
Output Return Loss			10		dB	
Output Third-Order Intercept Point	OIP3					0 dB Tx attenuation
800 MHz			29		dBm	
2600 MHz			28		dBm	
3800 MHz			26.5		dBm	
4800 MHz			29		dBm	
Carrier Leakage						With LO leakage correction active, 0dB Tx attenuation. Scales dB-for-dB with attenuation
Carrier Offset from LO						
800 MHz LO			-84		dBFS /MHz	
2600 MHz LO			-83		dBFS /MHz	
3800 MHz LO			-84		dBFS /MHz	
4800 MHz LO			-84		dBFS /MHz	
Error Vector Magnitude	EVM					PLL optimized for narrow-band noise, measured using LTE 20 MHz signal
800 MHz LO			0.38		%	50 kHz PLL bandwidth
2600 MHz LO			0.44		%	500 kHz PLL bandwidth
3800 MHz LO			0.53		%	200 kHz PLL bandwidth
4800 MHz LO			0.63		%	400 kHz PLL bandwidth
Transmitter Time Division Duplex (TDD) Parameters						

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Time from SPI_EN Going High to Change in Tx Attenuation	t _{SCH}		12		ns	
Time Between Consecutive Microattenuation Steps	t _{ACh}		20		ns	A large change in attenuation may be broken up into a series of smaller attenuation changes
Attenuation Overshoot During Transition			0.1		dB	
Change in Attenuation per Microstep			0.1		dB	
RECEIVERS (Rx)						
Center Frequency		650		6000	MHz	ADRV9020
Gain Range			30		dB	
Attenuation Accuracy						
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
Residual Gain Step Error			1		dB	Attenuator steps from 6 dB to 30 dB
Gain Temperature Slope			0.1		dB	
Internal LO Delay Temperature Slope			-6.4		mdB/°C	
Frequency Response						
Peak-to-Peak Gain Deviation			1		dB	200 MHz BW, includes compensation by programmable FIR filter
Peak-to-Peak Gain Deviation			0.2		dB	Any 20 MHz span, includes compensation by programmable FIR filter
Rx Bandwidth				200	MHz	Zero-IF mode
Rx Alias Band Rejection		80			dB	Due to digital filters
Maximum Useable Input Level	P _{HIGH}		-11		dBm	This CW signal level corresponds to the input power that produces -2 dBFS at the digital output with at 0 dB channel attenuation
800 MHz			-12.4		dBm	
2600 MHz			-11.9		dBm	
3800 MHz			-11.0		dBm	
4800 MHz			-12.0		dBm	
Maximum Source VSWR				3		
Input Impedance	Z _{IN}		100		Ω	Differential
Input Port Return Loss			10		dB	Unmatched differential port return loss
Noise Figure	NF					0 dB attenuation, at Rx port
800 MHz			11		dB	
2600 MHz			11.9		dB	
3800 MHz			12.8		dB	
4800 MHz			13.3		dB	
Noise Figure Ripple			1.5		dB	At band edge
Second-Order Input Intermodulation Intercept Point	IIP2					0 dB attenuation, complex
800 MHz			65		dBm	
2600 MHz			65		dBm	
3800 MHz			65		dBm	
4800 MHz			62		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Wide-band Third-Order Input Intermodulation Intercept Point, Difference Product	WB-IIP3 _{DIFF}					Two tones near the band edge. Test condition: P _{HIGH} -9dB/tone.
800 MHz			15		dBm	
2600 MHz			17		dBm	
3800 MHz			17		dBm	
4800 MHz			17		dBm	
Mid-band Third-Order Input Intermodulation Intercept Point, Difference Product	MB-IIP3 _{DIFF}					Two tones near middle of the band. Test condition: P _{HIGH} -9 dB/tone.
800 MHz			18		dBm	
2600 MHz			21		dBm	
3800 MHz			22		dBm	
4800 MHz			22		dBm	
Wide-band Third-Order Input Intermodulation Intercept Point, Sum Product	WB-IIP3 _{SUM}					Two tones approximately BW/6 offset from the LO. Test condition: P _{HIGH} -9 dB/tone.
800 MHz			17		dBm	
2600 MHz			20		dBm	
3800 MHz			23		dBm	
4800 MHz			23		dBm	
Third-order Harmonic Distortion	HD3		-72		dBc	P _{HIGH} -3 dB CW signal, HD3 product occurring anywhere in-band
Image Rejection						Quadrature error correction (QEC) active, within 200 MHz Rx BW
800 MHz			75		dB	
2600 MHz			75		dB	
3800 MHz			75		dB	
4800 MHz			75		dB	
Rx to Rx Signal Isolation						
800 MHz			75		dB	
2600 MHz			70		dB	
3800 MHz			65		dB	
4800 MHz			62		dB	
Rx Band Spurs Referenced to RF Input at Maximum Gain			-95		dBm	No more than one spur at this level per 10 MHz of Rx BW; excludes harmonics of the reference clock
Rx Input LO Leakage at Maximum Gain						Leakage decreased dB for dB with attenuation for first 12 dB
800 MHz			-68		dBm	
2600 MHz			-65		dBm	
3800 MHz			-65		dBm	
4800 MHz			-58		dBm	
Tx to Rx Signal Isolation – All Tx Output Effects on all Rx Inputs						
800 MHz			80		dB	
2600 MHz			75		dB	
3800 MHz			65		dB	
4800 MHz			65		dB	
OBSERVATION RECEIVER (ORx) Center Frequency						

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
		650		6000	MHz	ADRV9020
Gain Range			30		dB	
Attenuation Accuracy						
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 30 dB
Peak-to-Peak Gain Deviation			1		dB	450 MHz RF BW, compensation by programmable FIR filter
Peak-to-Peak Gain Deviation			0.1		dB	Any 20 MHz BW span, compensation by programmable FIR filter
Deviation from Linear Phase			1		Degrees	450 MHz RF BW
ORx Bandwidth				450	MHz	
ORx Alias Band Rejection		60			dB	Due to digital filters
Maximum Useable Input Level	P _{HIGH}		-11		dBm	This CW signal level corresponds to the input power that produces -2 dBFS at the digital output with at 0 dB channel attenuation
Input Source VSWR				3		
Input Impedance	Z _{IN}		100		Ω	Differential
Input Port Return Loss			10		dB	Unmatched differential port return loss
Integrated Noise						
450 MHz BW			-58.5		dBFS	Sample rate at maximum value Integrated from 500 kHz to 225 MHz, no input signal
491.52 MHz BW (Nyquist)			-57.5		dBFS	Sample rate at maximum value Integrated from 500 kHz to 245.76 MHz, no input signal
Second-Order Input Intermodulation Intercept Point	IIP ₂					Maximum ORx gain. Test condition: P _{HIGH} -11 dB/tone.
800 MHz			55		dBm	
2600 MHz			55		dBm	
3800 MHz			48		dBm	
4800 MHz			45		dBm	
Third-Order Input Intermodulation Intercept Point						Maximum ORx gain. Test condition: P _{HIGH} -11 dB/tone.
Narrow-Band	IIP _{3NB}					IM3 product < 130 MHz at baseband. Test condition: P _{HIGH} -11 dB/tone, 491.52 MSPS
800 MHz			13.6		dBm	
2600 MHz			16.5		dBm	
3800 MHz			18		dBm	
4800 MHz			18		dBm	
Wide-Band	IIP _{3WB}					IM3 products > 130 MHz at baseband. Test condition: P _{HIGH} -11 dB/tone, 491.52 MSPS
800 MHz			7.8		dBm	
2600 MHz			11		dBm	
3800 MHz			13		dBm	
4800 MHz			13		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
3rd Order Intermodulation Product						
Narrow Band	IM3 _{NB}					IM3 product < 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-74		dBc	
2600 MHz			-78.6		dBc	
3800 MHz			-80.4		dBc	
4800 MHz			-79.8		dBc	
Wide Band	IM3 _{WB}					IM3 product > 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-62.4		dBc	
2600 MHz			-67.6		dBc	
3800 MHz			-70.4		dBc	
4800 MHz			-69.8		dBc	
5th Order Intermodulation Product						
Narrow Band	IM5 _{NB}					IM5 product < 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-83		dBc	
2600 MHz			-84		dBc	
3800 MHz			-80		dBc	
4800 MHz			-78		dBc	
Wide Band	IM5 _{WB}					IM5 product > 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-83		dBc	
2600 MHz			-85		dBc	
3800 MHz			-80		dBc	
4800 MHz			-77		dBc	
7th Order Intermodulation Product						
Narrow Band	IM7 _{NB}					IM7 product < 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-74		dBc	
2600 MHz			-75		dBc	
3800 MHz			-73		dBc	
4800 MHz			-78		dBc	
Wide Band	IM7 _{WB}					IM7 product > 130 MHz at baseband. Test condition: 2 tones, each at P _{HIGH} -11 dB, 491.52 MSPS
800 MHz			-83		dBc	
2600 MHz			-83		dBc	
3800 MHz			-83		dBc	
4800 MHz			-85		dBc	
Spurious Free Dynamic Range	SFDR		64		dB	Non-intermodulation related spurs. Does not include harmonic distortion. Input set at P _{HIGH} -8 dB.
2nd Order Harmonic Distortion	HD2					Input set at P _{HIGH} -8 dB
In-band			-80		dBc	Inband HD falls within ±100MHz
Out-of-band			-73		dBc	Out of band HD falls with ±225 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments	
3rd Order Harmonic Distortion	HD3					Input set at P _{HIGH} -8 dB	
In-band			-70		dBc	Harmonic distortion falls within ±100 MHz	
Out-of-band				-65		dBc	Harmonic distortion falls within ±225 MHz
Image Rejection				75		dB	After online tone calibration, QEC active
Tx to ORx Signal Isolation – All Tx Output Effects on all ORx Inputs			75		dB		
LO SYNTHESIZER (LO1 and LO2)							
LO Frequency Step			7.3		Hz	1.6 GHz to 3.2 GHz, 245.76 MHz phase frequency detector (PFD) frequency	
LO Spectral Purity			-80		dBc	Integrated from 1 kHz to 100 MHz PLL BW optimized to minimize phase noise at offsets > 200 kHz PLL BW optimized for integrated phase noise and phase noise at offsets > 1 MHz and phase noise at offsets > 1 MHz	
Integrated Phase Noise							
Narrow Bandwidth Optimized							
800 MHz			0.12		°rms		
2600 MHz			0.66		°rms		
3800 MHz			0.53		°rms		
4800 MHz			0.91		°rms		
Wide Bandwidth Optimized							
800 MHz			0.07		°rms		
2600 MHz			0.17		°rms		
3800 MHz			0.26		°rms		
4800 MHz			0.30		°rms		
Spot Phase Noise - Narrowband							PLL optimized to minimize phase noise at offsets > 200 kHz
800 MHz LO							
100 kHz Offset			-115		dBc/Hz		
1 MHz Offset			-141		dBc/Hz		
10 MHz Offset			-162		dBc/Hz		
2600 MHz LO							
100 kHz Offset			-97		dBc/Hz		
1 MHz Offset			-124		dBc/Hz		
10 MHz Offset			-150		dBc/Hz		
3800 MHz LO							
100 kHz Offset			-100		dBc/Hz		
1 MHz Offset			-126		dBc/Hz		
10 MHz Offset			-149		dBc/Hz		
4800 MHz LO							
100 kHz Offset			-94		dBc/Hz		
1 MHz Offset			-120		dBc/Hz		
10 MHz Offset			-145		dBc/Hz		
Spot Phase Noise - Wideband						PLL BW optimized for integrated phase noise and phase noise at offsets > 1 MHz	
800 MHz LO							
100 kHz Offset			-114		dBc/Hz		

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
1 MHz Offset			-141		dBc/Hz	
10 MHz Offset			-162		dBc/Hz	
2600 MHz LO						
100 kHz Offset			-112		dBc/Hz	
1.0 MHz Offset			-120		dBc/Hz	
10 MHz Offset			-149		dBc/Hz	
3800 MHz LO						
100 kHz Offset			-104		dBc/Hz	
1 MHz Offset			-125		dBc/Hz	
10 MHz Offset			-149		dBc/Hz	
4800 MHz LO						
100 kHz Offset			-106		dBc/Hz	
1 MHz Offset			-117		dBc/Hz	
10 MHz Offset			-144		dBc/Hz	
AUXILIARY SYNTHESIZER	LO3					
LO Frequency Step			1.8		Hz	1.625 GHz to 3.25 GHz, 61.44 MHz PFD frequency
LO Spectral Purity			-65		dBc	$ f_{RFLO} - f_{AUXLO} > 15$ MHz
Integrated Phase Noise						Integrated from 1 kHz to 100 MHz, PLL bandwidth optimized for integrated phase noise
800 MHz LO			0.18		°rms	
2600 MHz LO			0.46		°rms	
3800 MHz LO			0.43		°rms	
4800 MHz LO			0.70		°rms	
Spot Phase Noise						
800 MHz LO						
100 kHz Offset			-112		dBc/Hz	
1 MHz Offset			-121		dBc/Hz	
10 MHz Offset			-141		dBc/Hz	
2600 MHz LO						
100 kHz Offset			-103		dBc/Hz	
1 MHz Offset			-114		dBc/Hz	
10 MHz Offset			-132		dBc/Hz	
3800 MHz LO						
100 kHz Offset			-104		dBc/Hz	
1 MHz Offset			-114		dBc/Hz	
10 MHz Offset			-128		dBc/Hz	
4800 MHz LO						
100 kHz Offset			-100		dBc/Hz	
1 MHz Offset			-110		dBc/Hz	
10 MHz Offset			-127		dBc/Hz	
LO PHASE SYNCHRONIZATION						
Initial Phase Sync Accuracy			0.9		ps	
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	1600		7600	MHz	Input frequency must be 2× the desired frequency for LO frequency ($f_{LO} \geq 1$ GHz and 4× the desired f_{LO} for $f_{LO} < 1$ GHz)
Input Signal Power		-6	0	6	dBm	50 Ω matching at the source
Input Signal Differential Phase Balance				15	Degrees	To ensure adequate quadrature error correction
Input Signal Differential Amplitude Balance				2	dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Signal Duty Cycle Error				2	%	
CLOCK SYNTHESIZER						
4915.2 MHz Sample Clock Integrated Phase Noise			0.69		°rms	1 kHz to 10 MHz, PLL bandwidth optimized for integrated phase noise PLL bandwidth optimized for integrated phase noise
Spot Phase Noise						
100 kHz Offset			-96		dBc/Hz	
1 MHz Offset			-113		dBc/Hz	
10 MHz Offset			-140		dBc/Hz	
3932.16 MHz Sample Clock Integrated Phase Noise			0.89		°rms	1 kHz to 10 MHz, PLL bandwidth optimized to minimize phase noise at offsets >200kHz PLL bandwidth optimized to minimize phase noise at offsets >200kHz
Spot Phase Noise						
100 kHz Offset			-91		dBc/Hz	
1 MHz Offset			-120		dBc/Hz	
10 MHz Offset			-143		dBc/Hz	
REFERENCE CLOCK (DEV_CLK_IN SIGNAL)						
Frequency Range		15		1000	MHz	AC-coupled, common-mode voltage internally supplied; for best spurious performance and to meet the specified PLL performance parameters, use a 1 V p-p input clock
Signal Level (Differential)		0.2		1.0	V p-p	
SYSTEM REFERENCE INPUTS						
Logic Compliance	SYSREF+, SYSREF-		LVDS/LVP ECL			
Differential Input Voltage		400	800	1800	mV p-p	
Input Common-Mode Voltage			0.675	2.0	V	
Input Resistance (Differential)			18		kΩ	
Input Capacitance (Differential)			1		pF	
AUXILIARY CONVERTERS						
ADC						
Resolution			10		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			0.95		V	
DAC						
Resolution			12		Bits	
Output Voltage						
Minimum			0.1		V	
Maximum			VDDA_1 P8 - 0.1		V	
Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (CMOS)						
Logic Inputs						
Input Voltage						
High Level		VIF × 0.65		VIF + 0.18	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Low Level		-0.30		VIF × 0.35	V	
Input Current						
High Level		-10		+10	μA	
Low Level		-10		+10	μA	
Logic Outputs						
Output Voltage						
High Level		VIF - 0.45			V	
Low Level				0.45	V	
Drive Capability			10		mA	
DIGITAL SPECIFICATIONS (LVDS)						
Logic Inputs						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		-100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Differential Offset			225 1200		mV mV	
DIGITAL SPECIFICATIONS (CMOS), GPIO_ANA_x SIGNALS						
Logic Inputs						
Input Voltage						
High Level		VDDA_1P8 × 0.65		VDDA_1P8 + 0.18	V	
Low Level		-0.30		VDDA_1P8 × 0.35	V	
Input Current						
High Level		-10		+10	μA	
Low Level		-10		+10	μA	
Logic Outputs						
Output Voltage						
High Level		VDDA_1P8 - 0.45			V	
Low Level				0.45	V	
Drive Capability			10		mA	

POWER SUPPLY SPECIFICATIONS

Table 2. Power Supply Voltages

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
SUPPLY CHARACTERISTICS					
VDDA_1P0 Supply	0.95	1.0	1.05	V	
VDIG Supply	0.95	1.0	1.05	V	
VDDA_1P3 Supply	1.235	1.3	1.365	V	
VDDA_1P8 Supply	1.71	1.8	1.89	V	
VIF Supply	1.71	1.8	1.89	V	

CURRENT CONSUMPTION

TDD Operation (Typical Values)

Table 3. TDD Mode: 4 Rx Channels Enabled, Maximum Gain

Profile Conditions ¹	Supply (A)			Total Average Power (W)	75% Tx, 25% Rx Average Power (W)
	1.0 V	1.3 V	1.8 V		
USE CASE 51 LINK SHARING (16 BITS) 245.76 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.64	2.13	0.24	4.8	5.3

¹ All current measurements made at room temperature without a heatsink.

Table 4. TDD Mode: 4 Tx and 1 ORx Channels Enabled, 0 dB Attenuation, Maximum Gain

Profile Conditions ¹	Supply (A)			Total Average Power (W)	75% Tx, 25% Rx Average Power (W)
	1.0 V	1.3 V	1.8 V		
USE CASE 51 LINK SHARING (16 BITS) 245.76 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.91	1.89	0.64	5.5	5.3

¹ All current measurements made at room temperature without a heatsink.

FDD Operation (Typical Values)

Table 5. FDD Mode (LO1 and LO2): 4 Rx, 4 Tx, and 1 ORx Channels Enabled, Maximum Gain, 0 dB Attenuation

Profile Conditions ¹	Supply (A)			Total Average Power (W)
	1.0 V	1.3 V	1.8 V	
USE CASE 51 LINK SHARING (16 BITS) 245.76 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	2.38	3.08	0.79	7.8

DIGITAL INTERFACE AND TIMING SPECIFICATIONS

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL PERIPHERAL INTERFACE (SPI) TIMING						
SPI_CLK Period	t_{CP}	40			ns	
SPI_CLK Pulse Width	t_{MP}	10			ns	
SPI_EN Setup to First SPI_CLK Rising Edge	t_{SC}	4			ns	
Last SPI_CLK Falling Edge to SPI_EN Hold	t_{HC}	0			ns	
SPI_DIO Data Input Setup to SPI_CLK	t_S	4			ns	
SPI_DIO Data Input Hold to SPI_CLK	t_H	0			ns	
SPI_CLK Falling Edge to Output Data Delay (3- or 4-Wire Mode)	t_{CO}	10		8	ns	
Bus Turnaround Time After Baseband Processor (BBP) Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time After ADRV9020 Drives Last Address Bit	t_{HZS}	0		t_{CO}	ns	
DIGITAL TIMING						
TXn_EN Pulse Width		10			μs	
RXn_EN Pulse Width		10			μs	
ORXn_EN Pulse Width		10			μs	
TXn_EN to Valid Data			2		μs	
RXn_EN to Valid Data			2		μs	
ORXn_EN to Valid Data			3		μs	
JESD204B/C DATA OUTPUT TIMING						
Unit Interval	UI	40		330	ps	
Data Rate per Channel (Nonreturn to Zero (NRZ))		3000		25000	Mbps	
Rise Time	t_R	17	20		ps	20% to 80% in 100 Ω load
Fall Time	t_F	17	20		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Differential Output Voltage	V_{DIFF}	475		1050	mVppd	
Short-Circuit Current	I_{DSHORT}	-100		+100	mA	
Differential Termination Impedance	Z_{RDIFF}	80	100	120	Ω	
SYSREF_IN Signal Setup Time to DEV_CLK_IN Signal	t_S	2.5			ns	See Figure 2 and Figure 3
SYSREF_IN Signal Hold Time to DEV_CLK_IN Signal	t_H	-1.5			ns	See Figure 2 and Figure 3
JESD204B/C DATA INPUT TIMING						
Unit Interval	UI	40		330	ps	
Data Rate per Channel (NRZ)		3000		25000	Mbps	
Input Common-Mode Voltage	V_{CM}	0.05		1.65	V	AC-coupled
$V_{TT} = 1.0 V$		720		1200	mV	DC-coupled (not recommended)
Differential Input Voltage	V_{DIFF}	110		1050	mV	
V_{TT} Source Impedance	Z_{TT}		7.5	30	Ω	
Differential Termination Impedance	Z_{RDIFF}	80	100	120	Ω	
V_{TT}						
AC-Coupled		0.95		1.05	V	
DC-Coupled		0.95		1.05	V	

Timing Diagrams

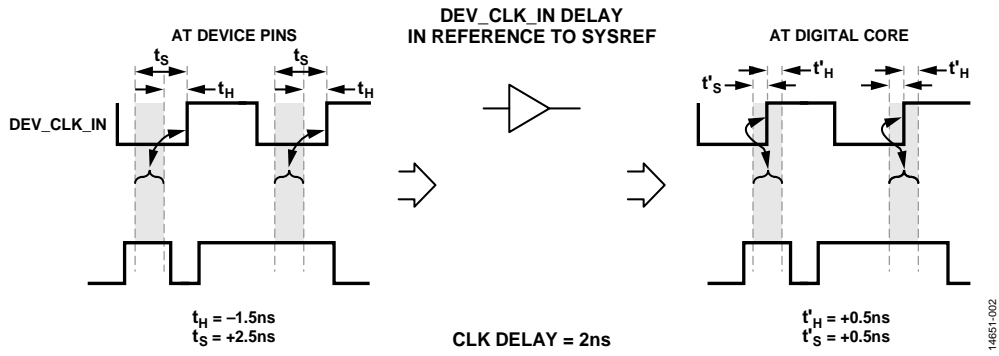


Figure 2. SYSREF_IN Signal Setup and Hold Timing

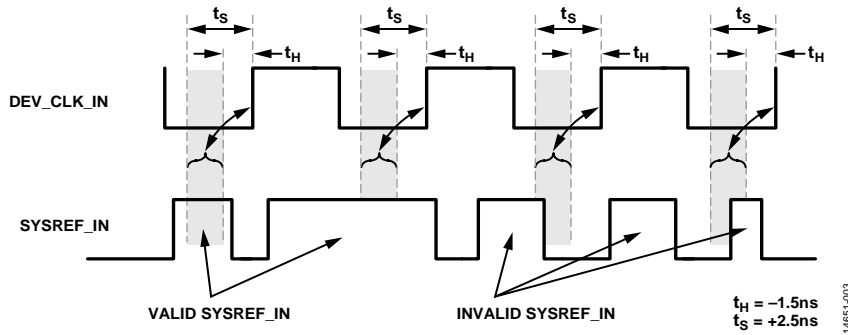


Figure 3. SYSREF_IN Signal Setup and Hold Timing Examples Relative to DEV_CLK_IN Signal

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VDDA_1P8 to VSSA	-0.3V to +2.2V
VDDA_1P3 to VSSA	-0.2V to +.5V
VDDA_1P0, VDIG_1P0 to VSSD, VSSA	-0.2V to +1.2V
VIF Referenced Logic Inputs and Outputs to VSSD	-0.3V to VIF + 0.3V
JESD204B Logic Outputs to VSSA	-0.3V to VDDA_SER
JESD204B Logic Inputs to VSSA	-0.3V to VDDA_DES
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Ports	See Table 9 for limits vs. survival time
Junction Temperature Range ¹	-40°C to +110°C
Storage Temperature Range	-65°C to +150°C

¹ The maximum junction temperature for continuous operation is 110°C. See the Junction Temperature section for more details.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

JUNCTION TEMPERATURE

The maximum junction temperature for continuous operation is 110°C. Although operation up to 125°C is supported, specification compliance is only guaranteed up to 110°C. To avoid a reduction in operating lifetime by operating above 110°C, the device must operate at a temperature less than 110°C for a period determined by the following equation:

$$t_{UNITS < 110} = (AF_{T > 110} - 1) / (1 - AF_{T < 110})$$

where $AF_{T > 110}$ and $AF_{T < 110}$ are acceleration factors obtained from Table 8.

For example, if the device operates at 125°C for 1 hour, expected device lifetime is maintained if the device operates at 100°C for 4.5 hours to offset the time operating above 110°C.

Table 8. Acceleration Factors for High Temperature Operation

Operating Junction Temperature (°C)	Acceleration Factor (AF)
125	3.75
120	2.44
115	1.57
110	1.00
105	0.63
100	0.39
95	0.24
90	0.14

Table 9. Maximum Input Power into RF Ports vs. Lifetime

RF Port Input Power, CW Signal (dBm)	Lifetime	
	Gain = -30 dB	Gain = 0 dB
7	>10 years	>10 years
10	>10 years	20,000 hours
20	>10 years	14 hours
23	>10 years	110 minutes
25	>7 years	60 minutes

REFLOW PROFILE

The ADRV9020 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal resistance values specified in Table 10 are calculated based on JEDEC specifications (unless specified otherwise) and should be used in compliance with JESD51-12. Note that using enhanced heat removal techniques (PCB, heat sink, air flow, and so forth) improves thermal resistance.

Table 10. Thermal Resistance Values

Package Type	θ_{JA} (°C/W)	θ_{Jtop} (°C/W)	θ_{JB} (°C/W)	ψ_{JC} (°C/W)	ψ_{JB} (°C/W)
BC-289-6	14.8	0.03	3.4	0.02	3.4

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSSA	VSSA	VSSA	TX3+	TX3-	VSSA	VTXLO_1P3	VSSA	VRXLO_1P3	VSSA	VSSA	VSSA	TX2+	TX2-	VSSA	VSSA	VSSA
B	RX3-	VSSA	VSSA	VANA3_1P8	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VVAUXVCO_1P3	VSSA	VSSA	VANA2_1P8	VSSA	VSSA	RX2+
C	RX3+	VSSA	NC	GPIO_ANA_7	GPIO_ANA_6	VVAUXSYN_1P3	VSSA	DEVCLK+	DEVCLK-	VSSA	VVAUXVCO_1P3	GPIO_ANA_1	GPIO_ANA_0	VSSA	RBIAS	VSSA	RX2-
D	VSSA	VSSA	VANA2_1P3	VSSA	VSSA	VSSA	VSSA	SYSREF+	SYSREF-	VSSA	VSSA	VSSA	VSSA	VSSA	VANA1_1P3	VSSA	VSSA
E	AUXADC_3	EXT_LO2-	VSSA	ORX3+	ORX3-	VSSA	TX3_EN	GPIO_11	GPIO_9	GPIO_3	TX2_EN	VSSA	ORX1+	ORX1-	VSSA	EXT_LO1+	AUXADC_1
F	AUXADC_2	EXT_LO2+	VSSA	VSSA	VSSA	VSSA	ORX_CTRL_C	GPIO_12	GPIO_10	GPIO_4	ORX_CTRL_B	VSSA	VSSA	VSSA	VSSA	EXT_LO1-	AUXADC_0
G	VSSA	VSSA	VRFVCO2_1P3	VSSA	VRFVCO2_1P0	VSSA	RX3_EN	GPIO_13	VDIG_1P0	GPIO_5	RX2_EN	VSSA	VRFVCO1_1P0	VSSA	VRFVCO1_1P3	VSSA	VSSA
H	RX4-	VSSA	VCONV2_1P8	VSSA	VSSA	VSSA	GPIO_17	GPIO_14	VSSD	GPIO_6	GPIO_0	VSSA	VSSA	VSSA	VCONV1_1P8	VSSA	RX1+
J	RX4+	VSSA	VCONV2_1P3	VSSA	VRFVCO2_1P3	VSSA	RX4_EN	GPIO_15	VDIG_1P0	GPIO_7	RX1_EN	VSSA	VRFVCO1_1P3	VSSA	VCONV1_1P3	VSSA	RX1-
K	VSSA	VSSA	VCONV2_1P0	VSSA	VSSA	VSSA	GPIO_18	GPIO_16	VSSD	GPIO_8	GPIO_1	VSSA	VSSA	VSSA	VCONV1_1P0	VSSA	VSSA
L	GPIO_ANA_5	GPIO_ANA_4	VSSA	ORX4+	ORX4-	VSSA	ORX_CTRL_D	SPI_DIO	VDIG_1P0	SPI_EN	ORX_CTRL_A	VSSA	ORX2+	ORX2-	VSSA	GPIO_ANA_2	GPIO_ANA_3
M	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	TX4_EN	SPI_DO	VSSD	SPI_CLK	TX1_EN	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
N	TX4-	VANA4_1P8	VSSA	VSSA	VCLKVCO_1P3	SYNCIN3+	GPINT2	GPINT1	VIF	RESETB	GPIO_2	SYNCIN1+	SYNCIN1-	SYNCOUT2+	SYNCOUT2-	VANA1_1P8	TX1+
P	TX4+	VSSA	VSSA	VSSA	VCLKVCO_1P0	SYNCIN3-	SYNCIN2+	SYNCIN2-	VSSA	TEST_EN	VJVC0_1P8	VDES_1P0	VDES_1P0	VTT_DES	SYNCOUT1+	VSSA	TX1-
R	VSSA	VSSA	VSER_1P0	VSER_1P0	VSSA	VSSA	VCLKSYN_1P3	VSSA	VJSYN_1P0	VSSA	NC	VSSA	VSSA	VSSA	SYNCOUT1-	VSSA	VSSA
T	VSSA	VSSA	SERDOUTC+	SERDOUTC-	VSSA	VSSA	SERDOUTA+	SERDOUTA-	VSSA	SERDINA-	SERDINA+	VSSA	VSSA	SERDINC-	SERDINC+	VSSA	VSSA
U	SERDOUTD+	SERDOUTD-	VSSA	VSSA	SERDOUTB+	SERDOUTB-	VSSA	VSSA	VSSA	VSSA	VSSA	SERDINB+	SERDINB-	VSSA	VSSA	SERDIND+	SERDIND-

Figure 4. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1 to A3, A6, A8, A10 to A12, A15 to A17, B2, B3, B5 to B10, B12, B13, B15, B16, C2, C7, C10, C14, C16, D1, D2, D4 to D7, D10 to D14, D16, D17, E3, E6, E12, E15, F3 to F6, F12 to F15, G1, G2, G4, G6, G12, G14, G16, G17, H2, H4 to H6, H12 to H14, H16, J2, J4, J6, J12, J14, J16, K1, K2, K4 to K6, K12 to K14, K16, K17, L3, L6, L12, L15, M1 to M6, M12 to M17, N3, N4, P2 to P4, P9, P16, R1, R2, R5, R6, R8, R10, R12 to R14, R16, R17, T1, T2, T5, T6, T9, T12, T13, T16, T17, U3, U4, U7 to U11, U14, U15	I	VSSA	Analog ground.
A4, A5	O	TX3+, TX3-	Differential output for transmitter channel 3. Do not connect if unused.
A7	I	VTXLO_1P3	1.3 V supply input.
A9	I	VRXLO_1P3	1.3 V supply input.
A13, A14	O	TX2+, TX2-	Differential output for transmitter channel 2. Do not connect if unused.
B1, C1	I	RX3-, RX3+	Differential input for receiver channel 3. Connect to VSSA if unused.
B4	I	VANA3_1P8	1.8 V supply input.
B11	O	VAUXVCO_1P0	1.0 V internal supply node. Bypass this pin with a 4.7µF capacitor.
B14	I	VANA2_1P8	1.8 V supply input.
B17, C17	I	RX2+, RX2-	Differential input for receiver channel 2. Connect to VSSA if unused.
C3, R11	N/A	NC	Must leave disconnected.
C4, C5, L1, L2, L17, L16, C12, C13	I/O	GPIO_ANA_7 to GPIO_ANA_0	General-purpose inputs and outputs referenced to 1.8 V, can also function as auxiliary DAC outputs. If unused, these pins can be connected to VSSA with a 10kΩ resistor or configured as outputs, driven low, and left disconnected.
C6	I	VAUXSYN_1P3	1.3 V supply input.
C8, C9	I	DEVCLK+, DEVCLK-	Device clock differential input.
C11	I	VAUXVCO_1P3	1.3 V supply input.
C15	I	RBIAS	Bias Resistor Connection. This pin generates an internal current based on an external 1% resistor. Connect a 5 kΩ resistor between this pin and analog ground (VSSA).
D3	I	VANA2_1P3	1.3 V supply input.
D8, D9	I	SYSREF+, SYSREF-	LVDS System Reference Clock Inputs for the SERDES Interface.
D15	I	VANA1_1P3	1.3 V supply input.
E1	I	AUXADC_3	Auxiliary ADC 3 input. Do not connect if unused.
E2, F2	I/O	EXT_LO2-, EXT_LO2+	Differential External LO Input/Output 2. If used for the external LO input, the input frequency must be 2× the desired carrier frequency. Do not connect if unused.
E4, E5	I	ORX3+, ORX3-	Differential input for observation receiver channel 3. Connect to VSSA if unused.
E7	I	TX3_EN	Enable input for TX channel 3. Connect to VSSA if unused.

Pin No.	Type	Mnemonic	Description
H11, K11, N11, E10, F10, G10, H10, J10, K10, E9, F9, E8, F8, G8, H8, J8, K8, H7, K7	I/O	GPIO_0 to GPIO_18	General-purpose digital inputs and outputs. See Figure 4 to match the ball location to the GPIO_n signal name. If unused, these pins can be connected to VSSA with a 10kΩ resistor or configured as outputs, driven low, and left disconnected.
E11	I	TX2_EN	Enable input for TX channel 2. Connect to VSSA if unused.
E13, E14	I	ORX1+, ORX1-	Differential input for observation receiver channel 1. Connect to VSSA if unused.
E16, F16	I/O	EXT_LO1+, EXT_LO1-	Differential External LO Input/Output 1. If used for the external LO input, the input frequency must be 2× the desired carrier frequency. Do not connect if unused.
E17	I	AUXADC_1	Auxiliary ADC 1 input. Do not connect if unused.
F1	I	AUXADC_2	Auxiliary ADC 2 input. Do not connect if unused.
F7, F11, L7, L11	I	ORX_CTRL_C, ORX_CTRL_B, ORX_CTRL_D, ORX_CTRL_A	Used to determine active ORX path. Connect to VSSA directly or with a pull down resistor if unused.
F17	I	AUXADC_0	Auxiliary ADC 0 input. Do not connect if unused.
G3	I	VRVCO2_1P3	1.3 V supply input.
G5	O	VRVCO2_1P0	1.0 V internal supply node. Bypass this pin with a 4.7μF capacitor.
G7	I	RX3_EN	Enable input for RX channel 3. Connect to VSSA if unused.
G9, J9, L9	I	VDIG_1P0	1.0 V digital supply input.
G11	I	RX2_EN	Enable input for RX channel 2. Connect to VSSA if unused.
G13	O	VRVCO1_1P0	1.0 V internal supply node. Bypass this pin with a 4.7μF capacitor.
G15	I	VRVCO1_1P3	1.3 V supply input.
H1, J1	I	RX4-, RX4+	Differential input for receiver channel 4. Connect to VSSA if unused.
H3	I	VCONV2_1P8	1.8 V supply input.
H9, K9, M9	I	VSSD	Digital ground.
H15	I	VCONV1_1P8	1.8 V supply input.
H17, J17	I	RX1+, RX1-	Differential input for receiver channel 1. Connect to VSSA if unused.
J3	I	VCONV2_1P3	1.3 V supply input.
J5	I	VRFSYN2_1P3	1.3 V supply input.
J7	I	RX4_EN	Enable input for RX channel 4. Connect to VSSA if unused.
J11	I	RX1_EN	Enable input for RX channel 1. Connect to VSSA if unused.
J13	I	VRFSYN1_1P3	1.3 V supply input.
J15	I	VCONV1_1P3	1.3 V supply input.
K3	I	VCONV2_1P0	1.0 V internal supply node. Bypass this pin with a 4.7μF capacitor.
K15	I	VCONV1_1P0	1.0 V internal supply node. Bypass this pin with a 4.7μF capacitor.
L4, L5	I	ORX4+, ORX4-	Differential input for observation receiver channel 4. Connect to VSSA if unused.
L8	I/O	SPI_DIO	Serial data input in 4-wire mode or input/output in 3-wire mode.
L10	I	SPI_EN	Serial data bus chip select. Active low.
L13, L14	I	ORX2+, ORX2-	Differential input for observation receiver channel 2. Connect to VSSA if unused.
M7	I	TX4_EN	Enable input for TX channel 4. Connect to VSSA if unused.
M8	O	SPI_DO	Serial data output.
M10	I	SPI_CLK	Serial data bus clock input.
M11	I	TX1_EN	Enable input for TX channel 1. Connect to VSSA if unused.
N1, P1	O	TX4-, TX4+	Differential output for transmitter channel 4. Do not connect if unused.

Pin No.	Type	Mnemonic	Description
N2	I	VANA4_1P8	1.8 V supply input.
N5	I	VCLKVCO_1P3	1.3 V supply input.
N6, P6	I	SYNCIN3+, SYNCIN3-	LVDS sync signal input 3. Connect to VSSA if unused.
N7	O	GPINT2	General-purpose interrupt output 2. Do not connect if unused.
N8	O	GPINT1	General purpose interrupt output 1. Do not connect if unused.
N9	I	VIF	1.8V interface supply input.
N10	I	RESETB	Active low chip reset.
N12, N13	I	SYNCIN1+, SYNCIN1-	LVDS sync signal input 1. Connect to VSSA if unused.
N14, N15	O	SYNCOUT2+, SYNCOUT2-	LVDS sync signal output 2. Do not connect if unused.
N16	I	VANA1_1P8	1.8 V supply input.
N17, P17	O	TX1+, TX1-	Differential output for transmitter channel 1. Do not connect if unused.
P5	O	VCLKVCO_1P0	1.0 V internal supply node. Bypass this pin with a 4.7 μ F capacitor.
P7, P8	I	SYNCIN2+, SYNCIN2-	LVDS sync signal input 2. Connect to VSSA if unused.
P10	I	TEST_EN	Test input used for JTAG boundary scan. Pull high to enable boundary scan, tie to VSSA if unused.
P11	I	VJVC0_1P8	1.8 V supply input.
P12, P13	I	VDES_1P0	1.0 V analog supply input.
P14	I	VTT_DES	1.0 V analog supply input.
P15, R15	O	SYNCOUT1+, SYNCOUT1-	LVDS sync signal output 1. Do not connect if unused.
R3, R4	I	VSER_1P0	1.0 V analog supply input.
R7	I	VCLKSYN_1P3	1.3 V supply input.
R9	I	VJSYN_1P0	1.0 V analog supply input.
T3, T4	O	SERDOUTC+, SERDOUTC-	SERDES differential output C. Do not connect if unused.
T7, T8	O	SERDOUTA+, SERDOUTA-	SERDES differential output A. Do not connect if unused.
T10, T11	I	SERDINA-, SERDINA+	SERDES differential input A. Do not connect if unused.
T14, T15	I	SERDINC-, SERDINC+	SERDES differential input C. Do not connect if unused.
U1, U2	O	SERDOUTD+, SERDOUTD-	SERDES differential output D. Do not connect if unused.
U5, U6	O	SERDOUTB+, SERDOUTB-	SERDES differential output B. Do not connect if unused.
U12, U13	I	SERDINB+, SERDINB-	SERDES differential input B. Do not connect if unused.
U16, U17	I	SERDIND+, SERDIND-	SERDES differential input D. Do not connect if unused.

¹I is input, O is output, I/O is input/output, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 800 MHz, unless otherwise noted.

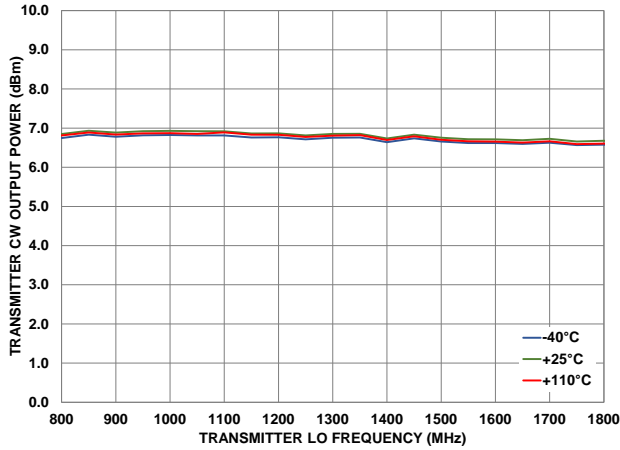


Figure 5. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

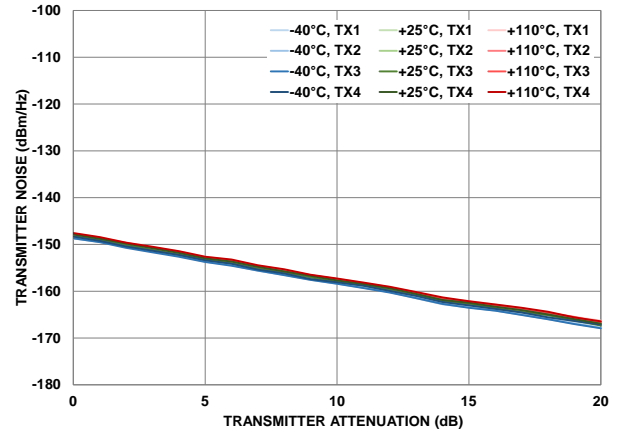


Figure 8. Transmitter Noise vs. Transmitter Attenuation, 10 MHz Offset

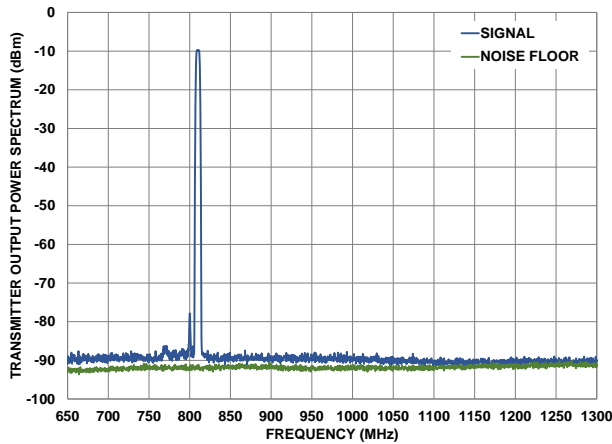


Figure 6. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, -10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

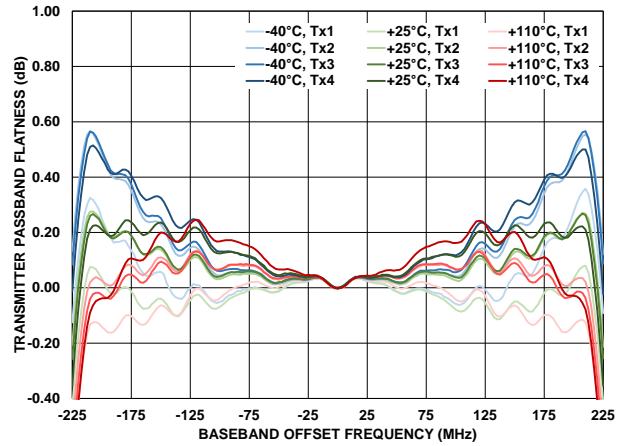


Figure 9. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

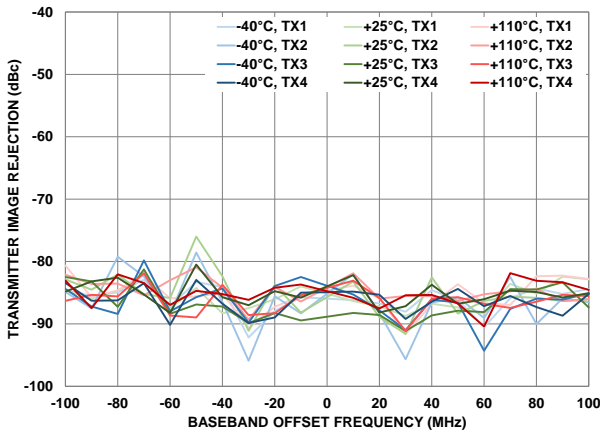


Figure 7. Transmitter Image Rejection Across Large Bandwidth vs. Baseband Offset Frequency

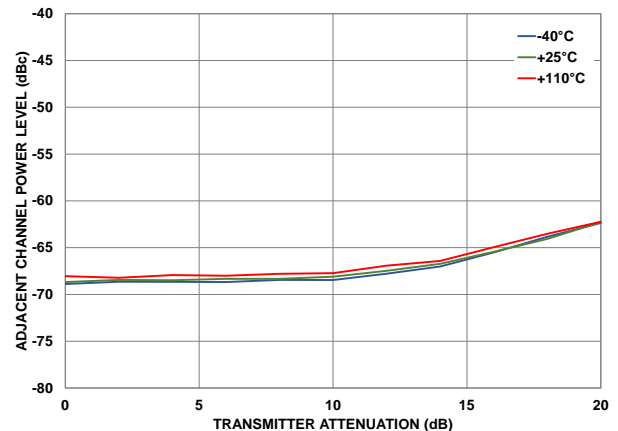


Figure 10. Adjacent Channel Power Level vs. Transmitter Attenuation, -10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

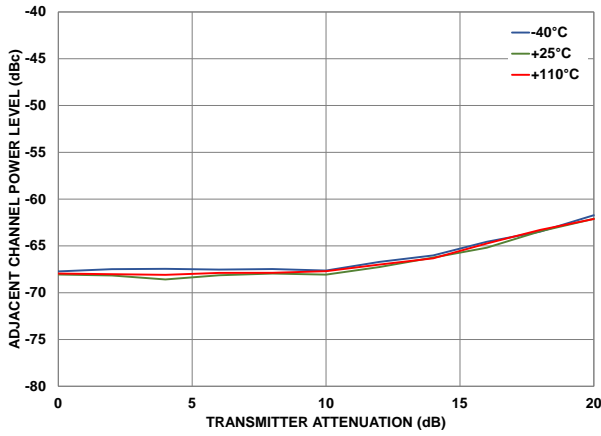


Figure 11. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

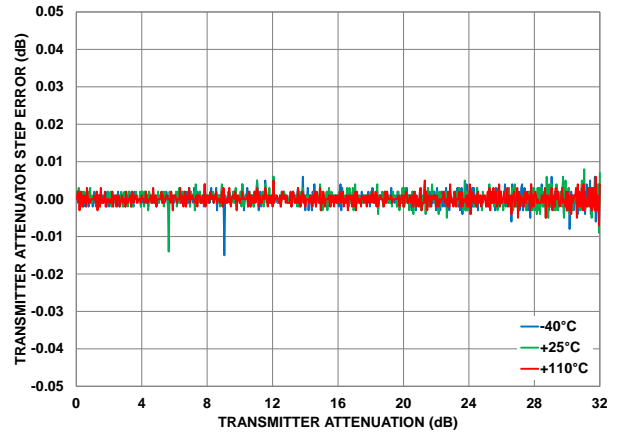


Figure 14. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

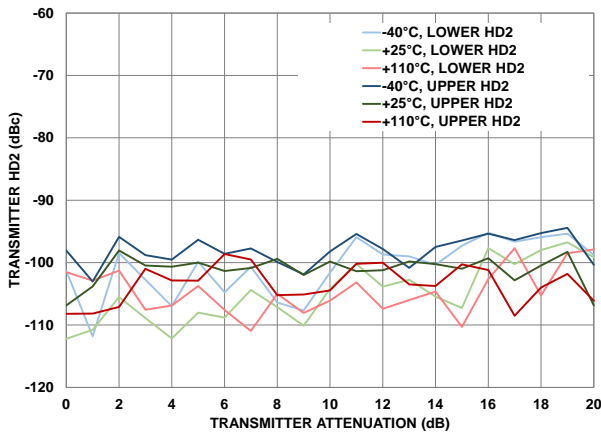


Figure 12. Transmitter Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 10 MHz Offset

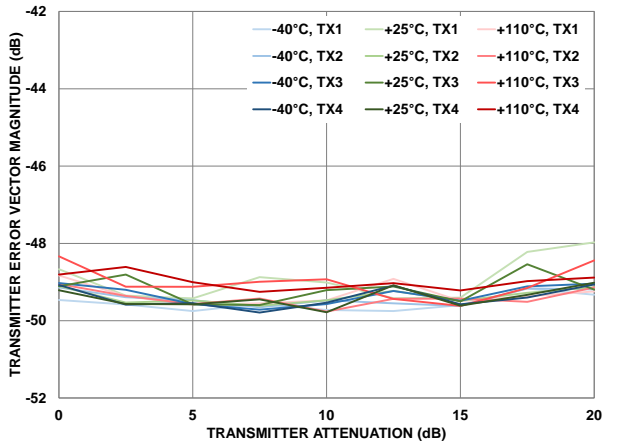


Figure 15. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 85°

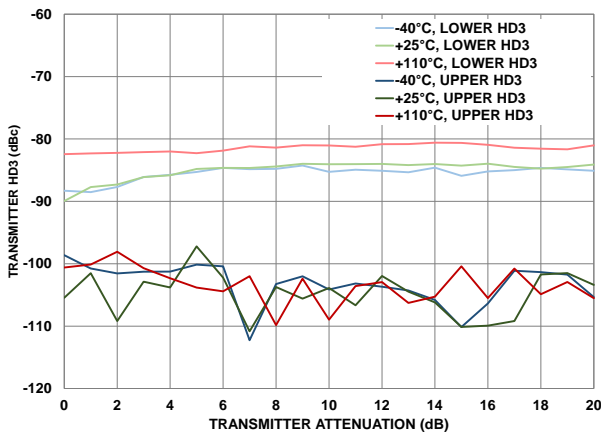


Figure 13. Transmitter Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 10 MHz Offset

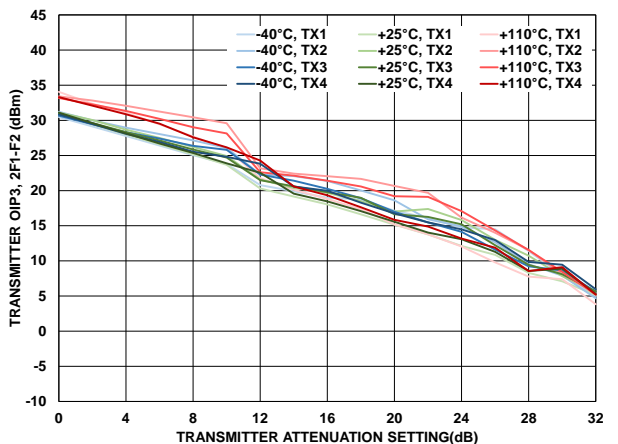


Figure 16. Transmitter OIP3, 2f1 - f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

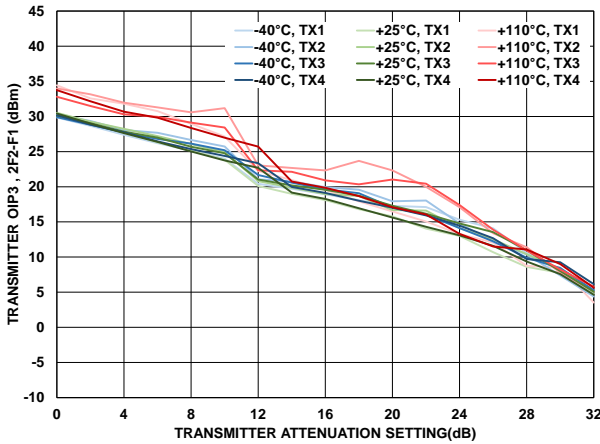


Figure 17. Transmitter OIP3, $2f_2 - f_1$ vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, $f_1 = 50.5$ MHz, $f_2 = 55.5$ MHz

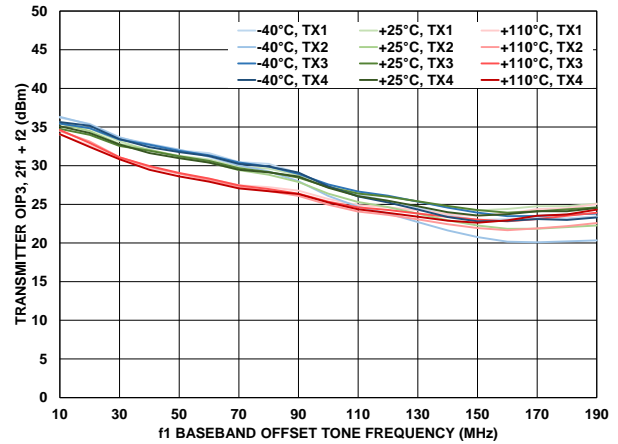


Figure 20. Transmitter OIP3, $2f_1 + f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

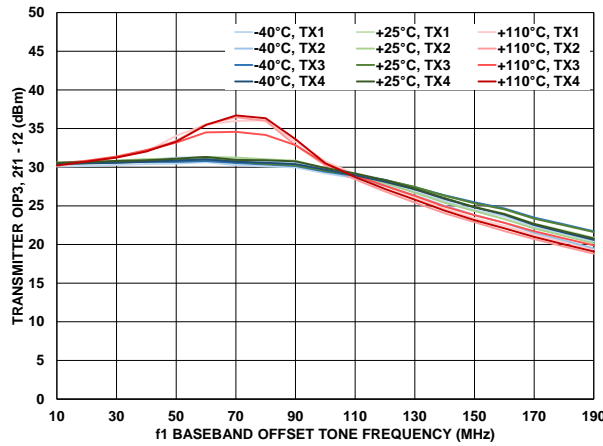


Figure 18. Transmitter OIP3, $2f_1 - f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

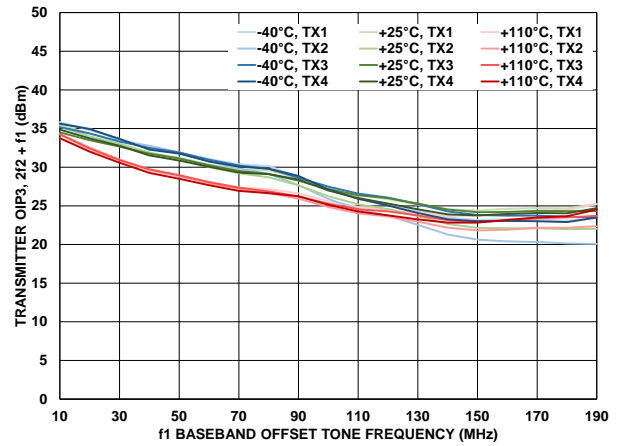


Figure 21. Transmitter OIP3, $2f_2 + f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

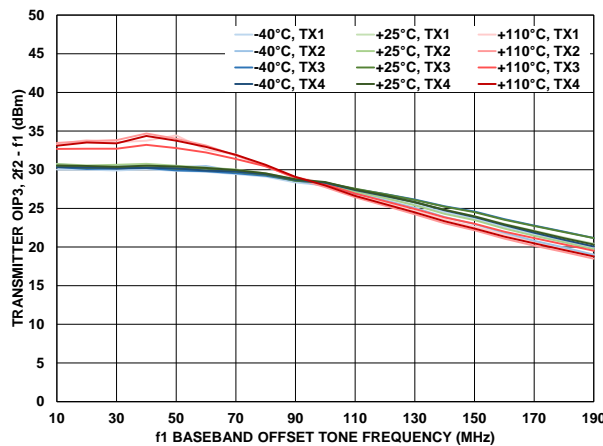


Figure 19. Transmitter OIP3, $2f_2 - f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

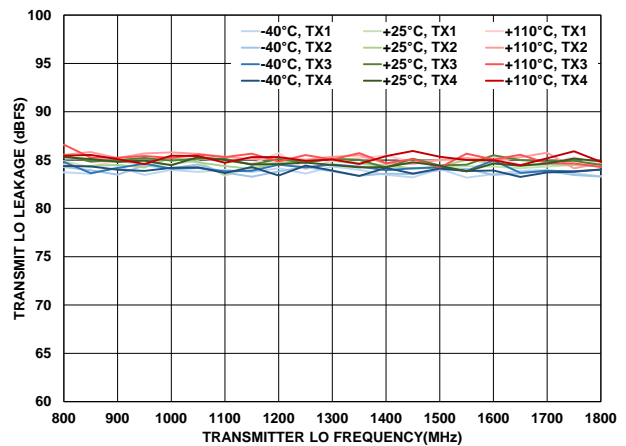


Figure 22. Transmitter LO Leakage vs. Transmitter LO Frequency

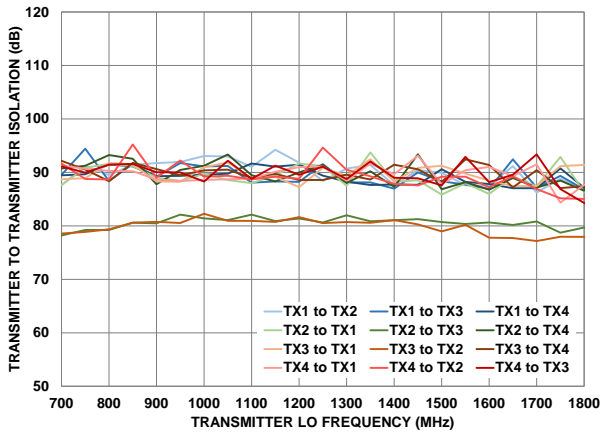


Figure 23. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

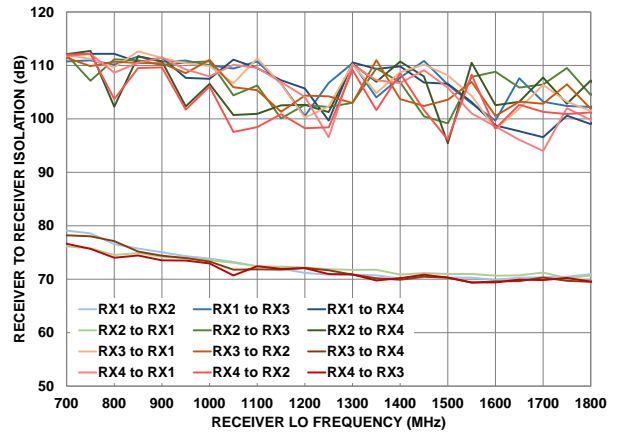


Figure 26. Receiver to Receiver Isolation vs. Receiver LO Frequency

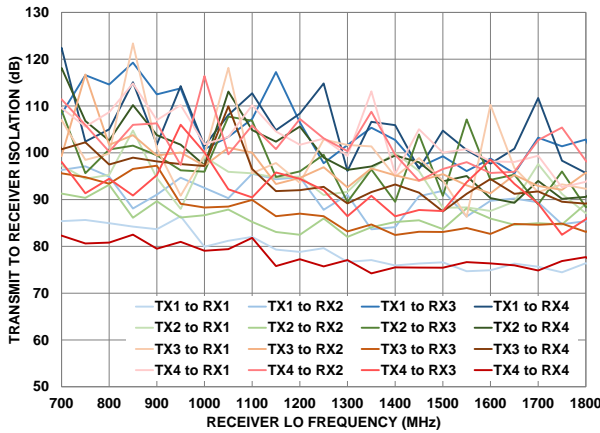


Figure 24. Transmitter to Receiver Isolation vs. Receiver LO Frequency

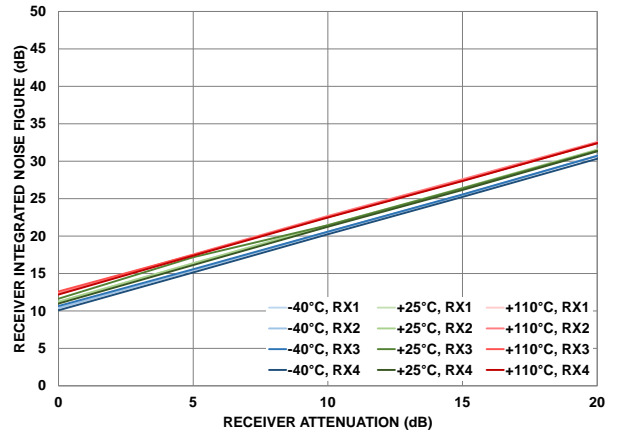


Figure 27. Receiver Integrated Noise Figure vs. Receiver Attenuation, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

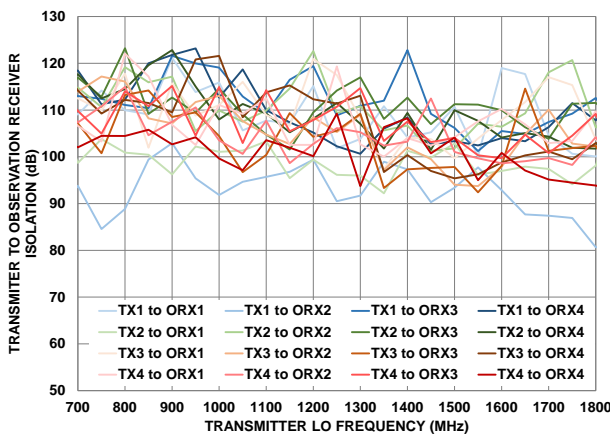


Figure 25. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

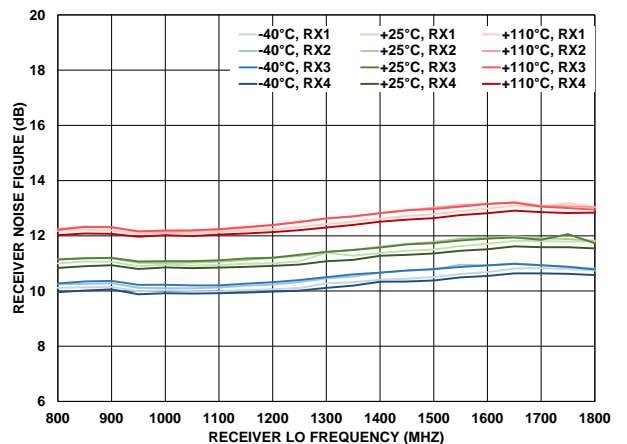


Figure 28. Receiver Integrated Noise Figure vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

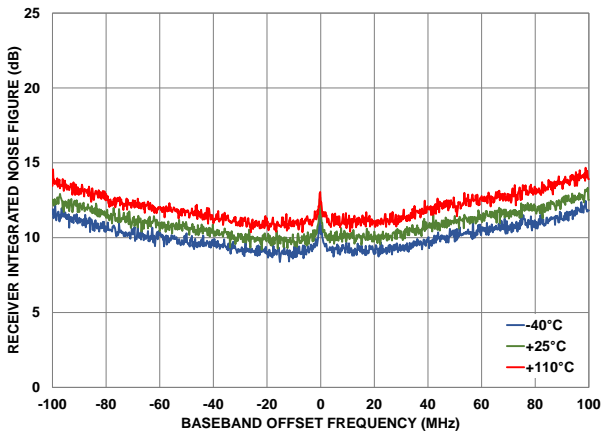


Figure 29. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

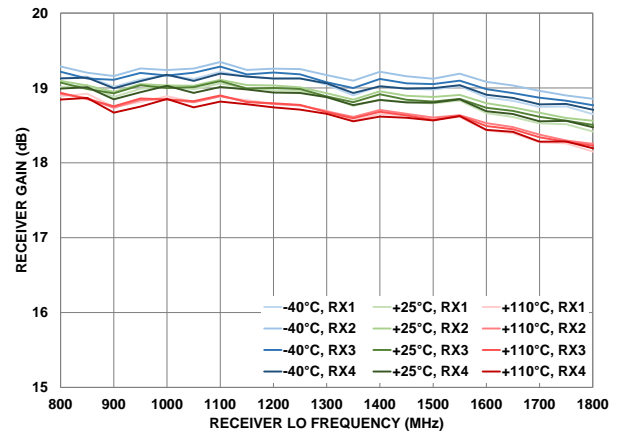


Figure 32. Receiver Gain vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

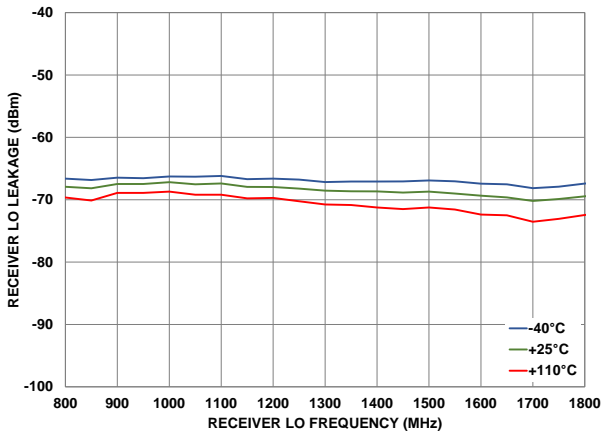


Figure 30. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

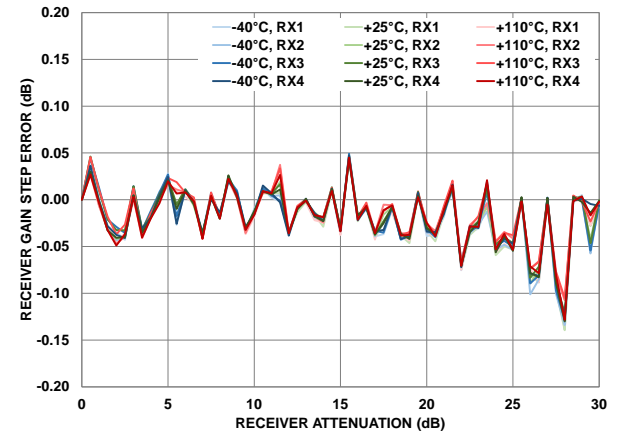


Figure 33. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

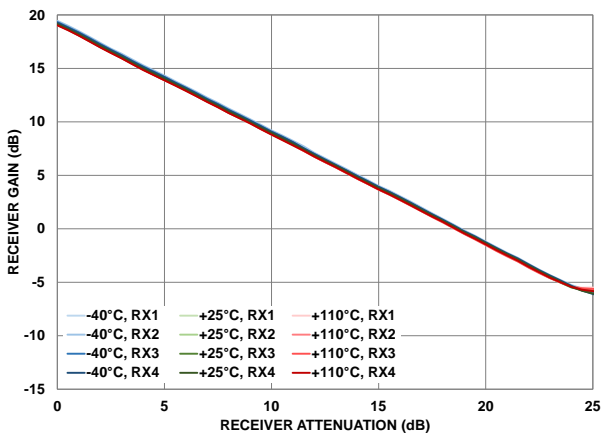


Figure 31. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

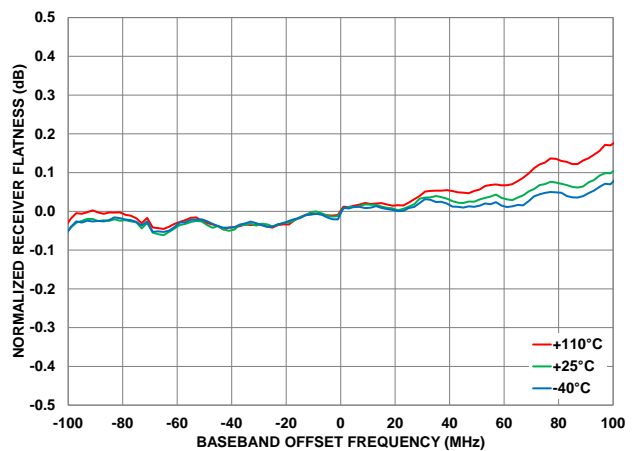


Figure 34. Normalized Receiver Flatness vs. Baseband Offset Frequency, -5 dBFS Input Signal

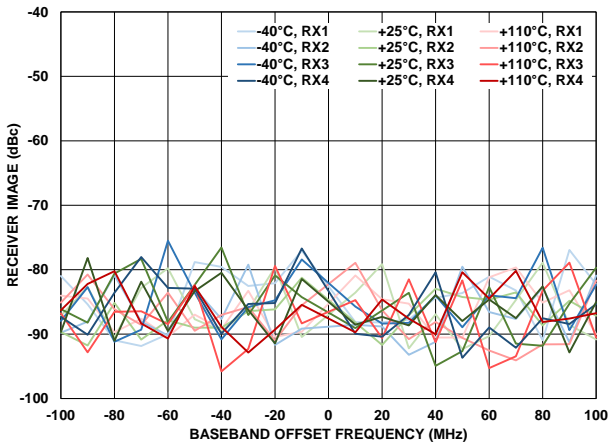


Figure 35. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS

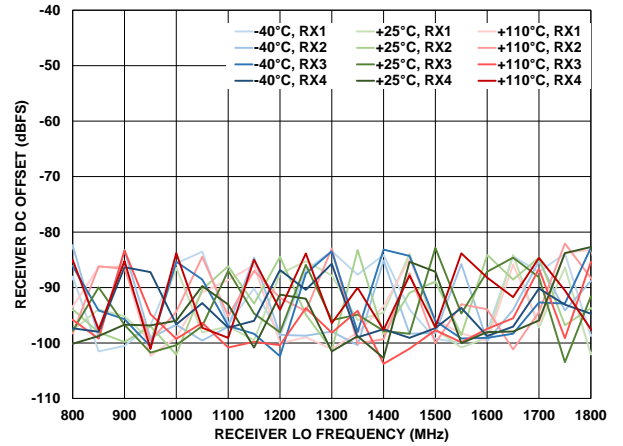


Figure 38. Receiver DC Offset vs. Receiver LO Frequency, 20 MHz Offset, -5 dBFS Input Signal

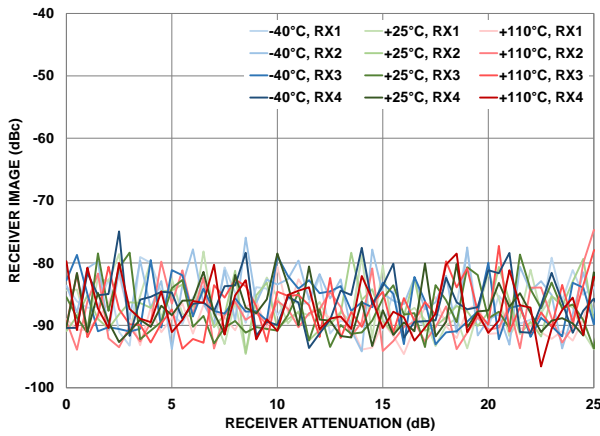


Figure 36. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS

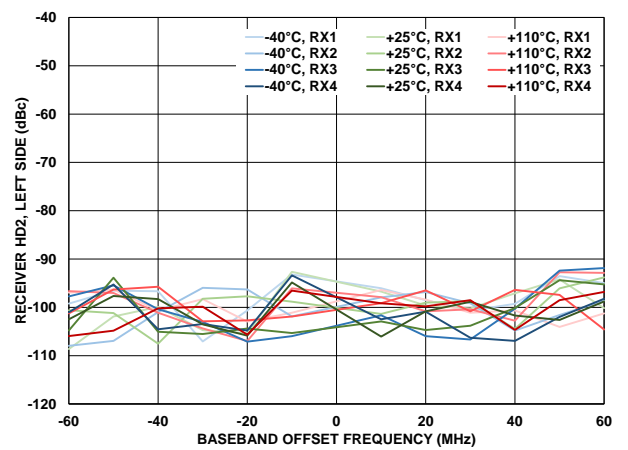


Figure 39. Receiver HD2, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Enabled)

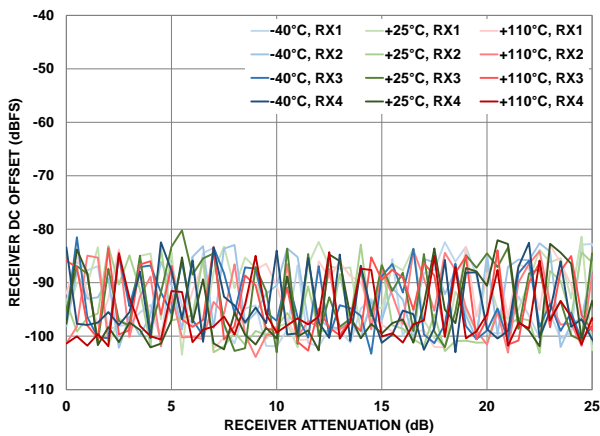


Figure 37. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

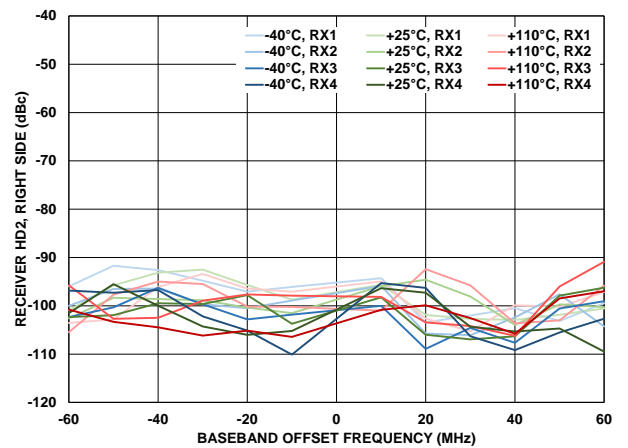


Figure 40. Receiver HD2, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Enabled)

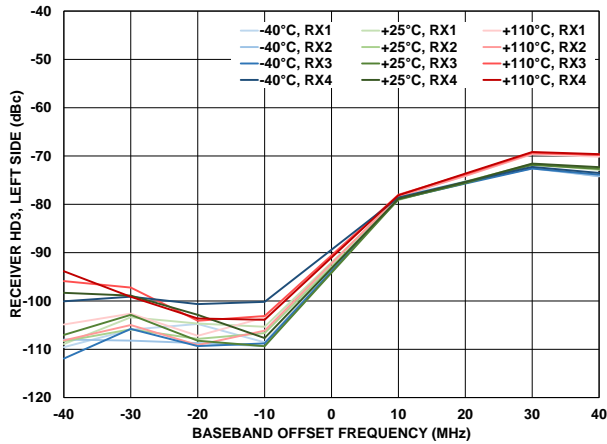


Figure 41. Receiver HD3, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

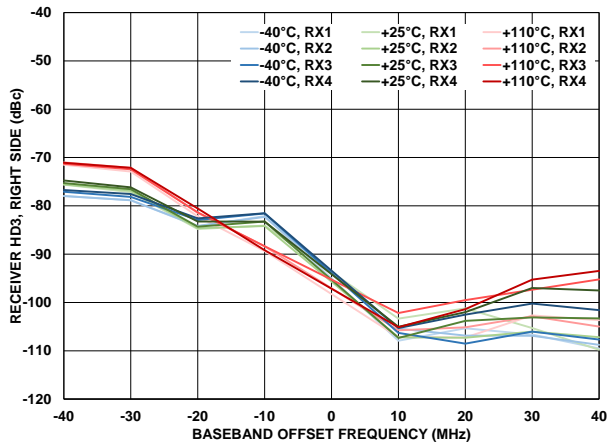


Figure 42. Receiver HD3, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

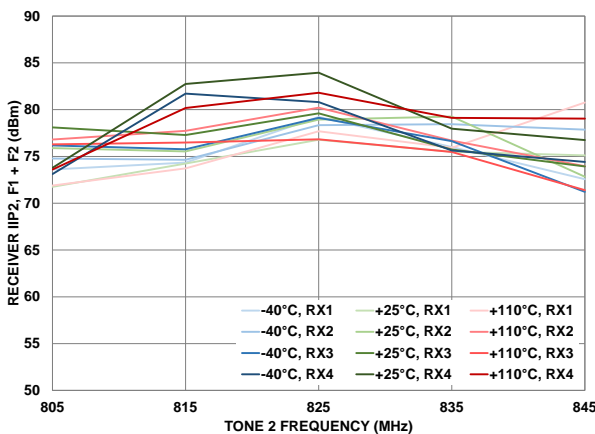


Figure 43. Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

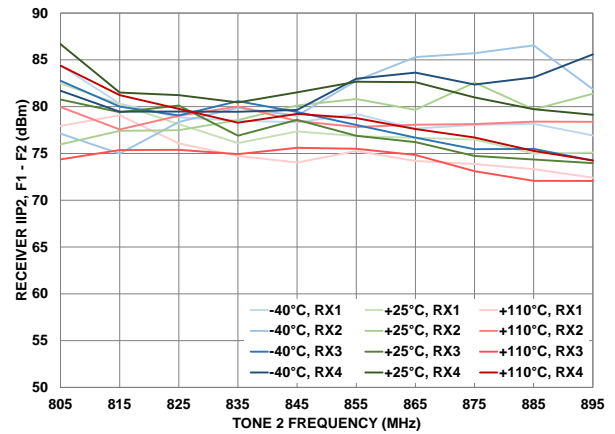


Figure 44. Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

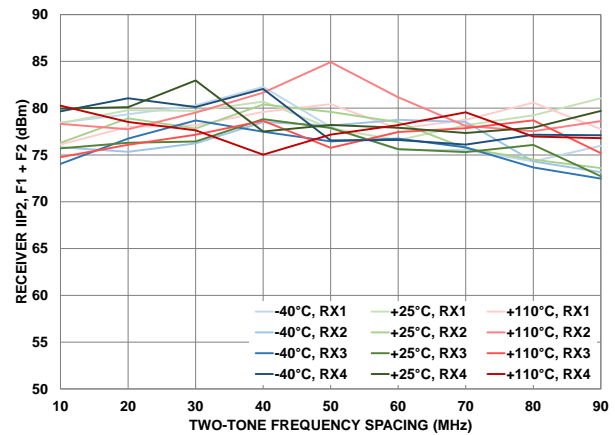


Figure 45. Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

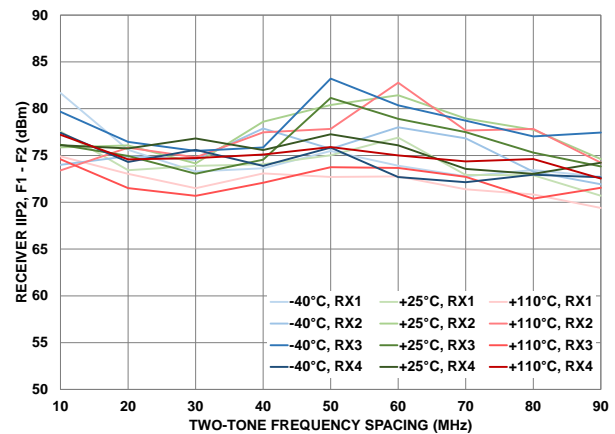


Figure 46. Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

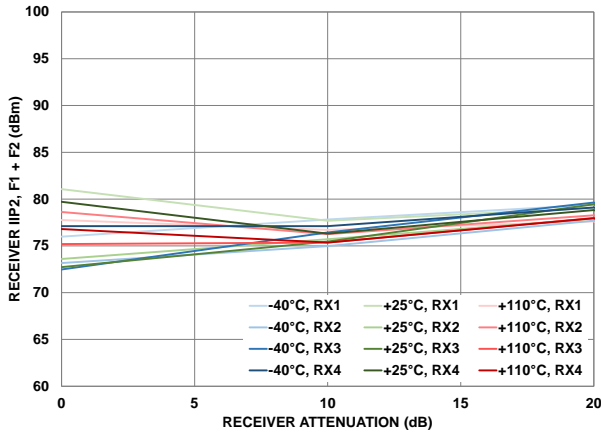


Figure 47. Receiver IIP2, $f_1 + f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

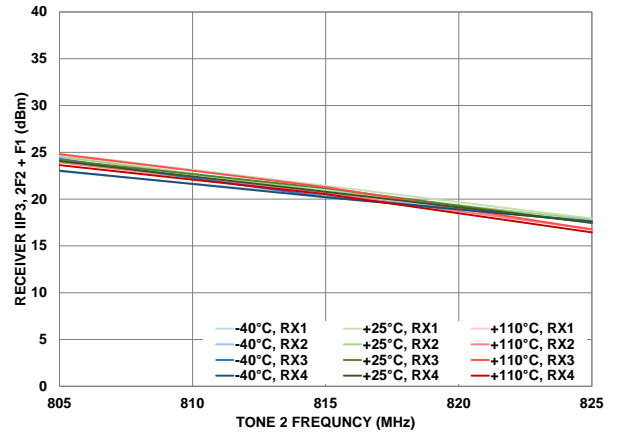


Figure 50. Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

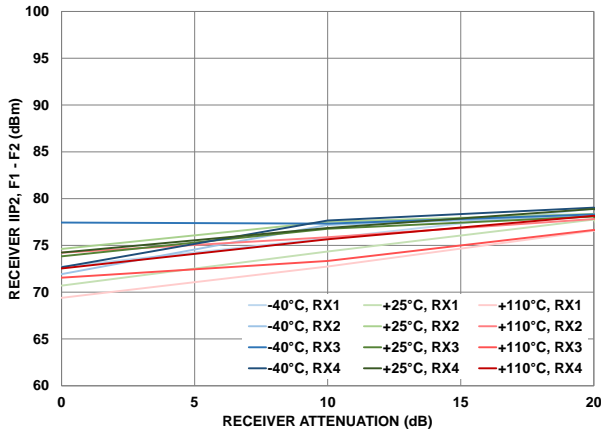


Figure 48. Receiver IIP2, $f_1 - f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

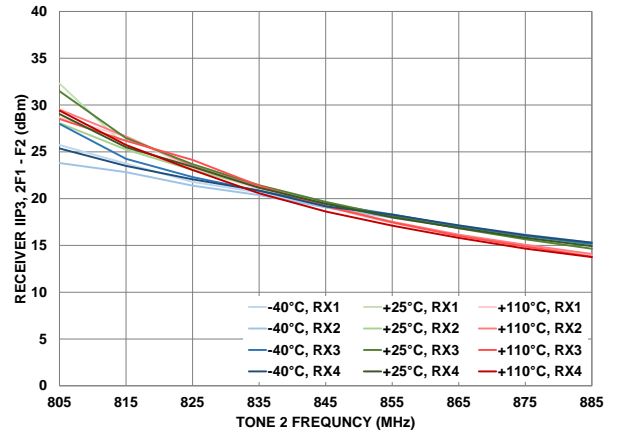


Figure 51. Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

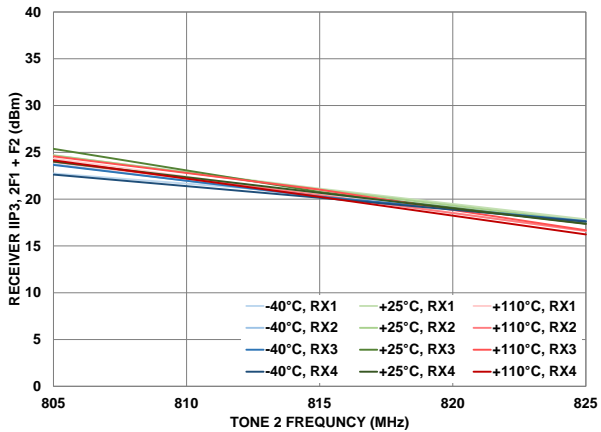


Figure 49. Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

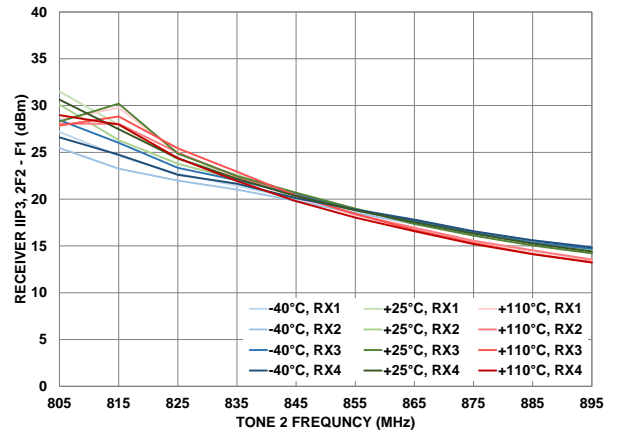


Figure 52. Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

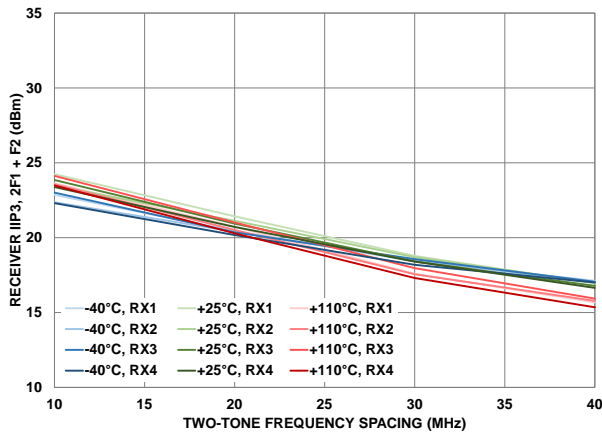


Figure 53. Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

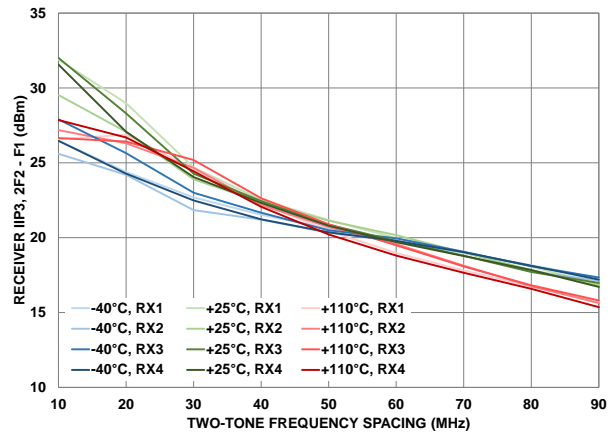


Figure 56. Receiver IIP3, $2f_2 - f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

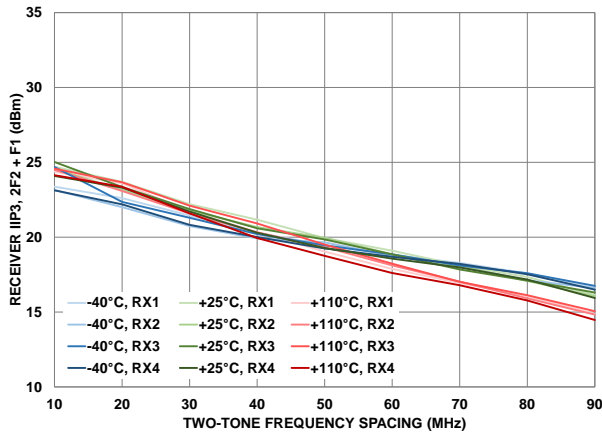


Figure 54. Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

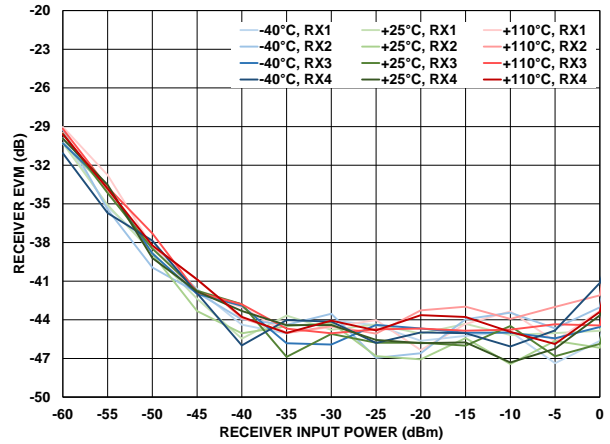


Figure 57. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 85°

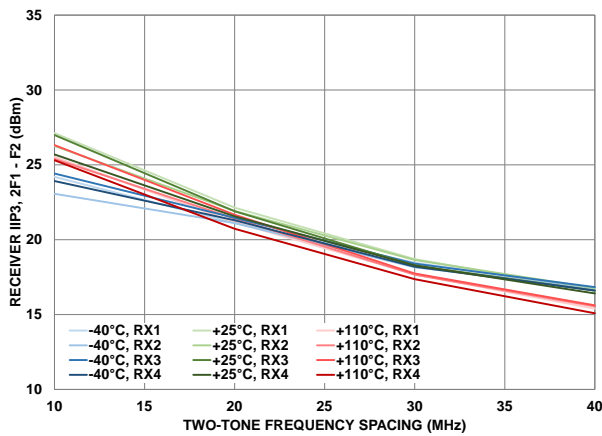


Figure 55. Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

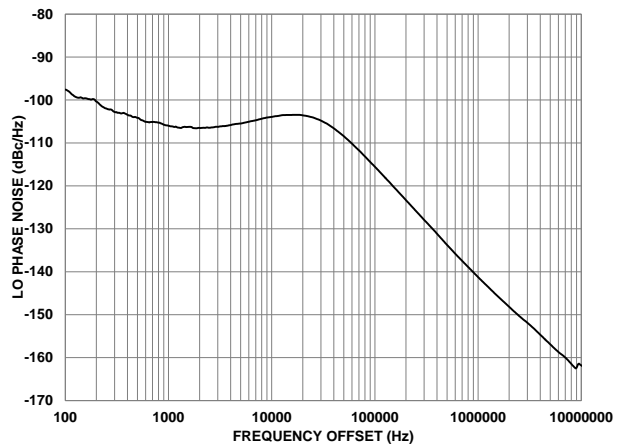


Figure 58. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 50 kHz, Phase Margin = 85°

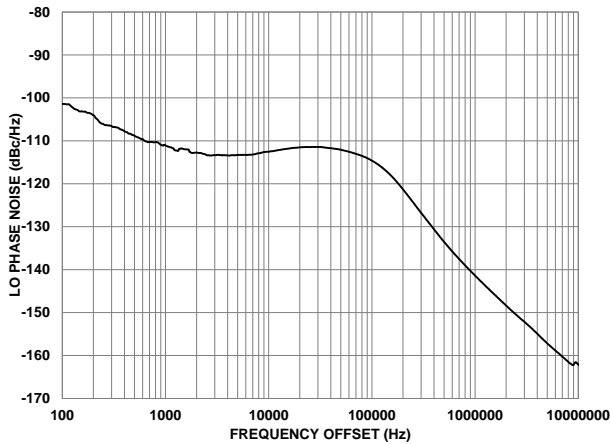


Figure 59. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 100 kHz, Phase Margin = 60°

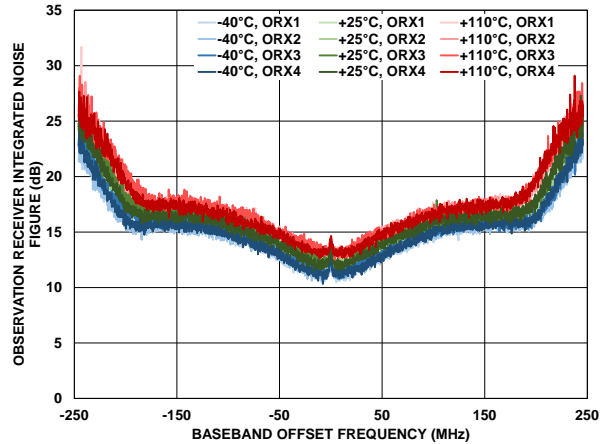


Figure 62. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

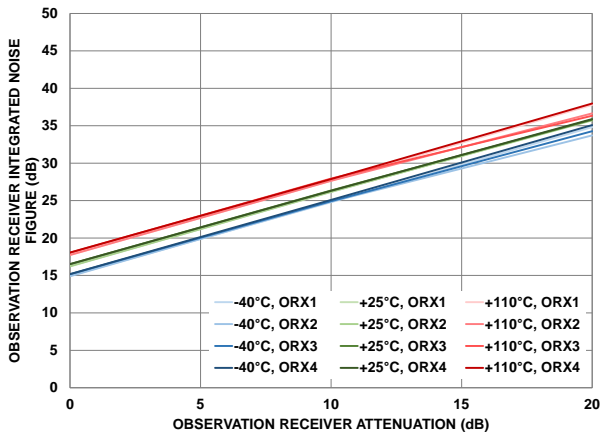


Figure 60. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

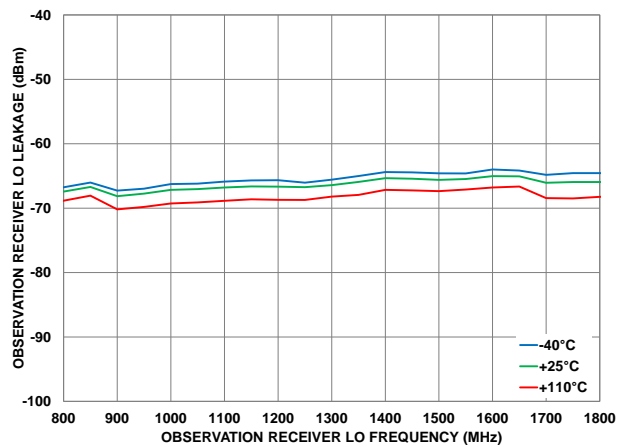


Figure 63. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

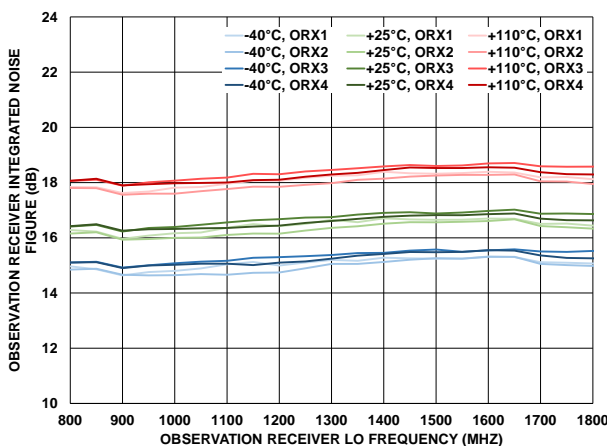


Figure 61. Observation Receiver Integrated Noise Figure vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

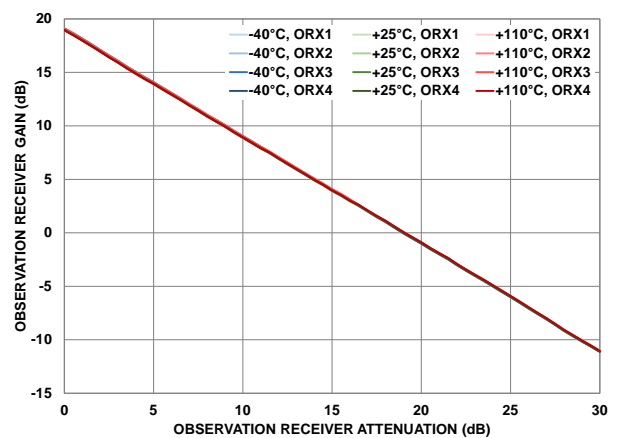


Figure 64. Observation Receiver Gain vs. Observation Receiver Attenuation, 45 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

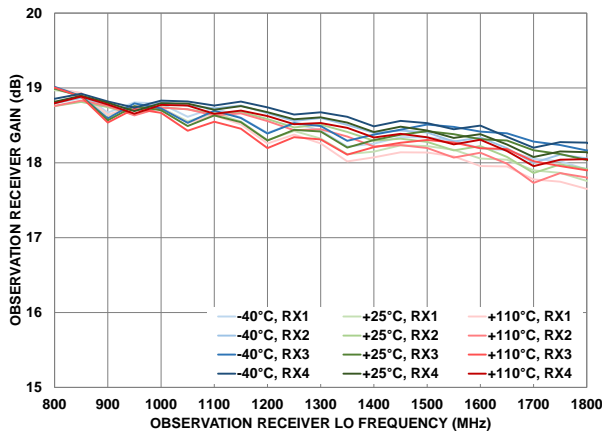


Figure 65. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

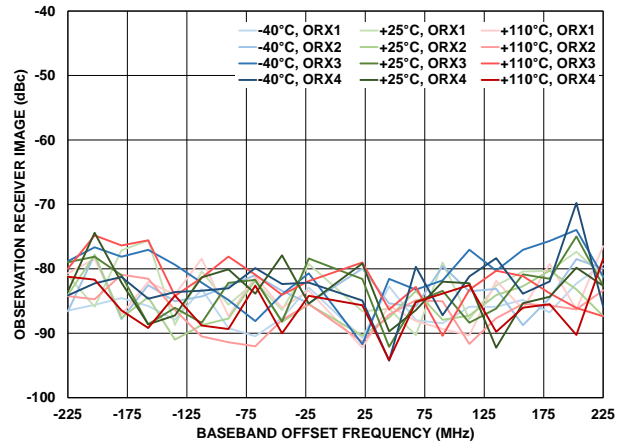


Figure 68. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

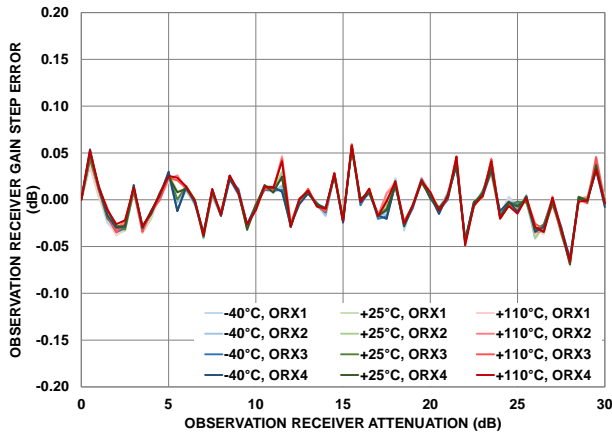


Figure 66. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 45 MHz Offset, -10 dBFS Input Signal

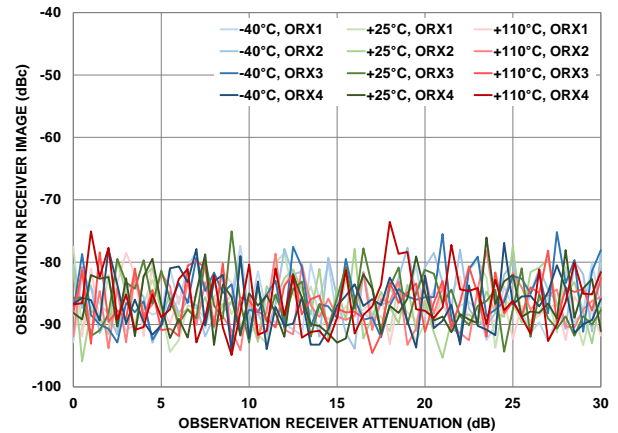


Figure 69. Observation Receiver Image vs. Observation Receiver Attenuation, 45 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

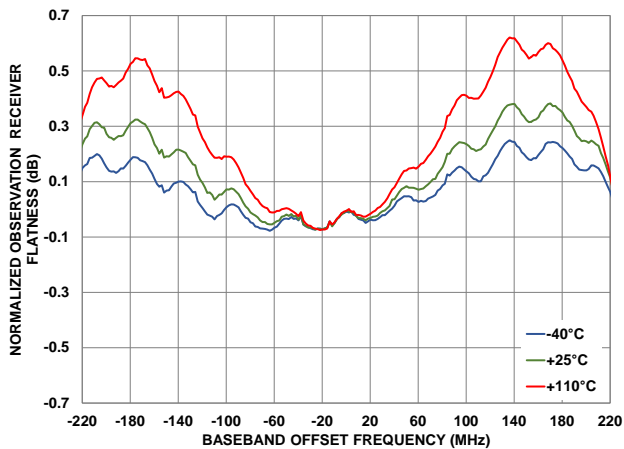


Figure 67. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, -10 dBFS Input Signal

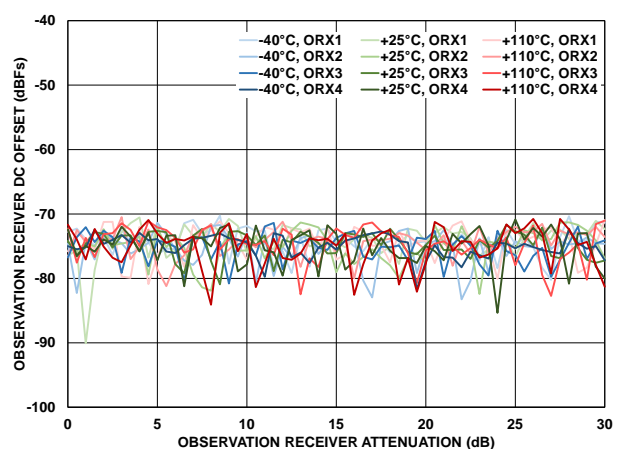


Figure 70. Observation Receiver DC Offset vs. Observation Receiver Attenuation, 45 MHz Offset, -10 dBFS Input Signal

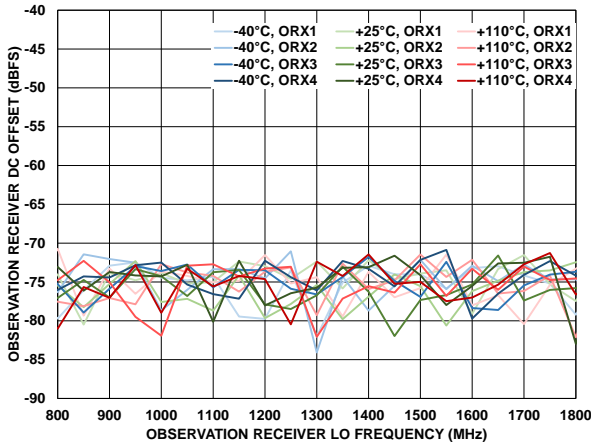


Figure 71. Observation Receiver DC Offset vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

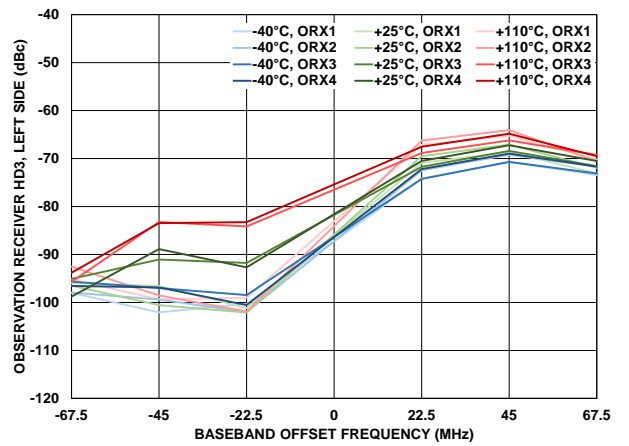


Figure 74. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

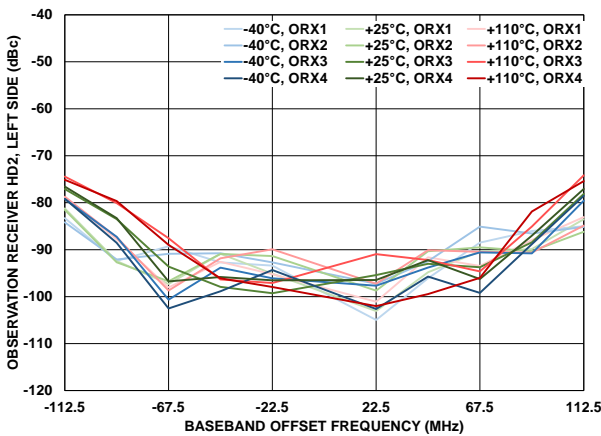


Figure 72. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

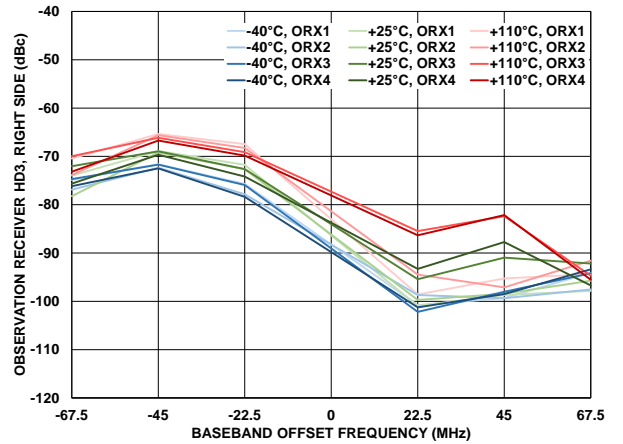


Figure 75. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

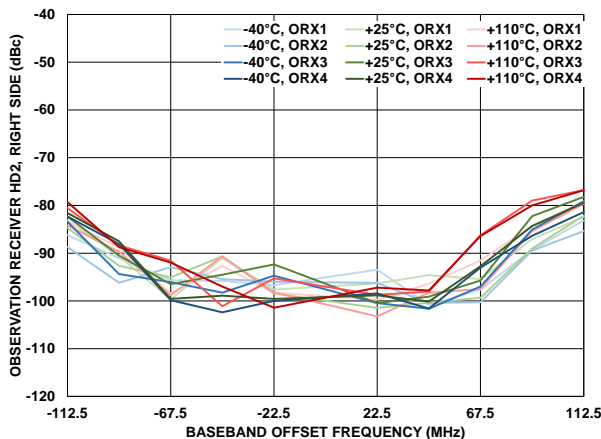


Figure 73. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

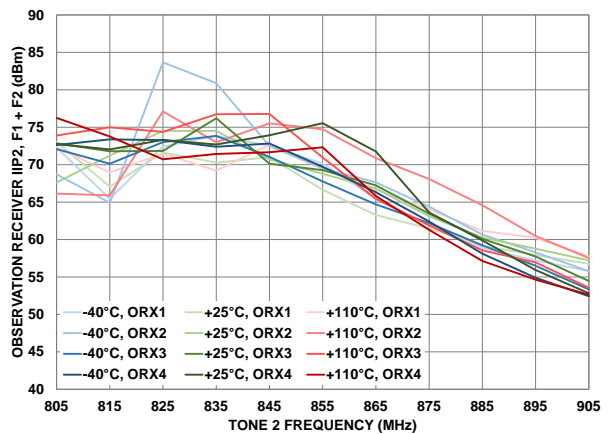


Figure 76. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at -13 dBFS, f1 = f2 + 2 MHz

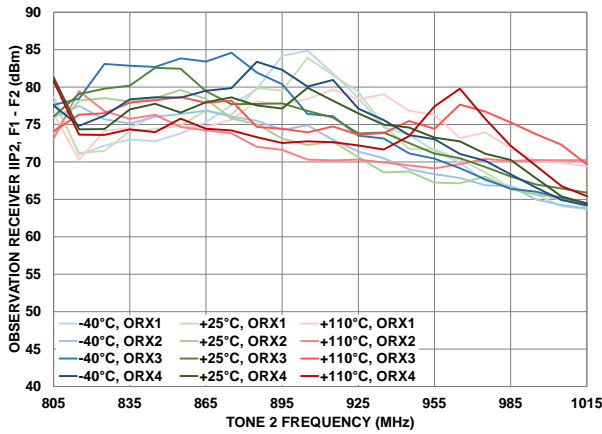


Figure 77. Observation Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

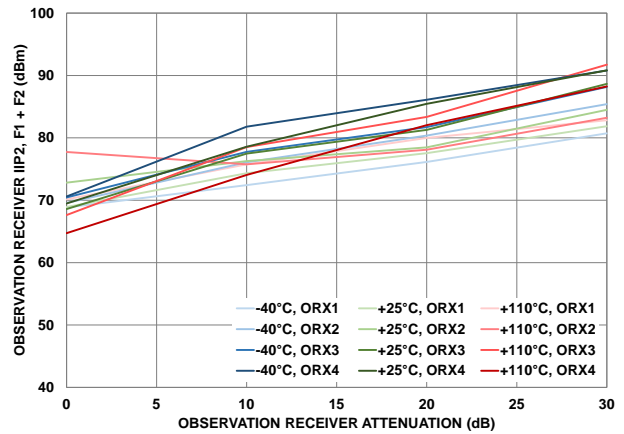


Figure 80. Observation Receiver IIP2, $f_1 + f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

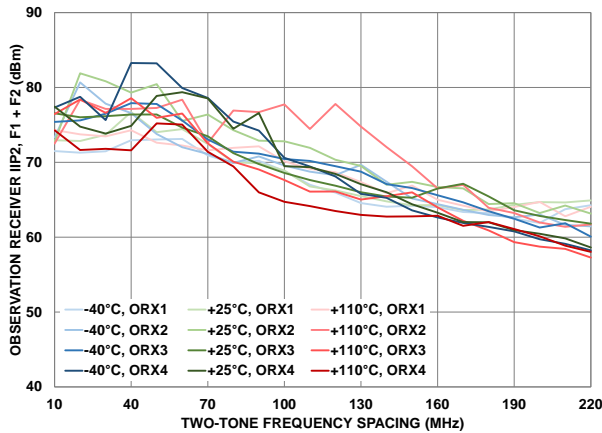


Figure 78. Observation Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

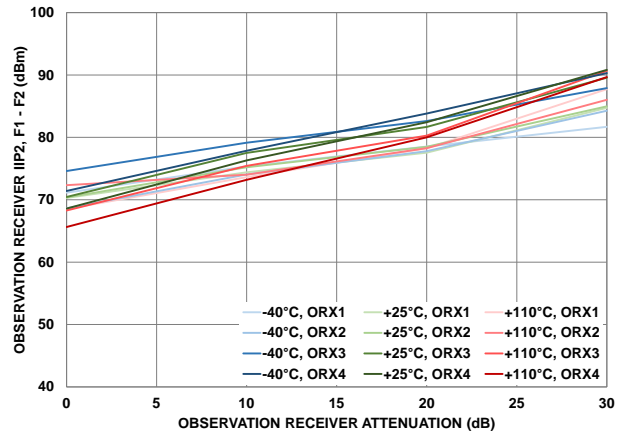


Figure 81. Observation Receiver IIP2, $f_1 - f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

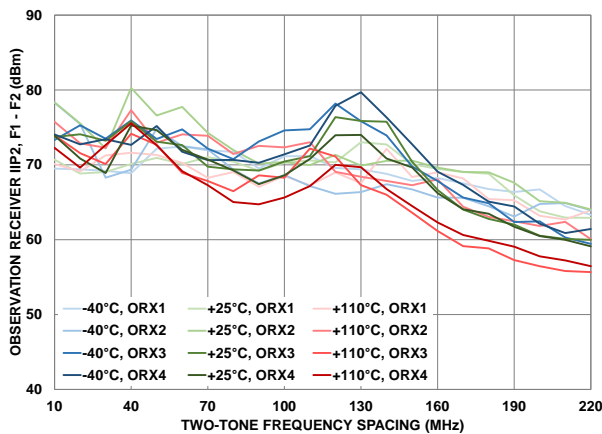


Figure 79. Observation Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

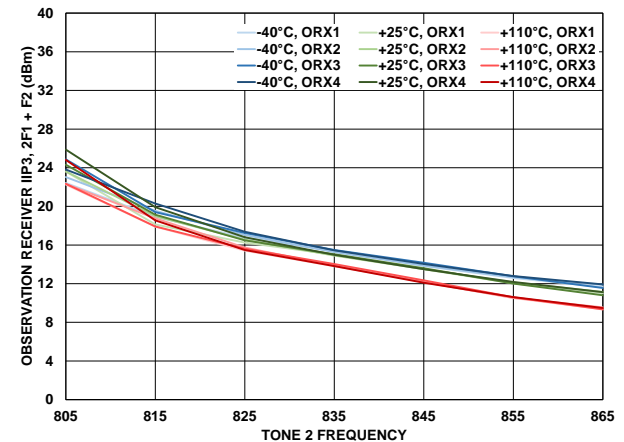


Figure 82. Observation Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

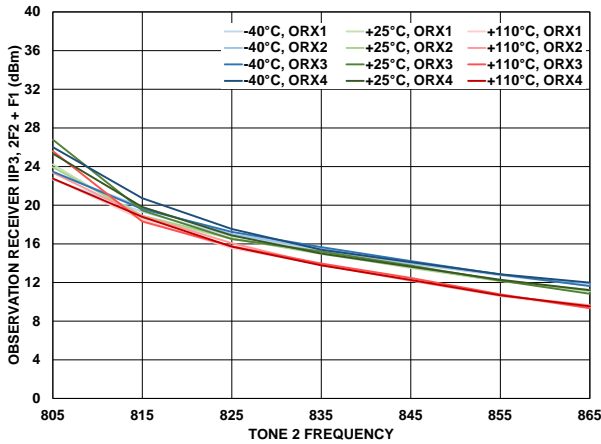


Figure 83. Observation Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

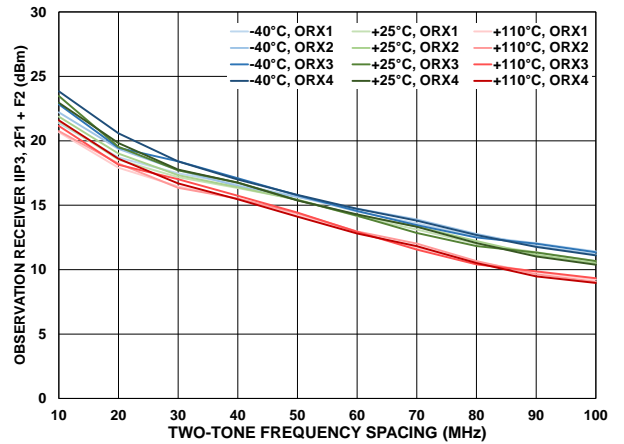


Figure 86. Observation Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

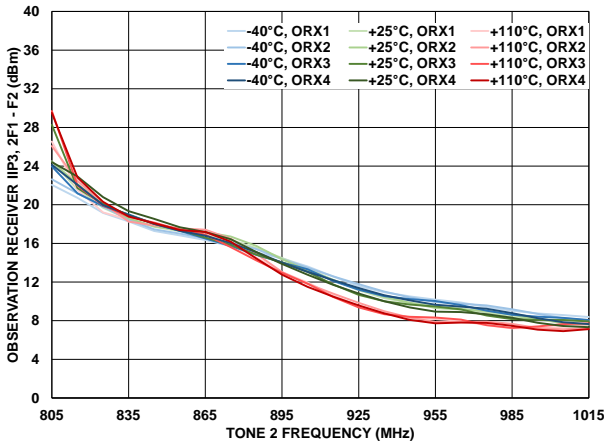


Figure 84. Observation Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

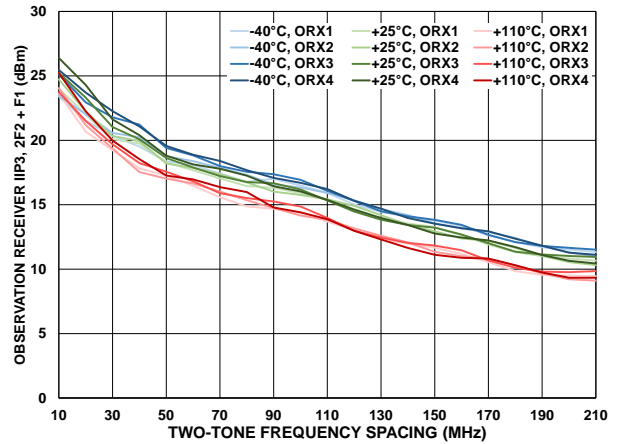


Figure 87. Observation Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

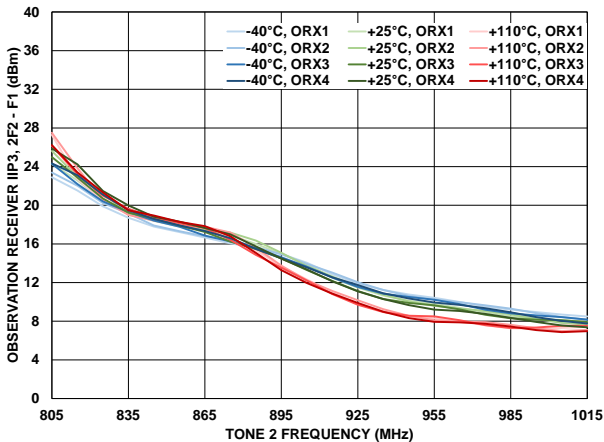


Figure 85. Observation Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

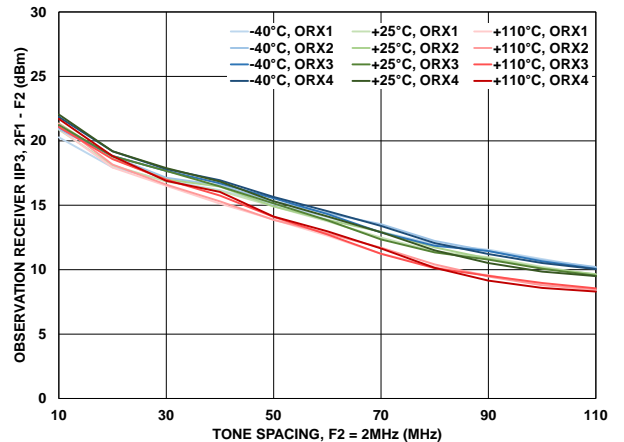


Figure 88. Observation Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

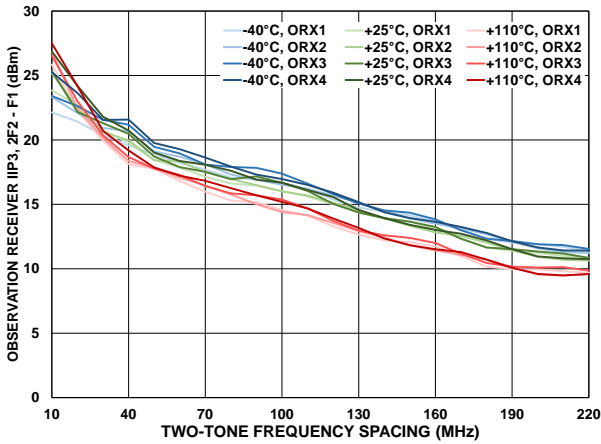


Figure 89. Observation Receiver IIP3, 2f2 - f1 vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, f2 = 2 MHz

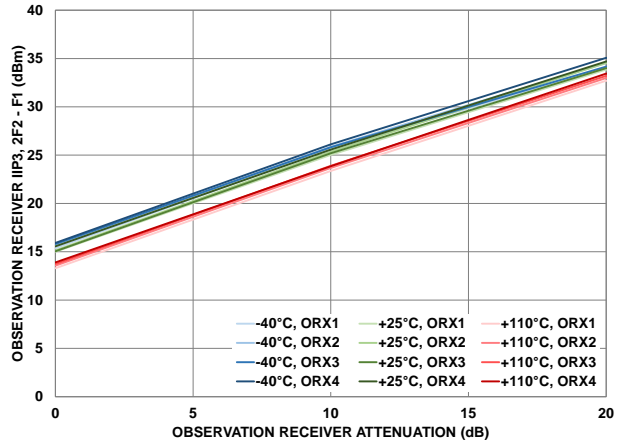


Figure 91. Observation Receiver IIP3, 2f2 - f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

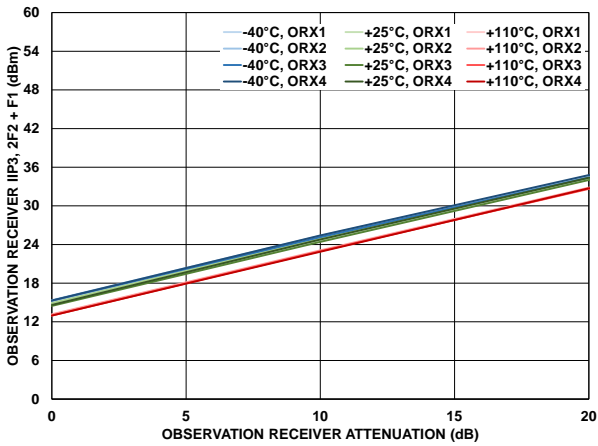


Figure 90. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

2600 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 2600 MHz, unless otherwise noted.

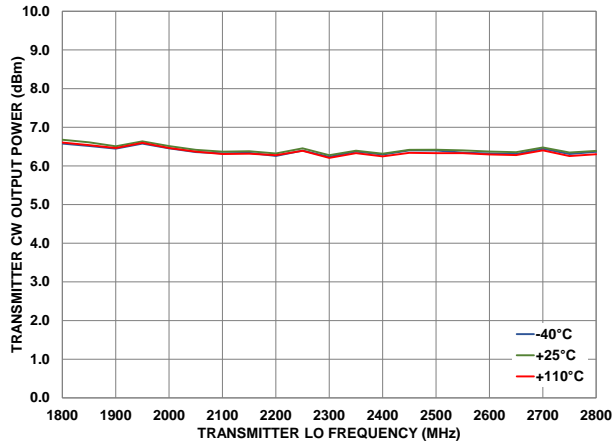


Figure 92. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

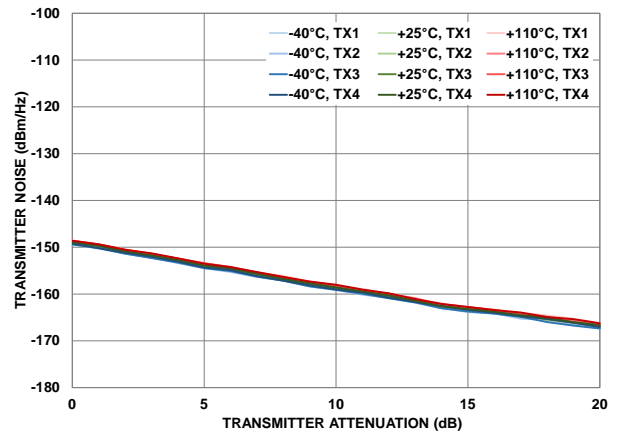


Figure 95. Transmitter Noise vs. Transmitter Attenuation, 10 MHz Offset

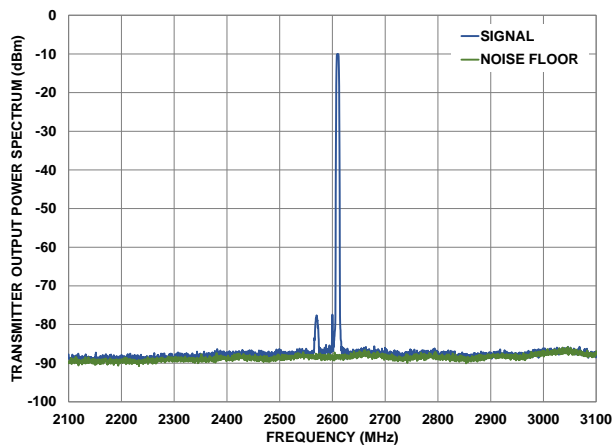


Figure 93. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, -10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

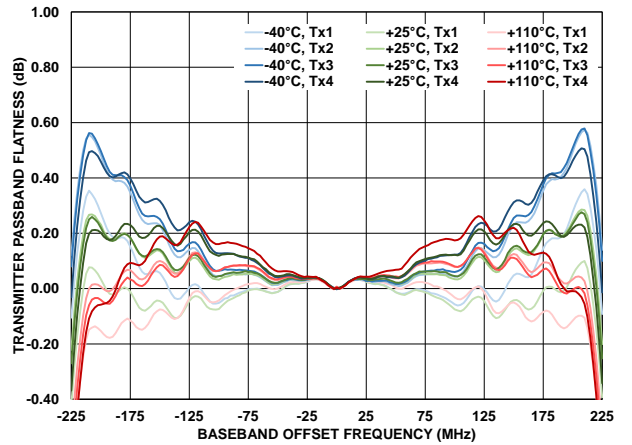


Figure 96. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

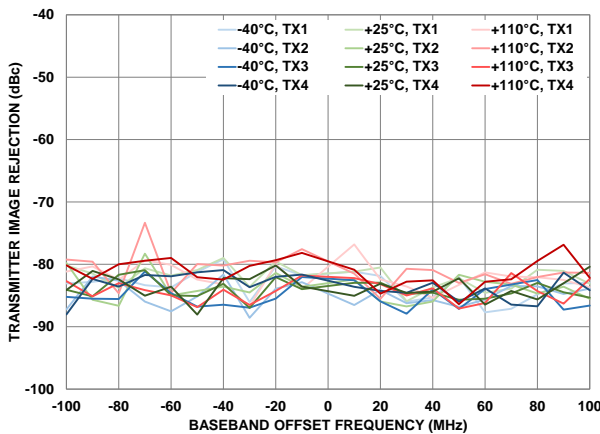


Figure 94. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency

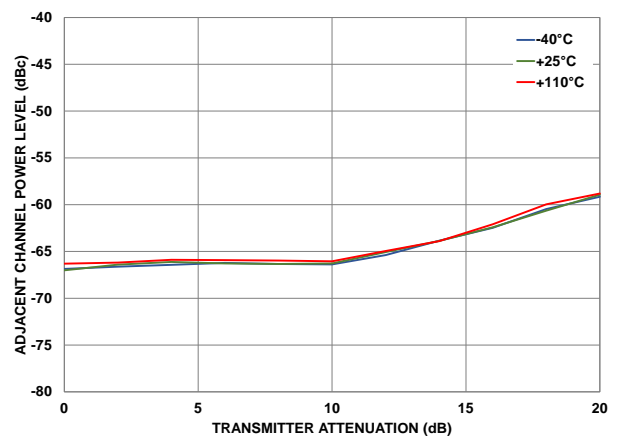


Figure 97. Adjacent Channel Power Level vs. Transmitter Attenuation, -10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

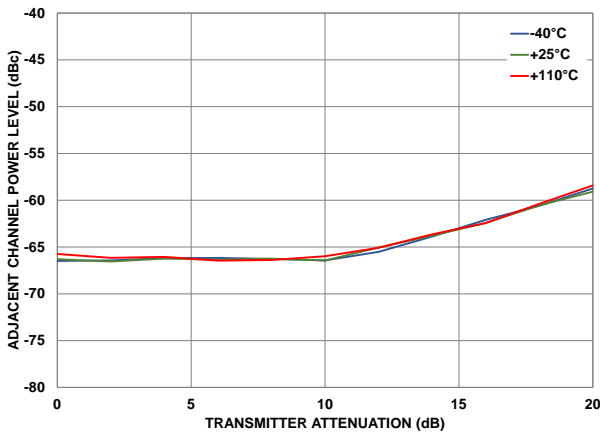


Figure 98. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

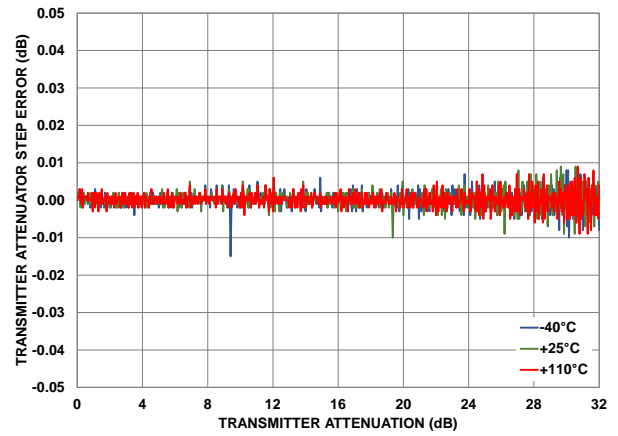


Figure 101. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

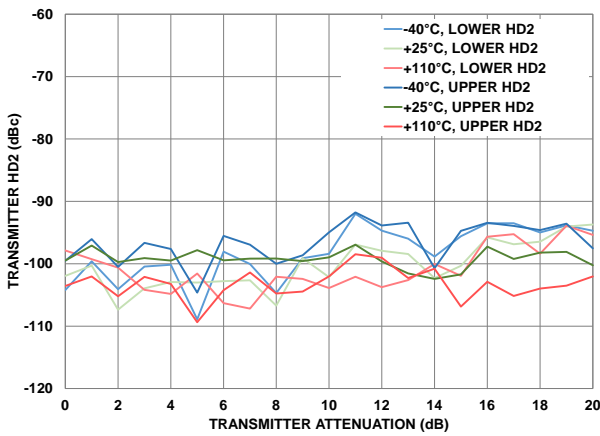


Figure 99. Transmitter Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 10 MHz Offset

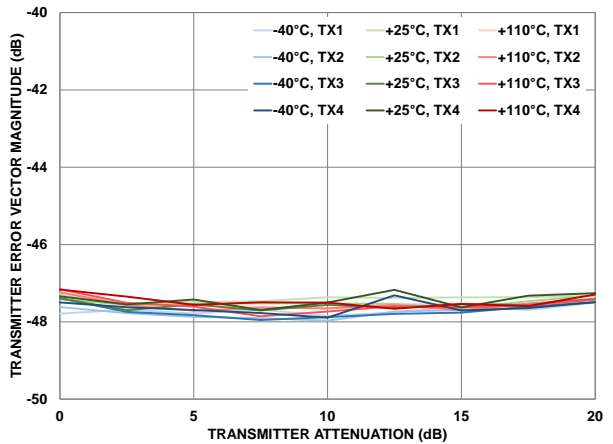


Figure 102. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

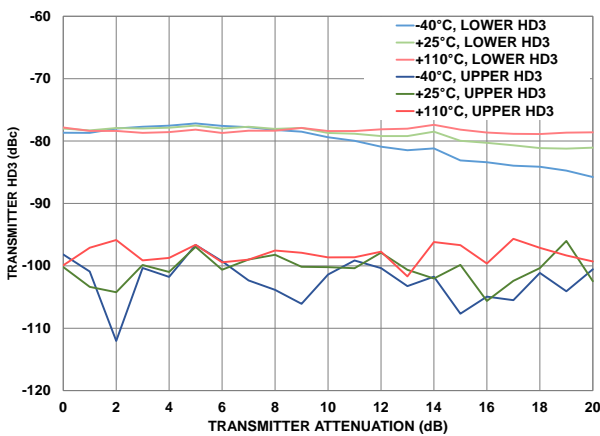


Figure 100. Transmitter Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 10 MHz Offset

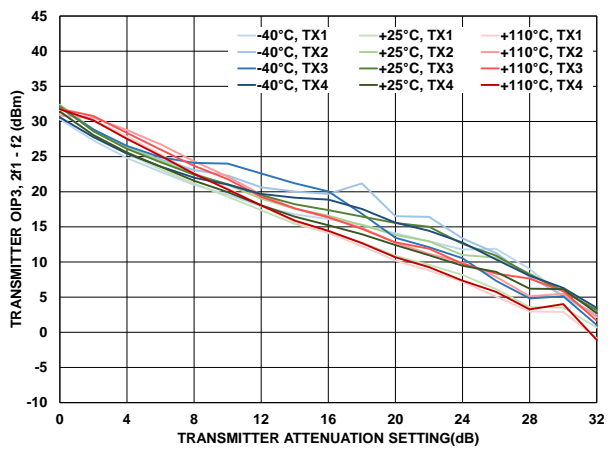


Figure 103. Transmitter OIP3, 2f1 - f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

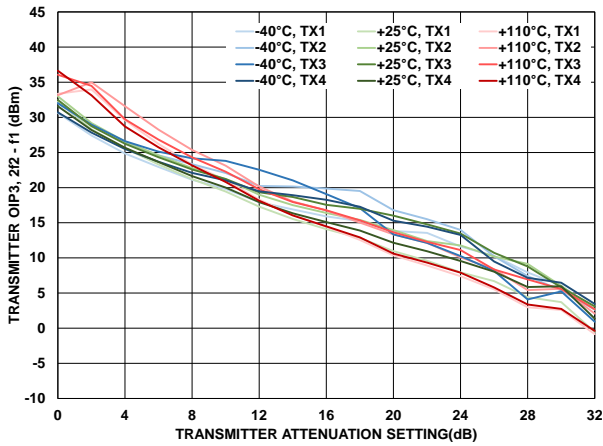


Figure 104. Transmitter OIP3, $2f_2 - f_1$ vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, $f_1 = 50.5$ MHz, $f_2 = 55.5$ MHz

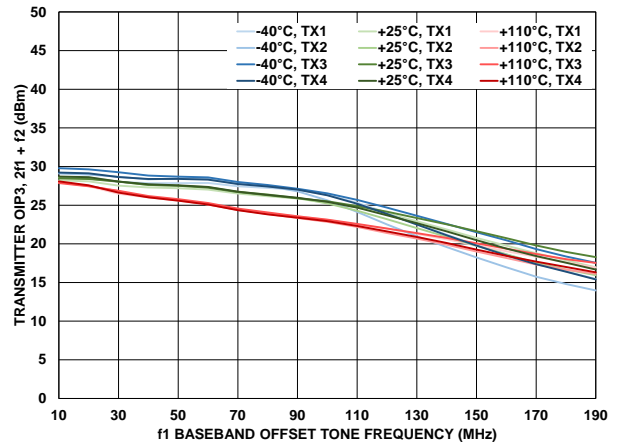


Figure 107. Transmitter OIP3, $2f_1 + f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

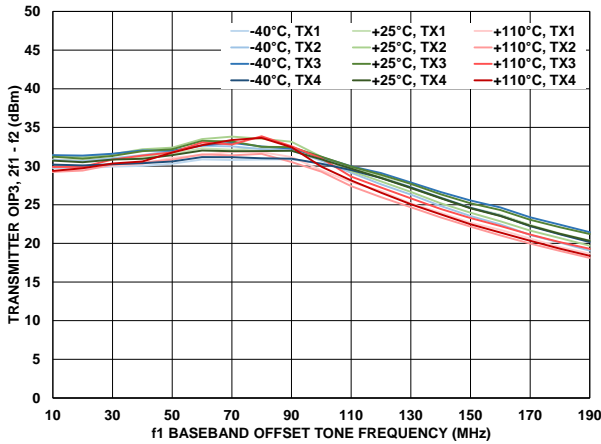


Figure 105. Transmitter OIP3, $2f_1 - f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

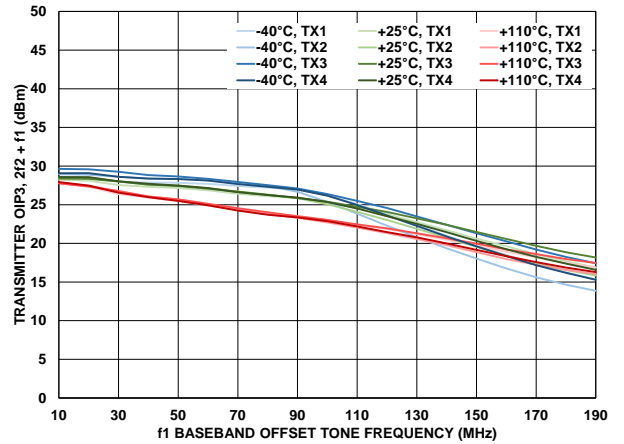


Figure 108. Transmitter OIP3, $2f_2 + f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

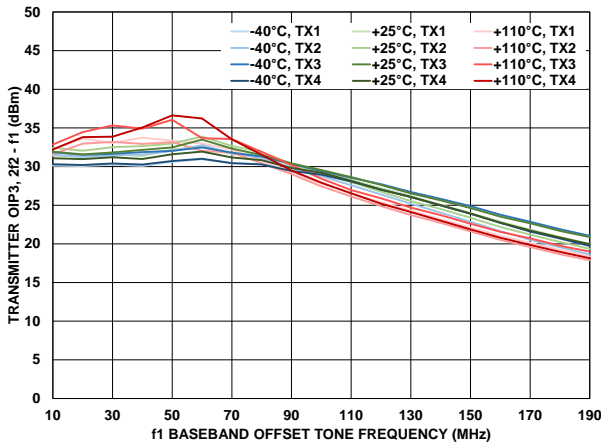


Figure 106. Transmitter OIP3, $2f_2 - f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

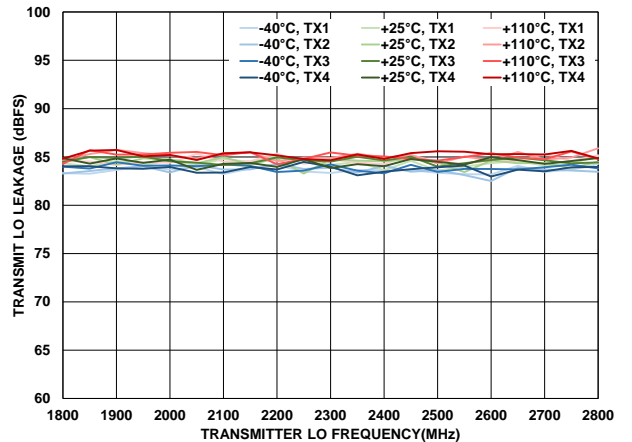


Figure 109. Transmitter LO Leakage vs. Transmitter LO Frequency

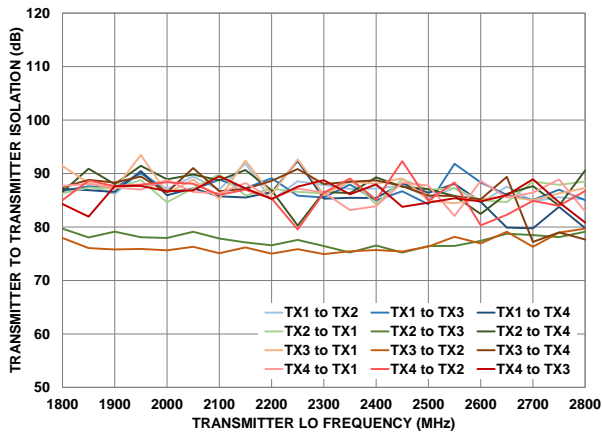


Figure 110. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

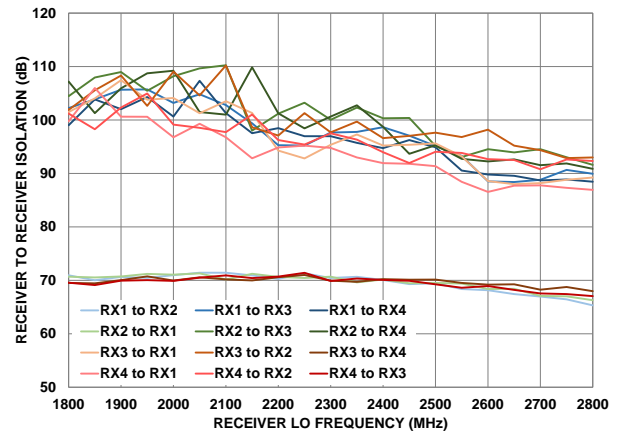


Figure 113. Receiver to Receiver Isolation vs. Receiver LO Frequency

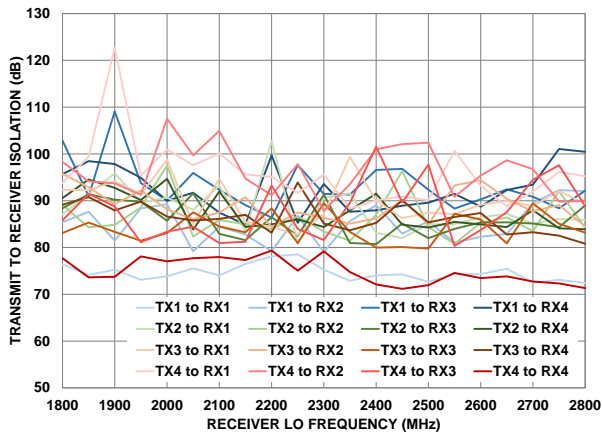


Figure 111. Transmitter to Receiver Isolation vs. Receiver LO Frequency

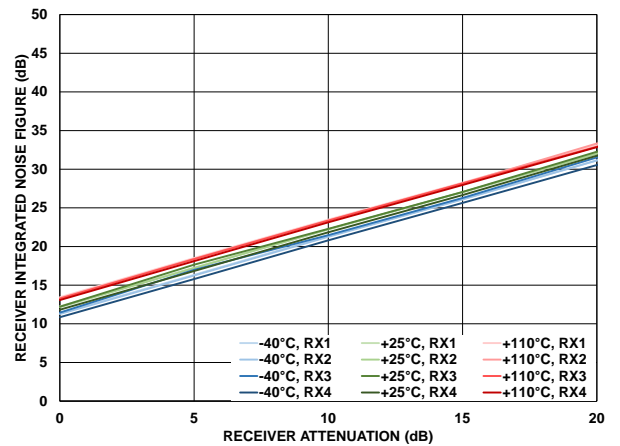


Figure 114. Receiver Integrated Noise Figure vs. Receiver Attenuation, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

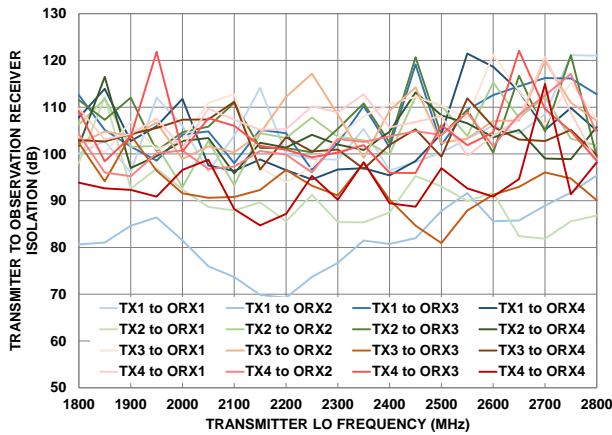


Figure 112. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

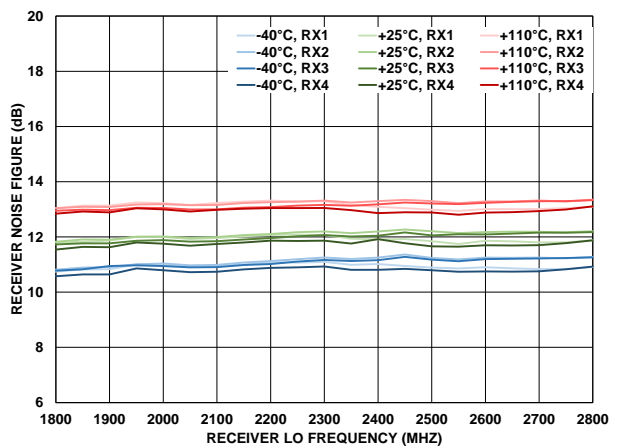


Figure 115. Receiver Integrated Noise Figure vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

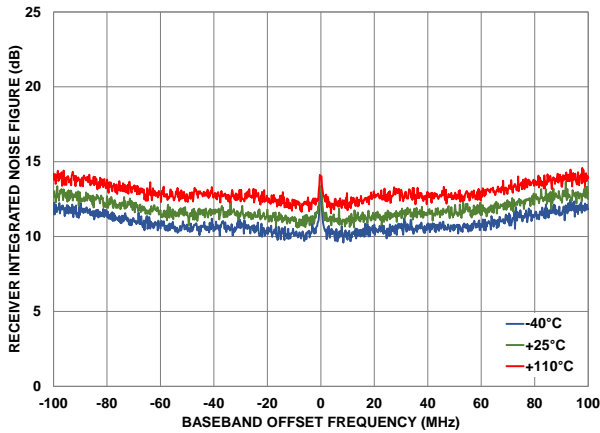


Figure 116. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

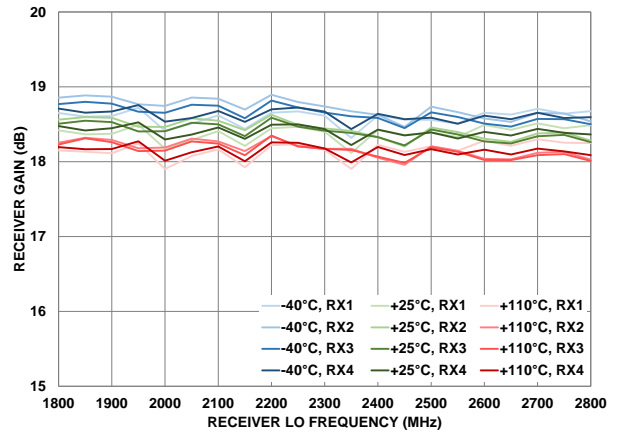


Figure 119. Receiver Gain vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

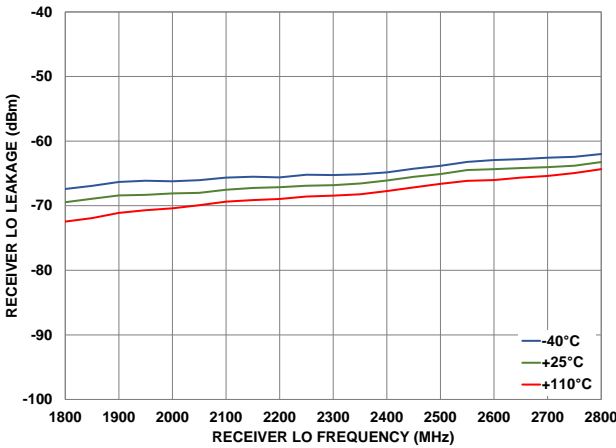


Figure 117. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

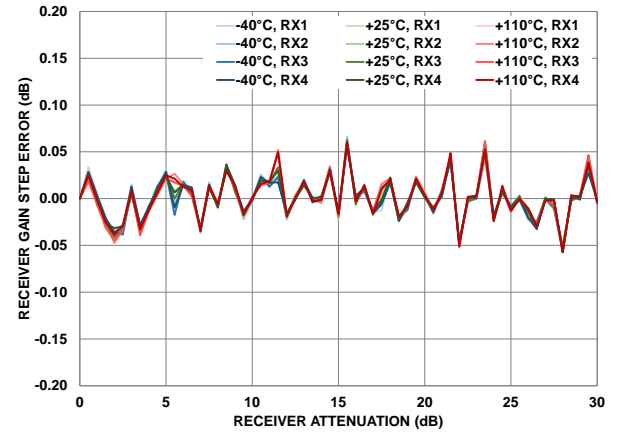


Figure 120. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

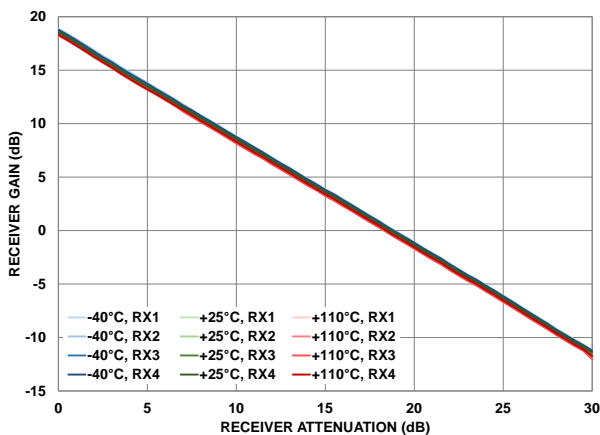


Figure 118. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

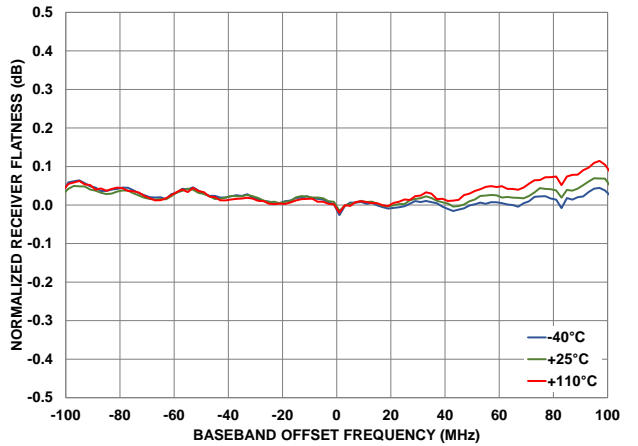


Figure 121. Normalized Receiver Flatness vs. Baseband Offset Frequency, -5 dBFS Input Signal

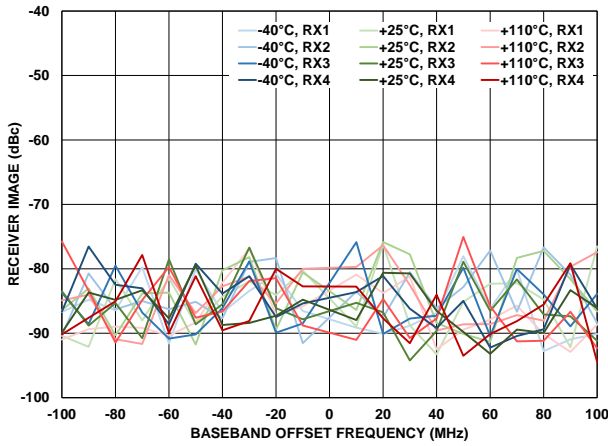


Figure 122. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS

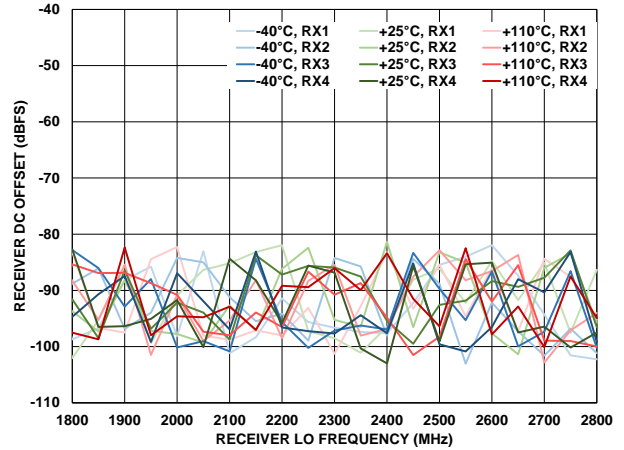


Figure 125. Receiver DC Offset vs. Receiver LO Frequency, 20 MHz Offset, -5 dBFS Input Signal

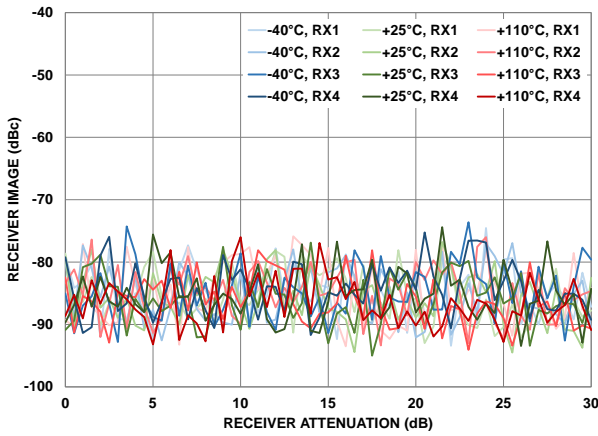


Figure 123. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS

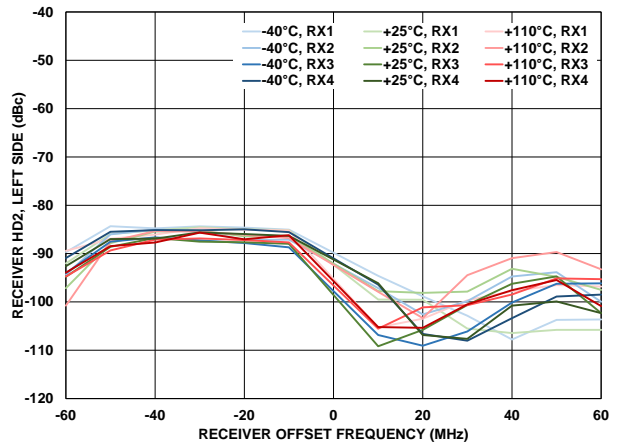


Figure 126. Receiver HD2, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

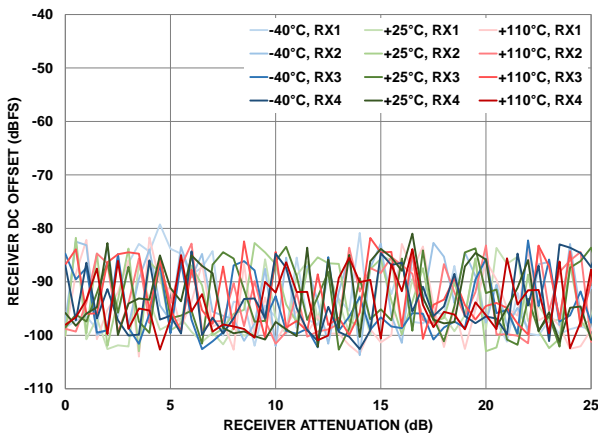


Figure 124. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

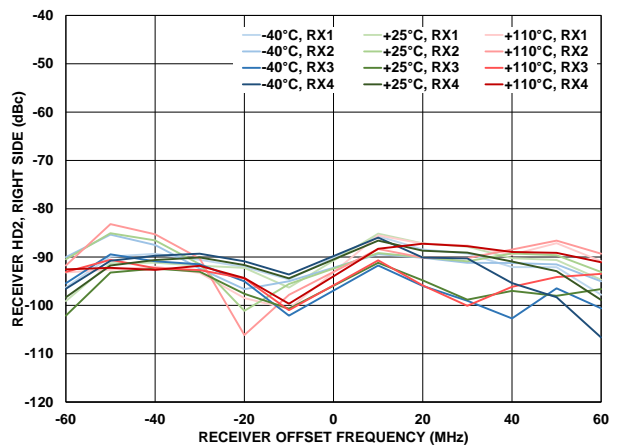


Figure 127. Receiver HD2, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

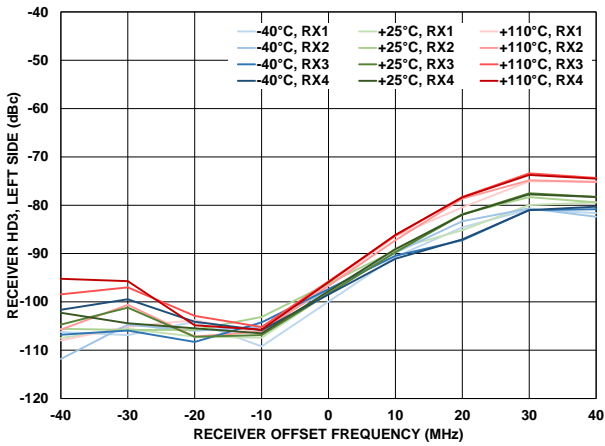


Figure 128. Receiver HD3, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

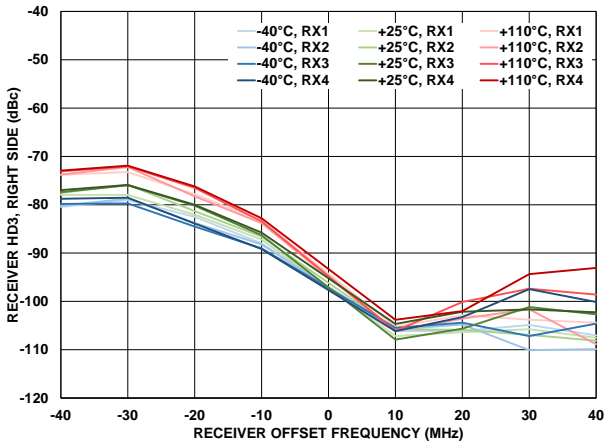


Figure 129. Receiver HD3, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

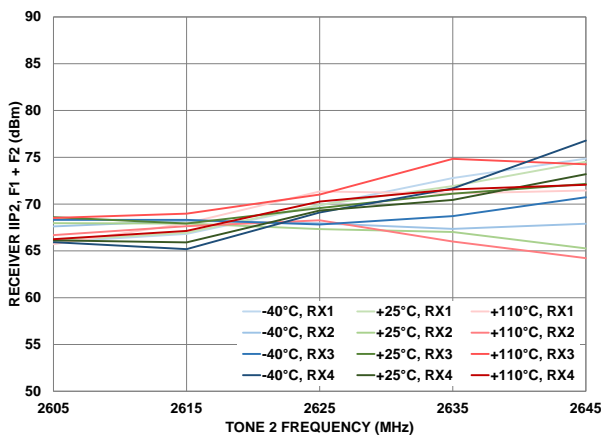


Figure 130. Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

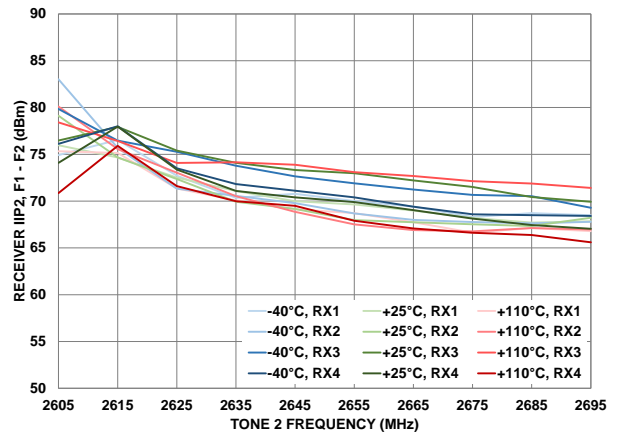


Figure 131. Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

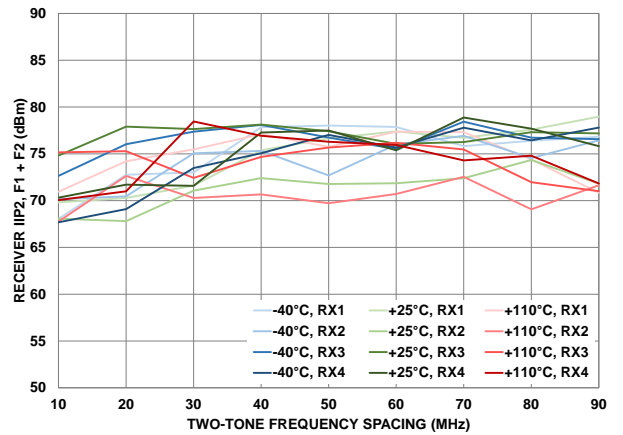


Figure 132. Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

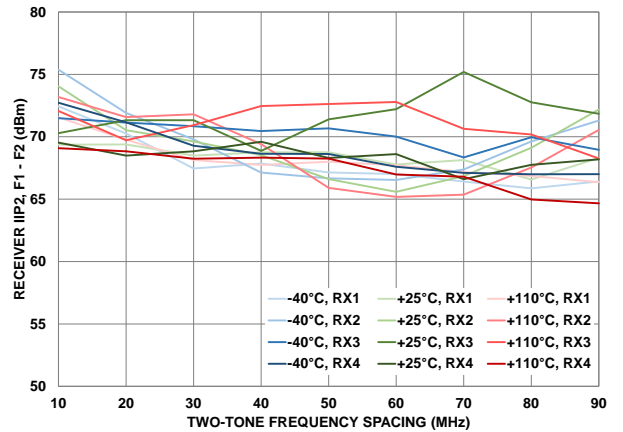


Figure 133. Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

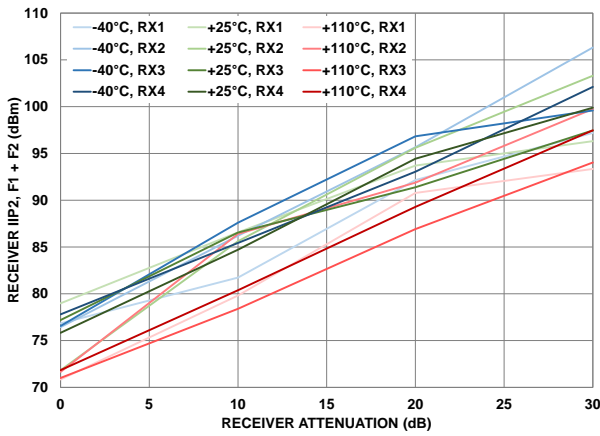


Figure 134. Receiver IIP2, $f_1 + f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

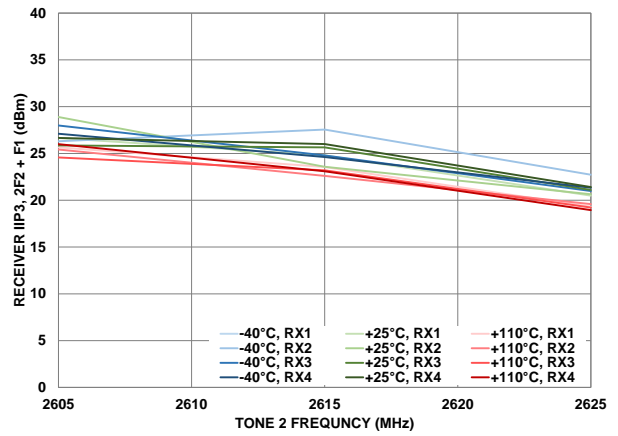


Figure 137. Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

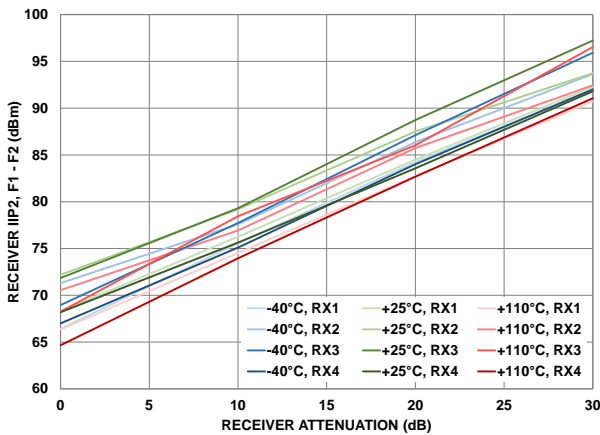


Figure 135. Receiver IIP2, $f_1 - f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

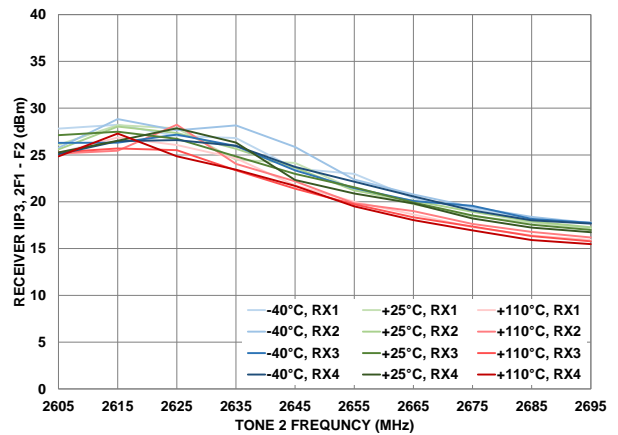


Figure 138. Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

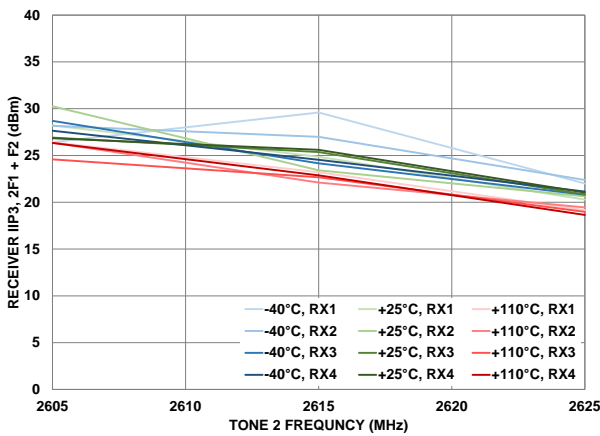


Figure 136. Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

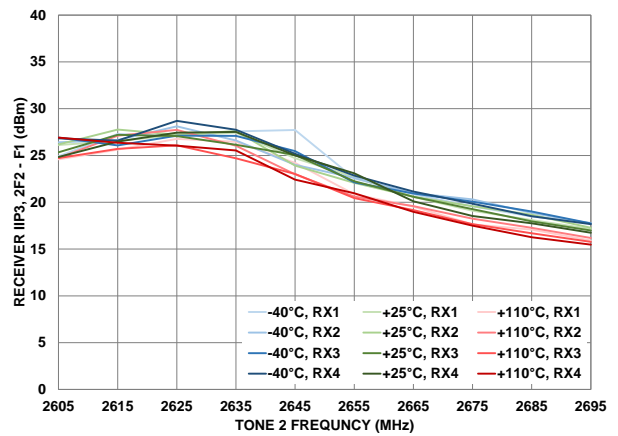


Figure 139. Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

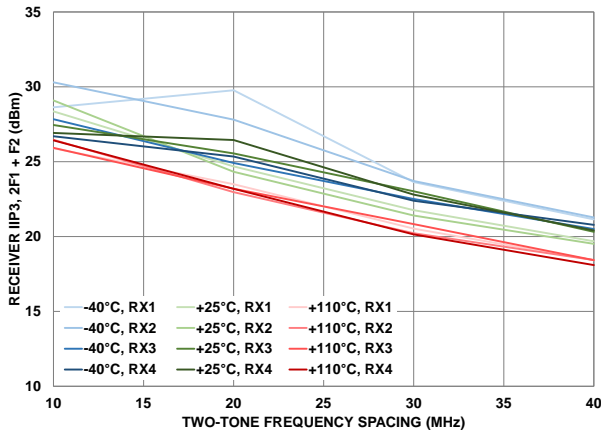


Figure 140. Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

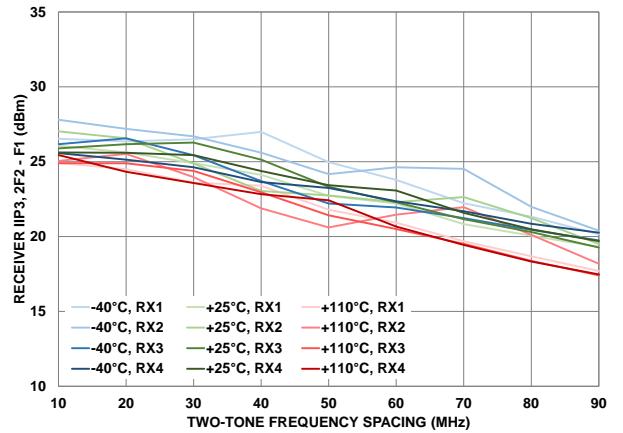


Figure 143. Receiver IIP3, $2f_2 - f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

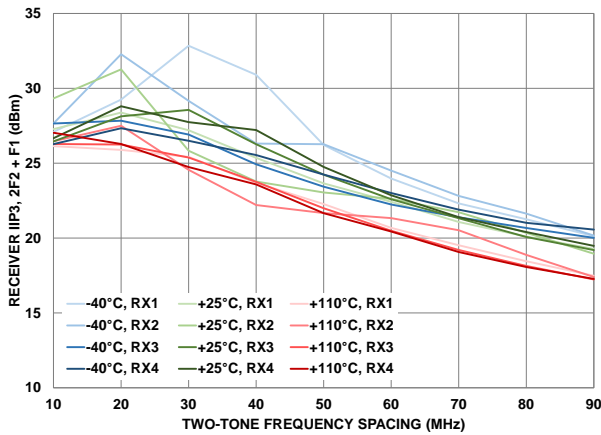


Figure 141. Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

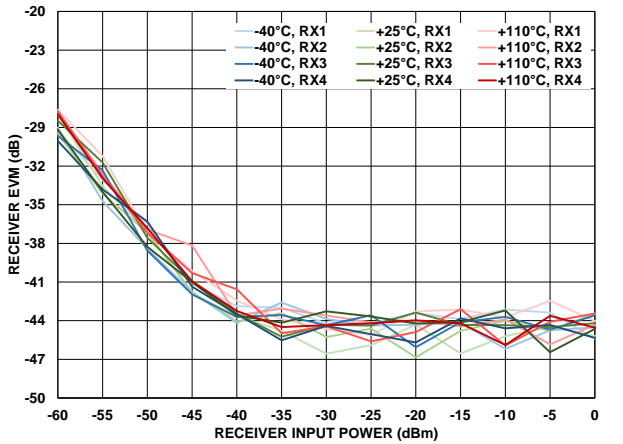


Figure 144. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

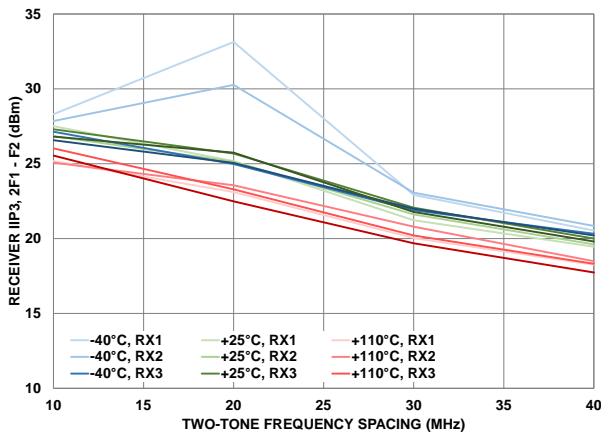


Figure 142. Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

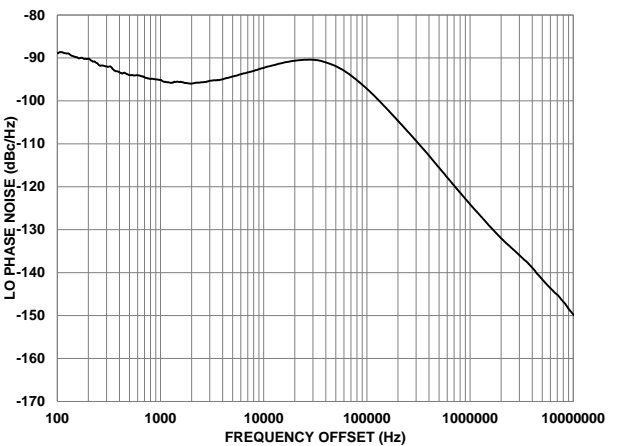


Figure 145. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

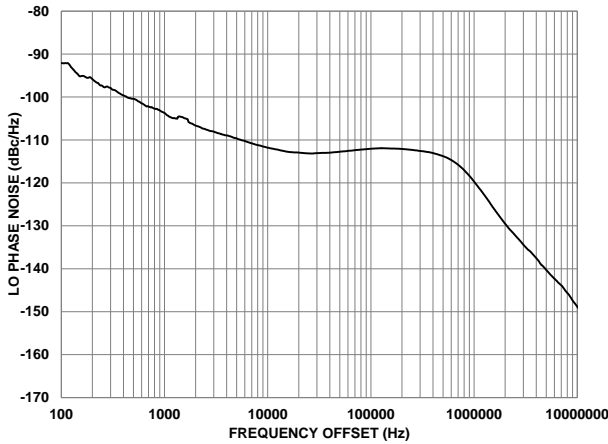


Figure 146. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 60°

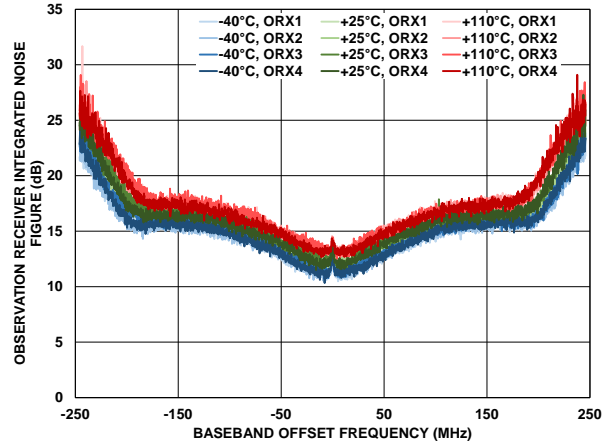


Figure 149. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

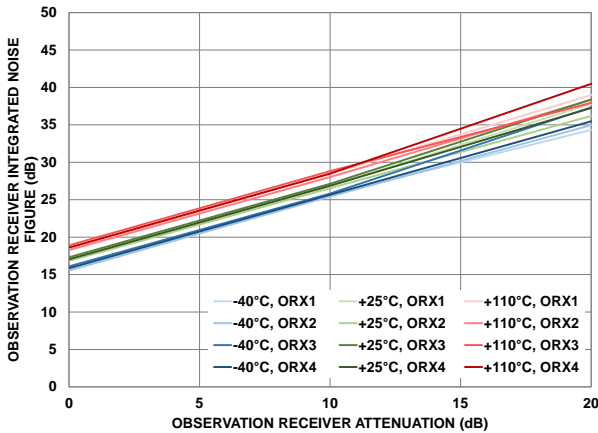


Figure 147. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

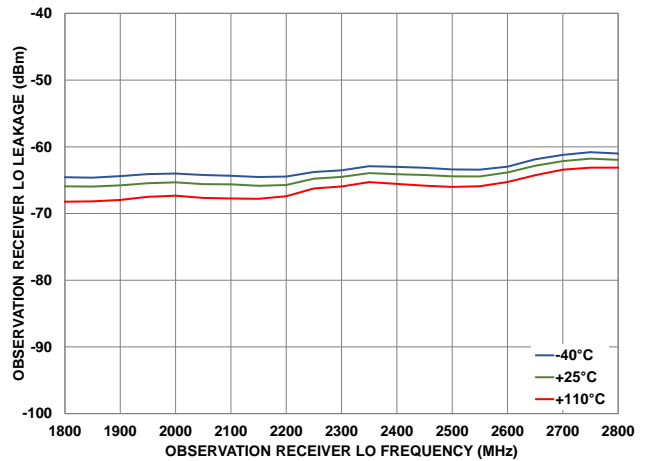


Figure 150. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

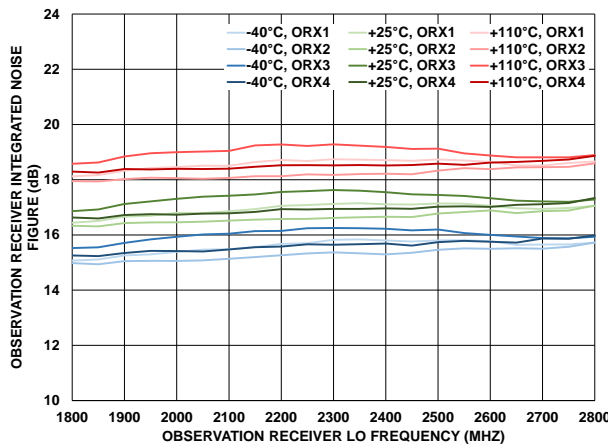


Figure 148. Observation Receiver Integrated Noise Figure vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

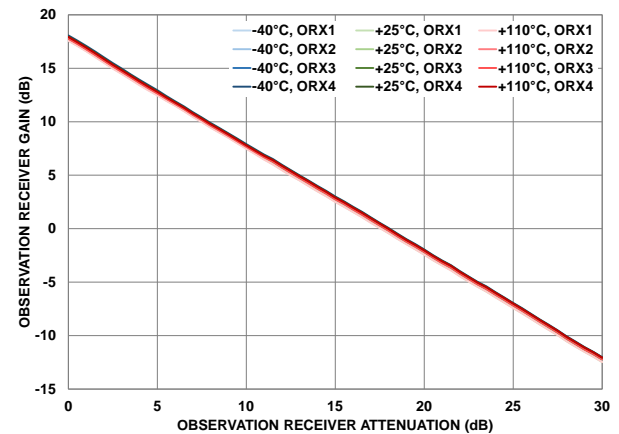


Figure 151. Observation Receiver Gain vs. Observation Receiver Attenuation, 45 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

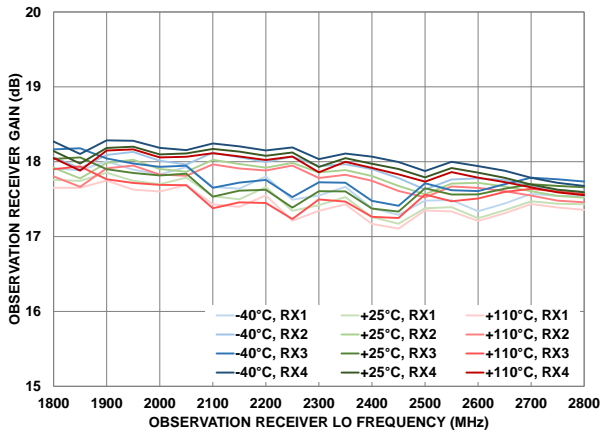


Figure 152. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

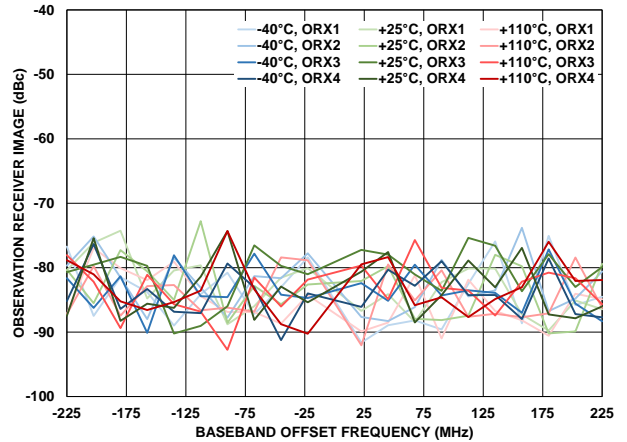


Figure 155. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

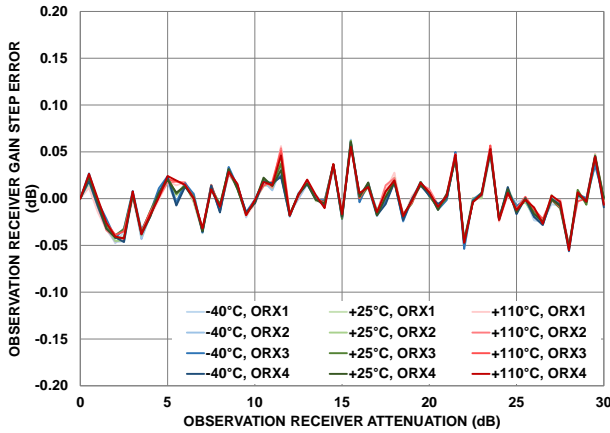


Figure 153. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 45 MHz Offset, -10 dBFS Input Signal

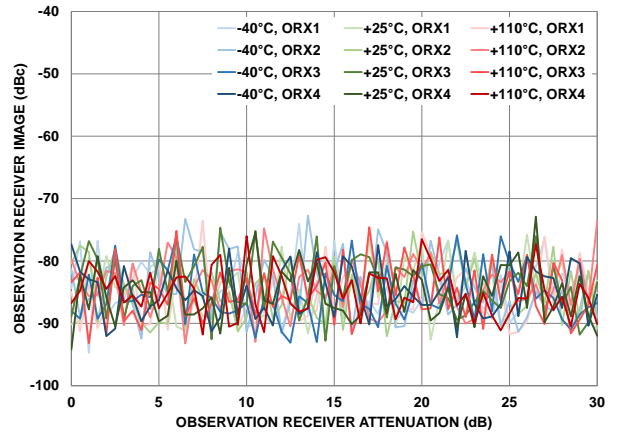


Figure 156. Observation Receiver Image vs. Observation Receiver Attenuation, 45 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

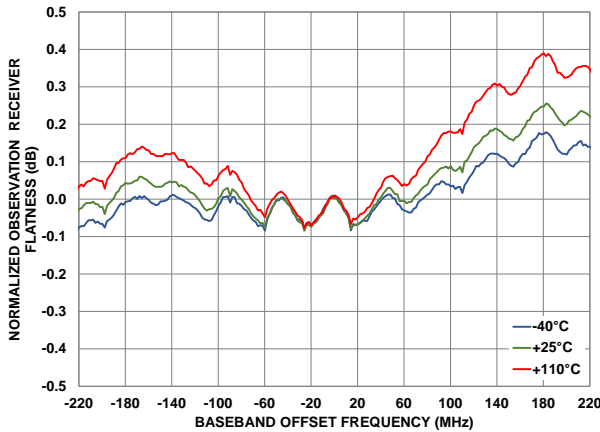


Figure 154. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, -10 dBFS Input Signal

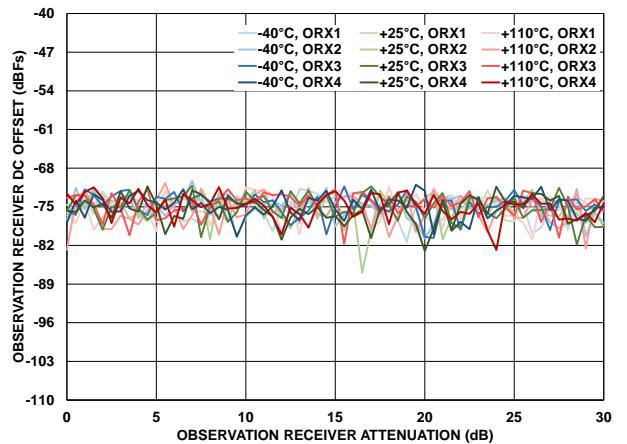


Figure 157. Observation Receiver DC Offset vs. Observation Receiver Attenuation, 45MHz Offset, -10 dBFS Input Signal

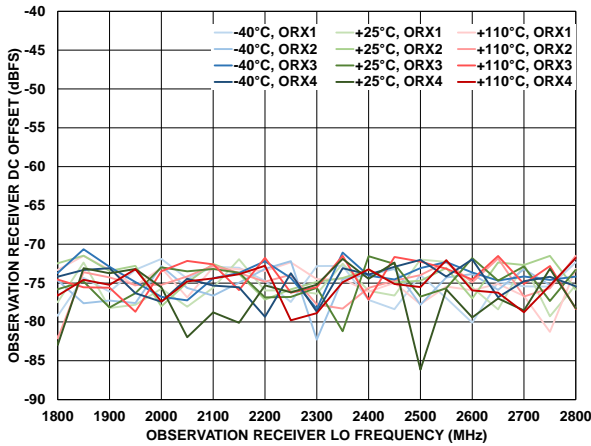


Figure 158. Observation Receiver DC Offset vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

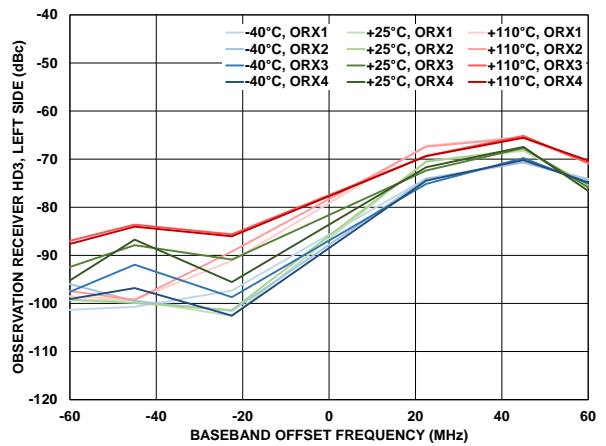


Figure 161. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

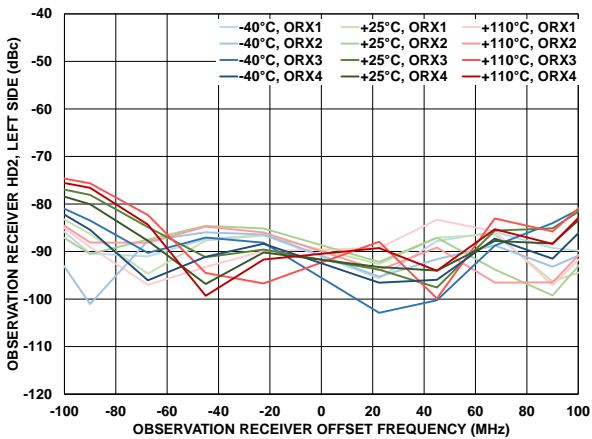


Figure 159. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

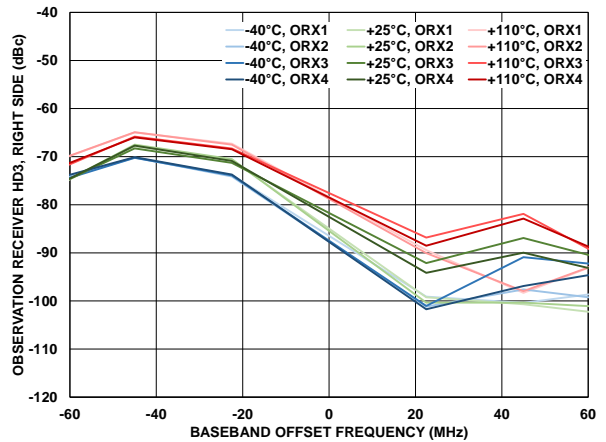


Figure 162. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

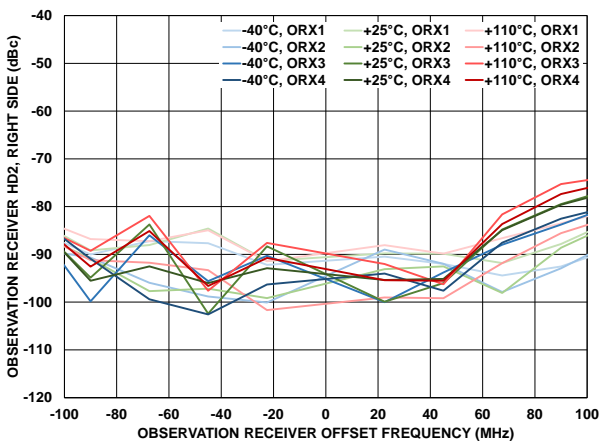


Figure 160. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

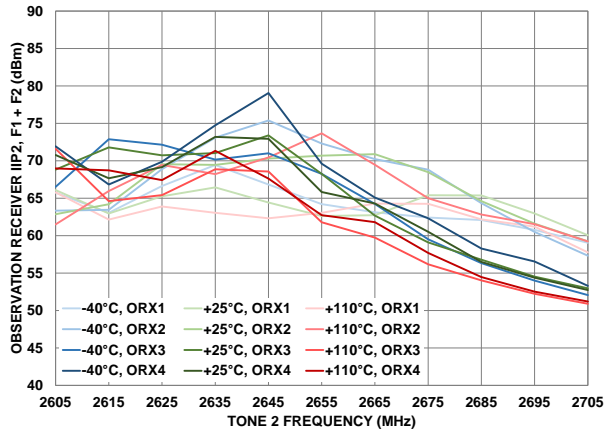


Figure 163. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at -13 dBFS, f1 = f2 + 2 MHz

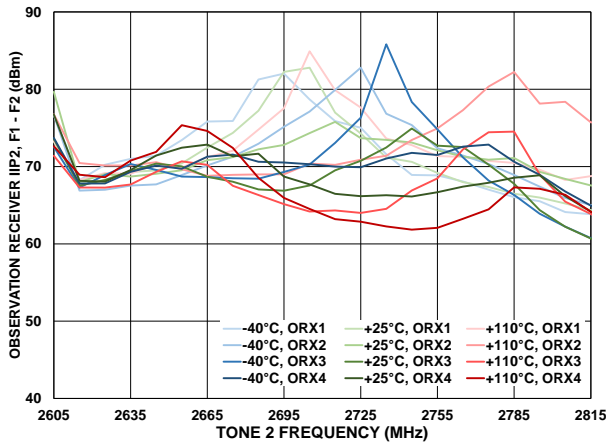


Figure 164. Observation Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

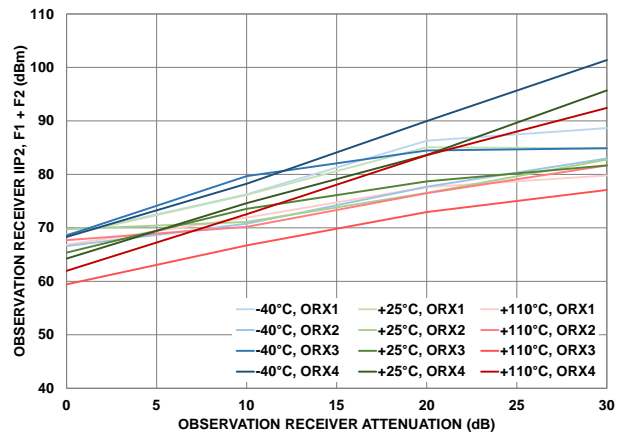


Figure 167. Observation Receiver IIP2, $f_1 + f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

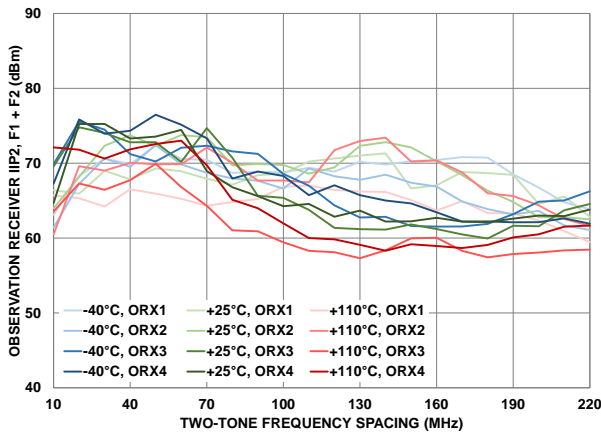


Figure 165. Observation Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

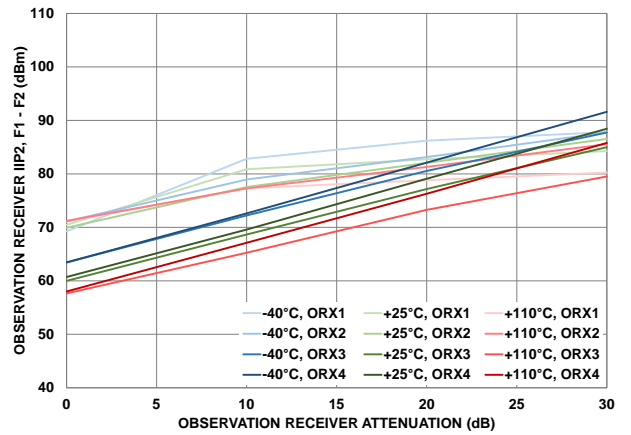


Figure 168. Observation Receiver IIP2, $f_1 - f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

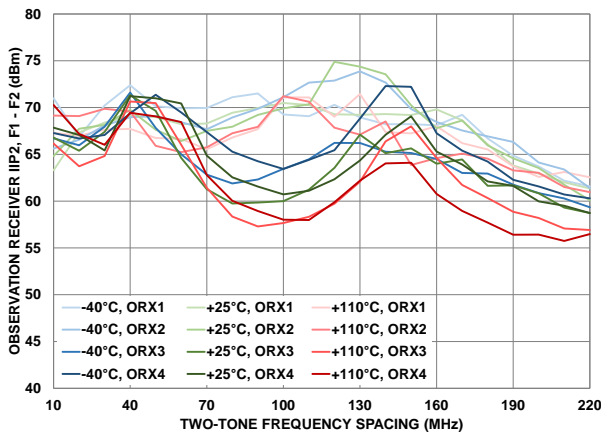


Figure 166. Observation Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

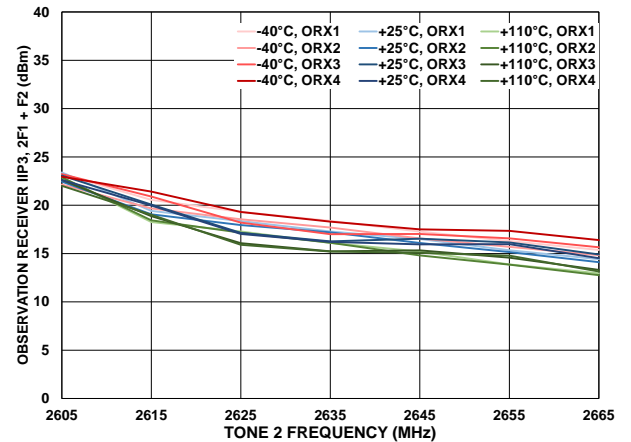


Figure 169. Observation Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

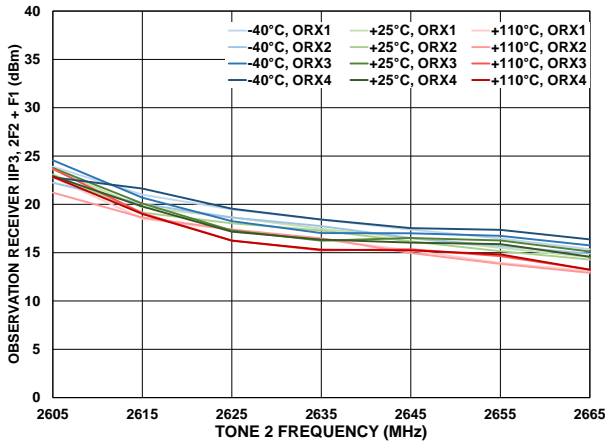


Figure 170. Observation Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

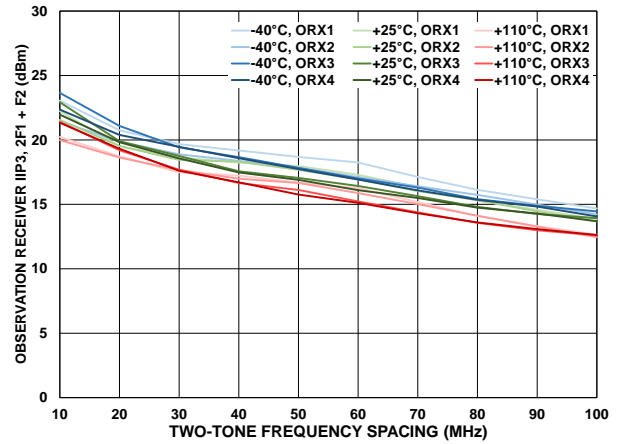


Figure 173. Observation Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

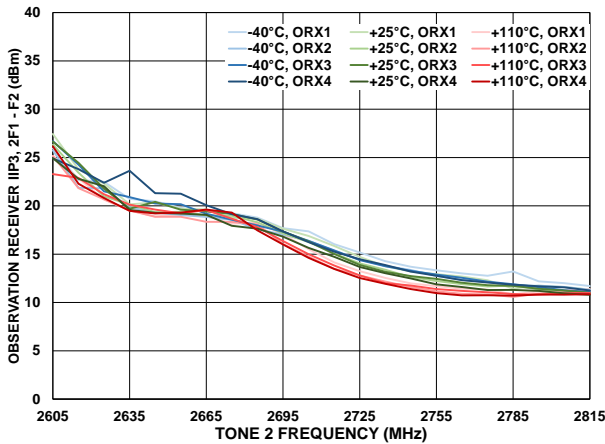


Figure 171. Observation Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

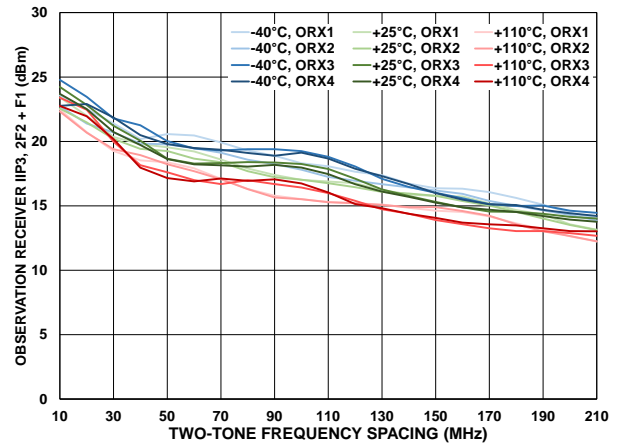


Figure 174. Observation Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

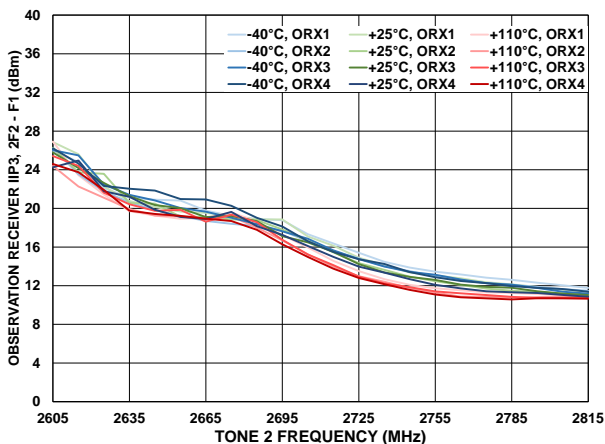


Figure 172. Observation Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

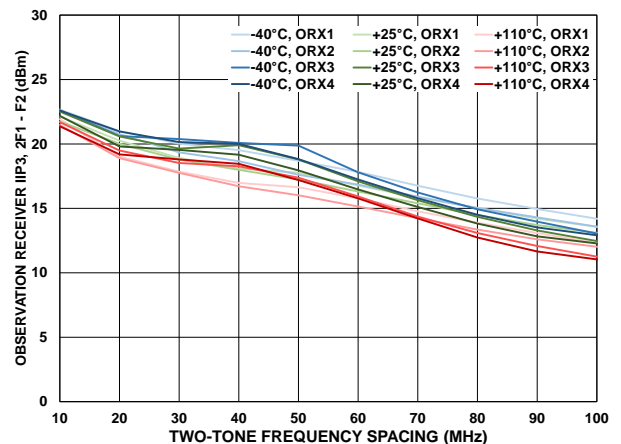


Figure 175. Observation Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

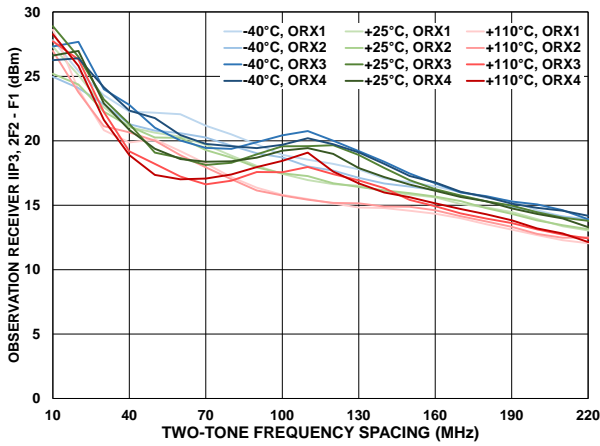


Figure 176. Observation Receiver IIP3, 2f2 - f1 vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, f2 = 2 MHz

Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

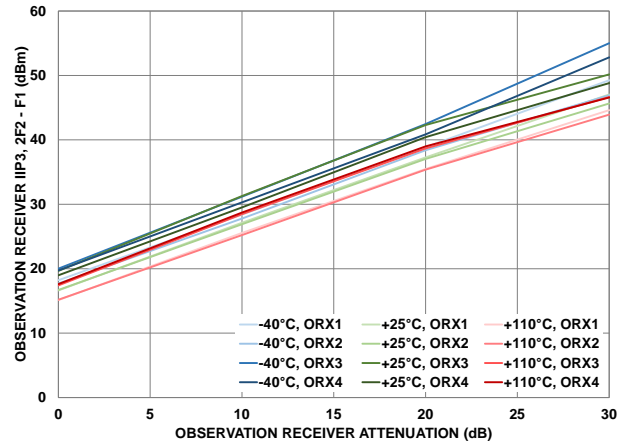


Figure 178. Observation Receiver IIP3, 2f2 - f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

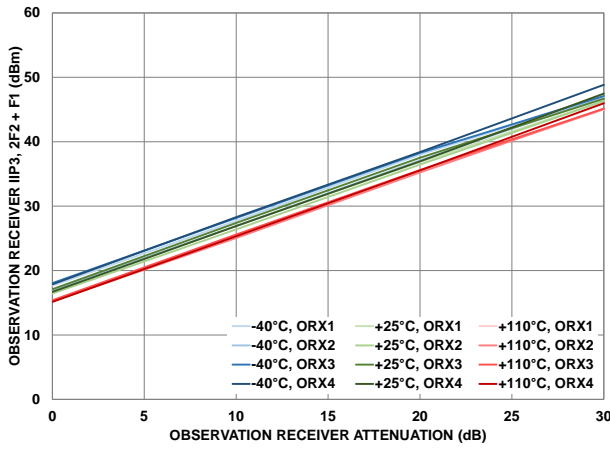


Figure 177. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

3800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 3800 MHz, unless otherwise noted.

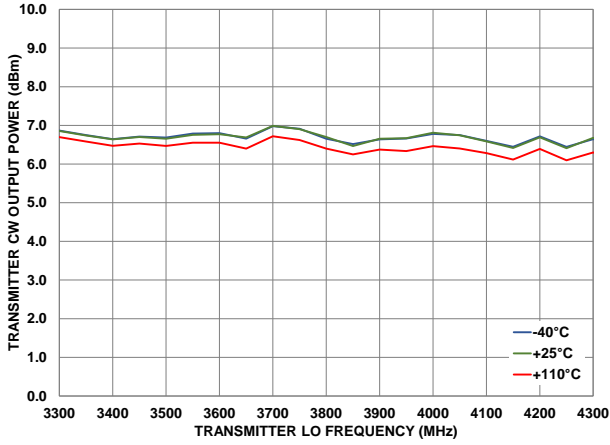


Figure 179. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

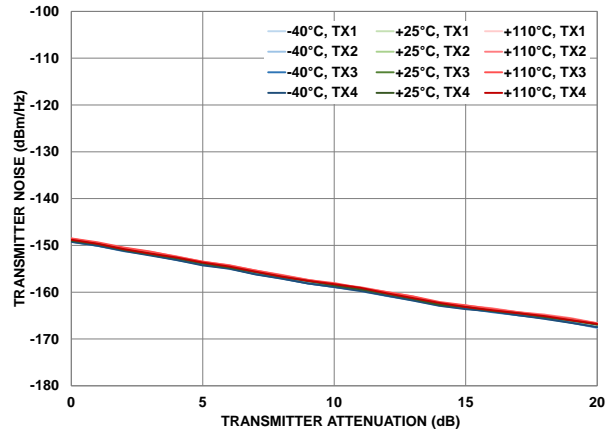


Figure 182. Transmitter Noise vs. Transmitter Attenuation, 10 MHz Offset Frequency

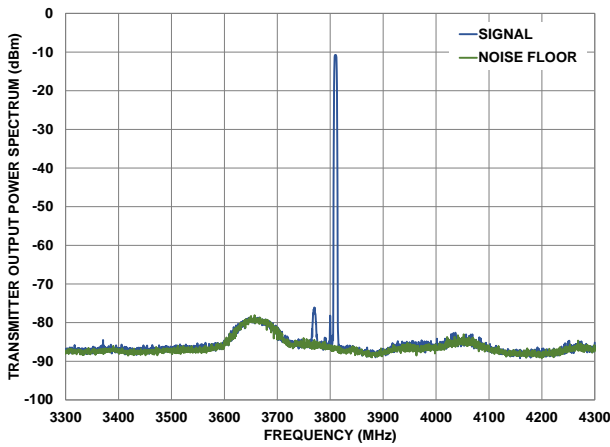


Figure 180. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, -10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C (Step at 3600 MHz Due to Spectrum Analyzer)

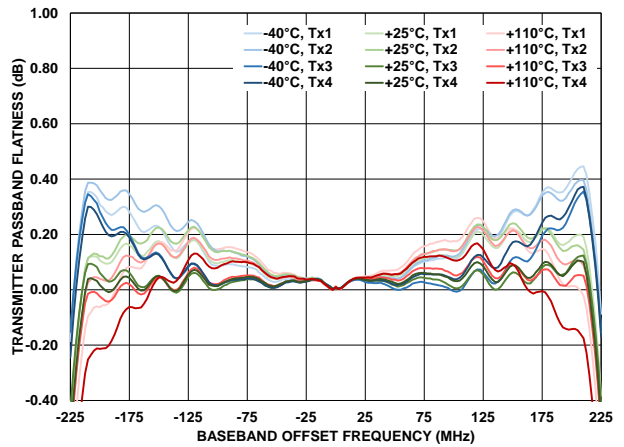


Figure 183. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

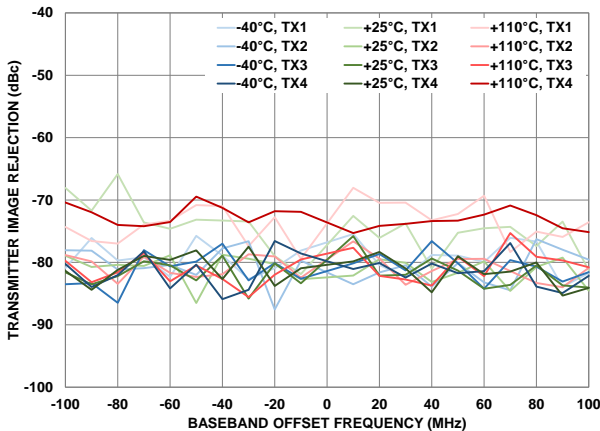


Figure 181. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency

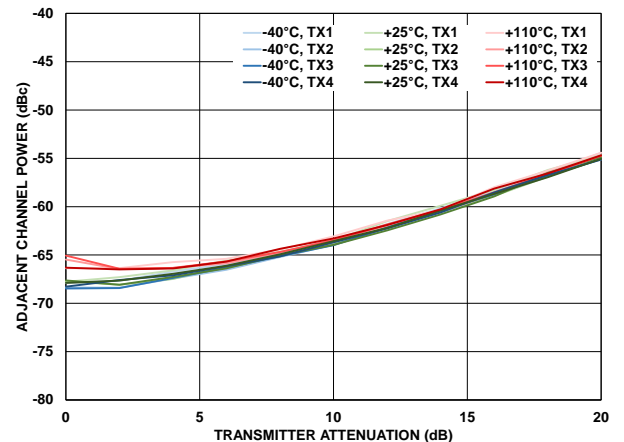


Figure 184. Adjacent Channel Power Level vs. Transmitter Attenuation, -10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

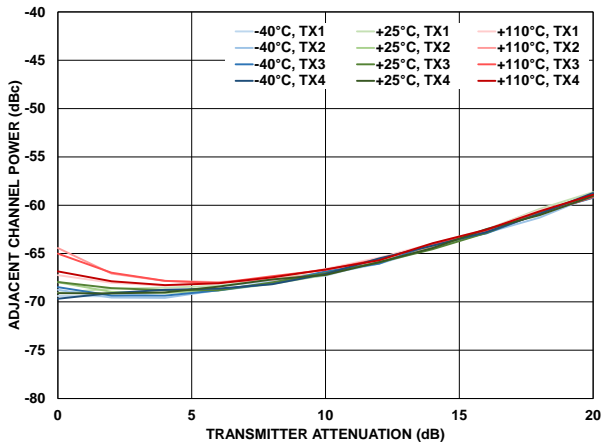


Figure 185. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

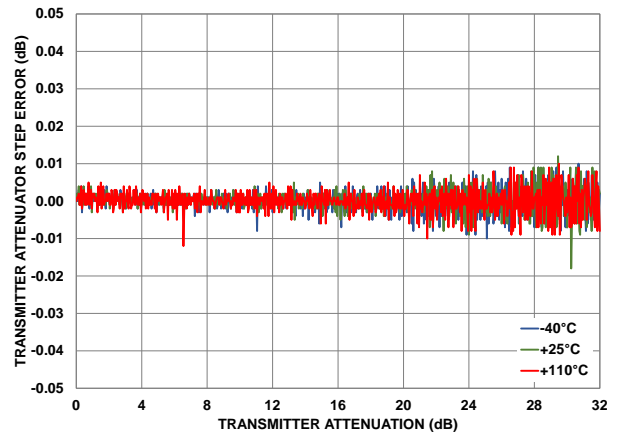


Figure 188. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

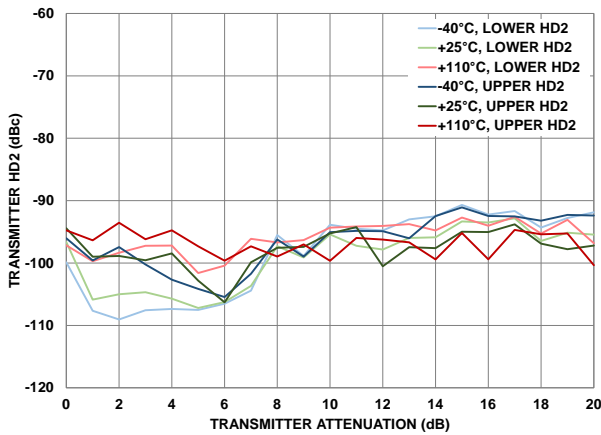


Figure 186. Transmitter Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 10 MHz Offset

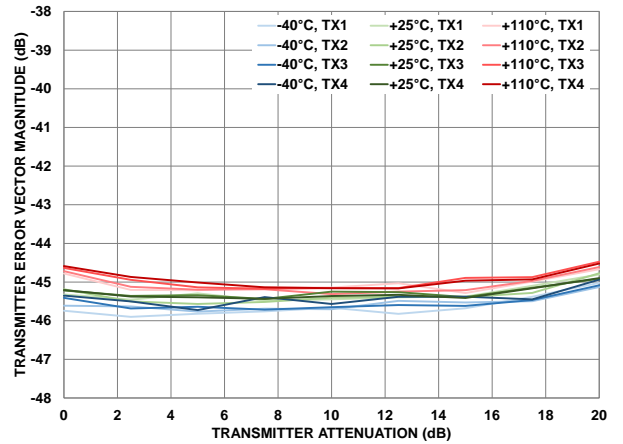


Figure 189. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MS/PS, Loop Filter Bandwidth = 200 kHz, Loop Filter Phase Margin = 60°

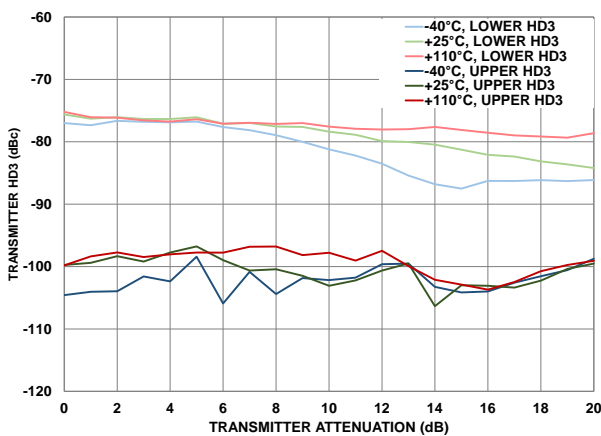


Figure 187. Transmitter Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 10 MHz Offset

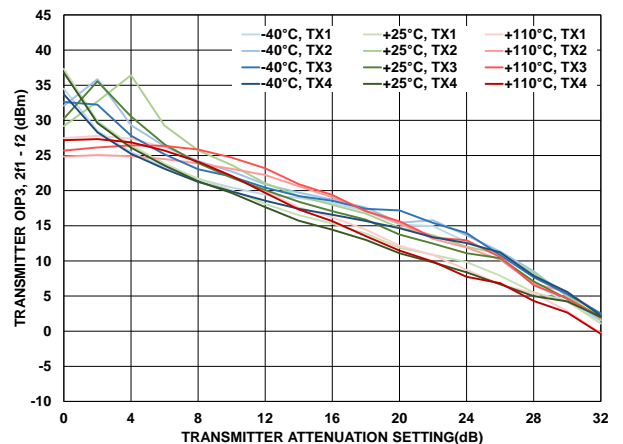


Figure 190. Transmitter OIP3, 2f1 - f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

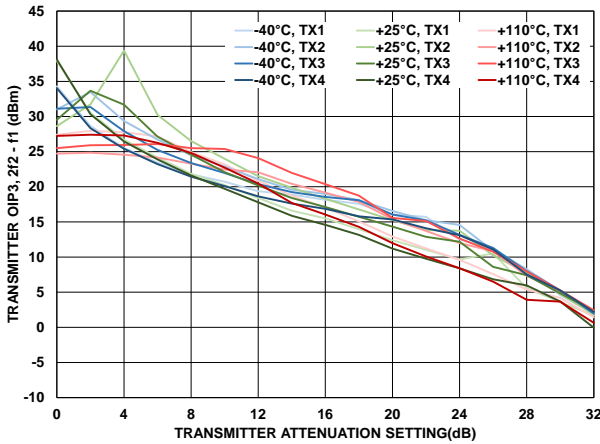


Figure 191. Transmitter OIP3, $2f_2 - f_1$ vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, $f_1 = 50.5$ MHz, $f_2 = 55.5$ MHz

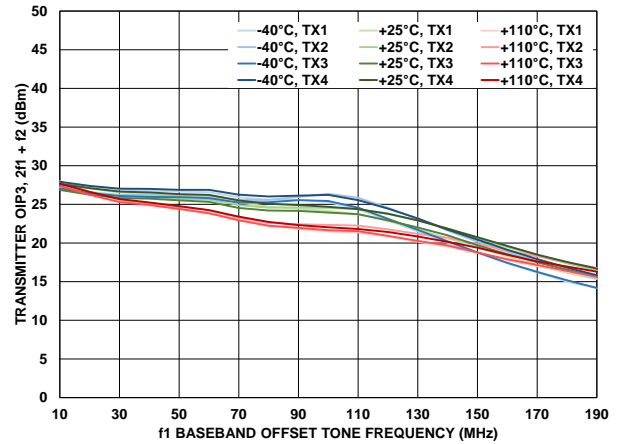


Figure 194. Transmitter OIP3, $2f_1 + f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

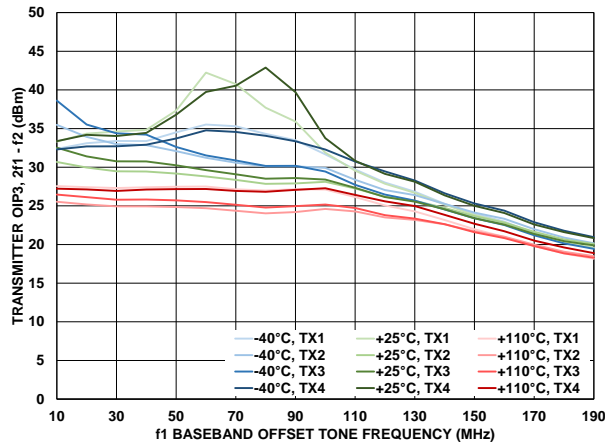


Figure 192. Transmitter OIP3, $2f_1 - f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

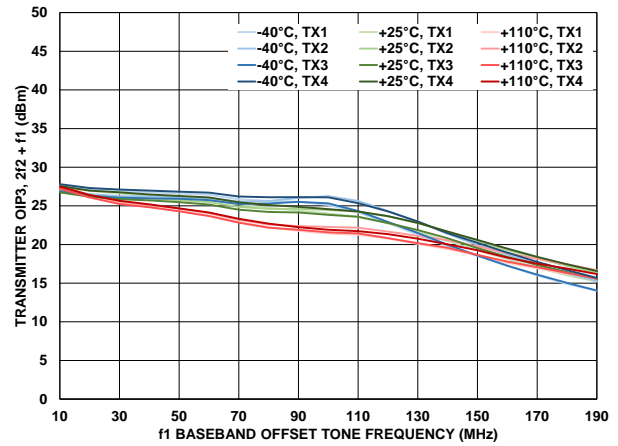


Figure 195. Transmitter OIP3, $2f_2 + f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

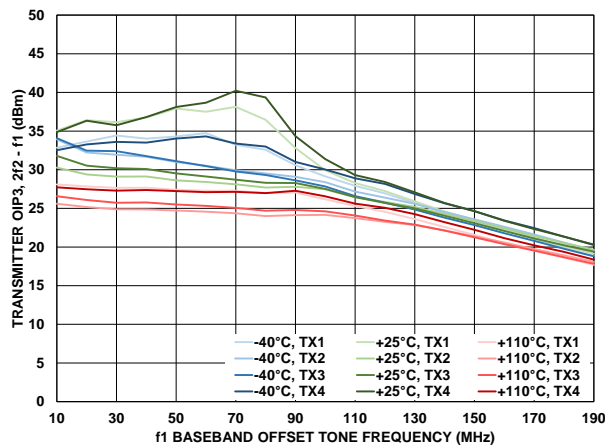


Figure 193. Transmitter OIP3, $2f_2 - f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

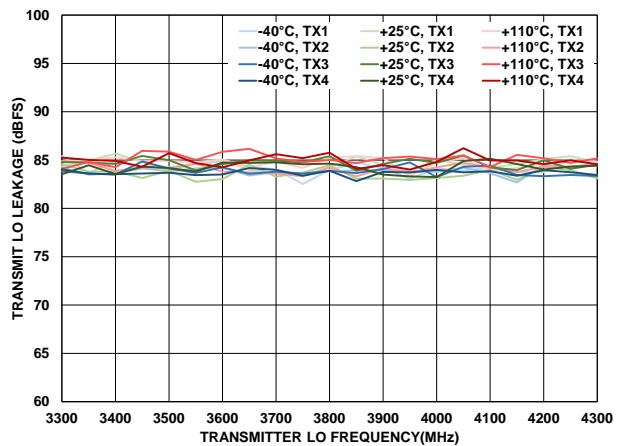


Figure 196. Transmitter LO Leakage vs. Transmitter LO Frequency

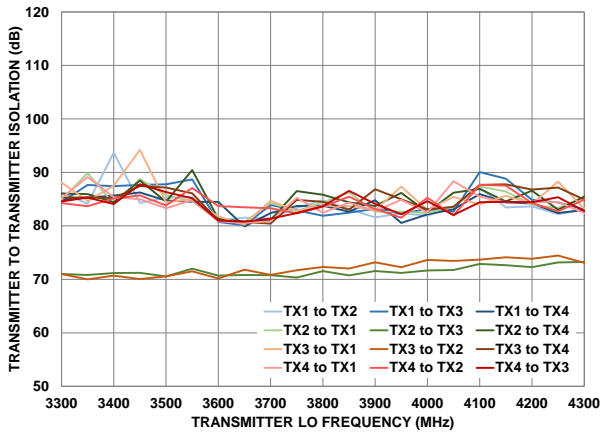


Figure 197. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

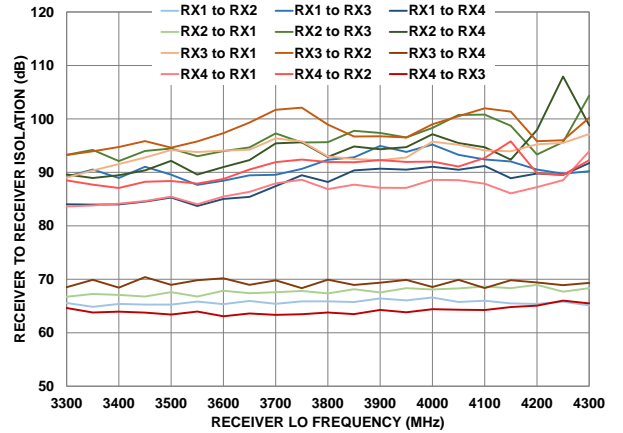


Figure 200. Receiver to Receiver Isolation vs. Receiver LO Frequency

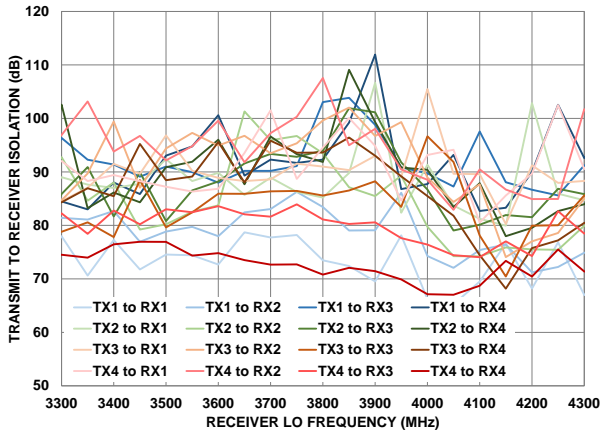


Figure 198. Transmitter to Receiver Isolation vs. Receiver LO Frequency

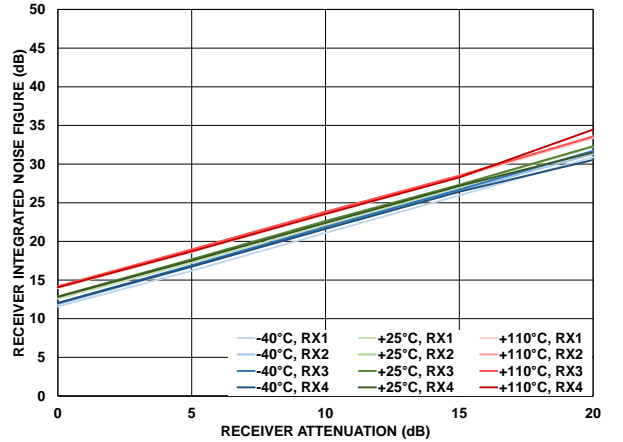


Figure 201. Receiver Integrated Noise Figure vs. Receiver Attenuation, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

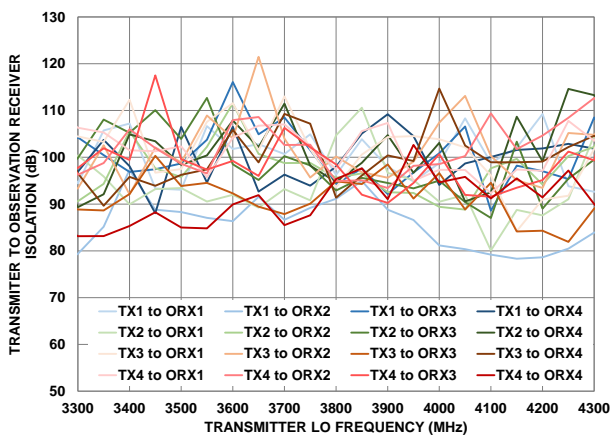


Figure 199. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

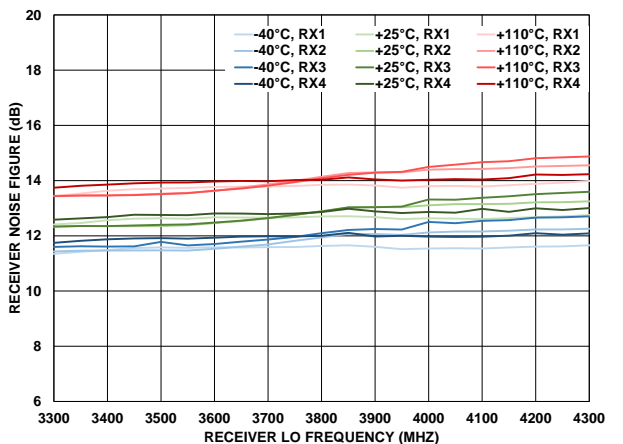


Figure 202. Receiver Integrated Noise Figure vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

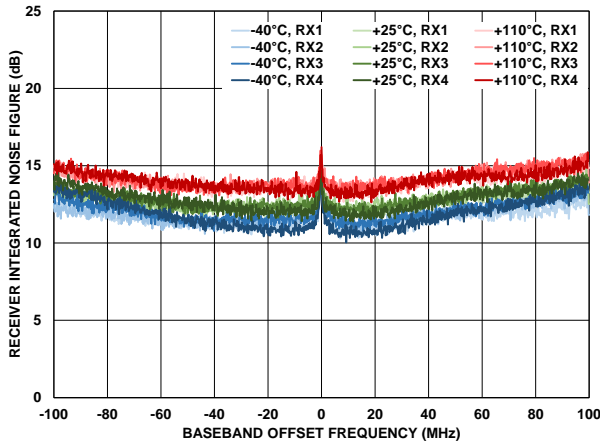


Figure 203. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

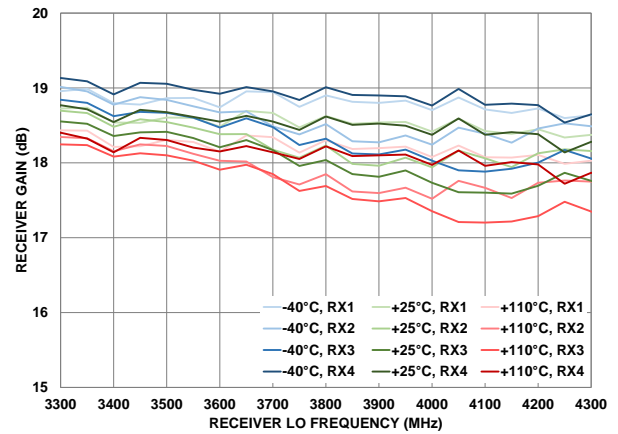


Figure 206. Receiver Gain vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

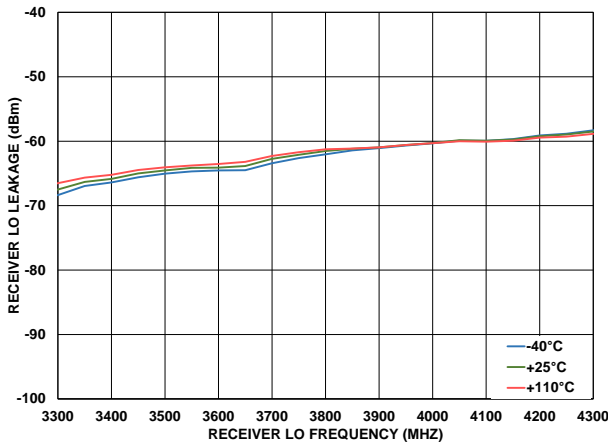


Figure 204. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

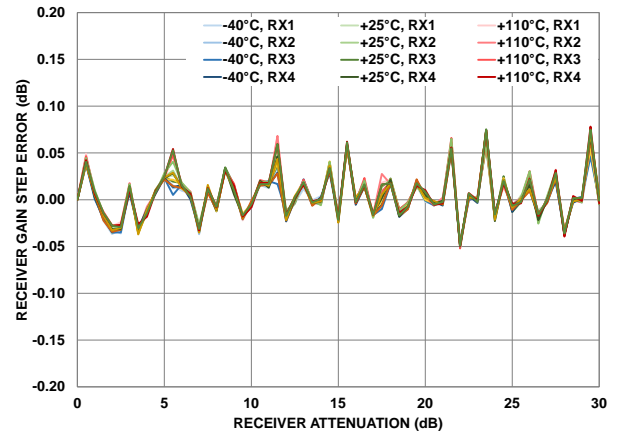


Figure 207. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

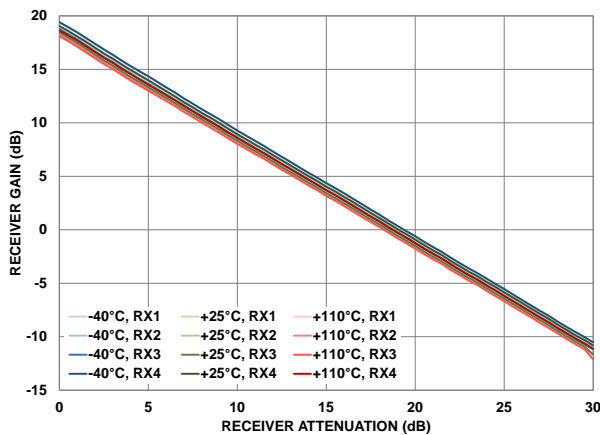


Figure 205. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

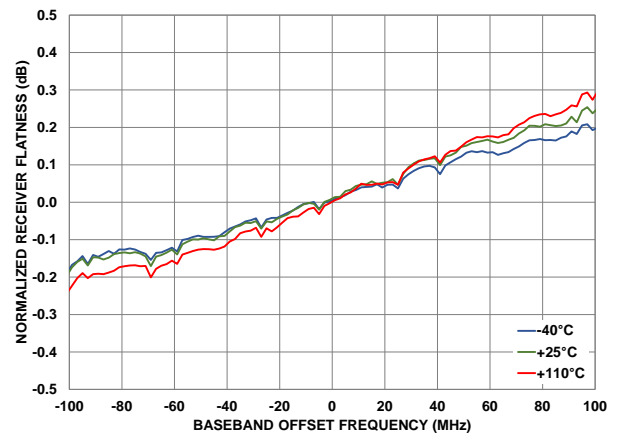


Figure 208. Normalized Receiver Flatness vs. Baseband Offset Frequency, -5 dBFS Input Signal

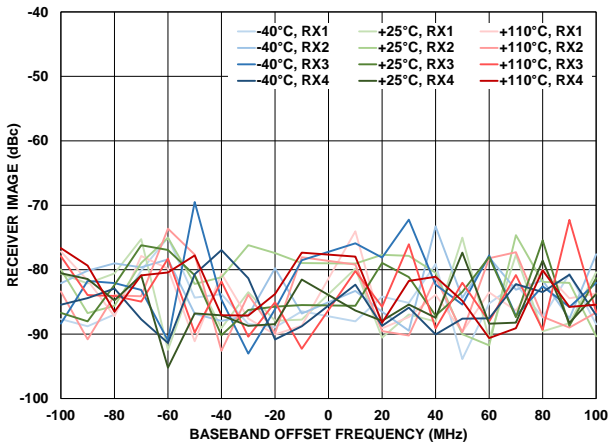


Figure 209. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS

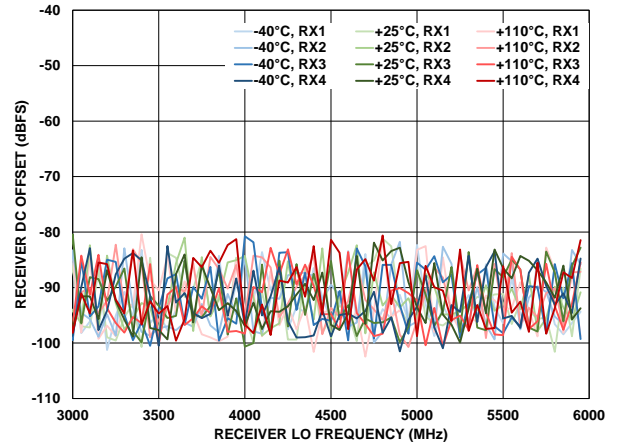


Figure 212. Receiver DC Offset vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

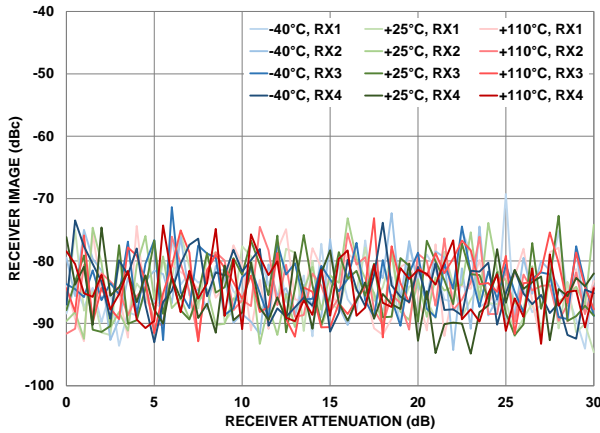


Figure 210. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS

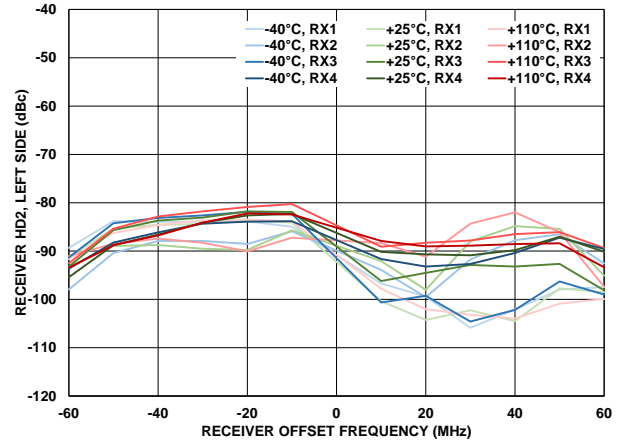


Figure 213. Receiver HD2, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

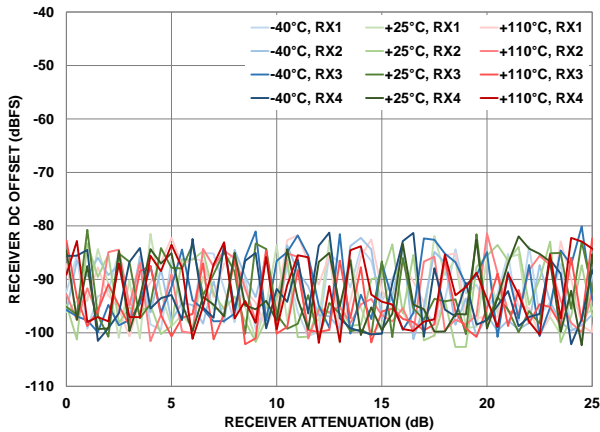


Figure 211. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal, Sample Rate = 245.76 MSPS

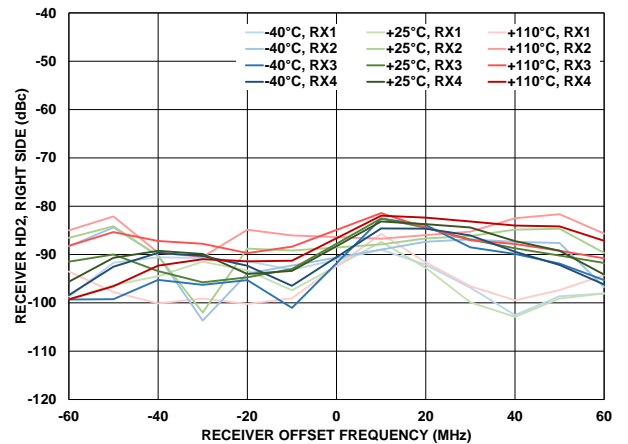


Figure 214. Receiver HD2, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

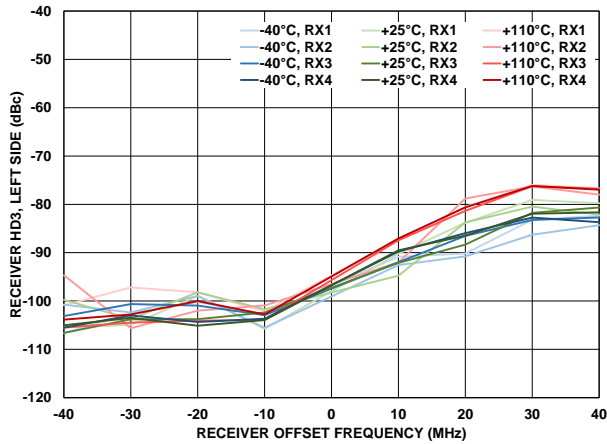


Figure 215. Receiver HD3, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

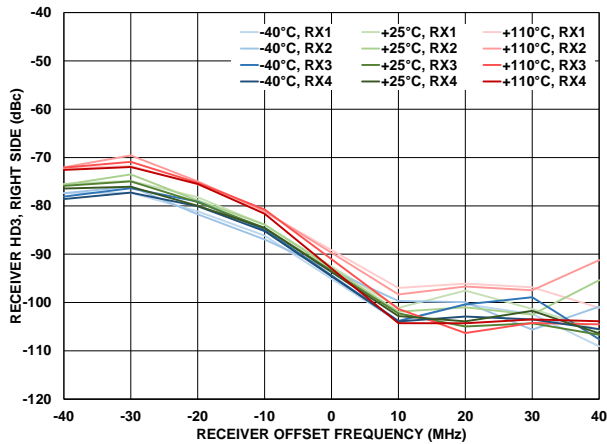


Figure 216. Receiver HD3, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

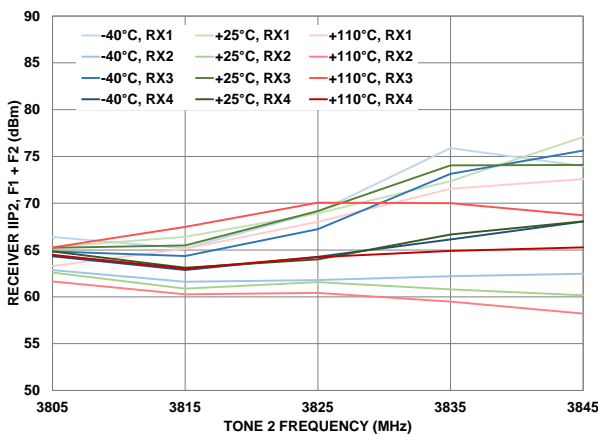


Figure 217. Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

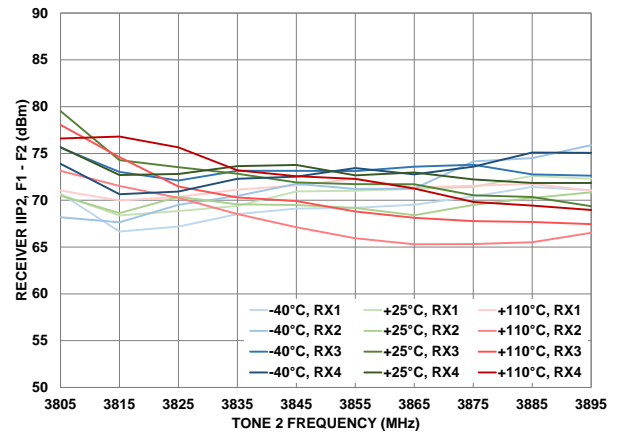


Figure 218. Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

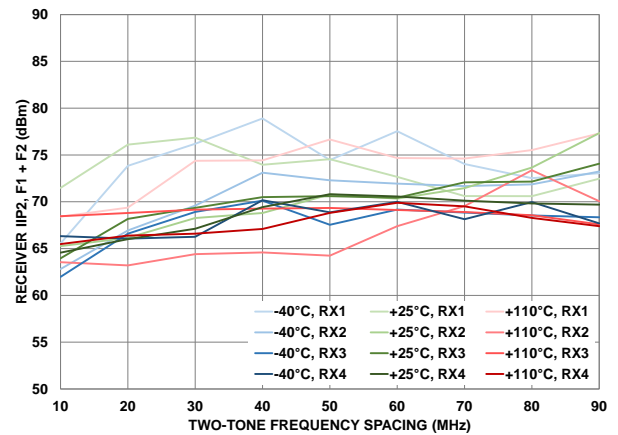


Figure 219. Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

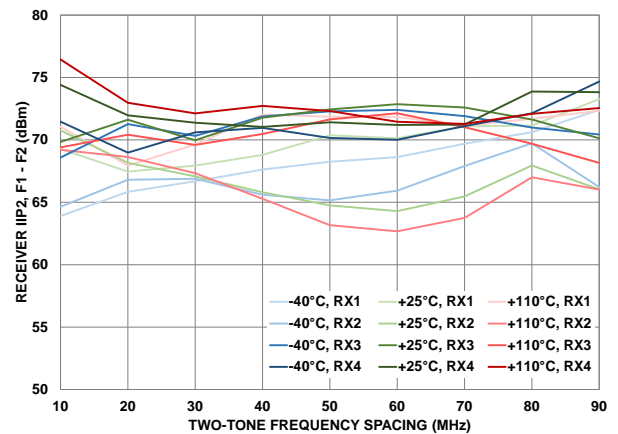


Figure 220. Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

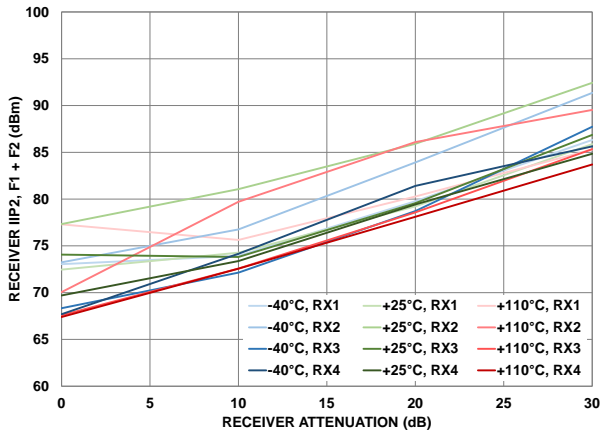


Figure 221. Receiver IIP2, $f_1 + f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

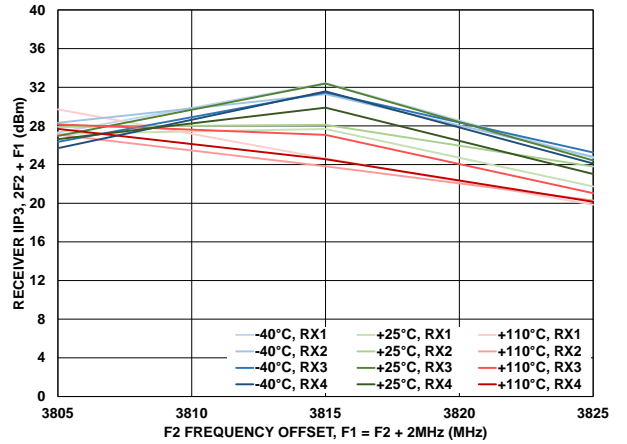


Figure 224. Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

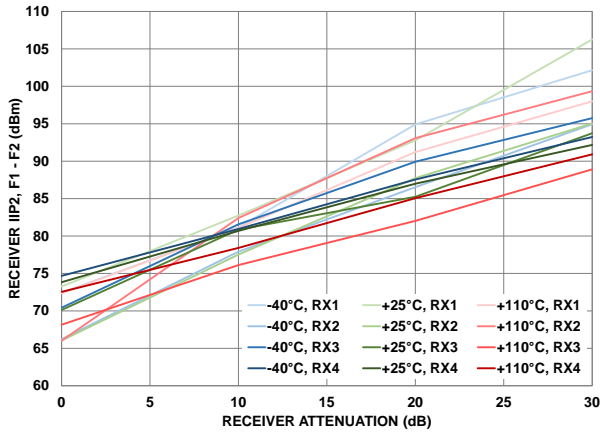


Figure 222. Receiver IIP2, $f_1 - f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

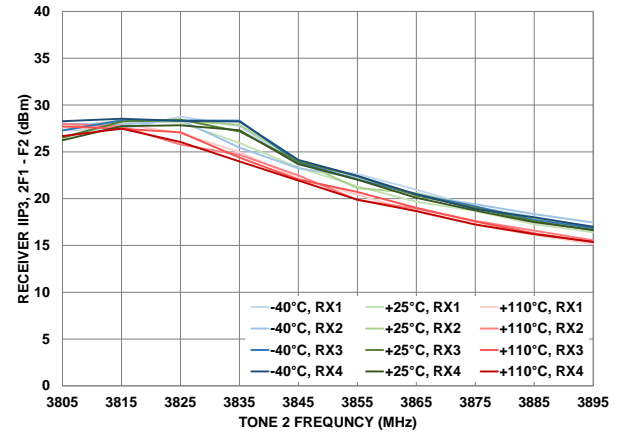


Figure 225. Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

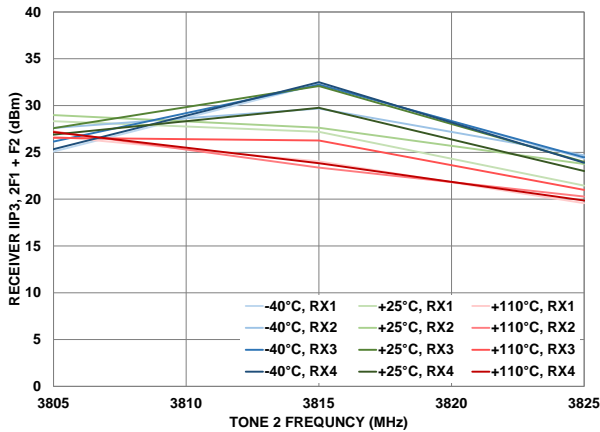


Figure 223. Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

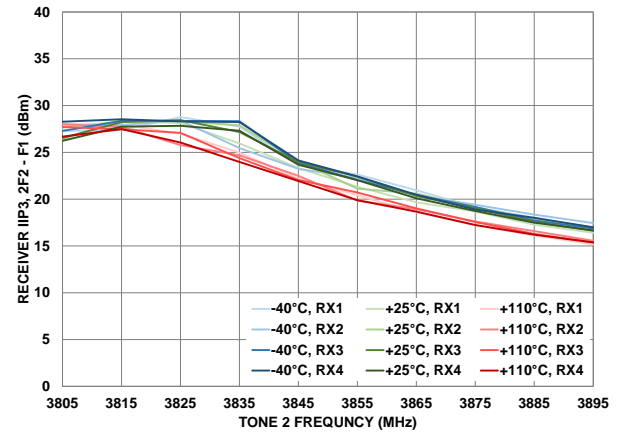


Figure 226. Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

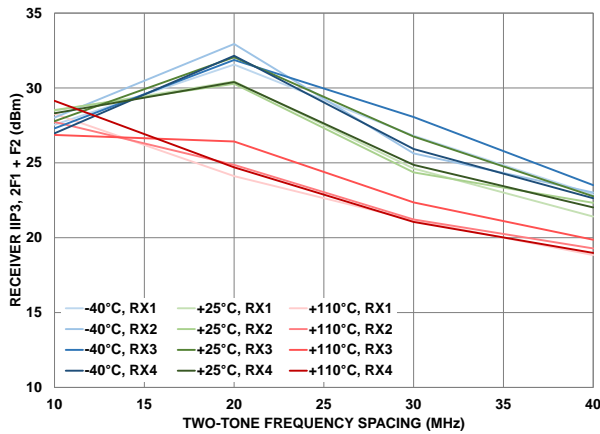


Figure 227. Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

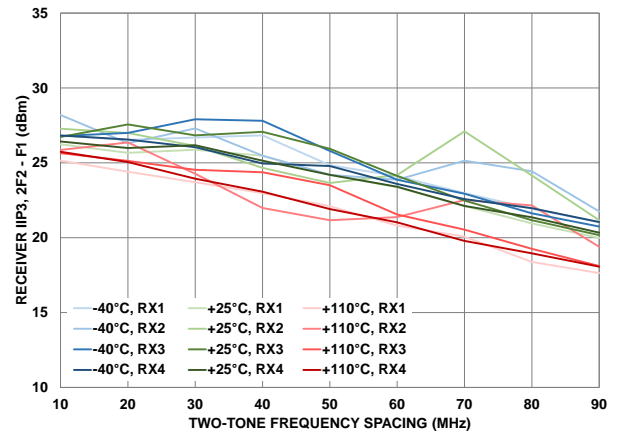


Figure 230. Receiver IIP3, $2f_2 - f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

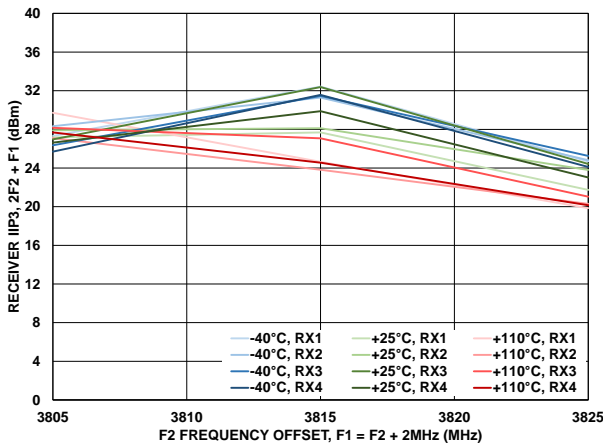


Figure 228. Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

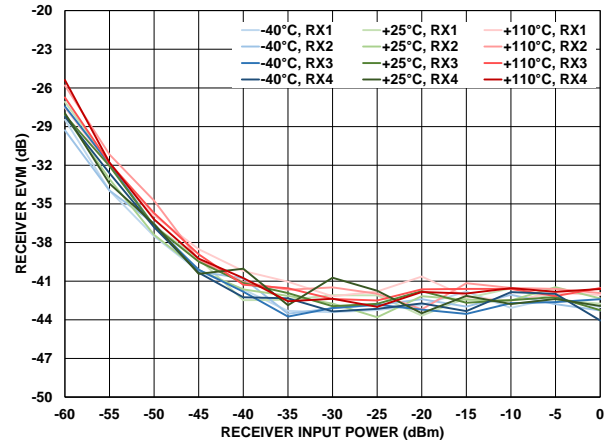


Figure 231. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 200 kHz, Loop Filter Phase Margin = 60°

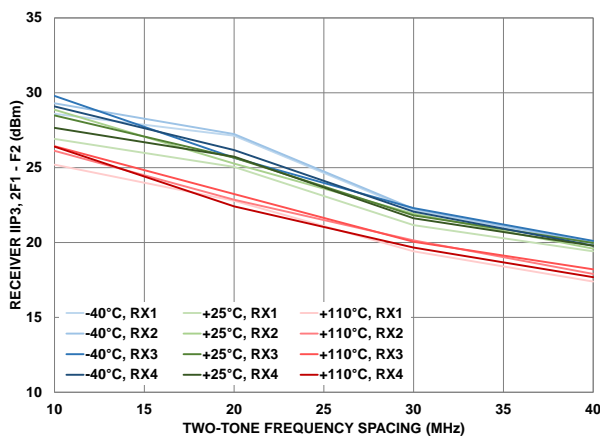


Figure 229. Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

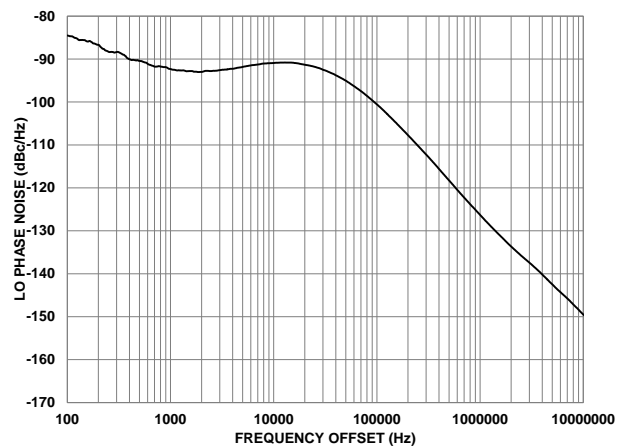


Figure 232. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

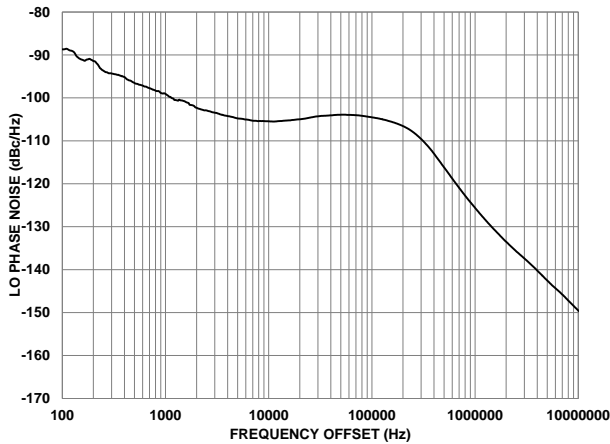


Figure 233. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 200 kHz, Phase Margin = 60°

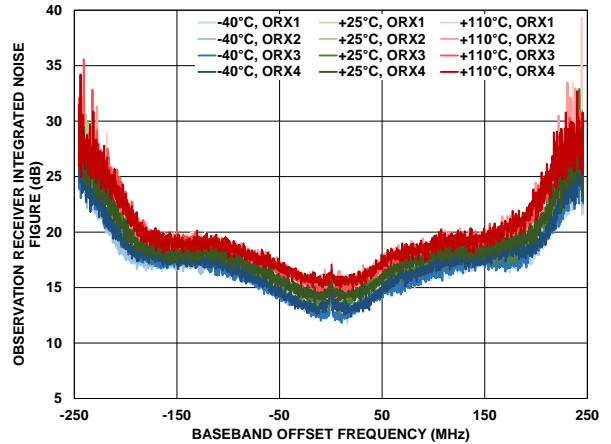


Figure 236. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

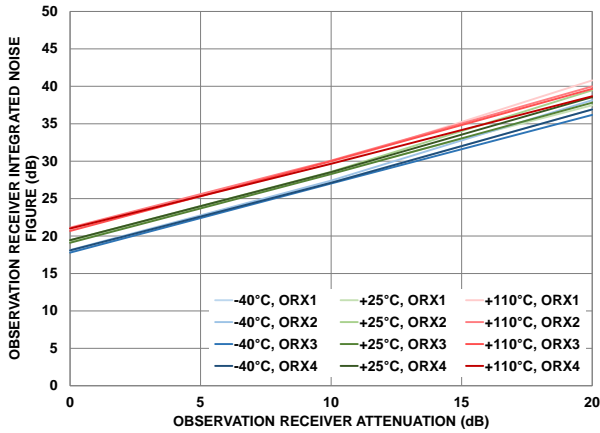


Figure 234. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

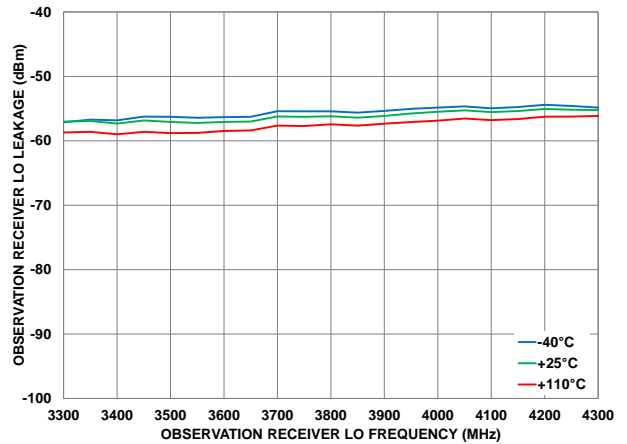


Figure 237. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

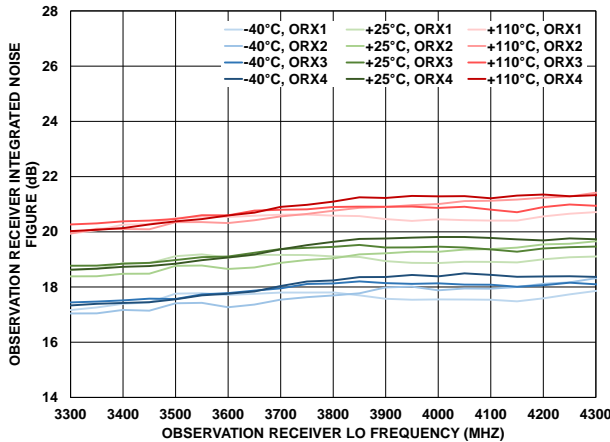


Figure 235. Observation Receiver Integrated Noise Figure vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

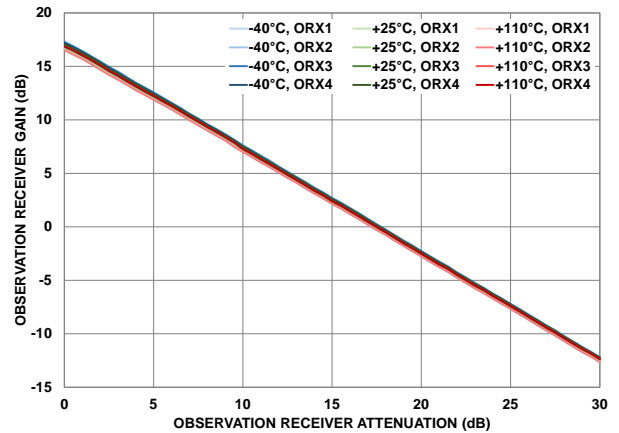


Figure 238. Observation Receiver Gain vs. Observation Receiver Attenuation, 45 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

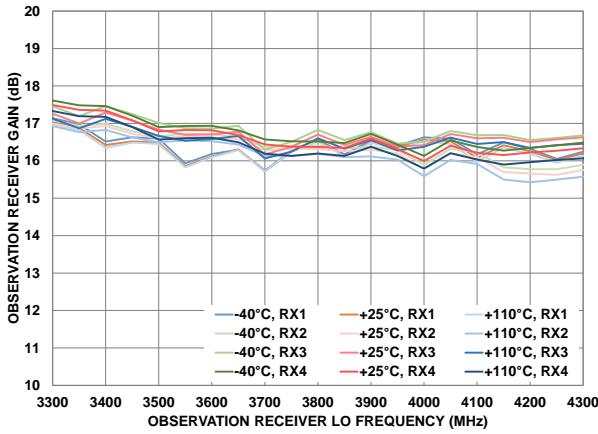


Figure 239. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

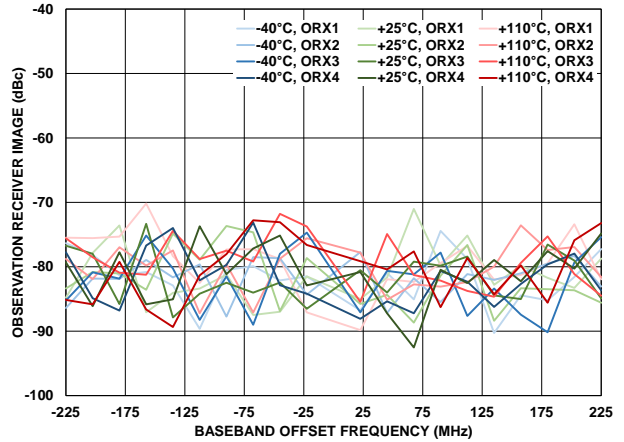


Figure 242. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

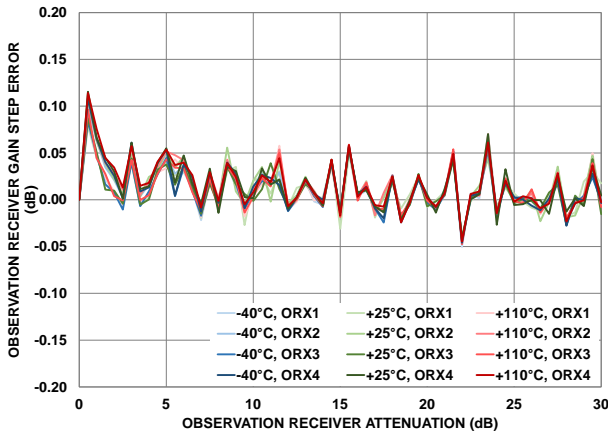


Figure 240. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 45 MHz Offset, -10 dBFS Input Signal

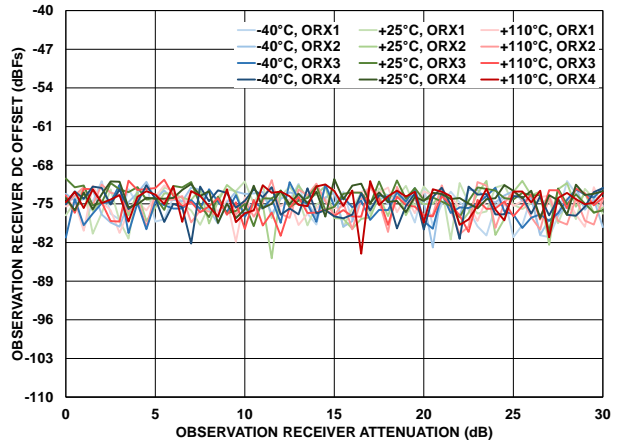


Figure 243. Observation Receiver DC Offset vs. Observation Receiver Attenuation, Sample Rate = 491.52 MSPS

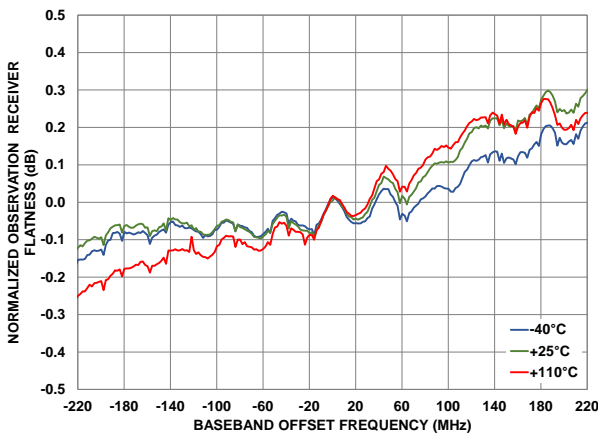


Figure 241. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, -10 dBFS Input Signal

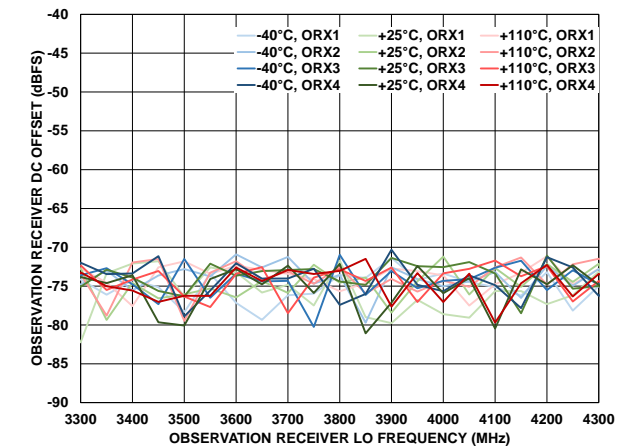


Figure 244. Observation Receiver DC Offset vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

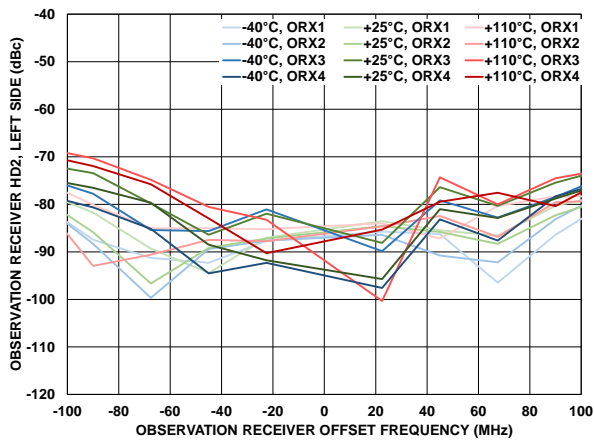


Figure 245. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

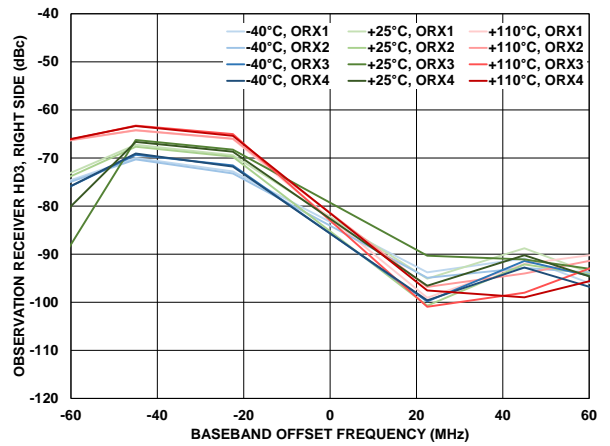


Figure 248. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

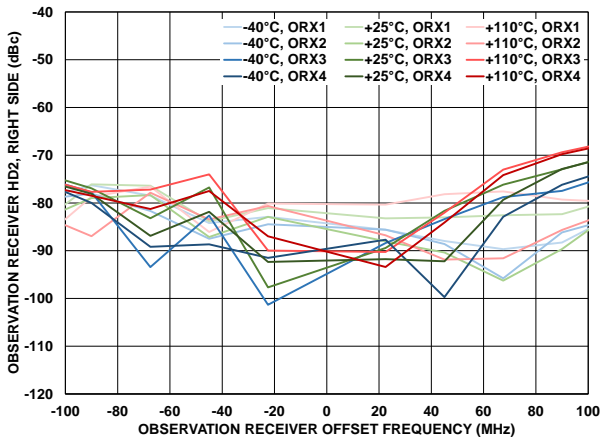


Figure 246. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

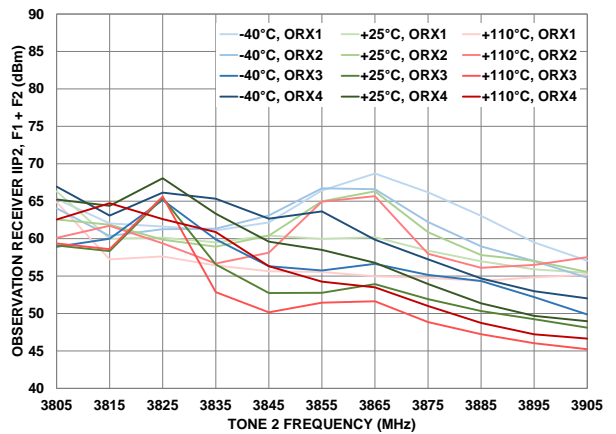


Figure 249. Observation Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

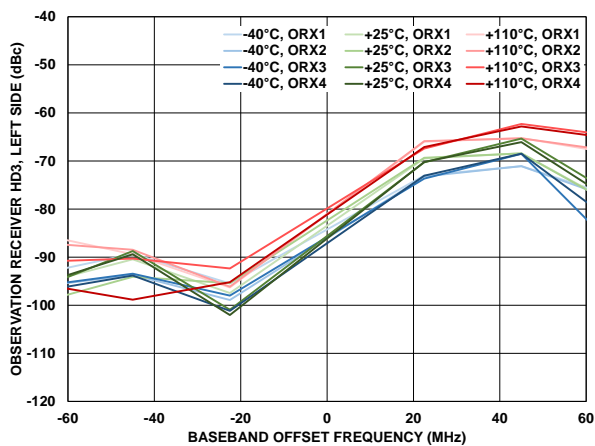


Figure 247. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

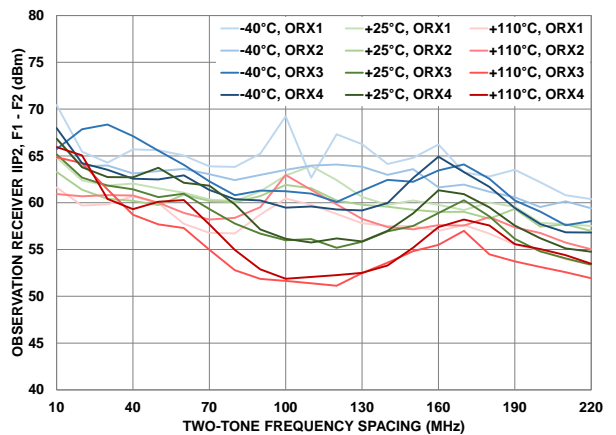


Figure 250. Observation Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

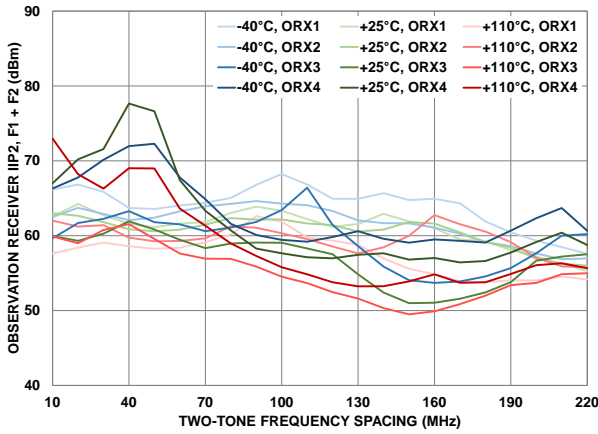


Figure 251. Observation Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

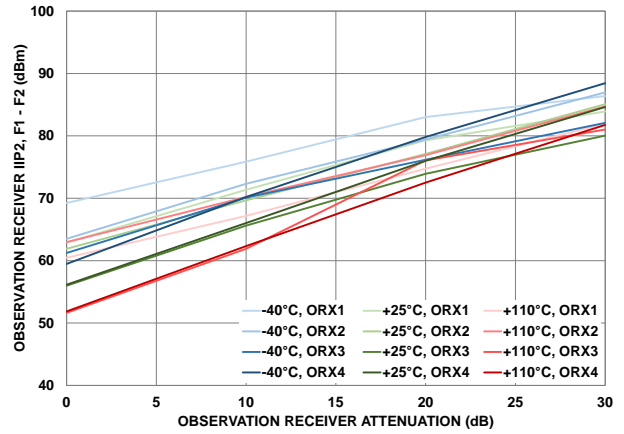


Figure 254. Observation Receiver IIP2, $f_1 - f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

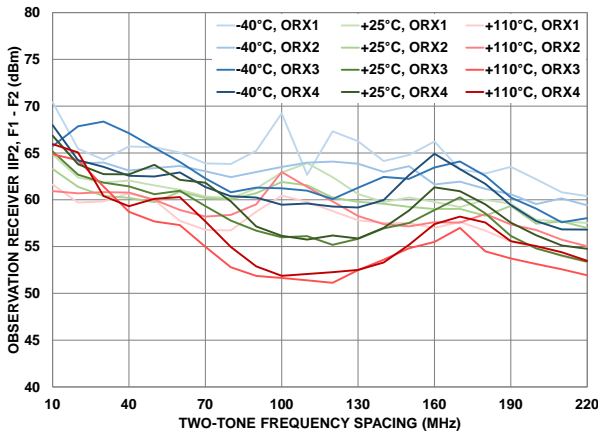


Figure 252. Observation Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

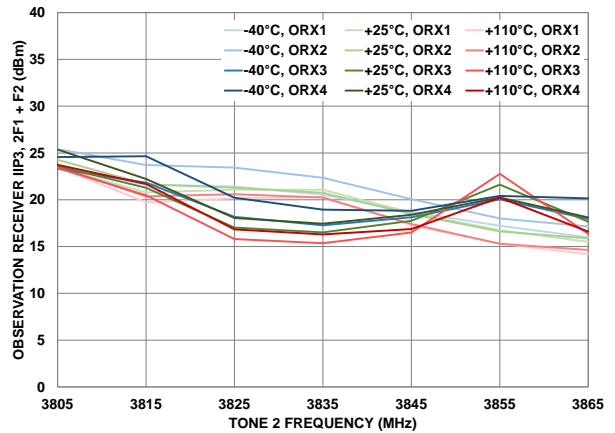


Figure 255. Observation Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

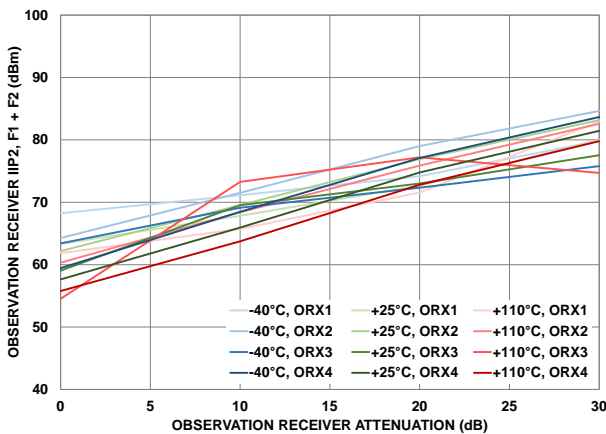


Figure 253. Observation Receiver IIP2, $f_1 + f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

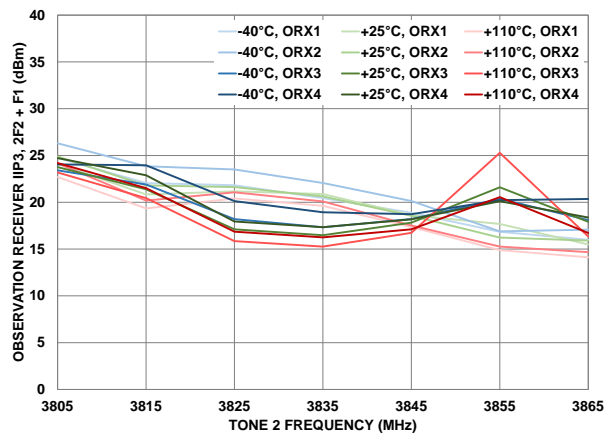


Figure 256. Observation Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

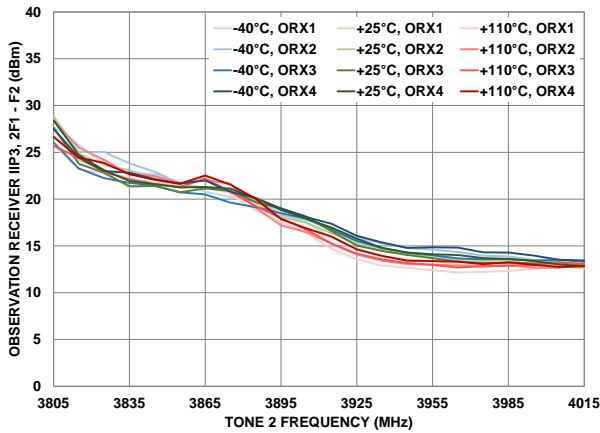


Figure 257. Observation Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

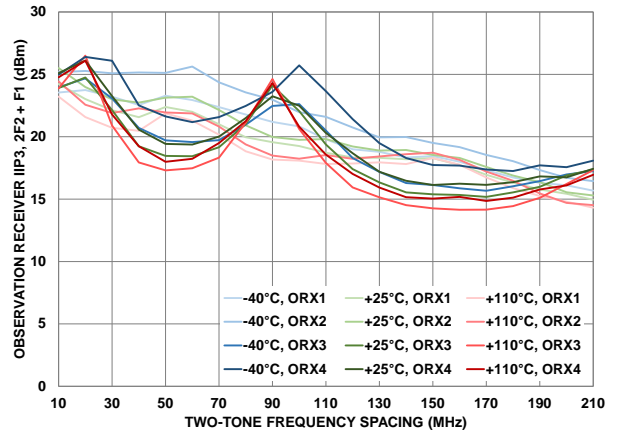


Figure 260. Observation Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

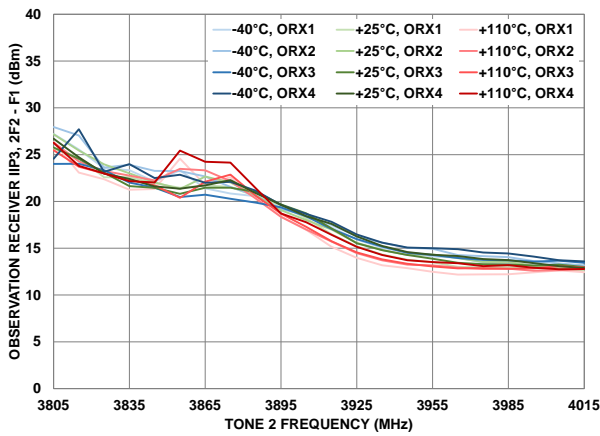


Figure 258. Observation Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

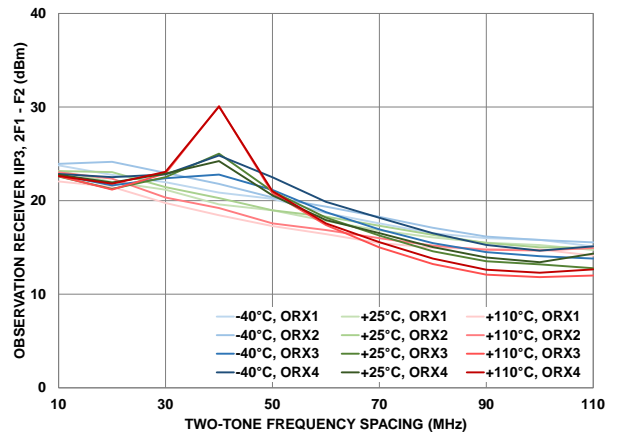


Figure 261. Observation Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

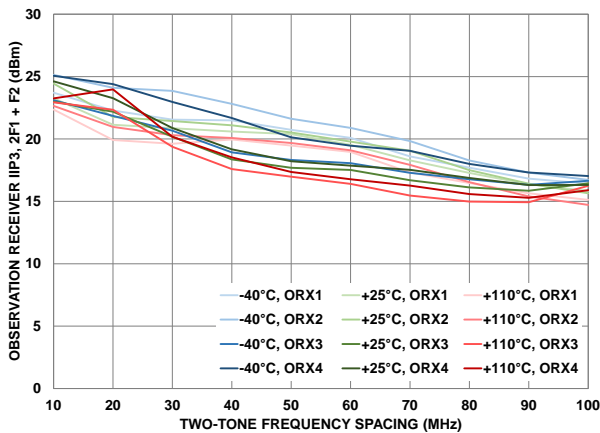


Figure 259. Observation Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

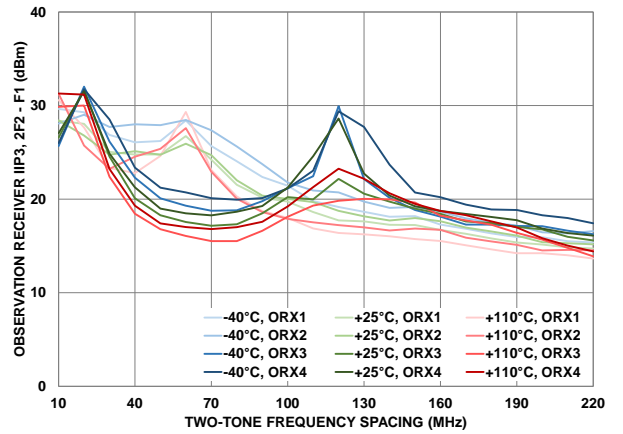


Figure 262. Observation Receiver IIP3, $2f_2 - f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

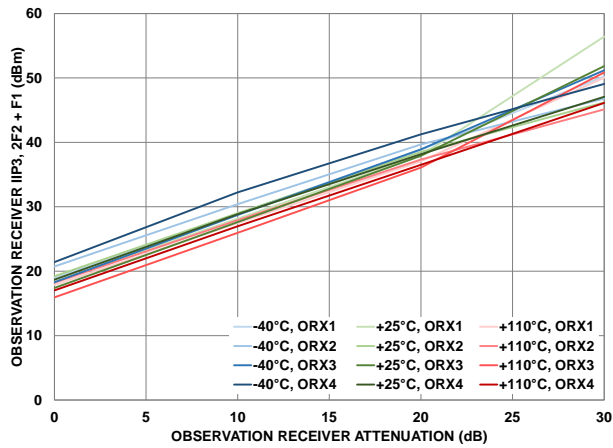


Figure 263. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

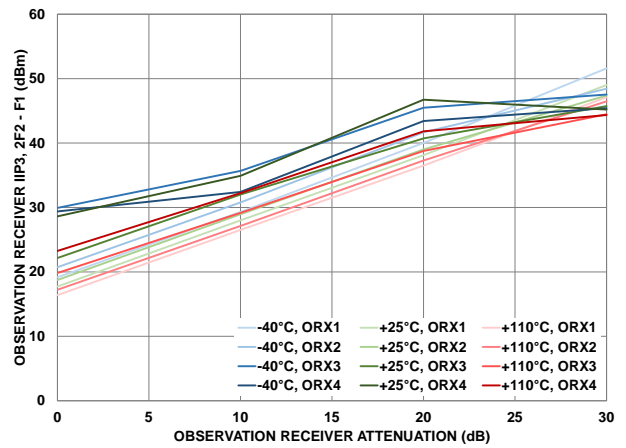


Figure 264. Observation Receiver IIP3, 2f2 - f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

4800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 4800 MHz, unless otherwise noted.

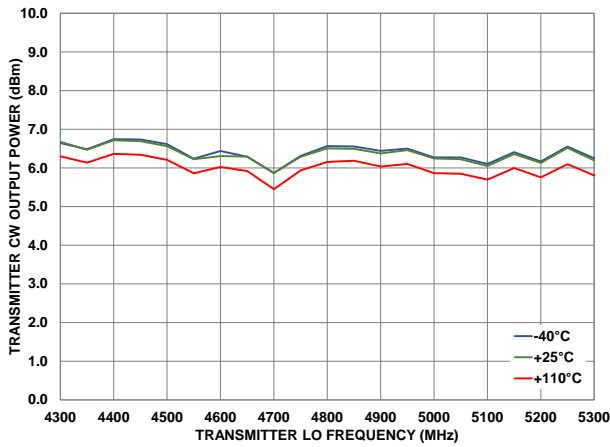


Figure 265. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

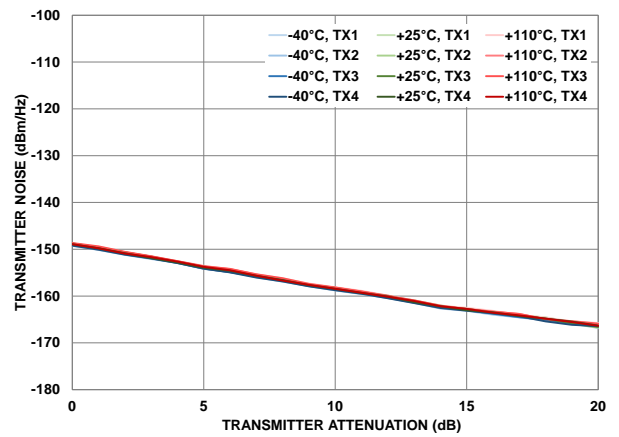


Figure 268. Transmitter Noise vs. Transmitter Attenuation, 10 MHz Offset Frequency

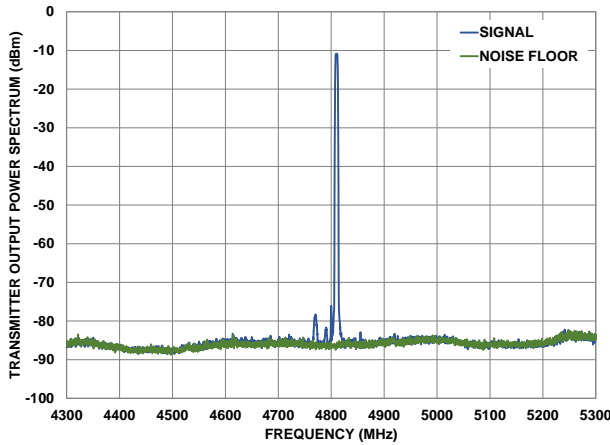


Figure 266. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, -10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

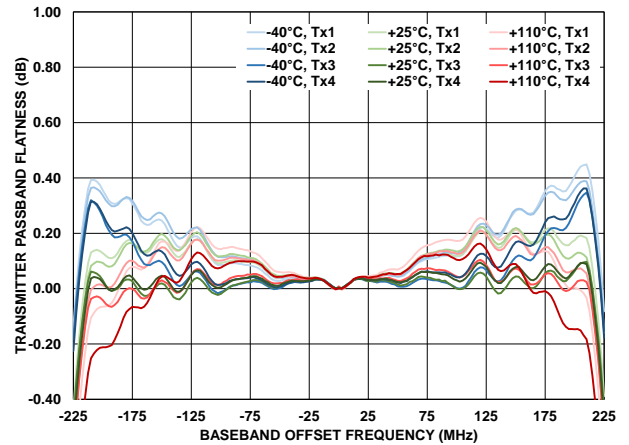


Figure 269. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

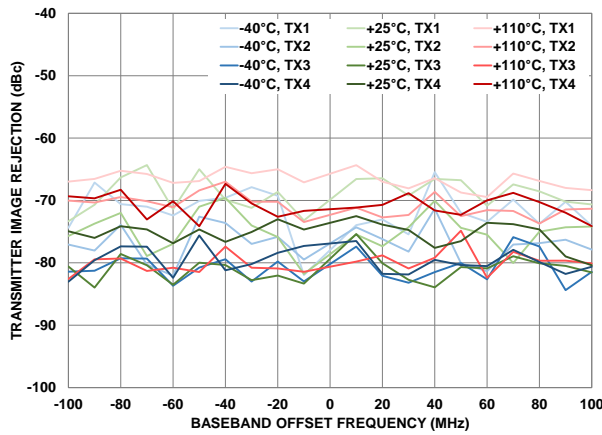


Figure 267. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency

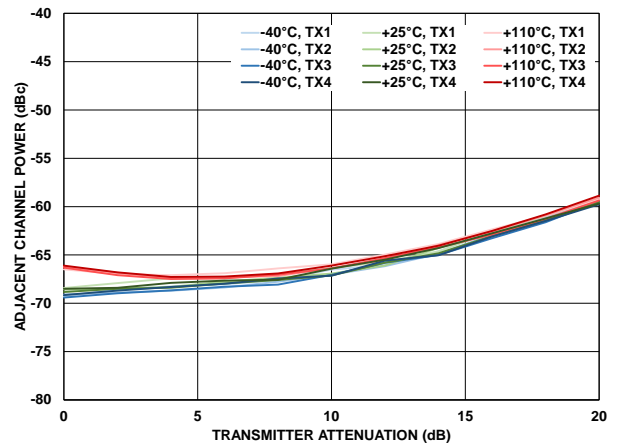


Figure 270. Adjacent Channel Power Level vs. Transmitter Attenuation, -10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

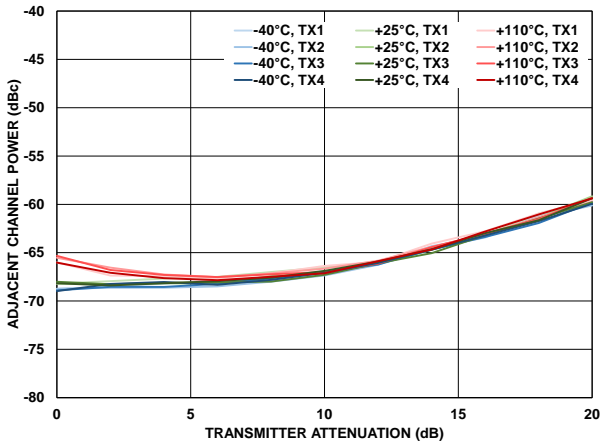


Figure 271. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB

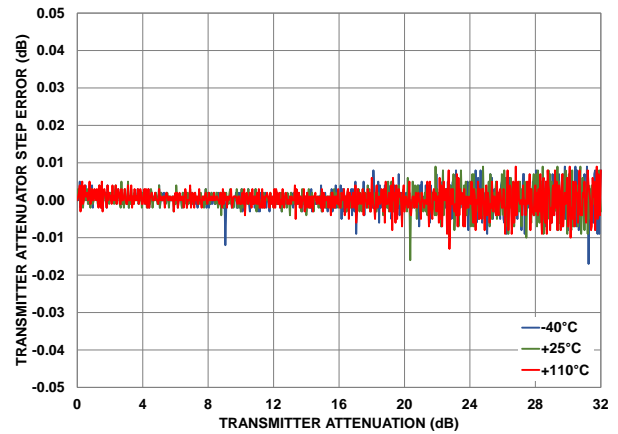


Figure 274. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

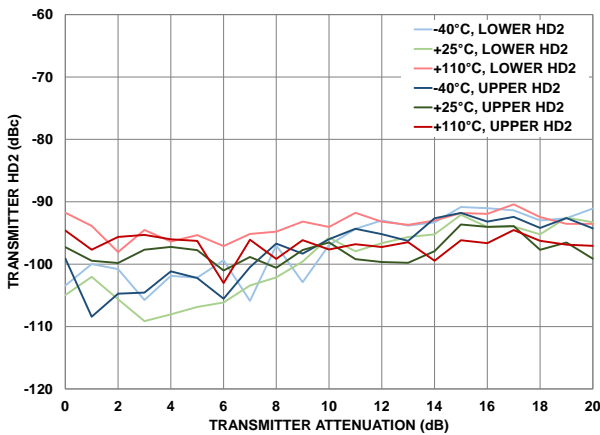


Figure 272. Transmitter Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 10 MHz Offset

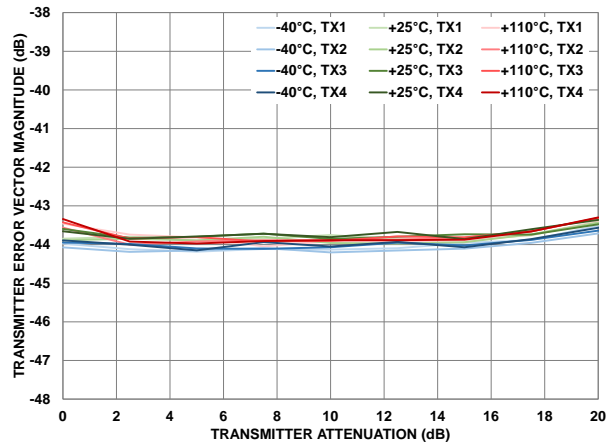


Figure 275. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, Loop Filter Bandwidth = 400 kHz, Loop Filter Phase Margin = 60°

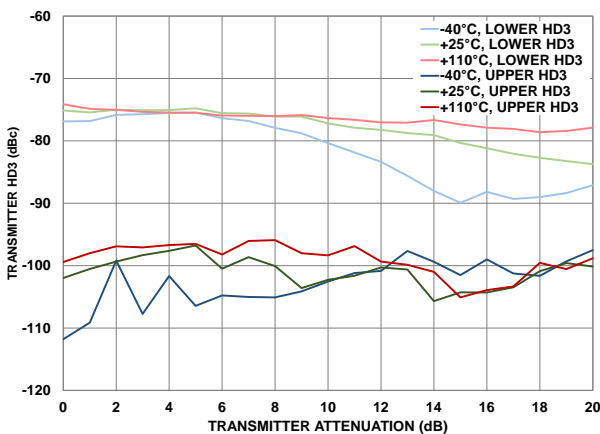


Figure 273. Transmitter Third Harmonic Distortion HD3 vs. Transmitter Attenuation, 10 MHz Offset

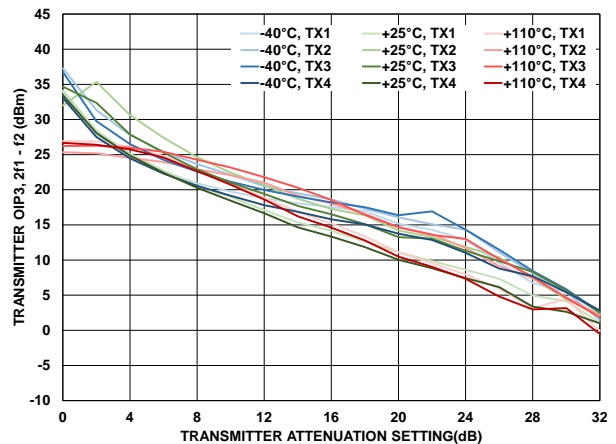


Figure 276. Transmitter OIP3, 2f1 - f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

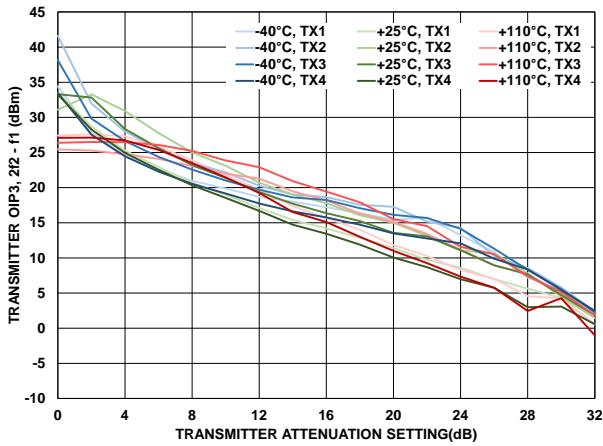


Figure 277. Transmitter OIP3, $2f_2 - f_1$ vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, $f_1 = 50.5$ MHz, $f_2 = 55.5$ MHz

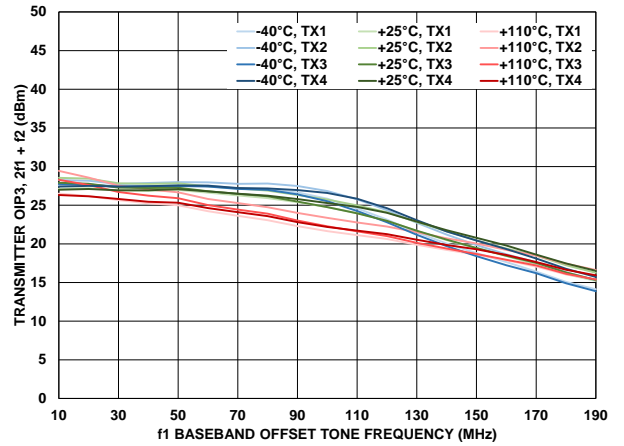


Figure 280. Transmitter OIP3, $2f_1 + f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

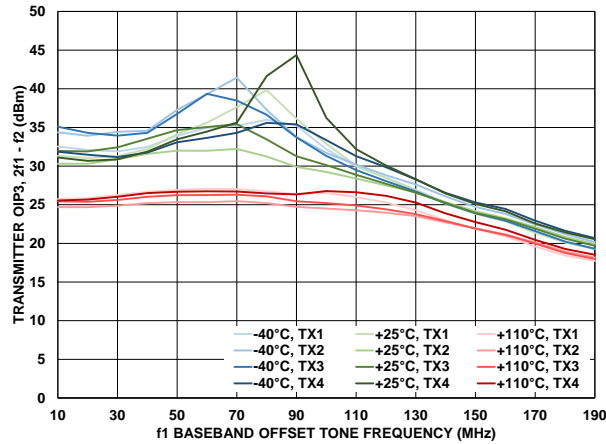


Figure 278. Transmitter OIP3, $2f_1 - f_2$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

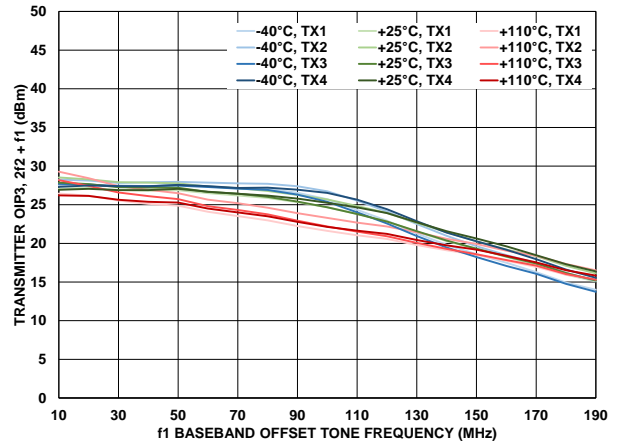


Figure 281. Transmitter OIP3, $2f_2 + f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

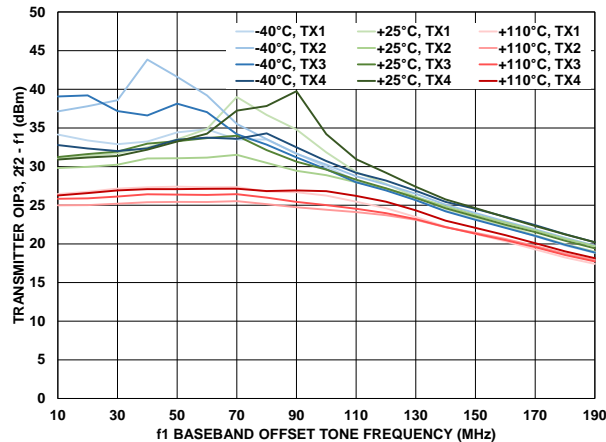


Figure 279. Transmitter OIP3, $2f_2 - f_1$ vs. f_1 Baseband Offset Tone Frequency, $f_2 = f_1 + 5$ MHz, 15 dB Digital Backoff per Tone

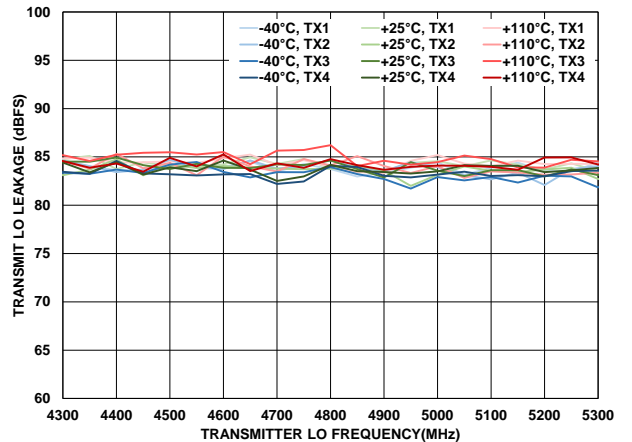


Figure 282. Transmitter LO Leakage vs. Transmitter LO Frequency

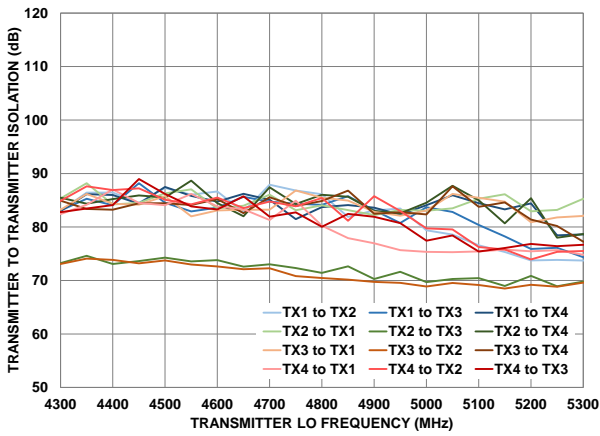


Figure 283. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

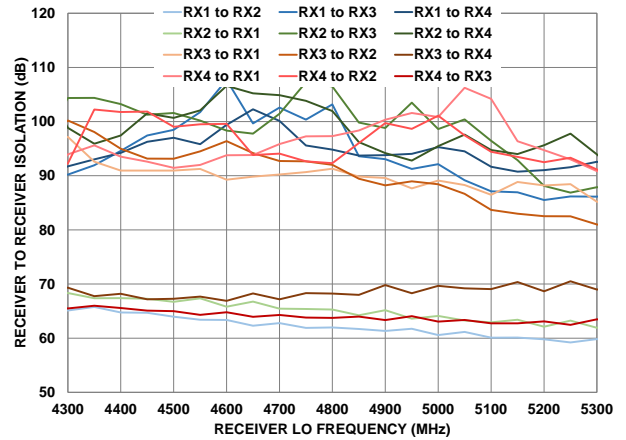


Figure 286. Receiver to Receiver Isolation vs. Receiver LO Frequency

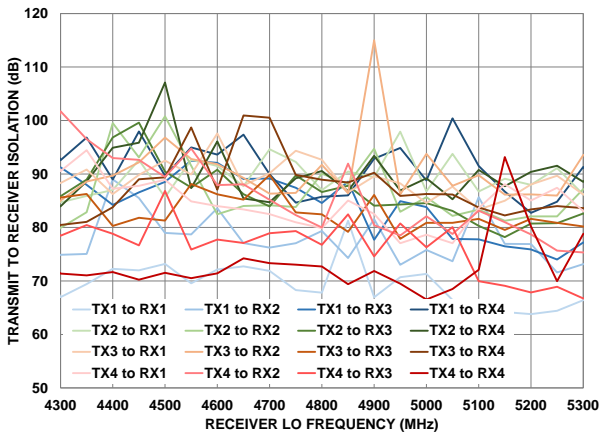


Figure 284. Transmitter to Receiver Isolation vs. Receiver LO Frequency

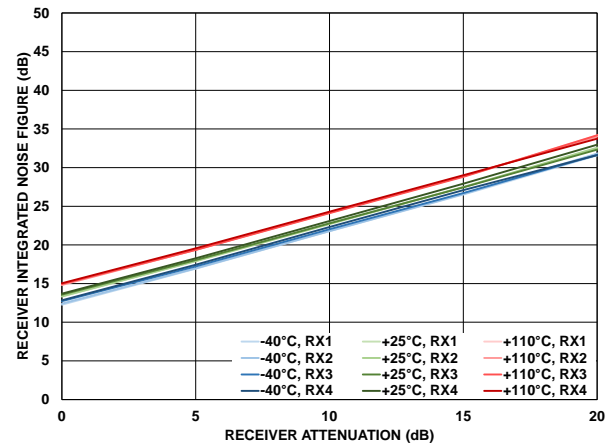


Figure 287. Receiver Integrated Noise Figure vs. Receiver Attenuation, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

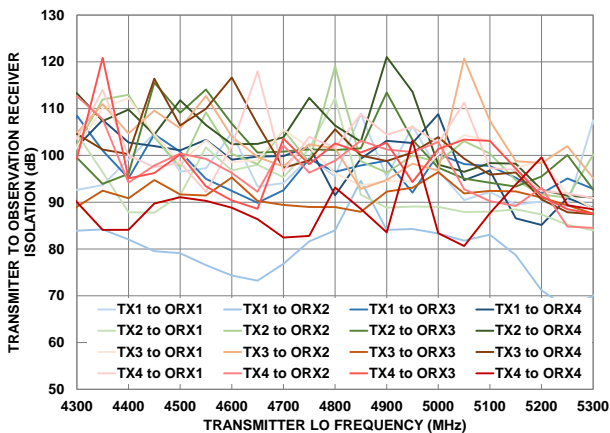


Figure 285. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

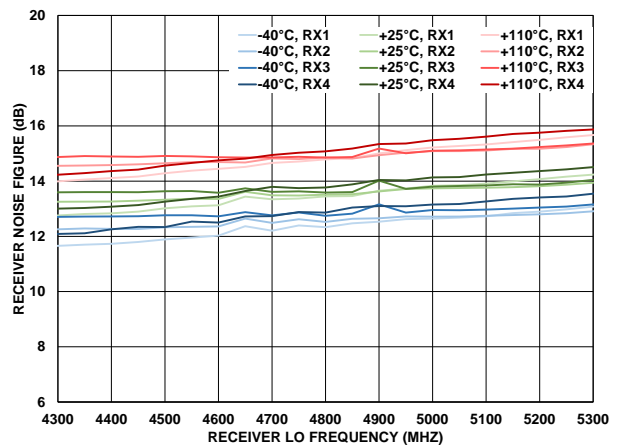


Figure 288. Receiver Integrated Noise Figure vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

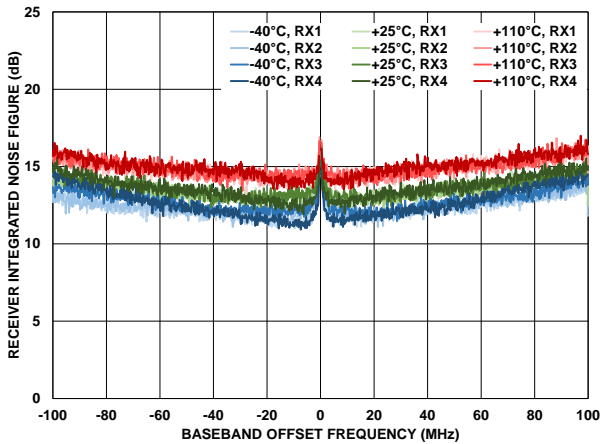


Figure 289. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

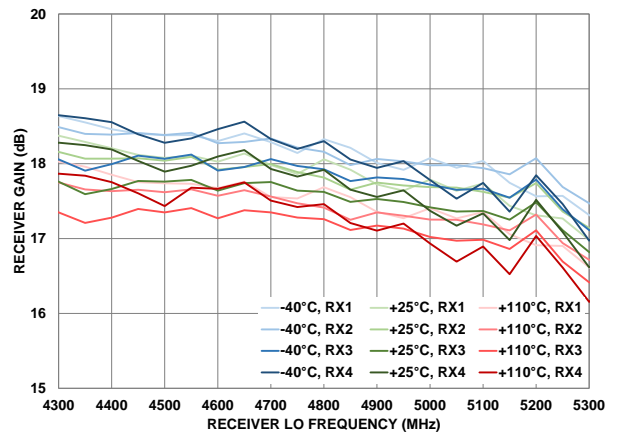


Figure 292. Receiver Gain vs. Receiver LO Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

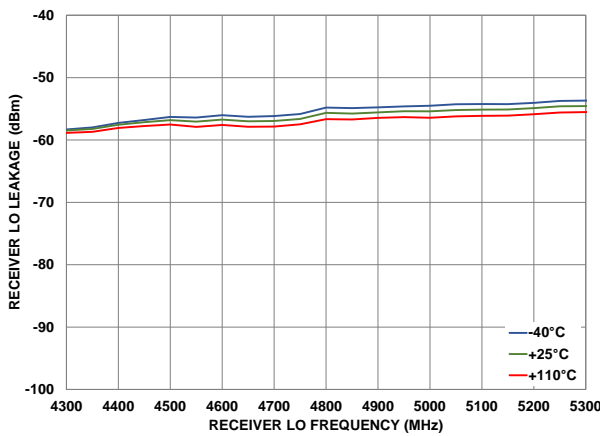


Figure 290. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

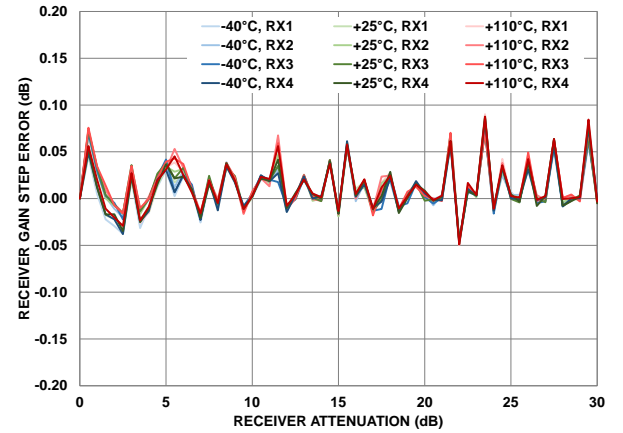


Figure 293. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal

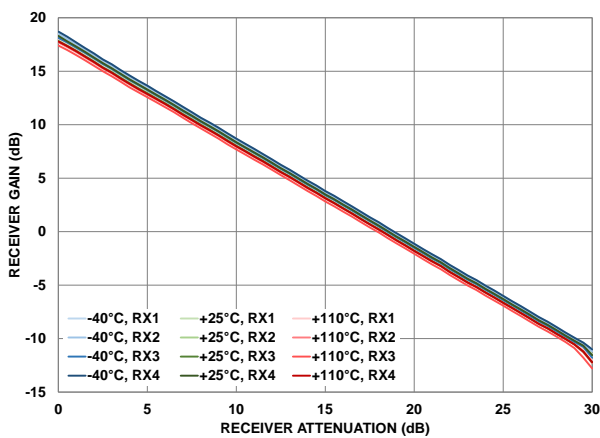


Figure 291. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

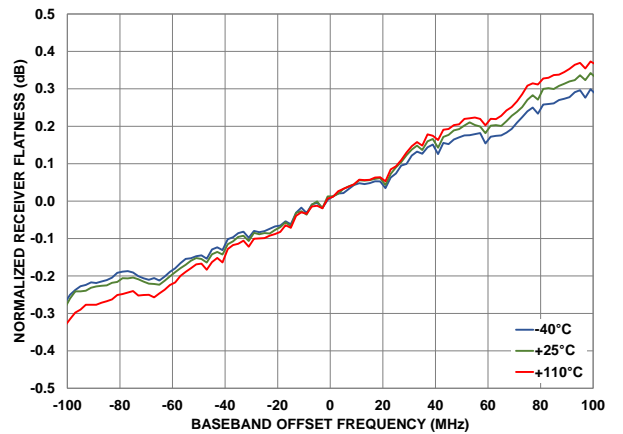


Figure 294. Normalized Receiver Flatness vs. Baseband Offset Frequency, -5 dBFS Input Signal

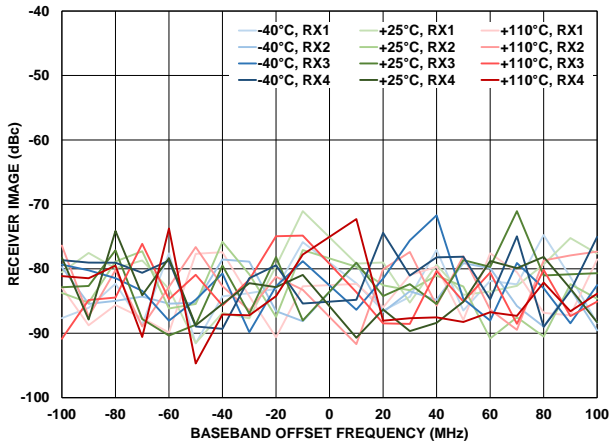


Figure 295. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS

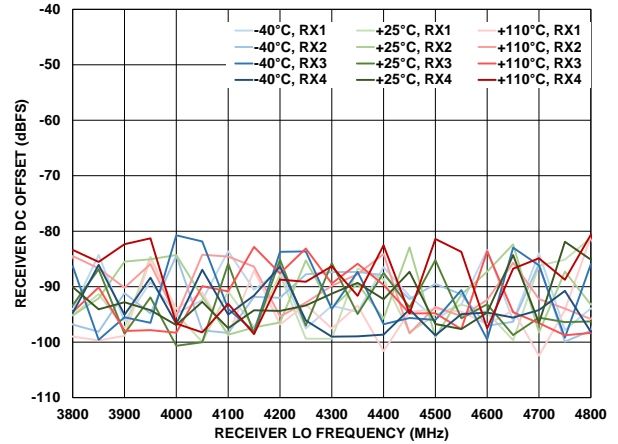


Figure 298. Receiver DC Offset vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

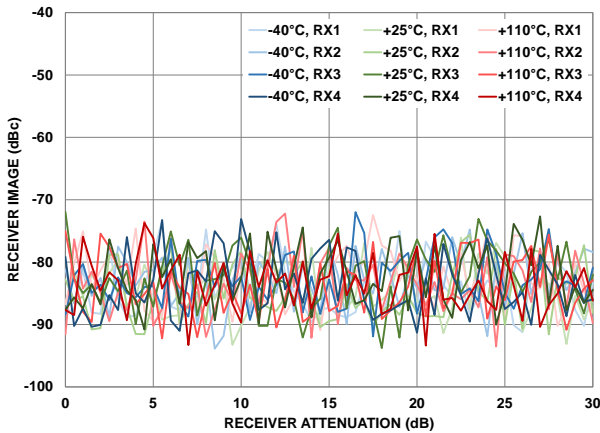


Figure 296. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS

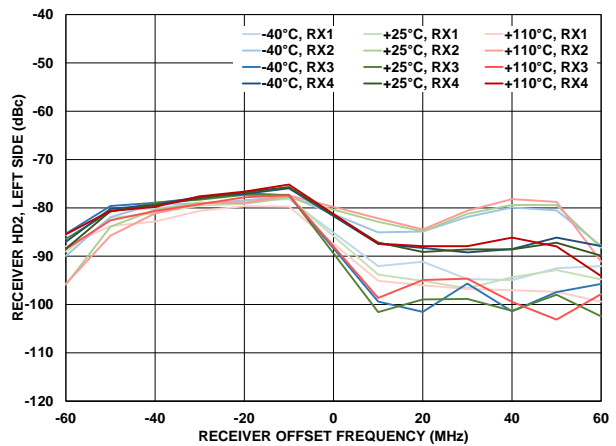


Figure 299. Receiver HD2, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

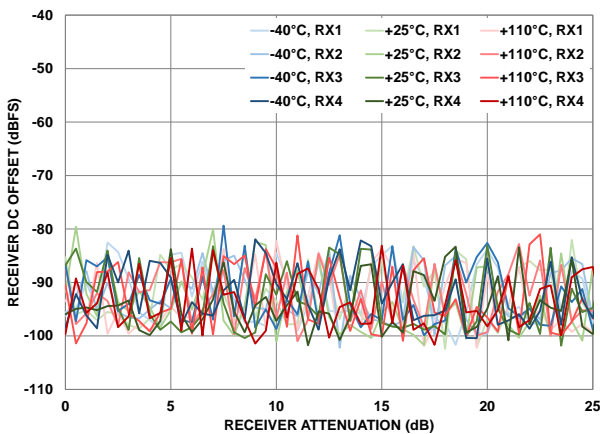


Figure 297. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, -5 dBFS Input Signal, Sample Rate = 245.76 MSPS

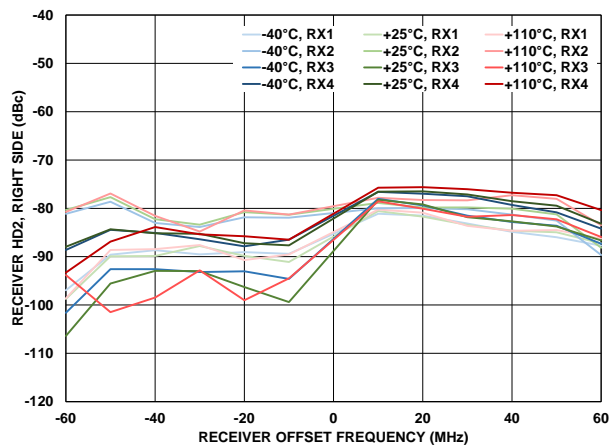


Figure 300. Receiver HD2, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

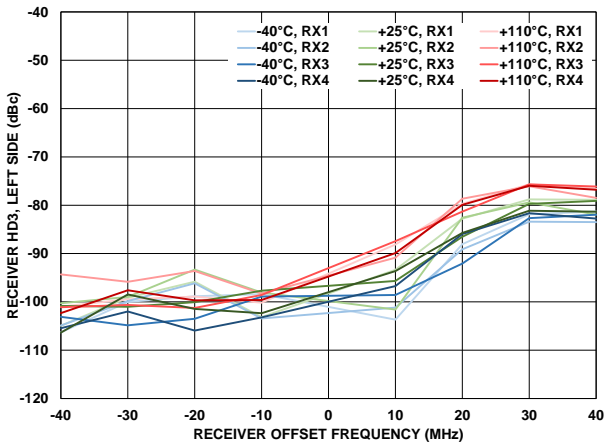


Figure 301. Receiver HD3, Left Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

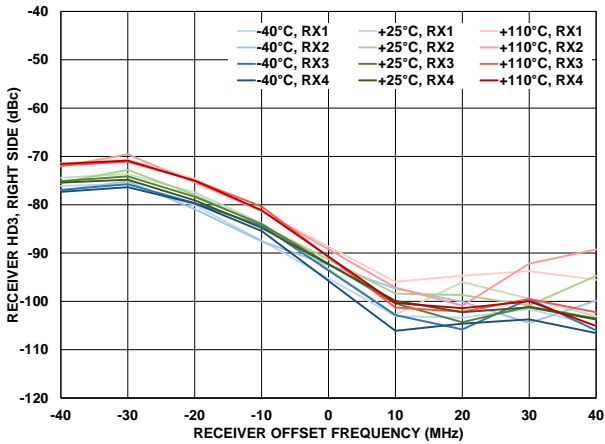


Figure 302. Receiver HD3, Right Side vs. Baseband Offset Frequency, -5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

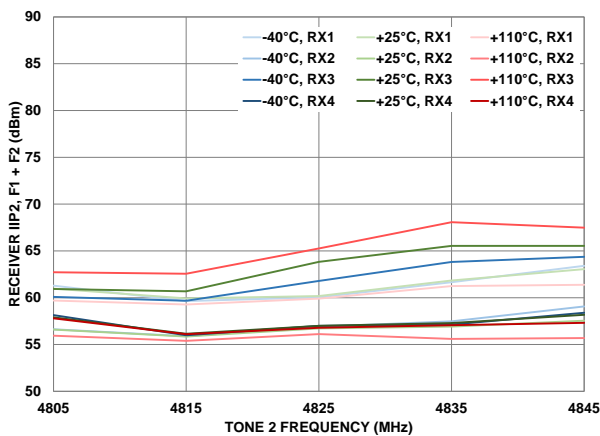


Figure 303. Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

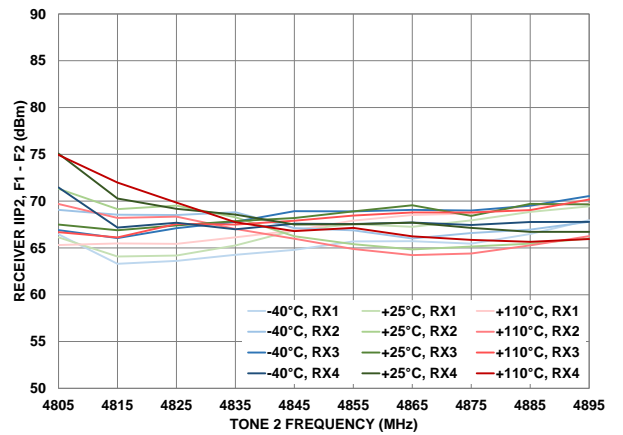


Figure 304. Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

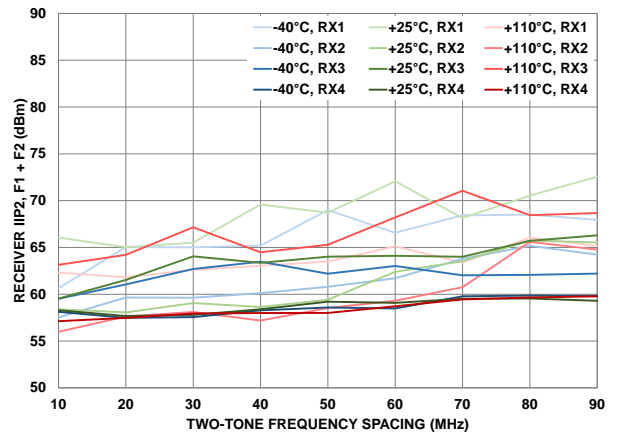


Figure 305. Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

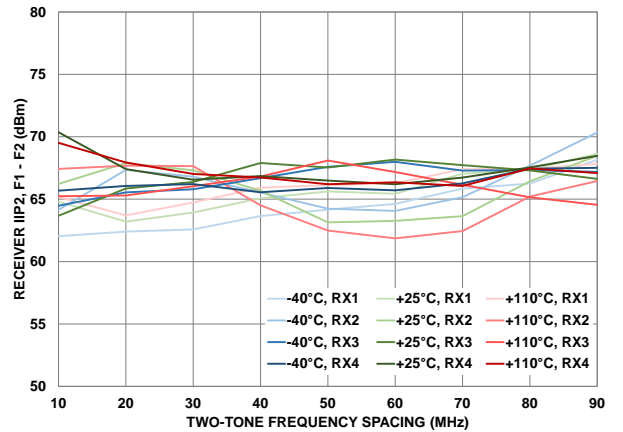


Figure 306. Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, $f_2 = 2$ MHz

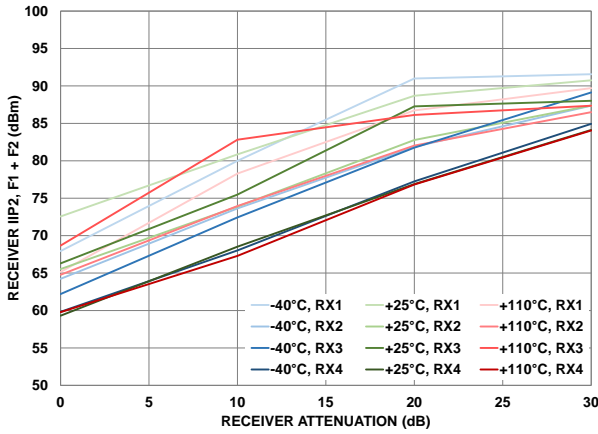


Figure 307. Receiver IIP2, $f_1 + f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

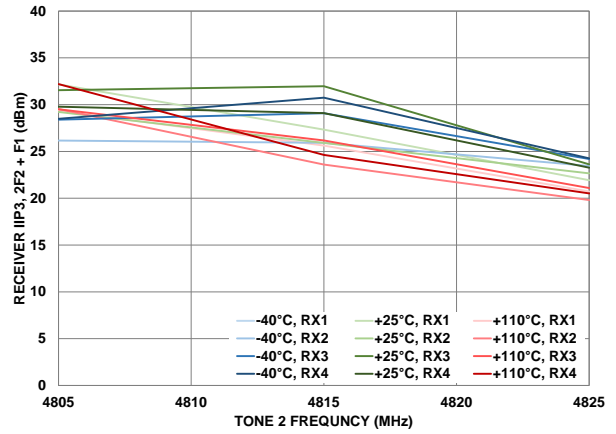


Figure 310. Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

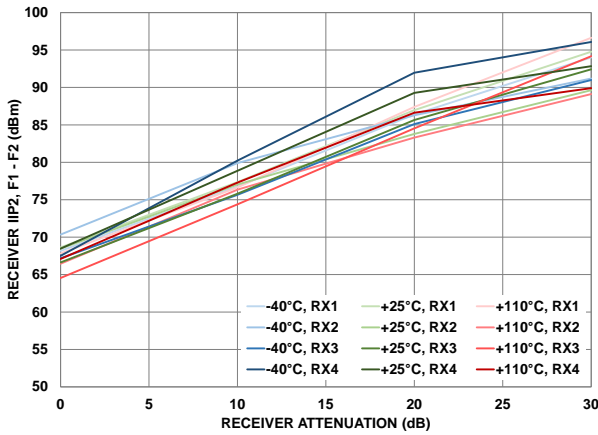


Figure 308. Receiver IIP2, $f_1 - f_2$ vs. Receiver Attenuation, Both Tones at -11 dBFS, $f_1 = 92$ MHz, $f_2 = 2$ MHz

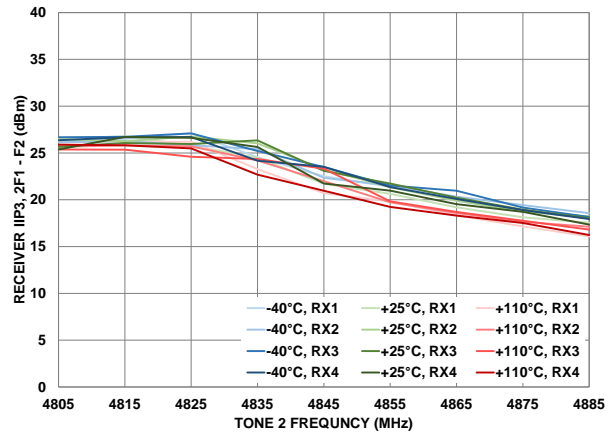


Figure 311. Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

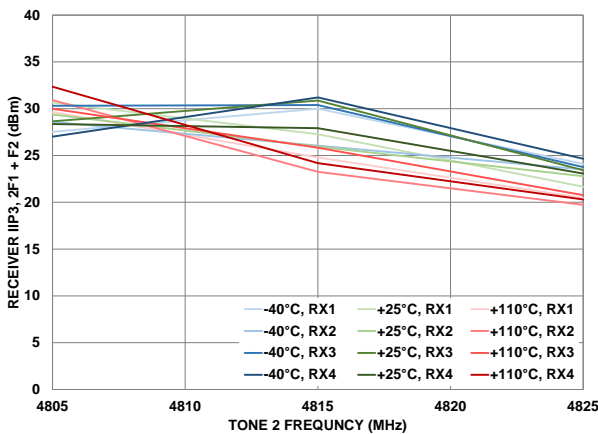


Figure 309. Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

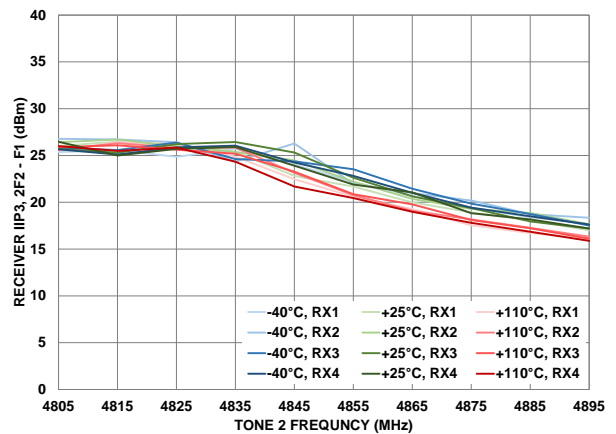


Figure 312. Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -11 dBFS, $f_1 = f_2 + 2$ MHz

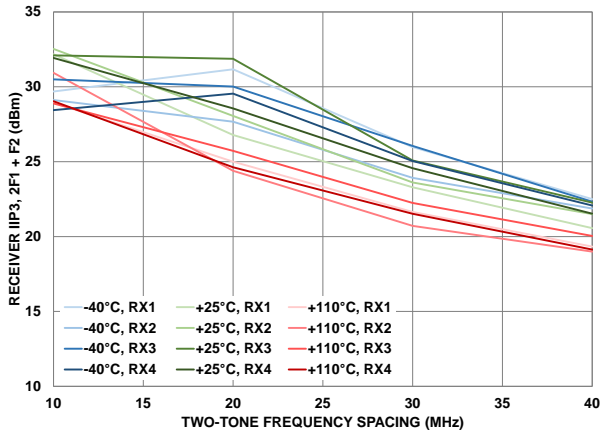


Figure 313. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, f2 = 2 MHz

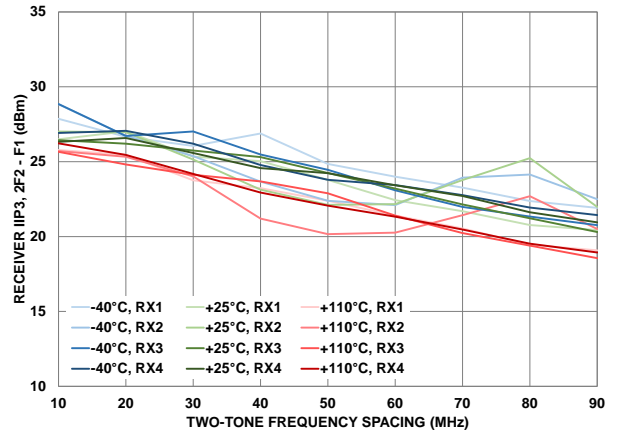


Figure 316. Receiver IIP3, 2f2 - f1 vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, f2 = 2 MHz

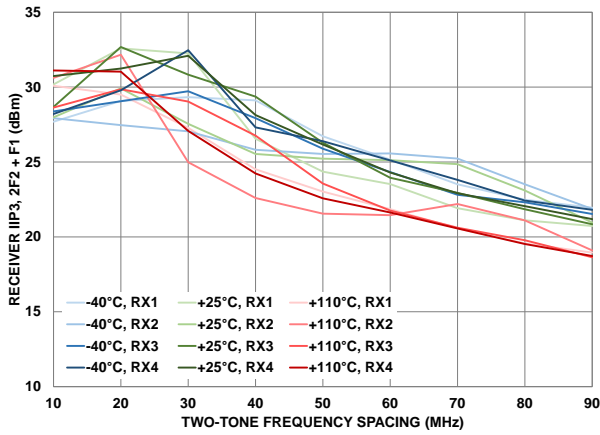


Figure 314. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, f2 = 2 MHz

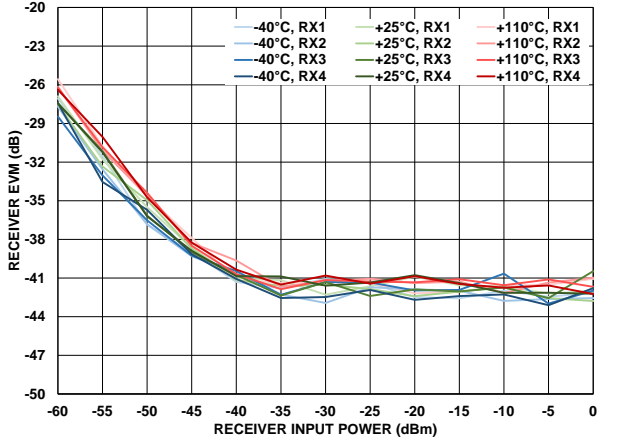


Figure 317. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 400 kHz, Loop Filter Phase Margin = 60°

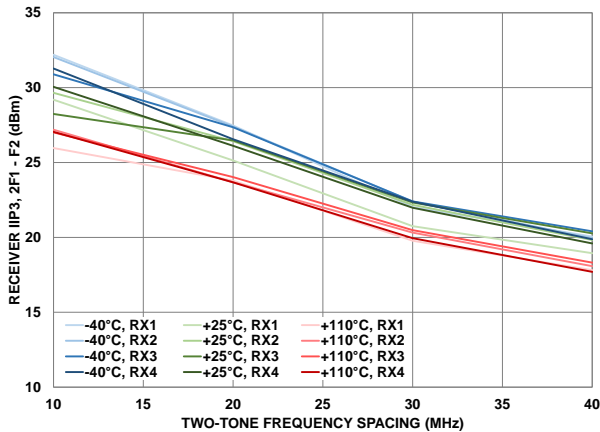


Figure 315. Receiver IIP3, 2f1 - f2 vs. Two-Tone Frequency Spacing, Both Tones at -11 dBFS, f2 = 2 MHz

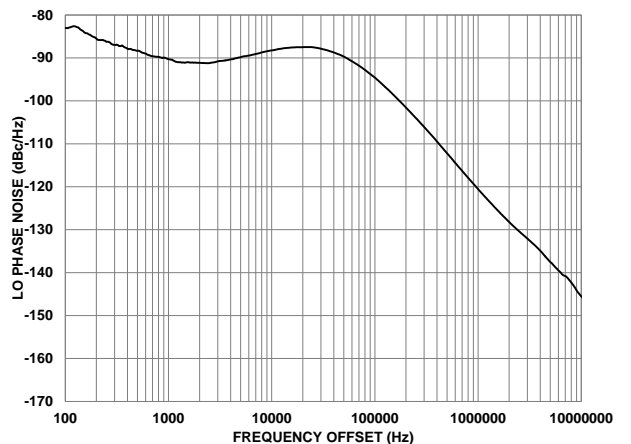


Figure 318. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

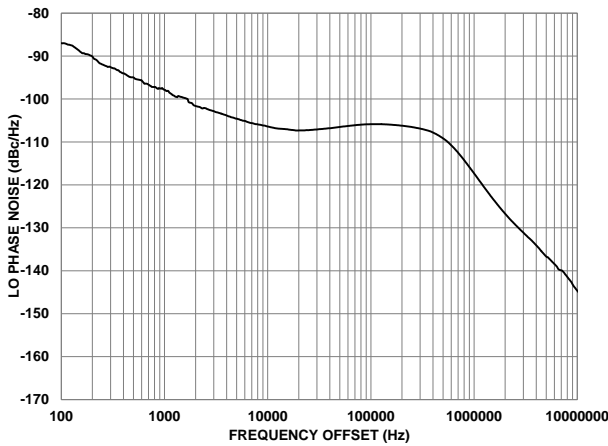


Figure 319. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 400 kHz, Phase Margin = 60°

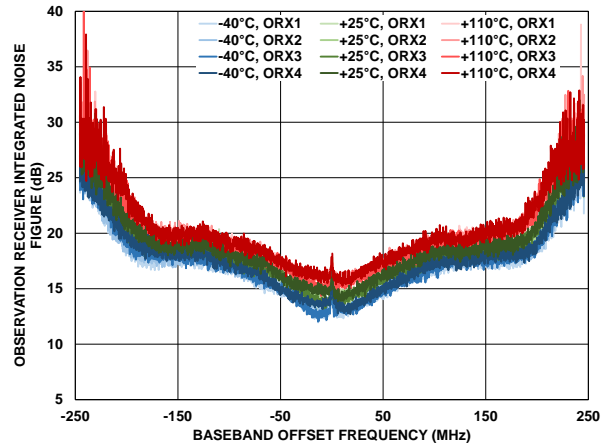


Figure 322. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

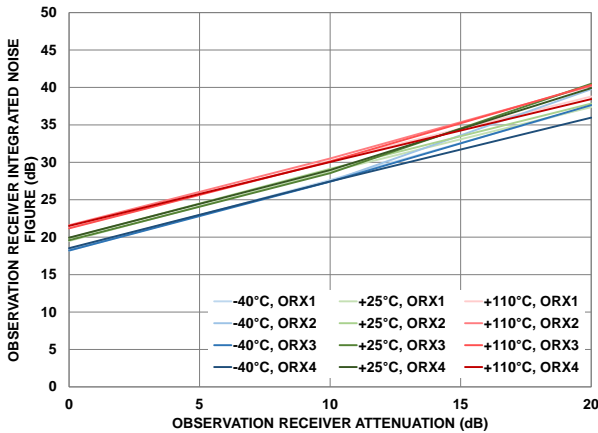


Figure 320. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

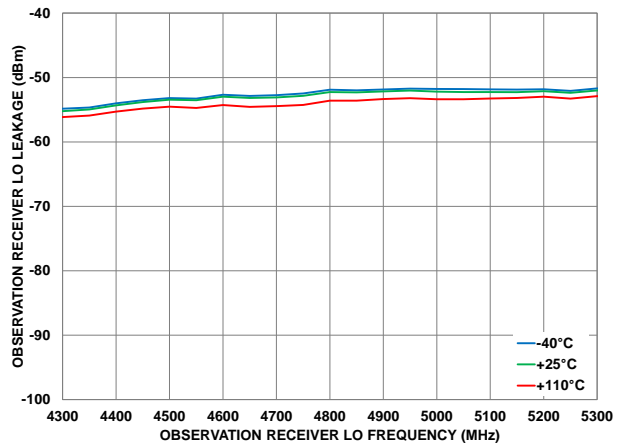


Figure 323. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

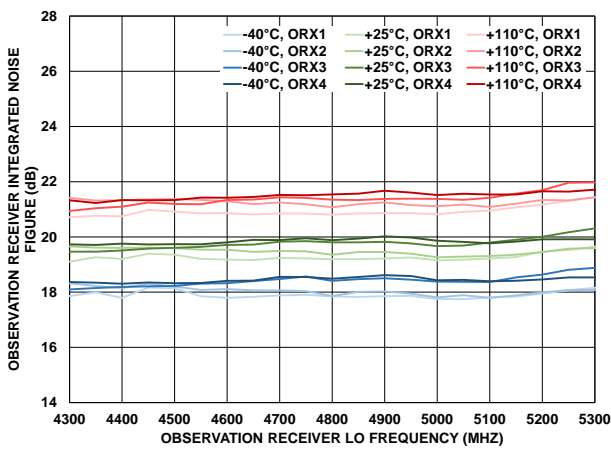


Figure 321. Observation Receiver Integrated Noise Figure vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 245.76 MHz

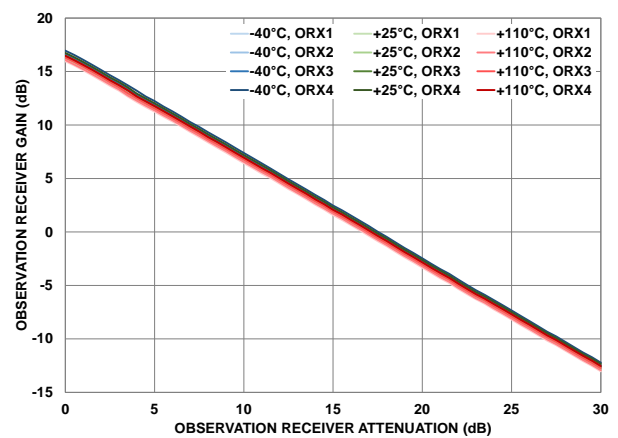


Figure 324. Observation Receiver Gain vs. Observation Receiver Attenuation, 45 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

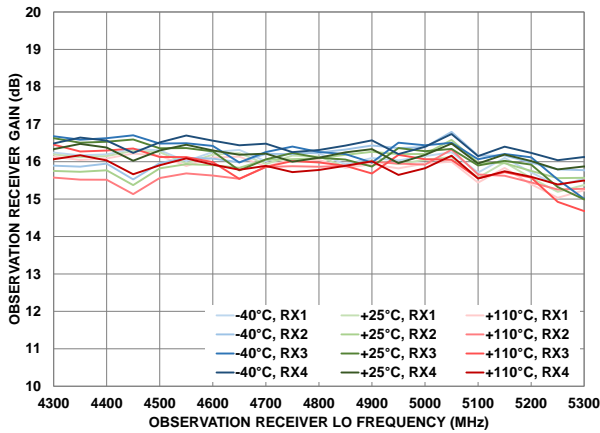


Figure 325. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

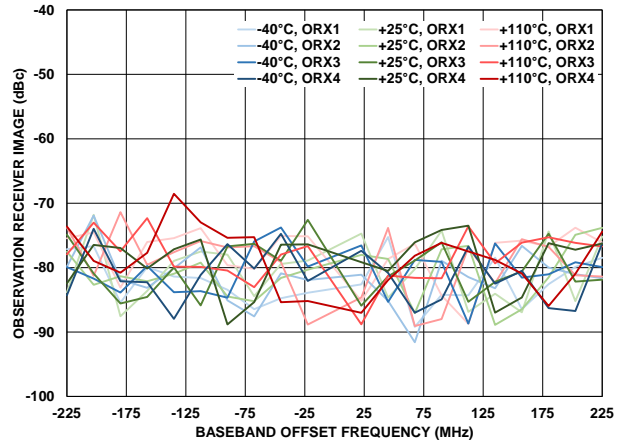


Figure 328. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

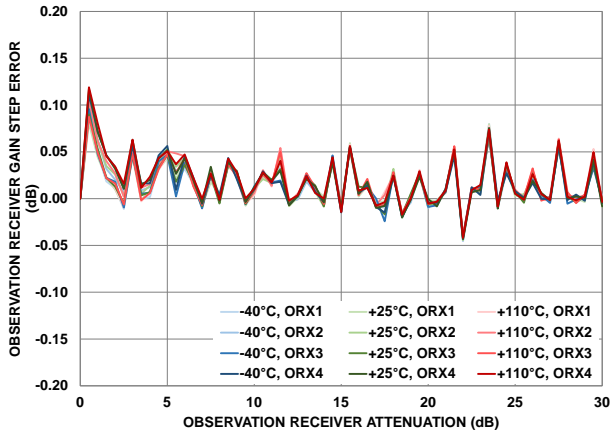


Figure 326. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 45 MHz Offset, -10 dBFS Input Signal

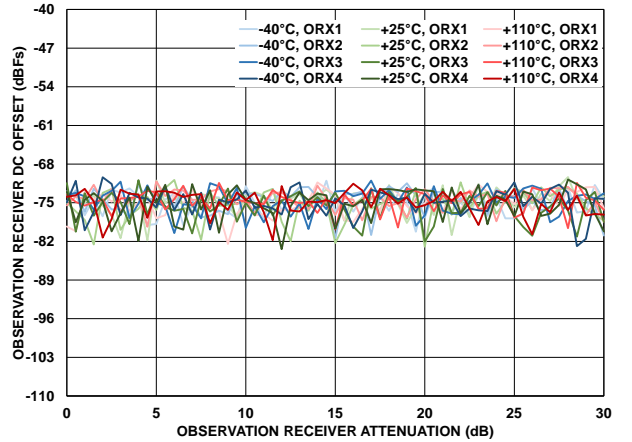


Figure 329. Observation Receiver DC Offset vs. Observation Receiver Attenuation, Sample Rate = 491.52 MSPS

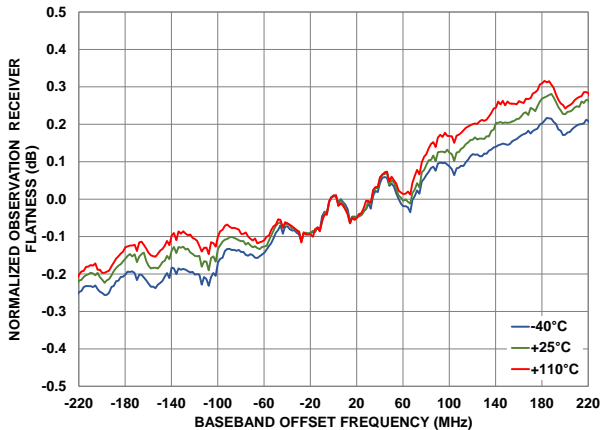


Figure 327. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, -10 dBFS Input Signal

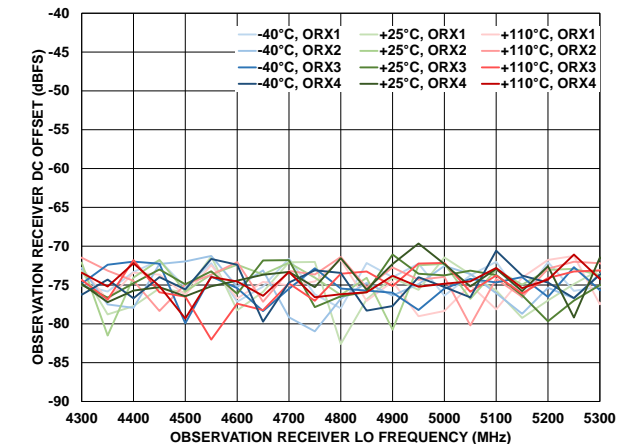


Figure 330. Observation Receiver DC Offset vs. Observation Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 491.52 MSPS

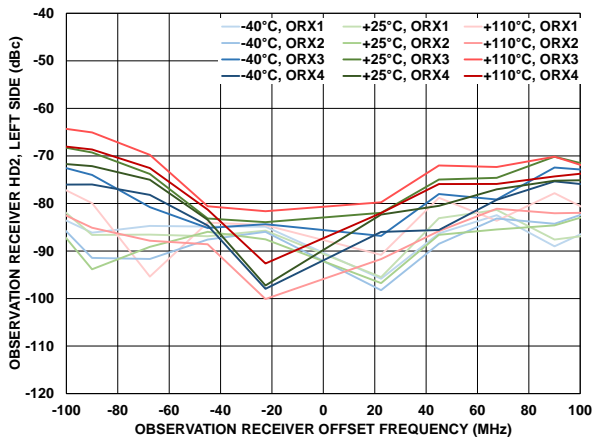


Figure 331. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

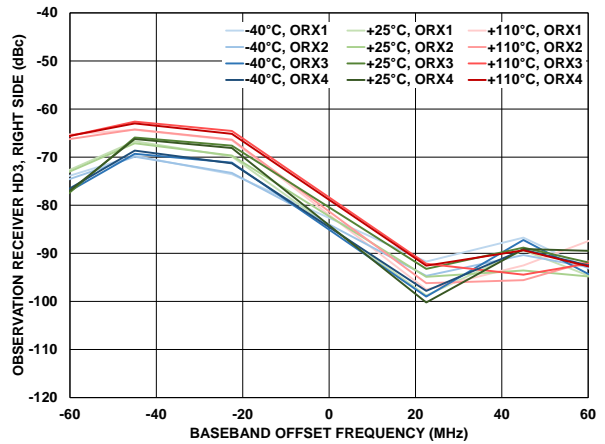


Figure 334. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

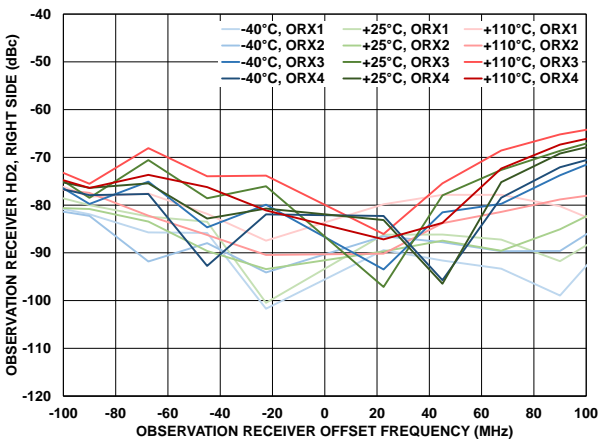


Figure 332. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

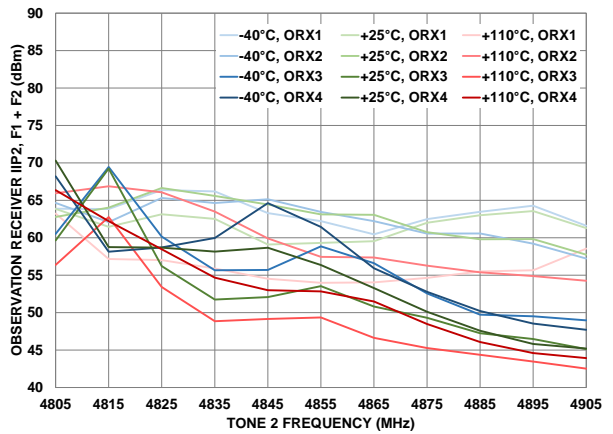


Figure 335. Observation Receiver IIP2, $f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

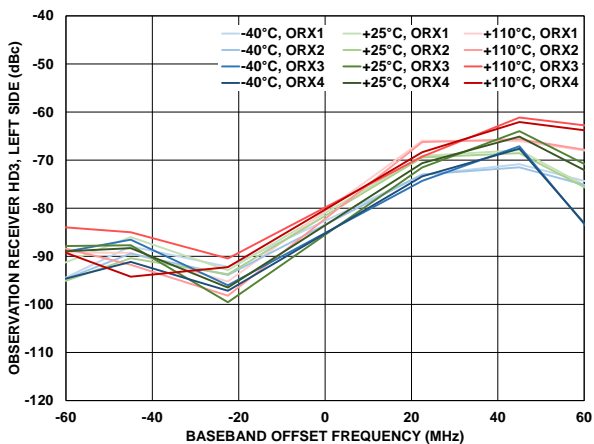


Figure 333. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, -10 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

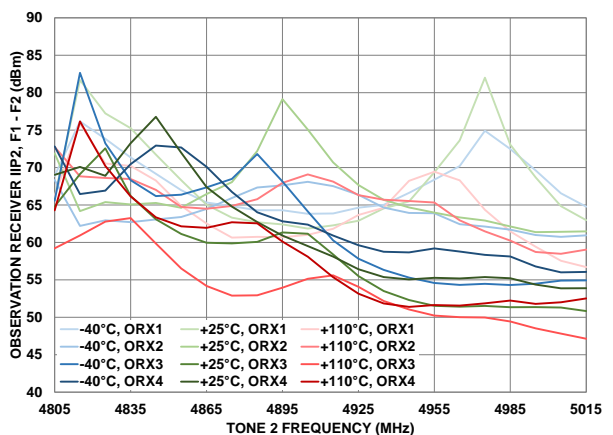


Figure 336. Observation Receiver IIP2, $f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

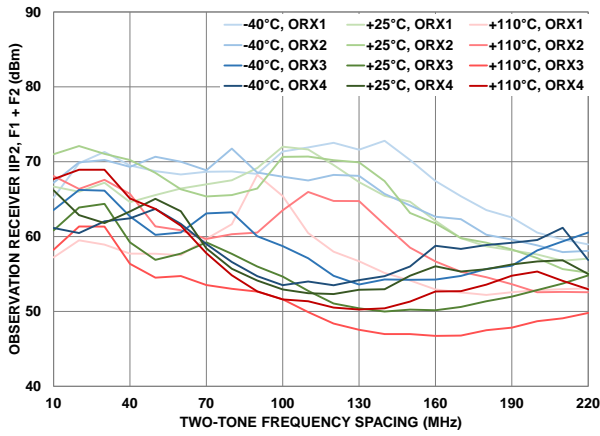


Figure 337. Observation Receiver IIP2, $f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

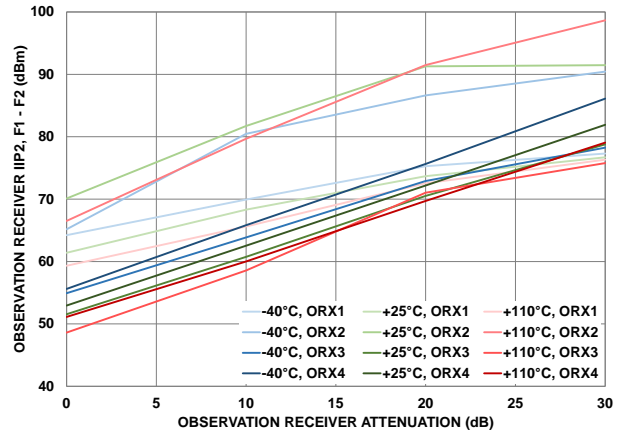


Figure 340. Observation Receiver IIP2, $f_1 - f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

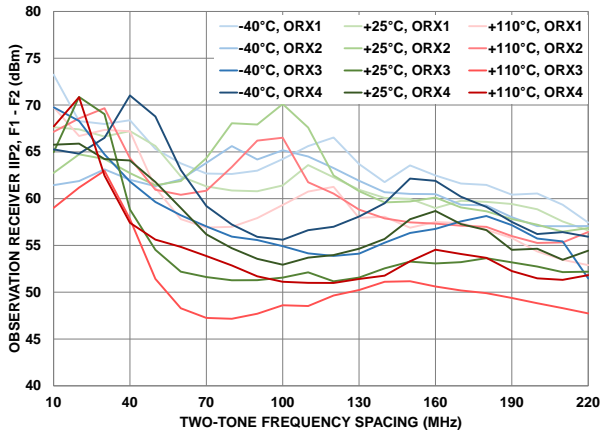


Figure 338. Observation Receiver IIP2, $f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

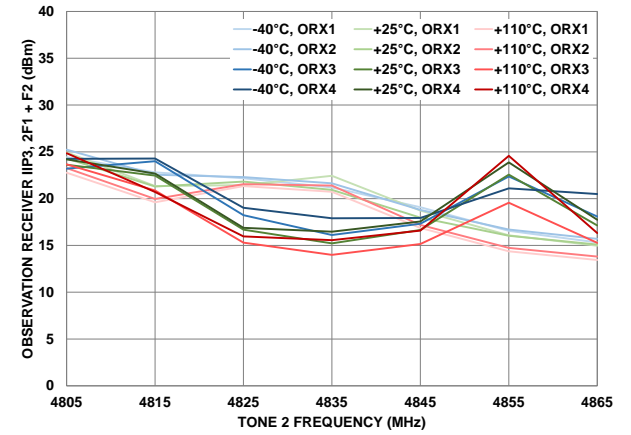


Figure 341. Observation Receiver IIP3, $2f_1 + f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

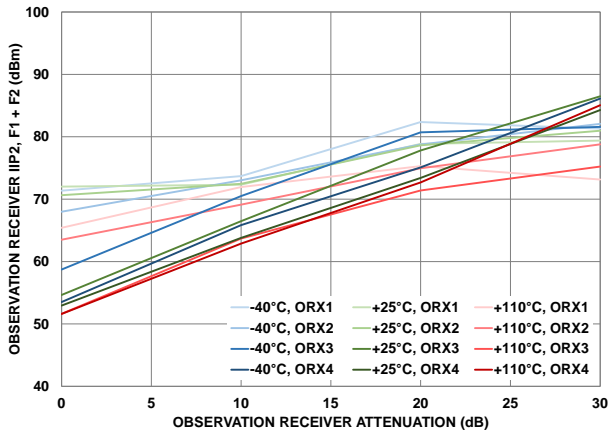


Figure 339. Observation Receiver IIP2, $f_1 + f_2$ vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, $f_1 = 102$ MHz, $f_2 = 2$ MHz

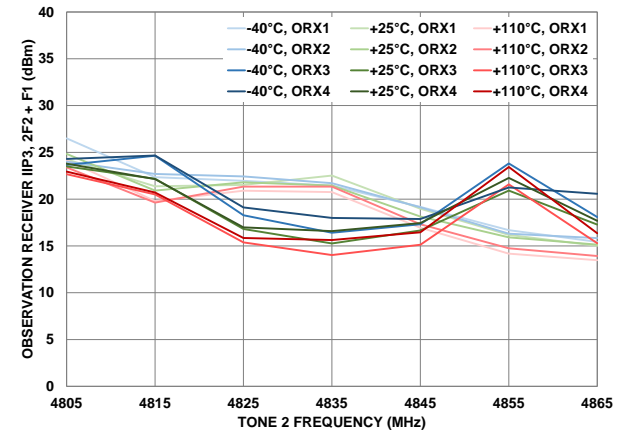


Figure 342. Observation Receiver IIP3, $2f_2 + f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

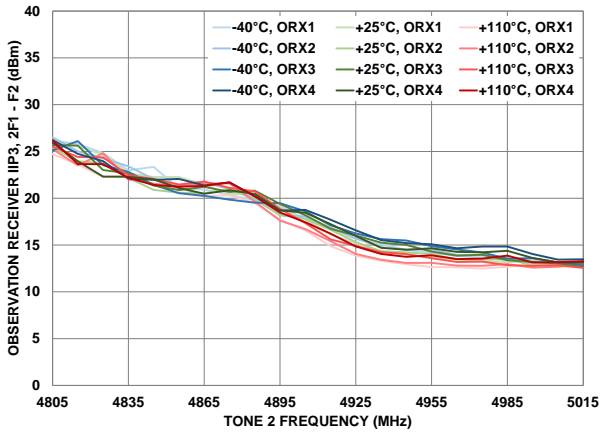


Figure 343. Observation Receiver IIP3, $2f_1 - f_2$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

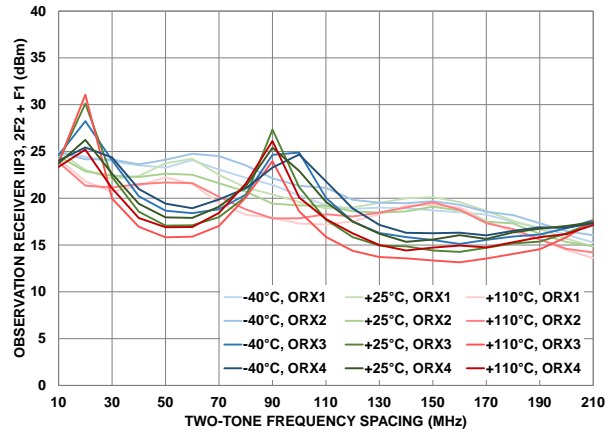


Figure 346. Observation Receiver IIP3, $2f_2 + f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

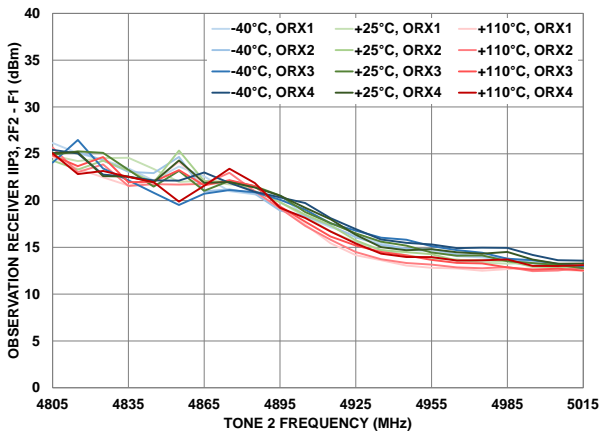


Figure 344. Observation Receiver IIP3, $2f_2 - f_1$ vs. Tone 2 Frequency, Both Tones at -13 dBFS, $f_1 = f_2 + 2$ MHz

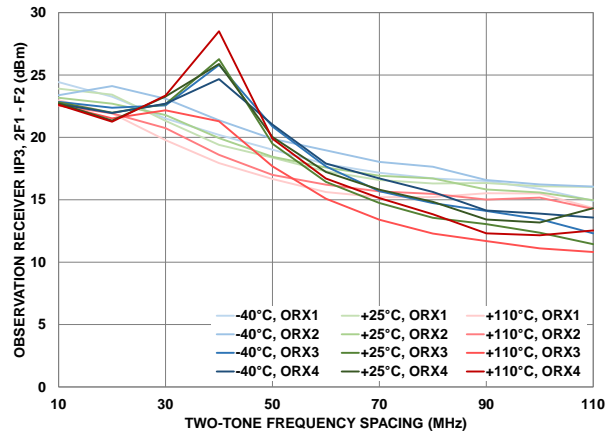


Figure 347. Observation Receiver IIP3, $2f_1 - f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

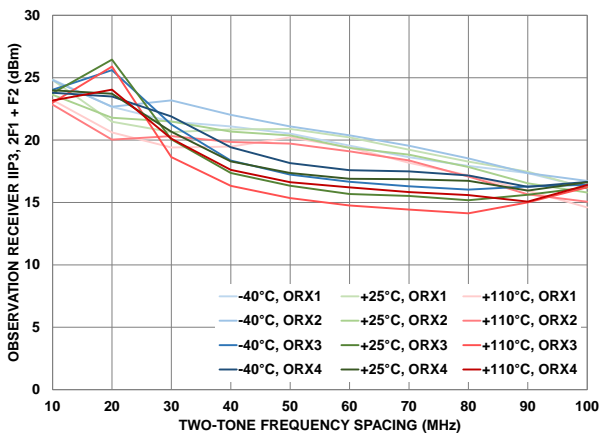


Figure 345. Observation Receiver IIP3, $2f_1 + f_2$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

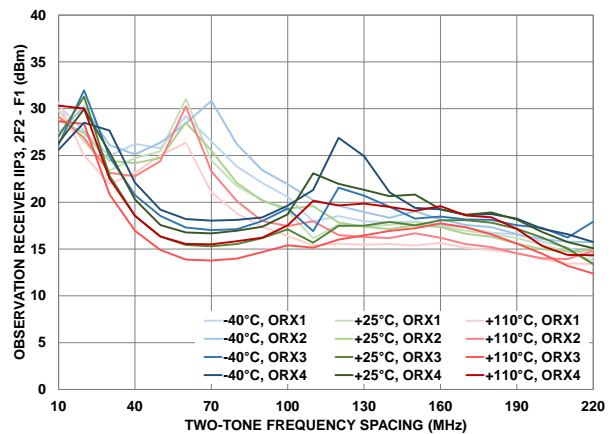


Figure 348. Observation Receiver IIP3, $2f_2 - f_1$ vs. Two-Tone Frequency Spacing, Both Tones at -13 dBFS, $f_2 = 2$ MHz

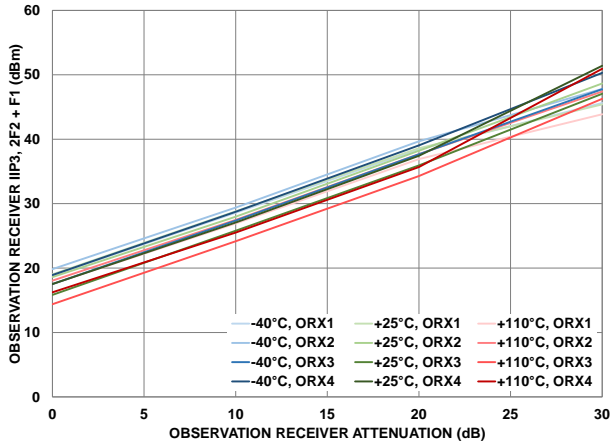


Figure 349. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

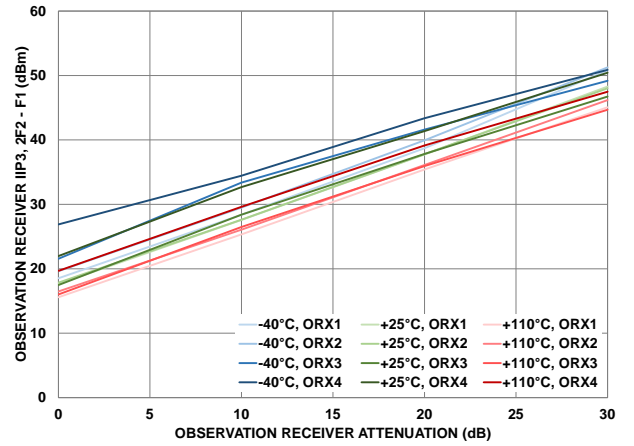


Figure 350. Observation Receiver IIP3, 2f2 - f1 vs. Observation Receiver Attenuation, Both Tones at -13 dBFS, f1 = 122 MHz, f2 = 2 MHz

THEORY OF OPERATION

GENERAL

The ADRV9020 is a highly integrated RF transceiver capable of being configured for a wide range of applications. The device integrates all the RF, mixed-signal, and digital blocks necessary to provide all transmitter, traffic receiver, and observation receiver functions in a single device. Programmability allows the device to be adapted for use in many TDD, 2G/3G/4G, cellular standards.

Four observation receiver channels are included to monitor the transmitter outputs and provide tracking correction of dc offset, quadrature error, and transmitter LO leakage to maintain a high performance level under varying temperatures and input signal conditions. Firmware supplied with the device implements all initialization and calibration with no user interaction. Additionally, the device includes test modes allowing system designers to debug designs during prototyping and to optimize radio configurations.

The ADRV9020 contains eight high speed serial interface (SERDES) links for the transmit chain and eight high speed links shared by the receiver and observation receiver chains (JESD204B Subclass 1 and Subclass 2 compliant and supports JESD204C).

TRANSMITTER

The ADRV9020 transmitter section consists of four identical and independently controlled channels that provide all the digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the SERDES lanes pass through a digital processing block that includes a series of programmable half-band filters, interpolation stages, and FIR filters, including a programmable FIR filter with variable interpolation rates and up to 80 taps. The output of this digital chain is connected to the digital-to-analog converter (DAC). The DAC sample rate is adjustable up to 2.5 GHz. The in-phase (I) and quadrature (Q) channels are identical in each transmitter signal chain.

After conversion to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. Each transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize signal-to-noise ratio (SNR).

RECEIVER

The ADRV9020 provides four independent receiver channels. Each channel contains all the blocks necessary to receive RF signals and convert these signals to digital data usable by a baseband processor. Each receiver can be configured as a direct conversion system that supports up to a 200 MHz bandwidth. Each channel contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization.

Two gain control options are available. Users can implement their own gain control algorithms using their baseband processor to manage manual gain control mode, or users can use the on-chip automatic gain control (AGC) system. Performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receive signal path. Additionally, each channel contains independent receive signal strength indication (RSSI) measurement capability, dc offset tracking, and all the circuitry necessary for self calibration.

The receivers include analog-to-digital converters (ADCs) and adjustable sample rates that produce data streams from the received signals. The signals can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate. The receiver outputs are all connected to the SERDES block, where the data is formatted and serialized for transmission to the baseband processor.

OBSERVATION RECEIVER

The ADRV9020 provides four independent observation receiver inputs. These inputs are similar in implementation to the standard receiver channels in terms of the mixers, ADCs, and filtering blocks. The main difference is that these receivers are designed to operate with an observation bandwidth up to 450 MHz, allowing the receivers to receive all the transmitter channel information needed for implementing digital correction algorithms.

Each input is used as the feedback monitor channel for the corresponding transmitter channel: ORx1 works with Tx1, ORx2 with Tx2, ORx3 with Tx3, and ORx4 with Tx4. The ORx channels can share a common frequency synthesizer with the transmitters or use the auxiliary synthesizer to offset the LO frequency from the transmitter channel being monitored.

CLOCK INPUT

The ADRV9020 requires a differential clock connected to the DEVCLK± pins. The frequency of the clock input must be between 15 MHz and 1000 MHz and must have low phase noise because this signal generates the RF LO and internal sampling clocks.

SYNTHESIZERS

The ADRV9020 contains four fractional-N PLLs to generate the RF LO for the signal paths and all internal clock sources. This group of PLLs includes two RF PLLs for transmit and receive LO generation, an auxiliary PLL that can be used by the observation receivers, and a clock PLL. Each PLL is independently controlled with no need for external components to set frequencies.

RF Synthesizers

The two RF synthesizers use fractional-N PLLs to generate RF LOs for the multiple receiver and transmitter channels. This PLL incorporates a four-core internal voltage-controlled oscillator (VCO) and loop filter, capable of generating low phase noise signals with no external components required. An internal LO multiplexer (mux) enables each PLL to supply LOs to any or all receivers and transmitters (for example, LO1 to all transmitters, LO2 to all receivers), resulting in maximum flexibility when configuring the device for TDD operation. The LOs on multiple devices can be phase synchronized to support active antenna systems and beam forming applications.

Auxiliary Synthesizer

The auxiliary synthesizer uses a single core VCO fractional-N PLL to generate the signals necessary to calibrate the device. The output of this block uses a separate mux system to route LOs for calibrating different functions during initialization. The auxiliary synthesizer can also be used to generate LO signals for the observation receivers or as an offset LO used in the receiver signal chains.

Clock Synthesizer

The ADRV9020 contains a single core VCO fractional-N PLL synthesizer that generates all baseband related clock signals and SERDES clocks. This PLL is programmed based on the data rate and sample rate requirements of the system, which typically require the system to operate in integer mode.

For JESD204B configurations with $N_p = 12$ and JESD204C configurations, a dedicated PLL included in the SERDES block generates the SERDES clocks.

External LO Inputs

The ADRV9020 provides two external LO inputs to allow an external synthesizer to be used with the device. These inputs must be $2\times$ the desired LO frequency. One input is multiplexed with the RF1 PLL, and the other input is multiplexed with the RF2 PLL. Each observation receiver can obtain the LO from either the same input as the associated transmitter channel or its own dedicated PLL.

SPI INTERFACE

The ADRV9020 uses a SPI to communicate with the baseband processor. This interface can be configured as a 4-wire interface with dedicated receive and transmit ports, or the interface can be configured as a 3-wire interface with a bidirectional data communications port. This bus allows the baseband processor to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first bit sets the bus direction of the bus transfer. The next 15 bits set the address where data is written. The final eight bits are the data being transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DIO pin, and the final eight bits are read from the ADRV9020, either on the SPI_DO pin in 4-wire mode or on the SPI_DIO pin in 3-wire mode.

POWER SUPPLY SEQUENCE

The ADRV9020 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDIG_1P0 supply is activated first. If the same supply is used to power VDDA_1P0, then all 1.0 V supplies can be powered on at the same time.

If VDIG_1P0 is isolated, all VDDA_1P8, VDDA_1P3, and VDDA_1P0 supplies must be powered up after VDIG_1P0 is activated. The VIF supply can be powered up at any time.

It is also recommended prior to configuration to toggle the RESET signal after power has stabilized.

If a power-down sequence is followed, to avoid any back biasing of the digital control lines, remove the VDIG_1P0 supply last. If no sequencing is used, it is recommended to power down all supplies simultaneously.

GPIO_X PINS

The ADRV9020 provides 19 general-purpose input/output signals (GPIOs) referenced to VIF that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the baseband processor, allowing the baseband processor to determine receiver performance. A pointer register selects what information is output to these pins.

Signals used for manual gain mode, calibration flags, state machine status, and various receiver parameters are among the outputs that can be monitored on these pins. Additionally, certain pins can be configured as inputs and used for various functions such as setting the receiver gain in real time.

AUXILIARY CONVERTERS

GPIO_ANA_x/AUXDAC_x

The ADRV9020 contains eight analog GPIOs (the GPIO_ANA_x pins) that are multiplexed with eight identical auxiliary DACs (AUXDAC_x). The analog GPIO ports can be used to control other analog devices or receive control inputs referenced to the VDDA_1P8 supply. The AUXDACs are 12-bit converters capable of supplying up to 10 mA in a voltage range of 0.1 V

to (VDDA_1P8 – 0.1 V). These outputs are typically used to supply bias current or variable control voltages for other related components with analog control inputs.

AUXADC_x

The ADRV9020 contains two auxiliary ADCs with four total input pins (AUXADC_x). These auxiliary ADCs provide 10-bit monotonic outputs with an input voltage range of 0.05 V to 0.95 V. When enabled, each auxiliary ADC is free running. An application programming interface (API) command latches the ADC output value to a register. The ADRV9020 also contains an ADC that supports a built-in diode-based temperature sensor.

DATA INTERFACE

The digital data interface for the ADRV9020 implements JEDEC Standard JESD204B Subclass 1, Subclass 2, and JESD204C. The serial interface operates at speeds of up to 24.33 Gbps.

Table 12,

Table 13, and Table 14 list example parameters for various JESD interface settings.

Table 12. Example Rx Interface Rates with 4 Channels Active (M=8) (other output rates, BW, and number of lanes also supported)

BW (MHz)	Output Rate (MSPS)	JESD Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
40	61.44	16	16	9830.4	1	16	8110.08	1
60	76.8	16	8	6144	2	8	5068.8	2
100	122.88	16	8	9830.4	2	16	8110.08	2
150	184.32	16	4	7372.8	4	4	6082.56	4
200	245.76	16	4	9830.4	4	4	8110.08	4
200	245.76	16	4	9830.4	4	4	16220.16	2
200	245.76	12	3	7372.8	4	3	6082.56	4
200	245.76	12	6	14745.6	2	12	24330.24	1

Table 13. Tx Interface Rates with 4 Channels Active (M=8) (other output rates, BW, and number of lanes also supported)

Primary Signal BW (MHz)	Total BW (MHz)	Input Rate (MSPS)	JESD Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
50	113	122.88	16	8	9830.4	2	8	8110.08	2
75	150	184.32	16	4	7372.8	4	4	6082.56	4
100	225	245.76	16	4	9830.4	4	4	8110.08	4
100	225	245.76	16	4	9830.4	4	8	16220.16	2
200	450*	245.76	16	4	9830.4	4	4	8110.08	4
200	450*	245.76	16	4	9830.4	4	8	16220.16	2
200	450	491.52	12	3	14745.6	4	6	24330.24	2

*Uses Internal DPD Interpolation filters

Table 14. Observation Path Interface Rates with 1 Channel Active (M=2) (other output rates, BW, and number of lanes also supported)

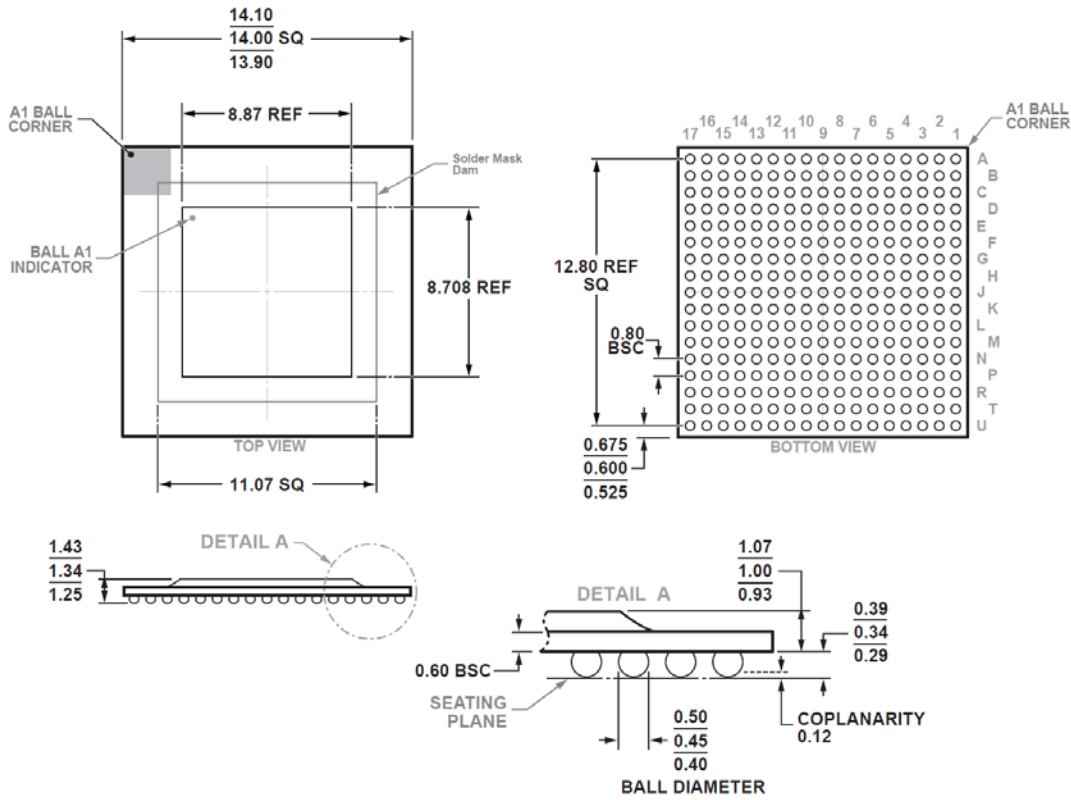
Total BW (MHz)	Output Rate (MSPS)	JESD Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
150	184.32	16	4	7372.8	1	4	6082.56	1
220	245.76	16	4	9830.4	1	4	8110.08	1
250	307.2	16	2	6144	2	2	5068.8	2
300	368.64	16	2	7372.8	2	2	6082.56	2
450	491.52	16	2	9830.4	2	2	8110.08	2
450	491.52	16	2	9830.4	2	4	16220.16	1
450	491.52	12	3	7372.8	2	3	6082.56	2
450	491.52	12	3	7372.8	2	3	12165.12	1

OUTLINE DIMENSIONS



289-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-289-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-275-JJAB-1

Figure 351. 289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-289-6) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADRV9020BBCZ	-40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-6
ADRV9020BBCZ-REEL	-40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-6

Z = RoHS Compliant Part.