XPC2443

4.5V to 17V Input, 12A, Synchronous, Step-Down Converter

FEATURES

- 4.5V to 17V Input Voltage Range
- Integrated 9.8mΩ/4.5mΩ MOSFETs
- 0.6V ±1% Voltage Reference
- Adjustable Output Voltage from 0.6V to 5.5V
- Supports Ceramic Output Capacitor
- Selectable Switching Frequency (400kHz/800kHz/1200kHz)
- Selectable Current Limit Level
- Power Good Indicator
- Programmable Soft-Start Time with a Default 1ms
- Monotonic Start-Up into Pre-Biased Outputs
- 18-Lead VQFN (FC) Package

APPLICATIONS

- Server, Storage and Network Equipment
- Telecom Infrastructure
- Point of Load (POL) Power Modules
- High Density DC-DC Converters
- High End Digital TV

DESCRIPTION

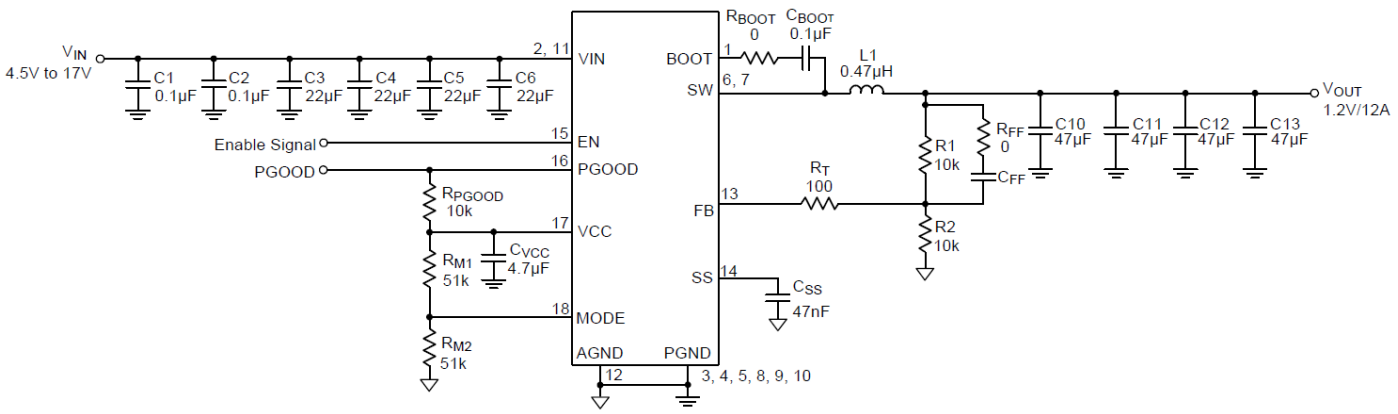
The XPC2443 is a high-performance, synchronous step-down converter that can deliver up to 12A output current with an input supply voltage range of 4.5V to 17V. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode for bootstrap circuit to offer a very compact solution.

The XPC2443 adopts Constant On-Time control architecture that provides ultrafast transient response and further reduce the external-component count. In steady states, this part operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers a variety of functions for more design flexibility. The selectable switching frequency, current limit level and PWM operation modes makes the XPC2443 easy-to-use over wide application range. Independent enable control input pin and power good indicator are also provided for easy sequence control. To control the inrush current during the startup, the device provides a programmable soft start-up by an external capacitor connected to the SS pin. Fully protection features are also integrated in the device including the cycle-by-cycle current limit, OVP, UVP, input UVLO and OTP.

The XPC2443 is available in a thermally enhanced VQFN-18L 3.5x3.5 (FC) package.

TYPICAL APPLICATION



Notes:

1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

2) Consider the noise immunity when the CFF is soldered on PCB, it is necessary to add RT = 100Ω between feedback network and chip FB pin.

Table 1. Suggested Component Selections for the Application of 400kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.6	0	10	0.68	88	188	NC
1.2	10		1.2	88	188	NC
3.3	45.2		2.4	88	188	100 to 200
5	73.2		3.3	88	188	100 to 200

Table 2. Suggested Component Selections for the Application of 800kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.6	0	10	0.47	88	188	NC
1.2	10		0.68	88	188	NC
3.3	45.2		1.5	88	188	100 to 200
5	73.2		2.4	88	188	100 to 200

Table 3. Suggested Component Selections for the Application of 1200kHz

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	L1(μH)	C_{OUT_MIN} (μF)	$C_{OUT\_TYPICAL}$(μF)	C_{FF} (pF)
0.6	0	10	0.33	88	188	NC
1.2	10		0.47	88	188	NC
3.3	45.2		1.2	88	188	100 to 200
5	73.2		1.5	88	188	100 to 200

Table 4. Suggested Inductors for Typical Application Circuit

Inductance (μH)	Part No.	I_{SAT} (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.47	744314047	20	1.35	7.0 x 7.0 x 5.0	WE-HCI
0.68	744311068	20	3.1	7.0 x 7.0 x 4.0	WE-HCI
1.2	744325120	25	1.8	10.5 x 10.5 x 5	WE-HCI
1.5	7443552150	17	5.3	10.5 x 10.5 x 4	WE-HCI
2.4	744325240	17	4.75	10.5 x 10.5 x 5	WE-HCI
3.3	744325330	15	5.9	10.5 x 10.5 x 5	WE-HCI

Table 5. Suggested Capacitor for Typical Application Circuit

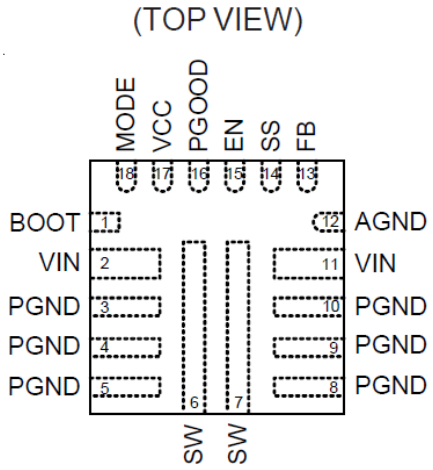
Capacitance (μF)	Part No.	Case Size	Component Supplier
22	C2012X5R1V226M125AC	0805	TDK
47	GRM21BR61A476ME15	0805	Murata
47	GRM31CR61C476ME44	1206	Murata
4.7	GRM188R61E475KE11	0603	Murata
0.1	C1608X7R1H104K080AA	0603	TDK

ORDERING INFORMATION

Part Number	EN	Top Marking	MPQ
XPC2443AQ35R	Internal Pull High	2443A	3,000
XPC2443BQ35R	Internal Pull Low	2443B	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN Configuration and Description



VQFN-18L 3.5x3.5 (FC)

Pin Configuration

Pin	Name	Description
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1uF ceramic capacitor between the BOOT and SW pins.
2, 11	VIN	Input voltage. Support 4.5V to 17V input voltage. Suggest placing equal-value input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
3, 4, 5, 8, 9, 10	PGND	System GND. The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections. The AGND and PGND are tied together with a short trace and at only one point to reduce circulating currents.
6, 7	SW	Switch node. Connect to the power inductor.
12	AGND	Analog GND. The AGND and PGND are tied together with a short trace and at only one point to reduce circulating currents.
13	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest placing the FB resistor divider as close to FB pin and AGND as possible.
14	SS	Soft-start time control pin. Connect a capacitor between the SS pin and AGND to set the soft-start time. The default internal start-up time is 1ms without external capacitor.
15	EN	IC enable. XPC2443AQ35R : Internal pull high. XPC2443BQ35R : Internal pull low.
16	PGOOD	Open-drain, power-good indication output. It is pulled low if the feed-back voltage is out of PGOOD threshold, IC shutdown from OTP and EN goes low, and before the soft start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
17	VCC	4.7V internal LDO output. Connect a 4.7μF capacitor as close to the VCC pin as possible. It is not recommended to connect VCC to supply other rails.
18	MODE	Switching frequency, current limit selection and light load operation mode selection pin. Connect this pin to a resistor divider from VCC and AGND for different MODE options.

Absolute Maximum Ratings (1)

Parameter	Min	Max	Units
Supply Input Voltage, VIN	-0.3	20	V
Enable Pin Voltage, EN	-0.3	6.5	V
SW	-0.3	20	V
SW (50ns transient)	-5	25	V
VIN-SW	-0.3	20	V
VIN-SW (10ns transient)	-5	25	V
BOOT	-0.3	26	V
BOOT−SW	-0.3	6	V
BOOT−SW (10ns transient)	-0.3	7.5	V
All Other Pins	-0.3	6	V
Power Dissipation, PD @ TA = 25°C VQFN-18L 3.5x3.5 (FC)		3.63	W
Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range	-65	150	°C
ESD Susceptibility (2) HBM (Human Body Model)	2		kV

RECOMMENDED OPERATING CONDITIONS (3)

Parameter	Symbol	Min	Max	Units
Control Input Voltage, VIN	V_{IN}	4.5	17	V
Junction Temperature Range	T_{OJ}	-40	+125	°C

Thermal Information(4)

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. In this case, θ_{JA}, $\theta_{JC(top)}$ and ΨJB are measured on four-layer XPC2443 EVB in still air box on natural convection. $\theta_{JC(Bottom)}$ and ΨJC(Top) are derived from thermal simulation result in accordance with JEDEC standard JESD51.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance (JEDEC standard)	θ_{JA}	27.5	°C/W
Junction-to- Case (Top) Thermal Resistance	$\theta_{JC(top)}$	2.5	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$\theta_{JC(Bottom)}$	0.5	°C/W
Junction-to-Ambient Thermal Resistance (specific EVB)	$\theta_{JA(EVB)}$	26.8	°C/W
Junction-to-Top Characterization Parameter	ΨJC(Top)	2.8	°C/W
Junction-to-Board Characterization Parameter	ΨJB	8	°C/W

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) Devices are ESD sensitive. Handling precaution is recommended.

(3) The device is not guaranteed to function outside its operating conditions.

(4) θJA is measured in the natural convection at TA = 25°C on a Four-layer Evaluation Board. θJC(top) is measured at the top of the package. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions

ELECTRICAL SPECIFICATIONS

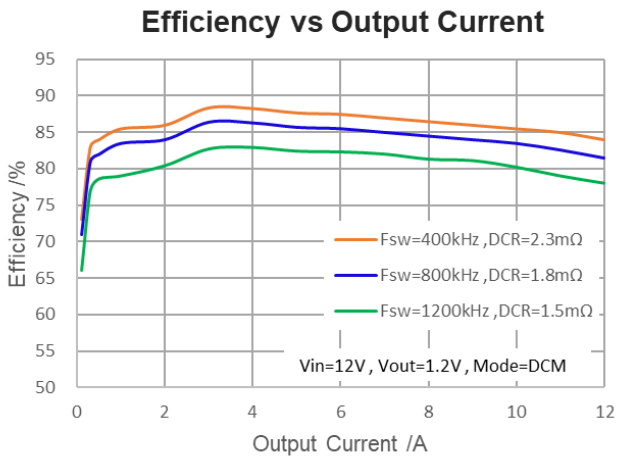
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

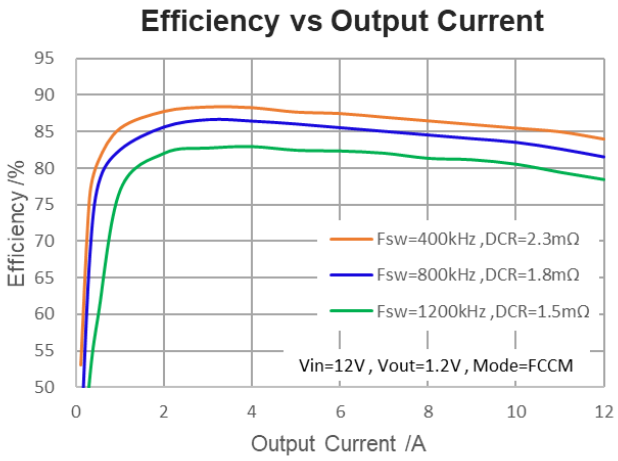
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage						
VIN Power Input Operating Voltage	VIN		4.5		17	V
VIN Shutdown Current	Isd	T_J = 25°C, V_{EN} = 0V	3	7	21	uA
VIN Quiescent Current	I_Q	T_J = 25°C, V_{EN} = 5V, non-switching	350	800	900	uA
EN Threshold Voltage	VIH	V_{EN} Rising	1.175	1.225	1.3	V
	VIL	V_{EN} Falling	1.025	1.104	1.15	V
EN Pull-Up Current (XPC2443A)	IENP1	V_{EN} = 1V	0.35	2	2.95	uA
	IENP2	V_{EN} = 1.3V	3	4.2	5.5	uA
EN Pull-Down Current (XPC2443B)	IENDN	T_J = 25°C, V_{EN} = 2V		2.5		uA
VFB Voltage						
FB Voltage	VFB		0.594	0.6	0.606	V
Switching Frequency						
Switching Frequency	f_{SW1}	T_J = 25°C, CCM	320	400	480	kHz
	f_{SW2}	T_J = 25°C, CCM	640	800	960	kHz
	f_{SW3}	T_J = 25°C, CCM	960	1200	1440	kHz
Internal MOSFET						
High Side ON Resistance	$R_{DS(ON)\_H}$	T_J = 25°C, VCC = 4.7V		9.8		mOhm
Low Side ON Resistance	$R_{DS(ON)\_L}$	T_J = 25°C, VCC = 4.7V		4.5		mOhm
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	VIN = 17V, VOUT = 0.6V f_{SW} = 1200kHz	40	50	70	ns
Minimum Off-Time	t_{OFF_MIN}	TJ = 25°C, VFB = 0.5V	200		310	ns
Soft-Start and Tracking						
Soft-Start Time	t_{SS}	Internal soft-start time	0.5	1.1	2	ms
Soft-Start Charge Current	I_{SS}		4.9	6	7.1	uA
Current Limit						
Low-Side Switch Current Limit	ILIM_1	Valley current	11.73	13.8	15.87	A
	ILIM_2		9.775	11.5	13.225	A
Low-Side Switch Negative Current Limit	ILIM_NEG				-5	A
UVLO						
UVLO Rising Threshold	V_{UVLOH}	V_{LDO} rising	4	4.4	4.5	V
UVLO Hysteresis	ΔV_{UVLO}	V_{LDO} hysteresis		700		mV

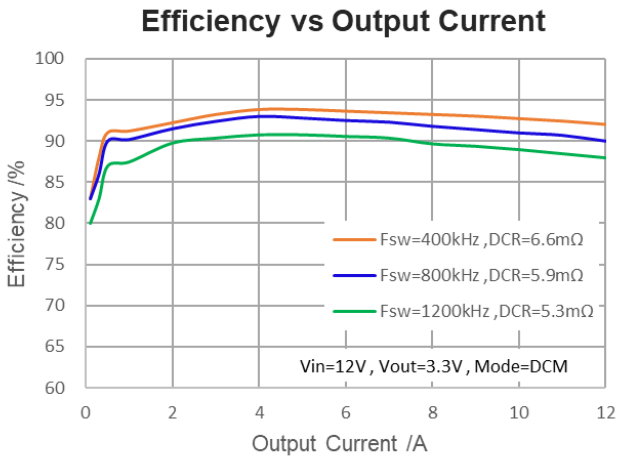
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

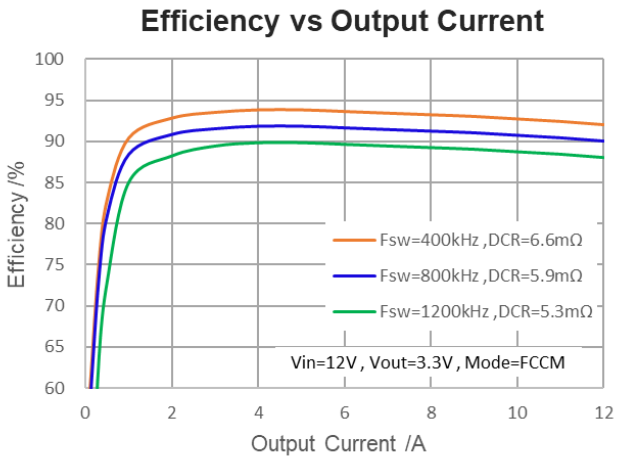
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LDO Output						
LDO Output Voltage	VCC		4.58	4.7	4.83	V
LDO Output Current Limit	ILIM_LDO		45		200	mA
Power Good						
Power Good Rising Threshold	rise_good	VFB rising (GOOD)	86	93	100	%V_{REF}
	rsie_fault	VFB rising (FAULT)	110	116	123	%V_{REF}
Power Good Falling Threshold	fall_fault	VFB falling (FAULT)	75	84	93	%V_{REF}
	fall_good	VFB falling (GOOD)	97	107	117	%V_{REF}
Power Good Low-level Voltage	$V_{PG,OL}$	Isink = 1mA		0.2	0.4	V
Output Under-Voltage and Over-Voltage Protections						
Output OVP Threshold	V_{OVP}	OVP detect	114	121	128	%V_{FB}
Output UVP Threshold	V_{UVP}	UVP detect	61	68	75	%V_{FB}
Over Temperature Protection						
Thermal Shutdown	Tsd			160		°C
Thermal Shutdown Hysteresis	ΔTsd			15		°C
LDO Thermal Shutdown Threshold	TSD_LDO			170		°C
LDO Thermal Shutdown Hysteresis	ΔTSD_LDO			20		°C

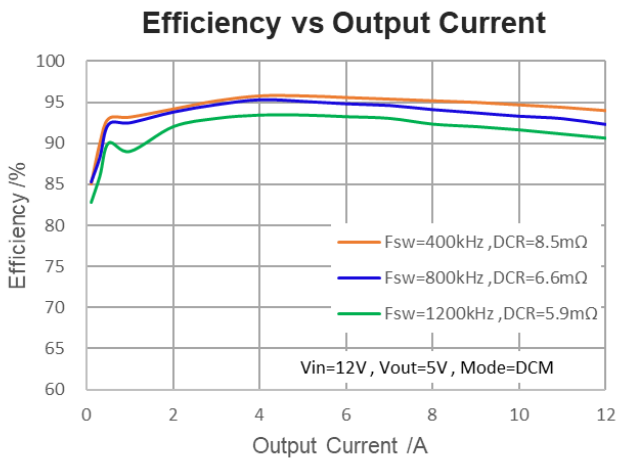
TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS

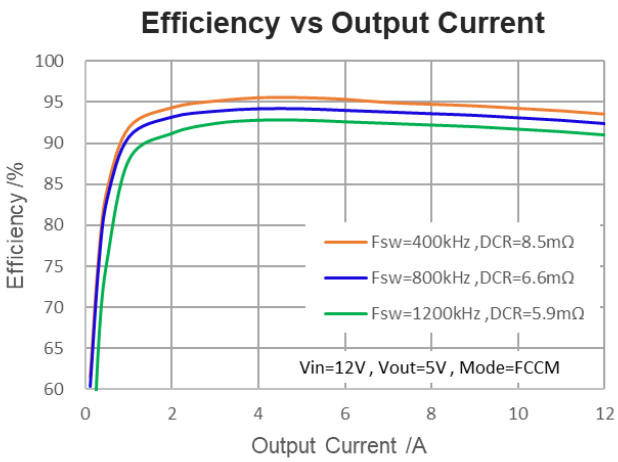


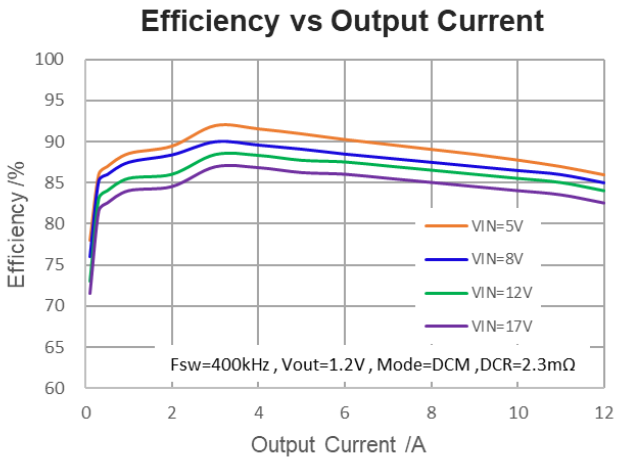








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Efficiency /%
Output Current /A
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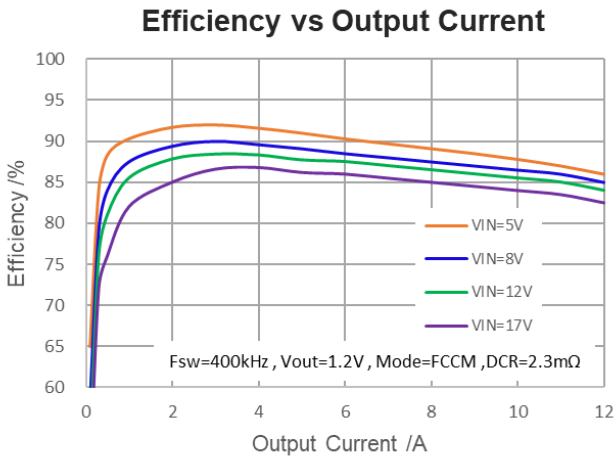
VIN=8V
VIN=12V
VIN=17V
Fsw=400kHz , Vout=1.2V , Mode=DCM ,DCR=2.3mΩ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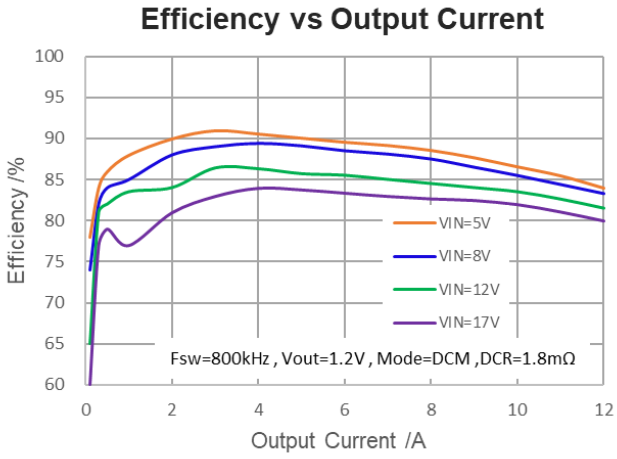
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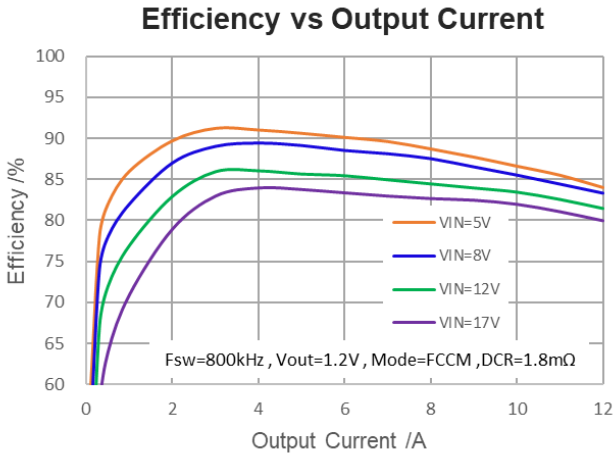
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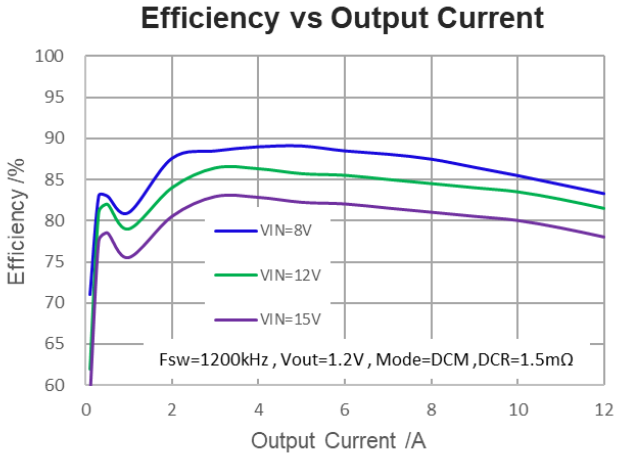
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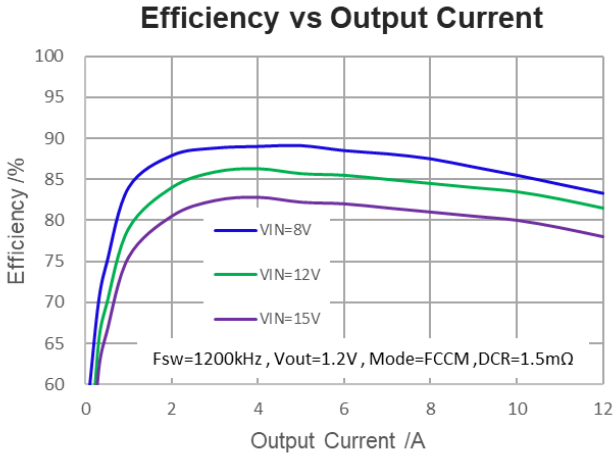
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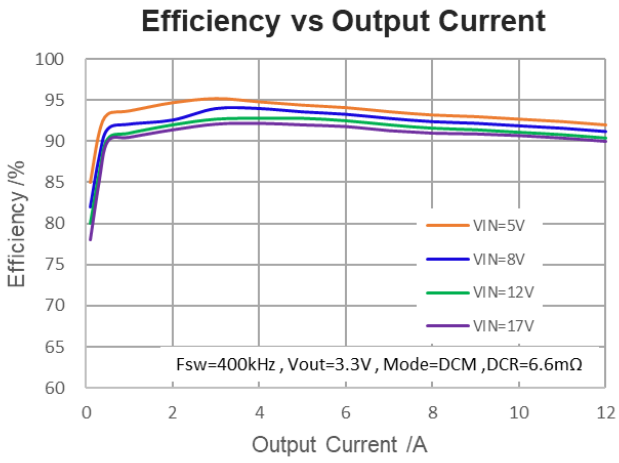
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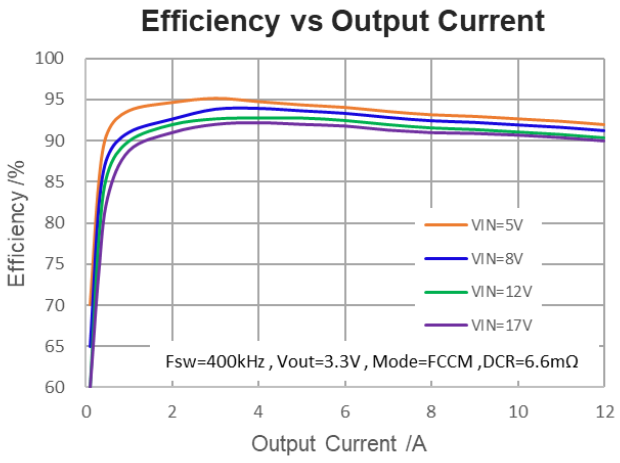
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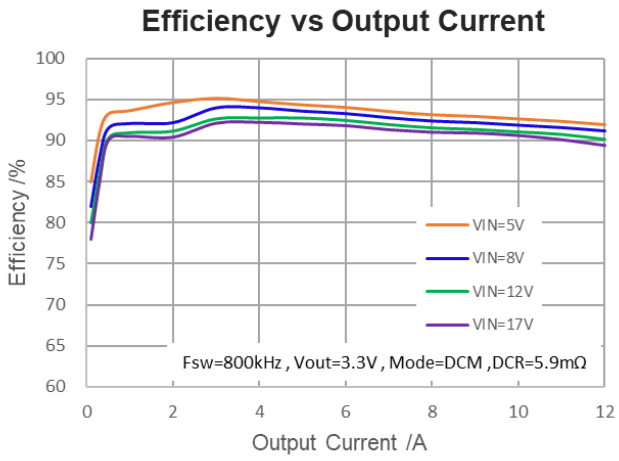
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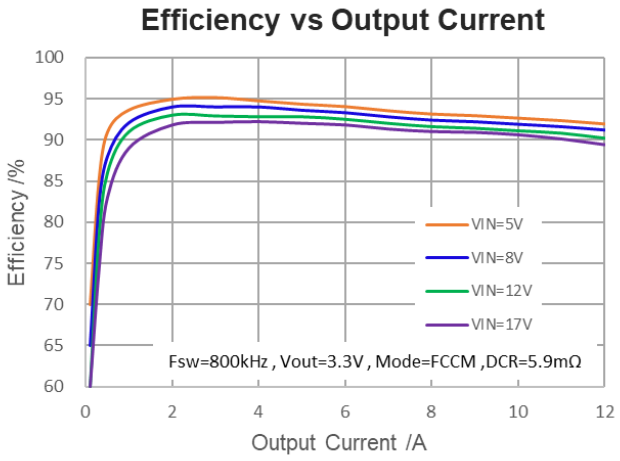
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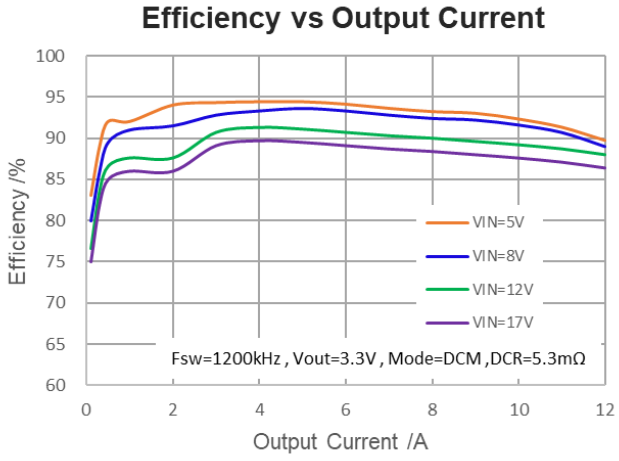
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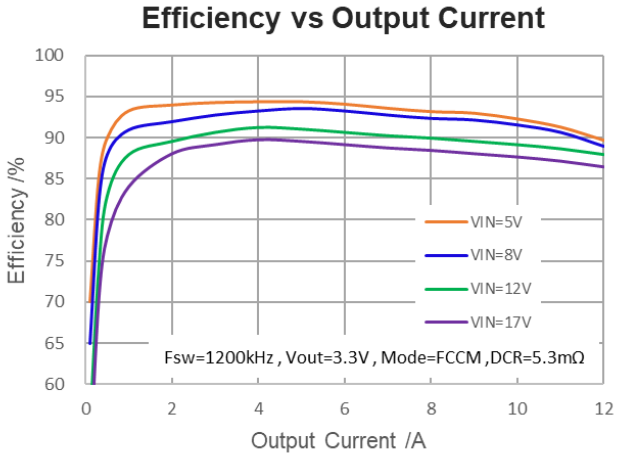
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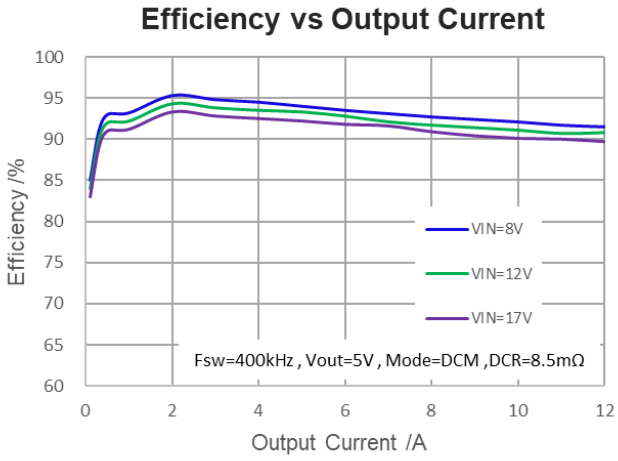
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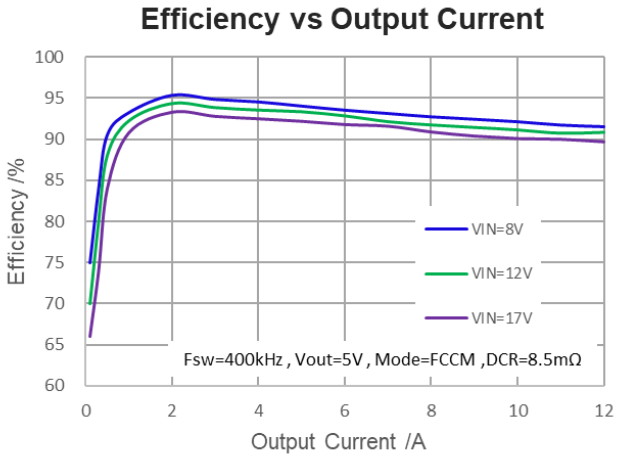
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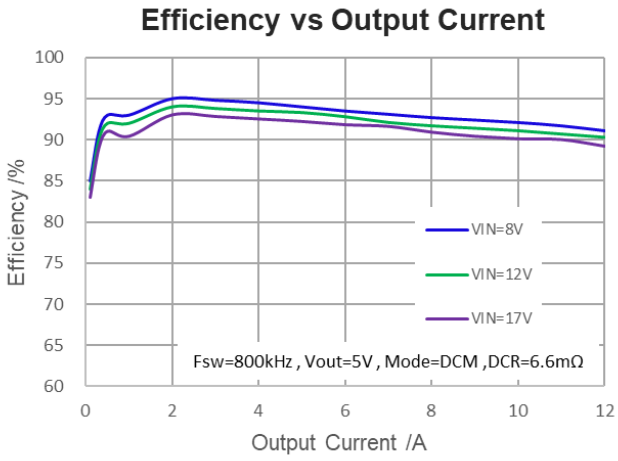
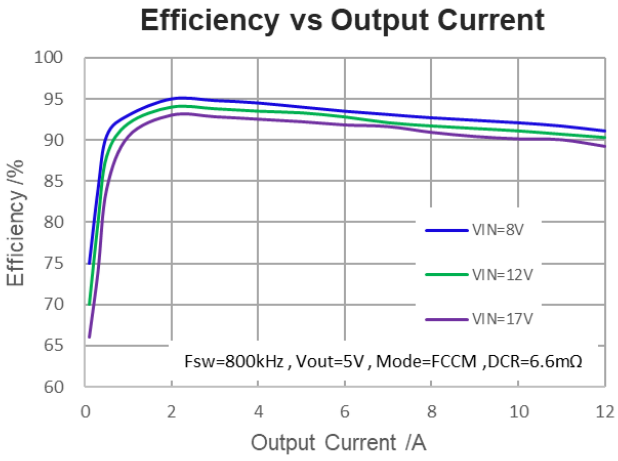
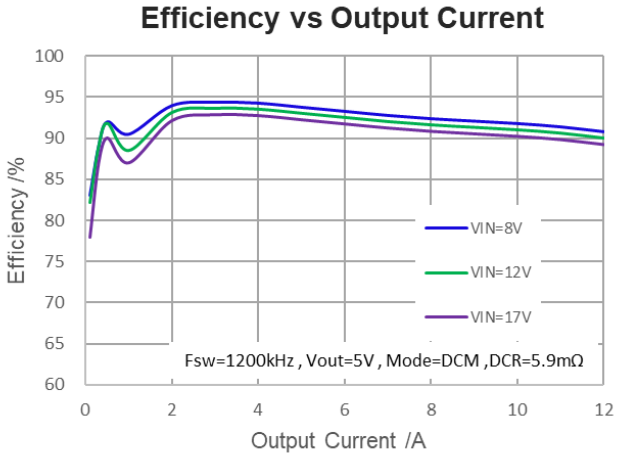
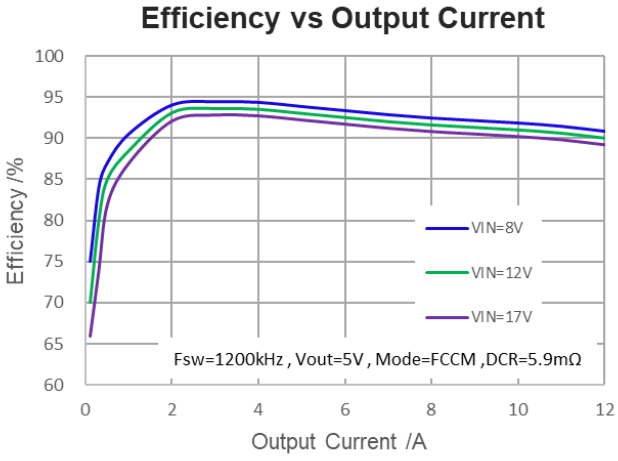
VIN=17V
Fsw=400kHz , Vout=5V , Mode=FCCM ,DCR=8.5mΩ

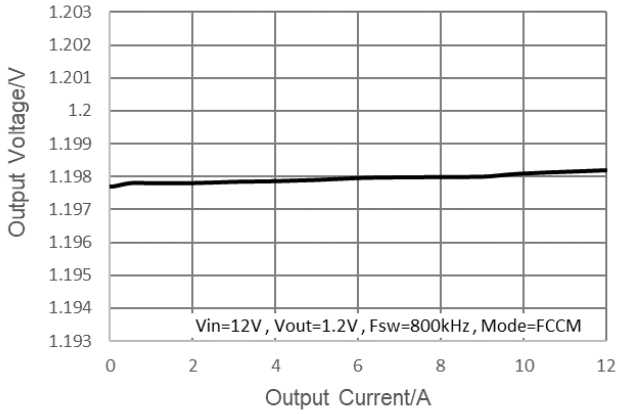

Efficiency vs Output Current
Efficiency /%
Output Current /A
VIN=8V
VIN=12V
VIN=17V
Fsw=800kHz , Vout=5V , Mode=DCM ,DCR=6.6mΩ


Efficiency vs Output Current
Efficiency /%
Output Current /A
VIN=8V
VIN=12V
VIN=17V
Fsw=800kHz , Vout=5V , Mode=FCCM ,DCR=6.6mΩ

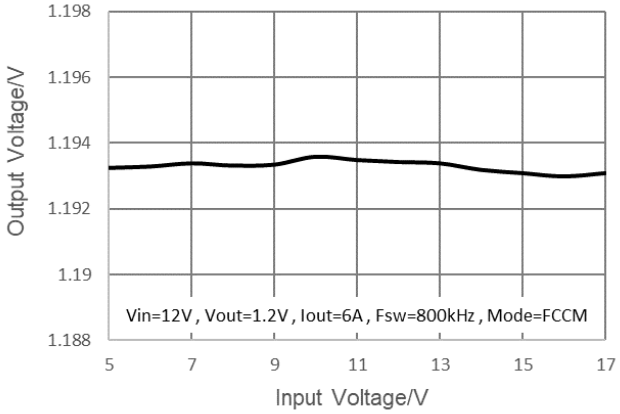

Efficiency vs Output Current
Efficiency /%
Output Current /A
VIN=8V
VIN=12V
VIN=17V
Fsw=1200kHz , Vout=5V , Mode=DCM ,DCR=5.9mΩ


Efficiency vs Output Current
Efficiency /%
Output Current /A
VIN=8V
VIN=12V
VIN=17V
Fsw=1200kHz , Vout=5V , Mode=FCCM ,DCR=5.9mΩ

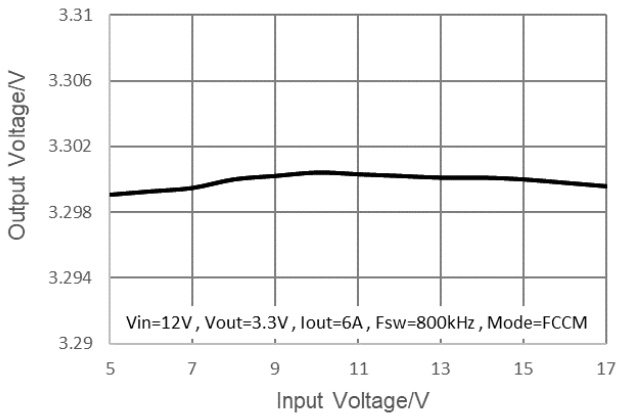
Output Voltage vs. Output Current



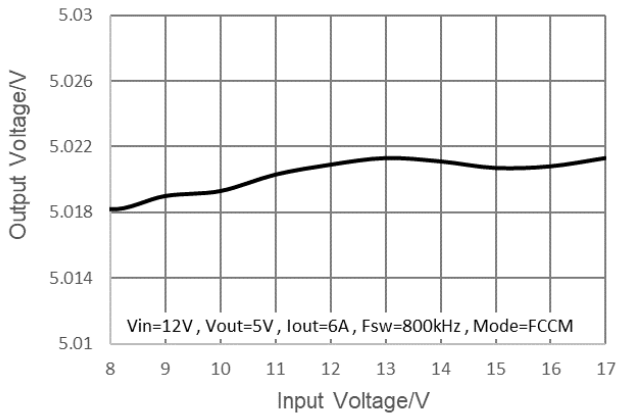
Output Voltage vs. Input Voltage



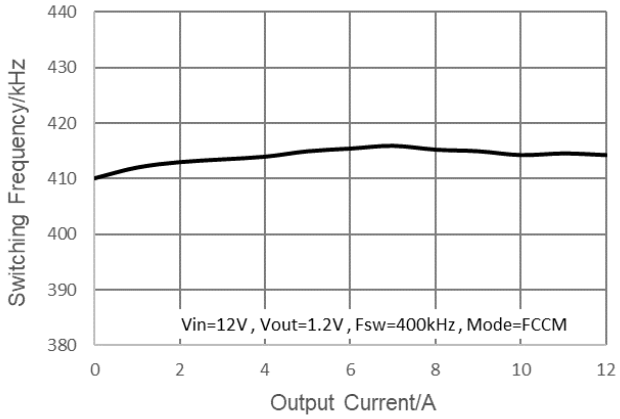
Output Voltage vs. Input Voltage



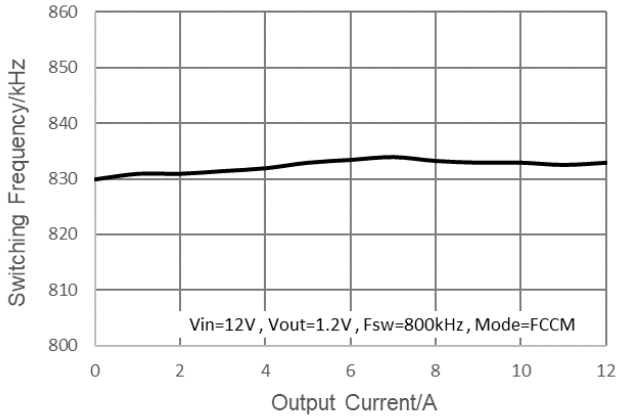
Output Voltage vs. Input Voltage



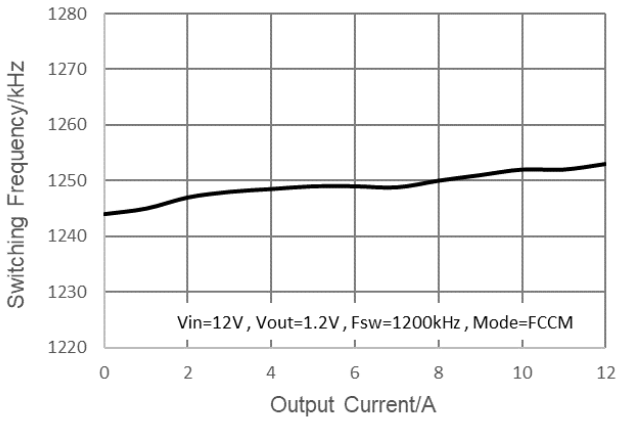
Switching Frequency vs. Output Current



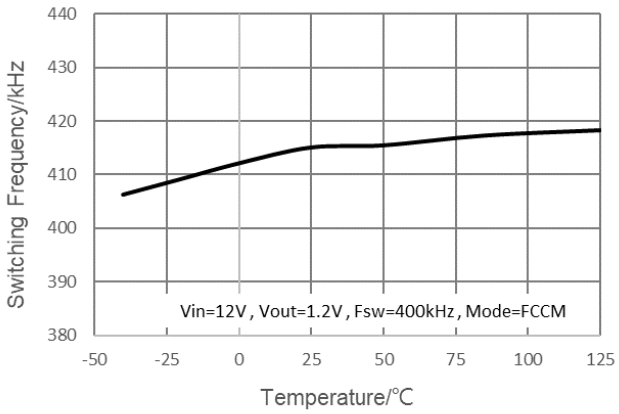
Switching Frequency vs. Output Current



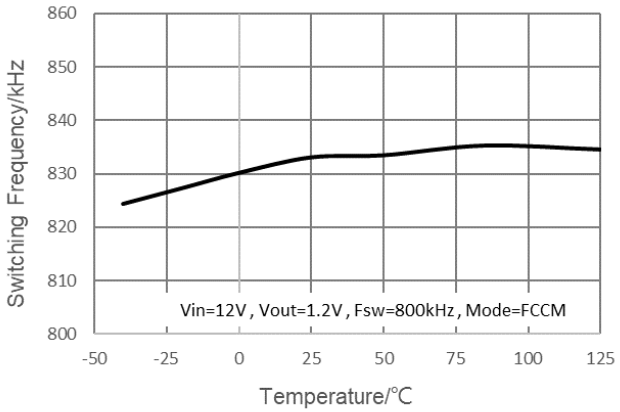
Switching Frequency vs. Output Current



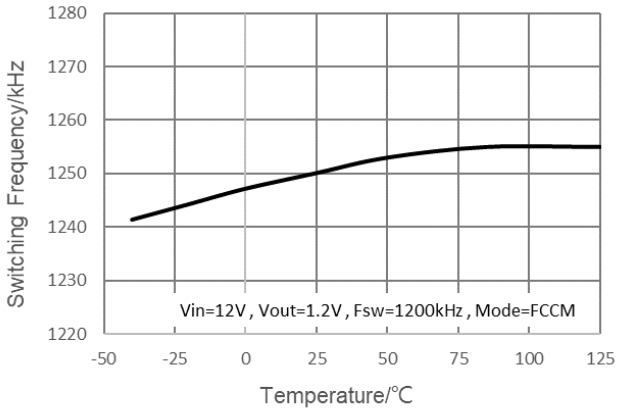
Switching Frequency vs. Temperature



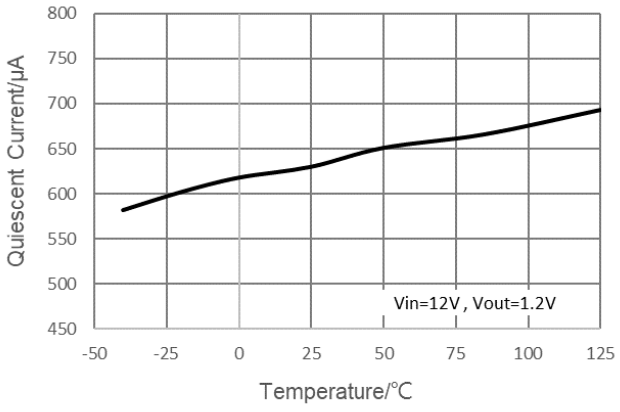
Switching Frequency vs. Temperature



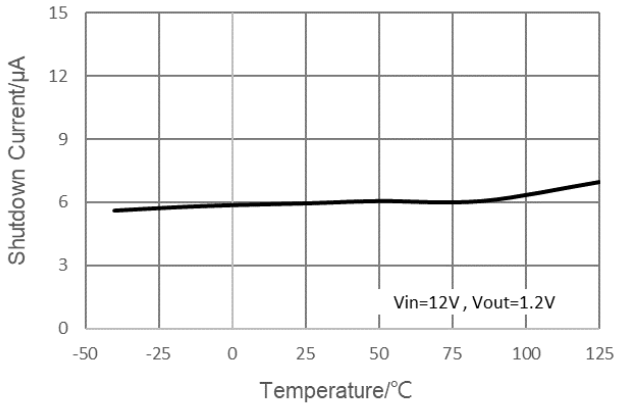
Switching Frequency vs. Temperature



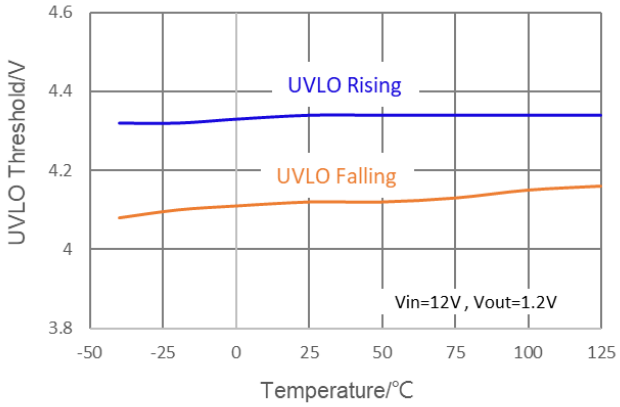
Quiescent Current vs. Temperature



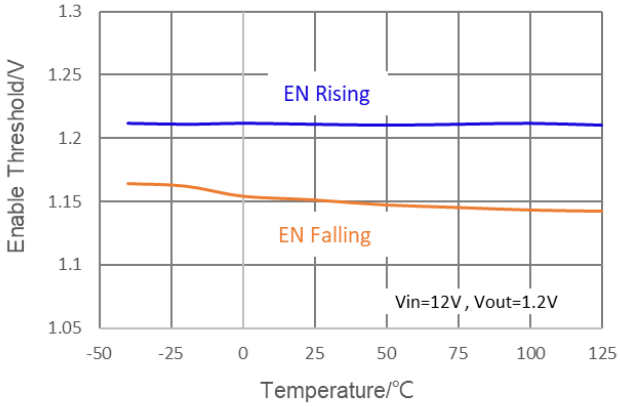
Shutdown Current vs. Temperature



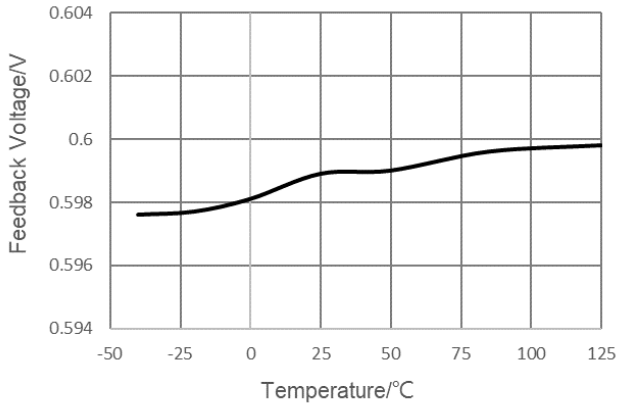
UVLO Threshold vs. Temperature



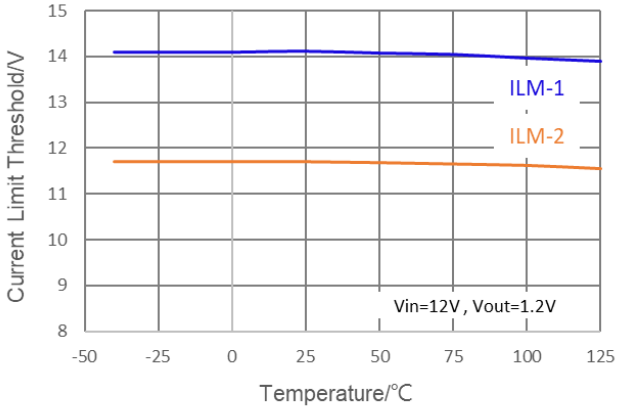
Enable Threshold vs. Temperature



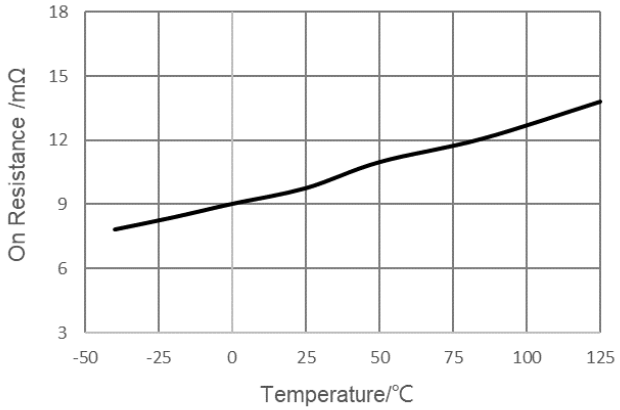
Feedback Voltage vs. Temperature



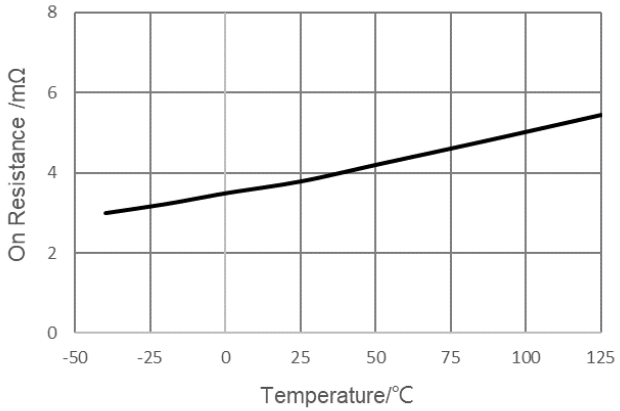
Current Limit Threshold vs. Temperature



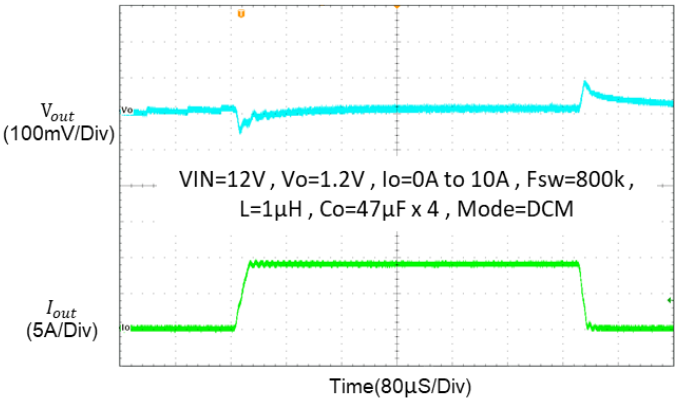
High-Side Rds(on) vs. Temperature



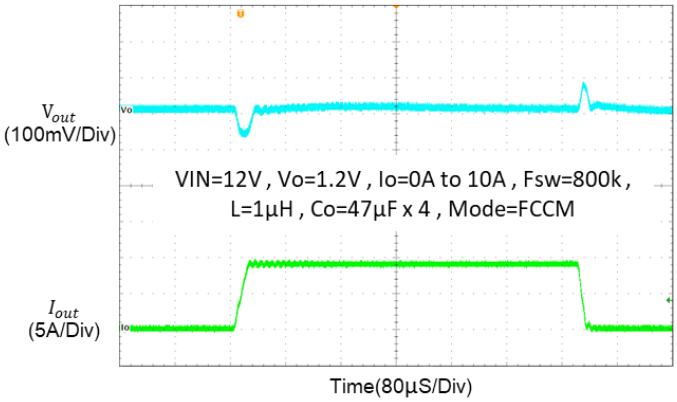
Low-Side Rds(on) vs. Temperature



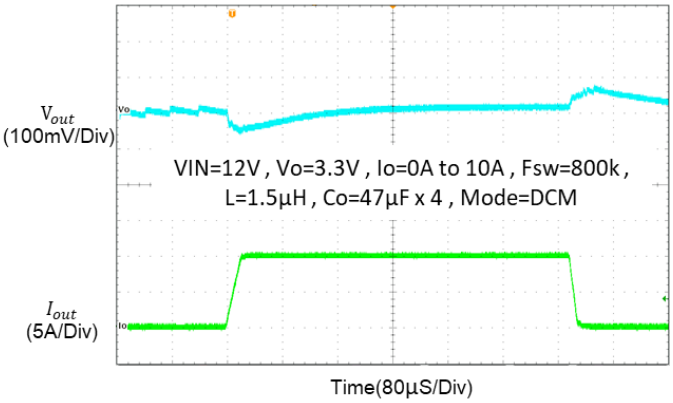
Load Transient Response



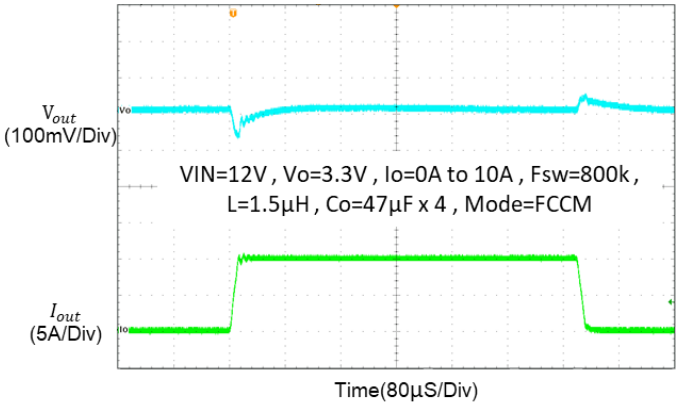
Load Transient Response



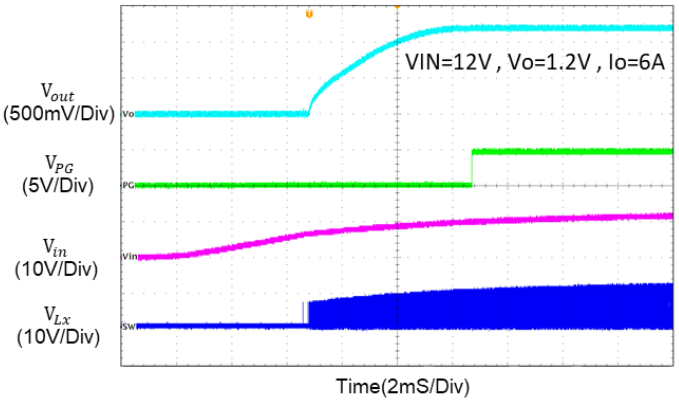
Load Transient Response



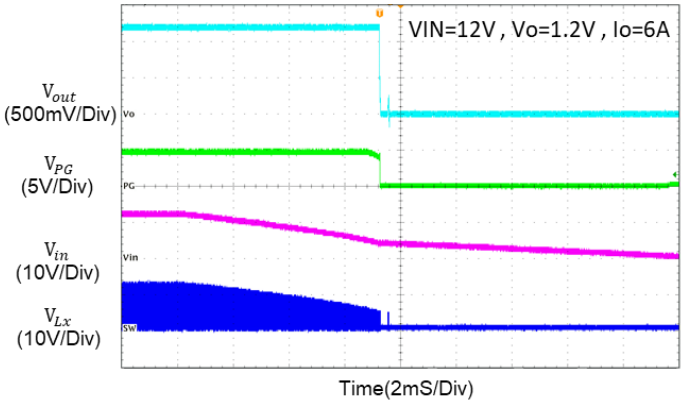
Load Transient Response



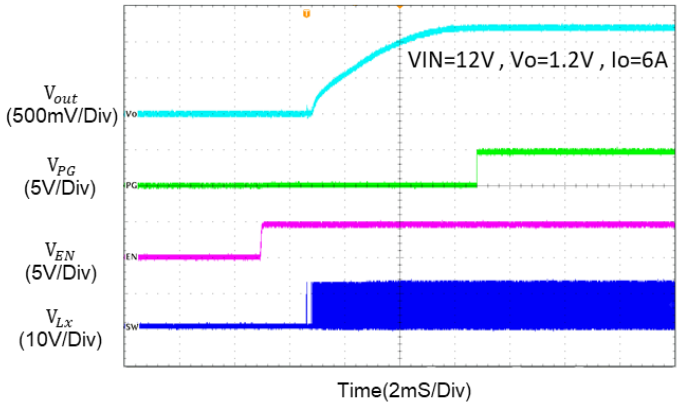
Power On from VIN



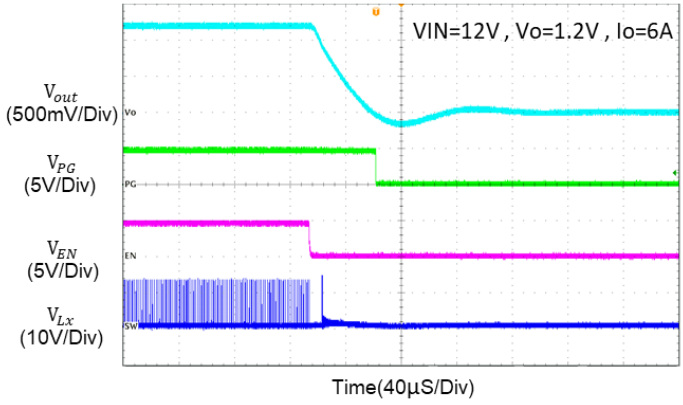
Power Off from VIN



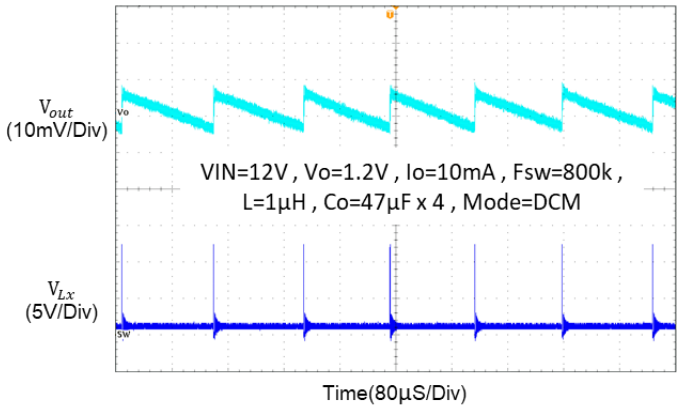
Power On from EN



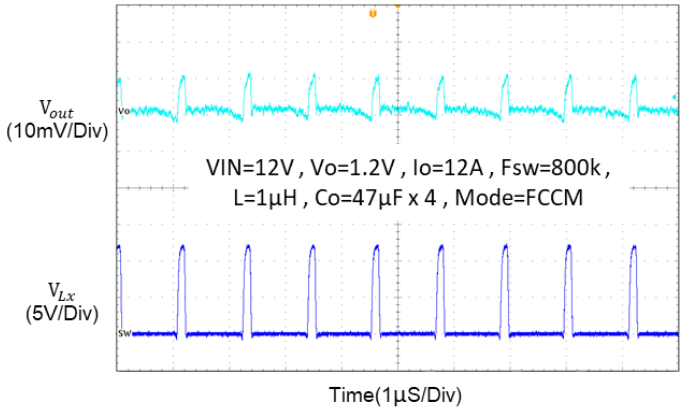
Power Off from EN



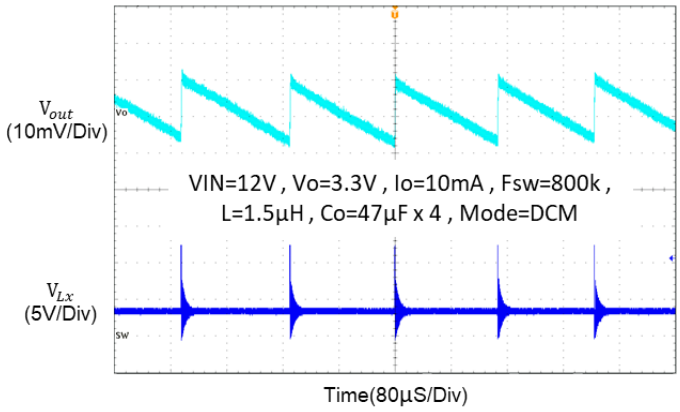
Output Ripple Voltage



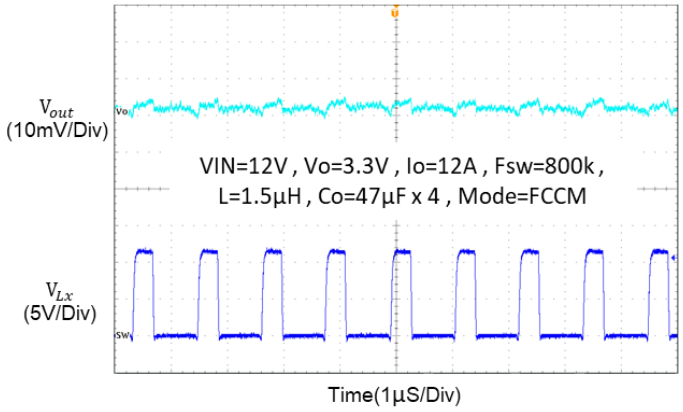
Output Ripple Voltage



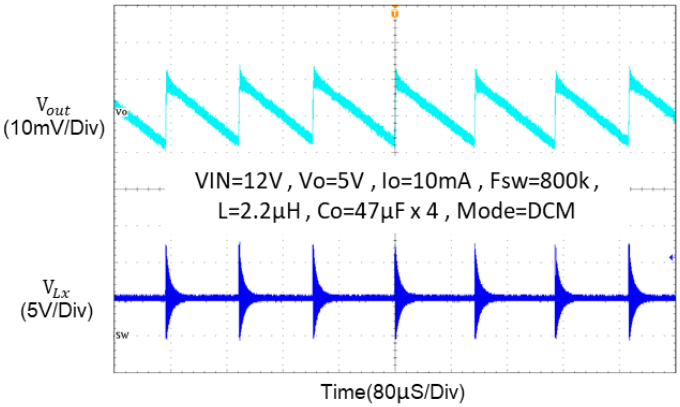
Output Ripple Voltage



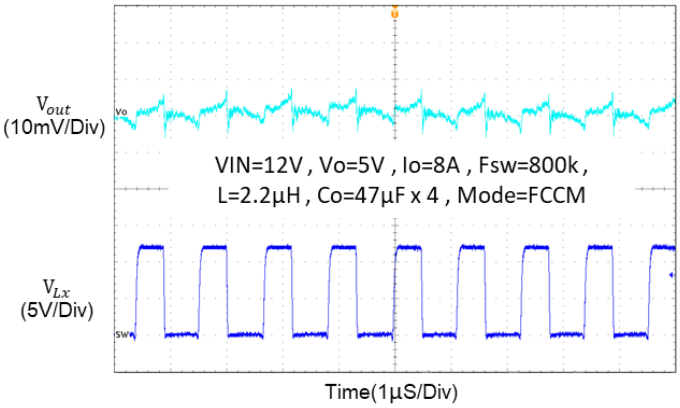
Output Ripple Voltage



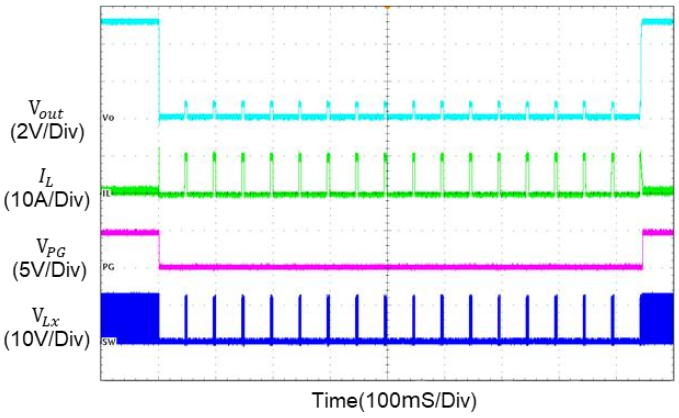
Output Ripple Voltage



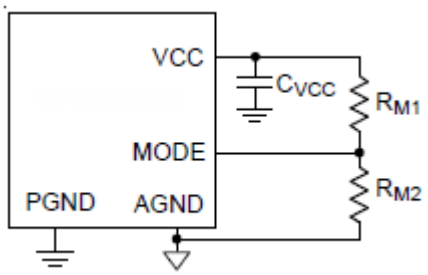
Output Ripple Voltage



Under Voltage Protection



MODE SETTING

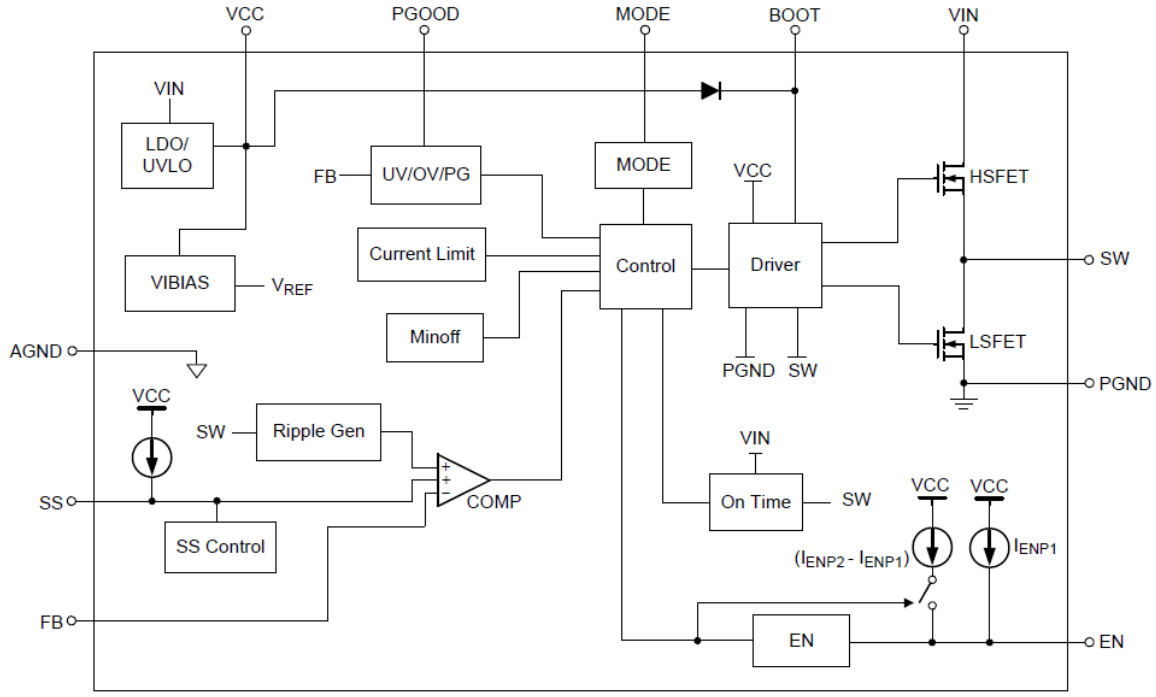


MODE Connection

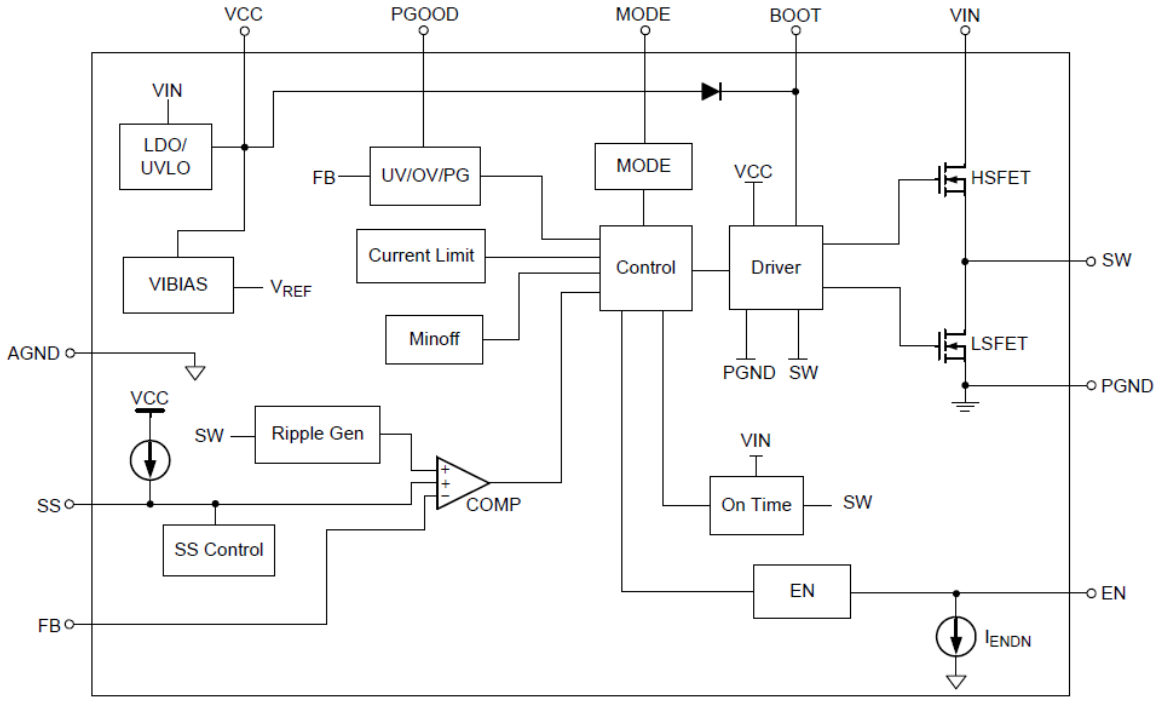
Table 6. MODE Setting

Mode	R_{M1} (kΩ)	R_{M2} (kΩ)	Light Load Mode	Current Limit	Switching Frequency (kHz)
1	300	5.1	FCCM	I_{LIM_2}	400
2	200	10	FCCM	I_{LIM_1}	400
3	160	20	FCCM	I_{LIM_2}	800
4	120	20	FCCM	I_{LIM_1}	800
5	200	51	FCCM	I_{LIM_2}	1200
6	180	51	FCCM	I_{LIM_1}	1200
7	150	51	DCM	I_{LIM_2}	400
8	120	51	DCM	I_{LIM_1}	400
9	91	51	DCM	I_{LIM_2}	800
10	82	51	DCM	I_{LIM_1}	800
11	62	51	DCM	I_{LIM_2}	1200
12	51	51	DCM	I_{LIM_1}	1200

FUNCTIONAL DESCRIPTION



XPC2443A Block diagram



XPC2443B Block diagram

Operation

The XPC2443 is a high efficiency synchronous stepdown converter utilizes the proprietary Constant On-Time control architecture. The ultrafast COT control enables the use of small capacitance to save the PCB size. During normal operation, the internal high-side power switch (HSFET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the HSFET turns off, the low-side power switch (LSFET) turns on. If the output capacitor ESR is large enough, the voltage ripple on the output has similar shape as the inductor current. Via the feedback resistor network, this voltage ripple compared with the internal reference. When the minimum off-time one-shot has timed out and the inductor current is below the current limit threshold, the One-shot is triggered again if the feedback voltage falls below the feedback reference voltage (0.6V, typ.). When it comes to low-ESR ceramic output capacitors, an internal ramp signal is added to the feedback reference voltage to simulate the output voltage ripple and make the loop stable. COT control architecture features ultrafast transient response. When a load is suddenly increased, the output voltage drops quickly, and almost immediately, a new On-time is triggered, and inductor current rises again. Traditional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. But even with defined input and output voltages, a fixed ON-time will mean that frequency will have to increase at higher load levels to compensate for the power losses in the MOSFETs and Inductor. XPC2443 further added a frequency locked loop system, which slowly adjusts the ON time to compensate the power losses, without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the XPC2443 are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator that generates 4.7V at VCC. The voltage on VCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains the C_{BOOT} voltage is sufficient to turn-on the HSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is above the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VCC rail that can pull a current higher than the internal LDO's current limit from the VCC, then the VCC drops below the UVLO falling threshold and thereby shutting down the output of the XPC2443.

Enable, Start-Up, Shutdown and UVLO

The XPC2443 implements Under-Voltage Lock Out protection (UVLO) to prevent operation without fully turning on the internal power MOSFETs. The UVLO monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device stops switching. UVLO is non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching and when the EN pin voltage falls below the turn-off threshold (V_{ENL}) it stops switching. The EN pin of the XPC2443A has internally pull-up with current source. However, the XPC2443B internally week pull-down the EN pin.

When appropriate voltages are present on the VIN, VCC, and EN pins, the XPC2443 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1.045ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 6μA current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower than the internal 1.045ms soft-start, the output voltage will be limited by the ramp rate on the SS pin instead.

Figure 1 below shows the typical power-up sequence of the device when the EN pin voltage crosses the EN input rising threshold. After the voltage on VCC pin crosses the UVLO rising threshold it takes 400μS to read the first MODE setting and approximately 55μS form there to finish the last MODE setting. The output voltage starts ramping after the MODE setting reading is completed.

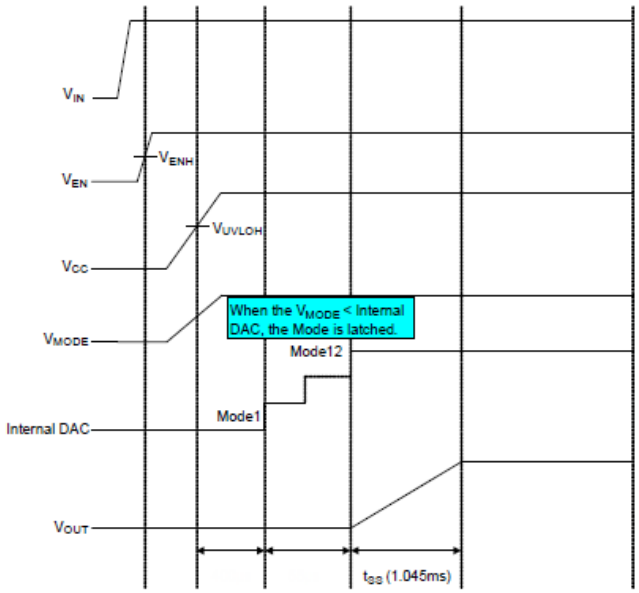


Figure 1. Power Up Sequence

Pre-Bias

If there is a residual voltage on output voltage before startup, both of internal HSFET and LSFET are prohibited switching until the soft start ramp is higher than feedback voltage. When the soft start ramps cross above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated target.

Mode Selection

MODE pin offers 12 different states of operation as a combination of Light Load operation, Switching Frequency and Current Limit. As shown in the Figure 3, use a resistor divider from VCC to AGND can set the MODE pin voltage.

It is important that the voltage for the MODE pin is derived from the VCC rail only since internally this voltage is referenced to detect the MODE option. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 1.

The MODE pin setting can be reset only by a VIN power cycling. The two resistors (R_{M1} and R_{M2}) are suggested to use 1% resistors.

Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero-current-detect circuitry which utilizing the LSFET $R_{DS(ON)}$ to sense the inductor current. The LSFET is turned off when the inductor current drops to zero, resulting in discontinuous operation (DCM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the feedback voltage falls below the feedback reference voltage. DCM operation maintains high efficiency at light load, while setting MODE to Forced PWM (FCCM) operation helps meet tight voltage regulation accuracy requirements.

Switching Frequency, Minimum On-Time and Minimum Off-Time

The XPC2443 offers three different switching frequency of 400kHz, 800kHz and 1200kHz by setting the MODE pin voltage. Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies not only improves efficiency by reducing internal gate charge and transition loss, but also requires larger inductance values and/or capacitance to maintain low output ripple voltage.

An additional constraint on operating frequency is the minimum controllable on-time and off-time. The Minimum on-time is the smallest duration of time in which the high-side power MOSFET (HSFET) can be in its “on” state.
In continuous mode operation, the minimum duty cycle can be estimated by ignoring component losses. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the XPC2443 are able to turn on the low-side power MOSFET (LSFET), tripping the current comparator and turning the power MOSFET back off.

Current Limit and Output Under-Voltage Protection

As shown in Table 1, the XPC2443 can operate at two different current limits I_{LIM_1} and I_{LIM_2} to support an output continuous current of 12A and 10A respectively. The device cycle-by-cycle compares the valley current of the inductor against the current limit threshold, hence the output current will be half the ripple current higher than the valley current.

The inductor current level is monitored by measuring the low-side MOSFET voltage between the SW pin and GND, which is proportional to the switch current, during the on-time of LSFET. If the measured drain to source voltage of the LSFET is above the voltage proportional to current limit, the LSFET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support.

When the output voltage falls below Output UVP Threshold (V_{UVP}), the UVP comparator detects it and shuts down the device to avoid the excessive heat. If the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated. When the overcurrent condition is removed, the output voltage shall return to the regulated value.

Power-Good Output

The PGOOD pin is an open-drain power-good indication which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold V_{TH_PGLH} (typically 93% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a V_{FB} falling hysteresis (typically 9% of the target value) or exceeds V_{FB} rising threshold V_{TH_PGHL} (typically 116% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{FB} falling hysteresis, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (typically 9% of the target value).

Once being started-up, if any protection is triggered (UVP and OTP) or EN is from high to low, PGOOD will be pulled to GND. The internal open-drain pull down device with 250Ω resistance will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients of dynamic VOUT changes the XPC2443's PGOOD falling edge includes a blanking delay of approximate 1us.

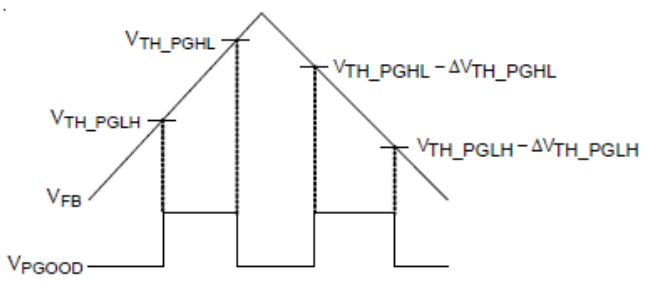


Figure 2. The Logic of PGOOD

Output Over-Voltage Protection (OVP)

The XPC2443 provides an over-voltage protection (OVP), If the FB voltage (V_{FB}) rises above 121% of the internal reference voltage, the over-voltage protection is triggered, the discharging switch from SW to GND is turned on to discharge output voltage.

Over-Temperature Protection (OTP)

The XPC2443 monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SD}, typically 160°C), the XPC2443 stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. During start up, if the device temperature is higher than 160°C the device does not start switching. The device re-starts switching when the temperature drops more than 15°C (typ.) but the MODE settings are not re-loaded again. If the temperature continues to rise and above LDO thermal shutdown threshold (T_{SD_LDO}, typically 171°C), the converter shuts down completely. Note that the over temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impact device reliability or permanently damage the device.

Output Voltage Discharge

An internal 500Ω discharge switch that discharges the V_{OUT} through SW node during any fault events like OVP, UVP, OTP , VCC voltage below UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

Layout Guidelines

- A four-layer or six-layer PCB with maximum ground plane is recommended for good thermal performance.
- The traces of the main current paths should be kept wide and short.
- Recommend having equal input caps on each side of the IC. Place them as close to VIN pins as possible.
- Place the VCC decoupling capacitor in close proximity to VCC pin.
- Place the bootstrap cap, CBOOT, as close to IC as possible.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the XPC2443 to additional ground planes within the circuit board and on the bottom side.
- Keep analog components away from the SW and BOOT nodes to prevent noise pickup.
- Connect the feedback sense network behind via of output capacitor.
- Figure 3 shows the recommended top side layout.

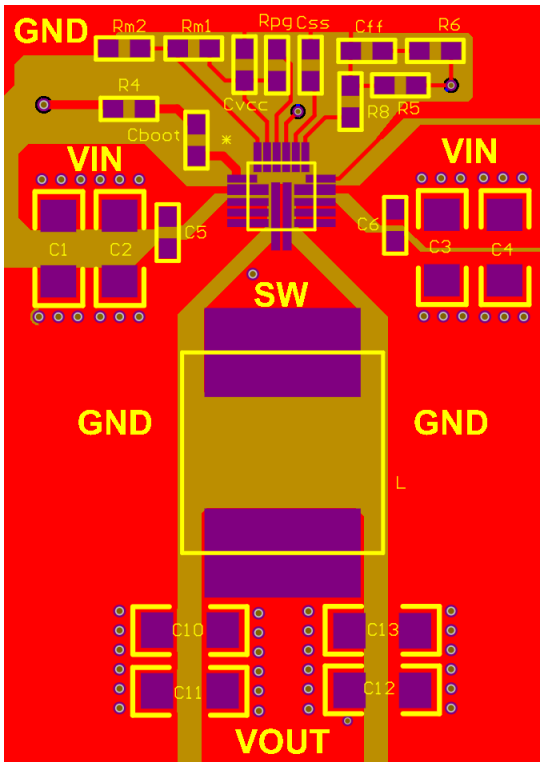
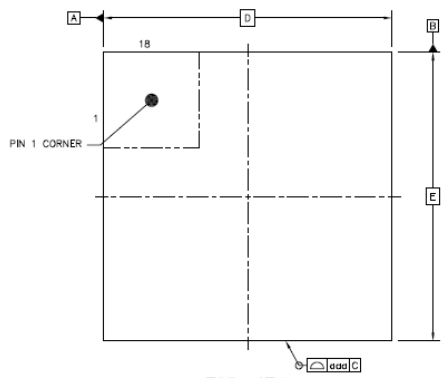


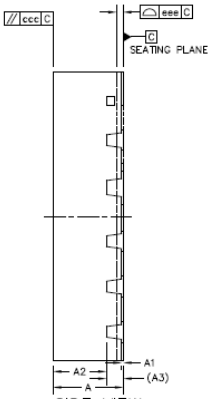
Figure 3. Layout Example (Top Layer)

PHYSICAL DIMENSIONS

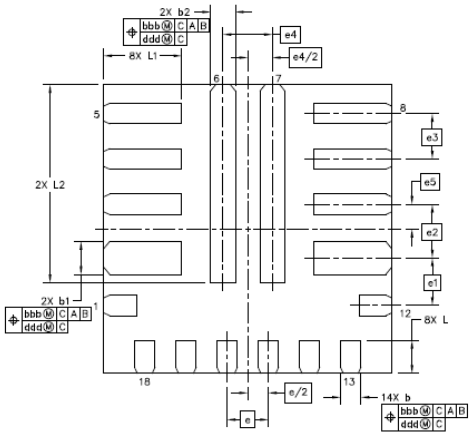
Table:Chip Dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW

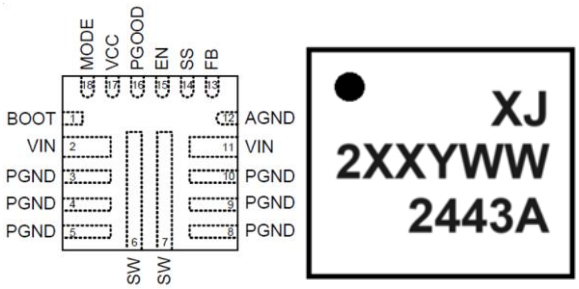
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.9	1.0
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.35	0.4	0.45
		b2	0.25	0.3	0.35
BODY SIZE	X	D		3.5 BSC	
	Y	E		3.5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.575 BSC	
		e2		0.65 BSC	
		e3		0.55 BSC	
		e4		0.6 BSC	
LEAD CENTRE TO PACKAGE CENTRE		e5		0.3 BSC	
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.85	0.95	1.05
		L2	2.3	2.4	2.5
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP·Sn8~20s

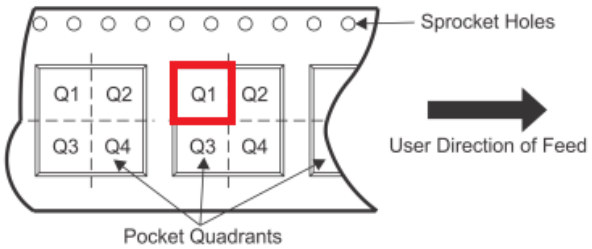
MARKING AND REEL INFORMATION

Format：

Top View



Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Letter height of 0.5mm

Side pitch of 0.4mm

Line space of 0.25mm

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1
   a) 1st digit: Assembly location code: JCET: 2
   b) 2nd & 3rd digit: Assembly lot number
   c) 4th digit: Year code.

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

   d) 5th & 6th digit: Week code, 01 means the 1st Work Week based on XinJi's calendar.

   WK01 means the 1st Work Week based on XinJi's calendar.

2. Product Number Code: Line 2

Product Name	P/N Code	Remark
XPC2443AQ35R	2443A	