XPC2452

2.9V to 17V Input, 20A Synchronous Buck Converter

FEATURES

- 2.9V to 17V Input Range with External 3.3V Bias
- 3.6V to 17V Input Range without External Bias
- Output Voltage Range: 0.6 V to 5.5 V
- 0.6V ± 1% Voltage Reference from −40°C to +125°C Junction Temperature Range
- COT Control for Ultra-fast Load-step Response
- Supports All Ceramic Output Capacitors
- Selectable FCCM or PSM Operation at Light Load
- Selectable Operation Switching Frequency (600KHz/800KHz/1MHz)
- Non-Latch for OCP, UVP, UVLO, and OTP Faults, Latch Off for OVP
- Differential Remote Sense for High Output Accuracy
- Open-drain Power-good Output
- Enable Control
- Programmable Soft-Start Time
- Programmable Current Limit with R_{TRIP}
- Monotonic Start-Up into Pre-Biased Outputs
- Output Voltage Tracking
- 4mm × 3mm, 19-pin FCQFN Package

APPLICATIONS

- Rack Server and Blade Server
- Hardware Accelerator and Add-in Cards
- Data Center Switches
- Industrial PC

DESCRIPTION

The XPC2452 is a high-performance, synchronous step-down converter that can deliver up to 20A output current with an input supply voltage range of 3.6V to 17V. The device integrates low $R_{DS(ON)}$ power MOSFETs, accurate 0.6V reference and an integrated diode for bootstrap circuit to offer a very compact solution.

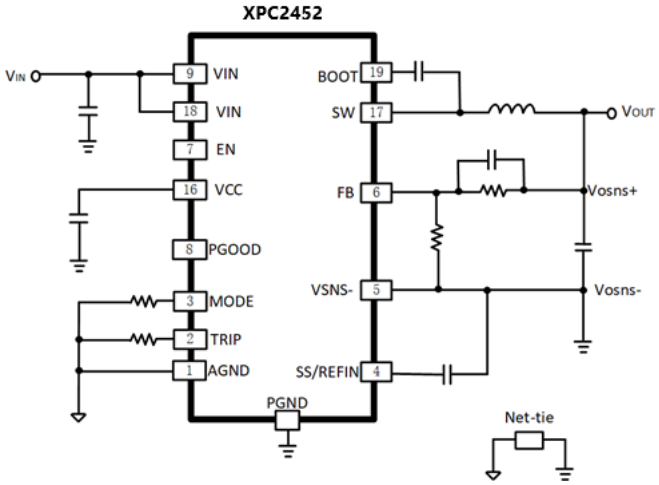
The XPC2452 adopts Constant On-Time control architecture that provides ultrafast transient response and further reduces the external-component count. In steady states, this part operates in nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

The device offers a variety of functions for more design flexibility. The selectable switching frequency, current limit level and PWM operation modes make the XPC2452 easy-to-use over wide application range. Independent enable control input pin and power-good indicator are also provided for easy sequence control. Dedicated enable control input pin and power good indicator are also provided for easy sequence control. To control the inrush current during the startup, the device provides a programmable soft-start by an external capacitor connected to the SS/REFIN pin.

Complete protection features are also integrated in the device including UVLO, OVP, UVP, overcurrent protection and thermal shutdown.

The XPC2452 is available in a thermally enhanced QFN-19L 3x4 (FC) package.

SIMPLIFIED APPLICATION CIRCUIT

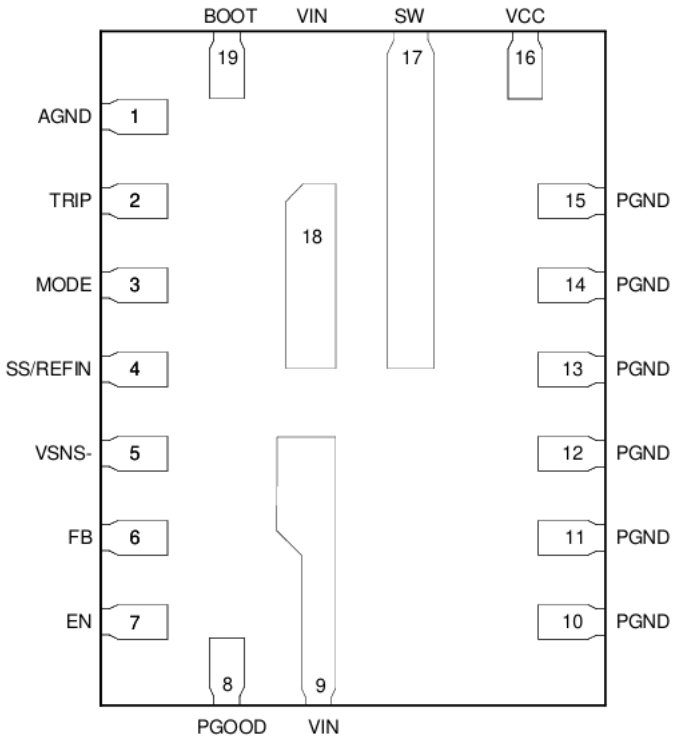


ORDERING INFORMATION

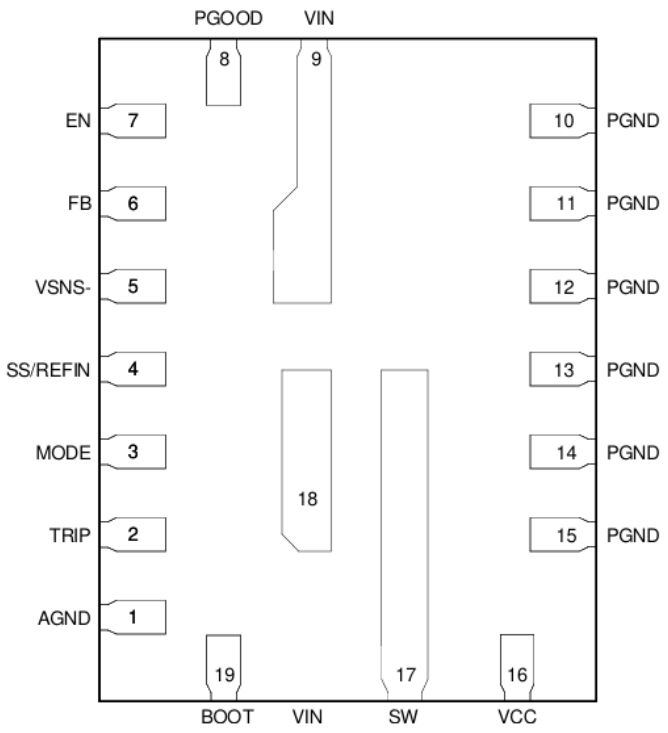
Part Number	Output Current (A)	Top Marking	MPQ
XPC2452Q19R	20	2452	3,000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN CONFIGURATION AND DESCRIPTION



Top View



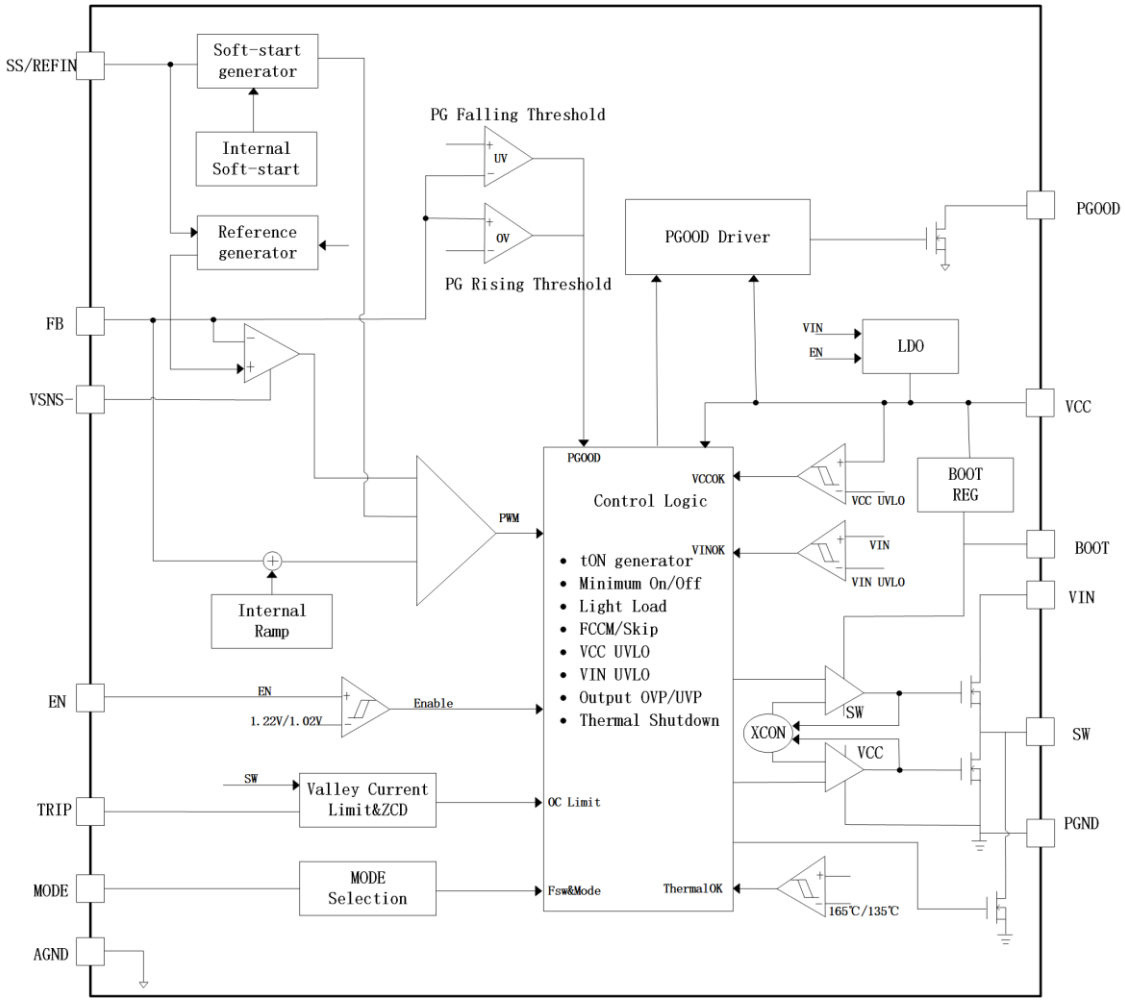
Bottom View

Pin Configuration

Pin	Name	Description
1	AGND	Analog ground. Reference point for the internal control circuit. Connect AGND and PGND with a short trace and at only one point to reduce circulating currents.
2	TRIP	Current limit setting pin. Connect a resistor from this pin to AGND to set the valley current limit value. At least ±1% resistor is required.
3	MODE	The MODE pin sets the Forced Continuous Conduction mode (FCCM) or Skip mode operation. It also selects the operating frequency by connecting a resistor from the MODE pin to AGND. At least ±1% resistor is required.
4	SS/REFIN	Dual-function pin. Soft-start function: Connect a capacitor to the VSNS– pin programs the soft-start time. Minimum soft-start time (1ms) is fixed internally. A minimum 22nF capacitor is required for this pin to avoid overshoot during the charge of the soft-start capacitor. REFIN function: The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. The internal reference voltage can be overridden by an external DC voltage source on this pin for tracking application.
5	VSNS–	Differential remote voltage sense. Connect this pin to the negative side of the remote voltage sense point. Short to GND as internal reference if the remote voltage sense is not used.
6	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. Suggest placing the FB resistor divider as close to FB pin as possible.
7	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Do not leave this pin floating.
8	PGOOD	Open-drain, power-good indication output. It is pulled low if the feedback voltage is out of the PGOOD threshold, IC shuts down from fault state and EN goes low, and before the soft-start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.

9, 18	VIN	Power input voltage. Support 3.6V to 17V input voltage. It is suggested to place decoupling input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
10,11,12,13,14,15	PGND	The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections.
16	VCC	3V internal LDO output. An external 3.3V±5% DC voltage source can be connected to this pin to reduce power losses on the internal LDO and supply both the internal circuitry and gate driver. Connect a 1μF, X7R ceramic capacitor as close to the VCC pin as possible. It is not allowed to connect VCC to supply other rails.
17	SW	Switching node. Output switching state between high-side MOSFET switching and low-side MOSFET switching of the power converter. Connect SW pin to the external inductor and bootstrap capacitor.
19	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (1)

Parameter	Min	Max	Units
Supply Input Voltage, VIN	-0.3	18	V
Enable Pin Voltage, EN	-0.3	6.5	V
SW	-0.3	18	V
SW (<25ns)	-5	25	V
VIN-SW	-0.3	18	V
VIN-SW (<25ns)	-4	25	V
BOOT	-0.3	24	V
BOOT−SW	-0.3	6	V
VCC	−0.3	4	V
All Other Pins	-0.3	4	V
Junction Temperature	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range	-65	150	°C
ESD HBM(2) (Human Body Model)	2		kV
ESD CDM(2) (Charged Device Model)	1		kV

RECOMMENDED OPERATING CONDITIONS (3)

Parameter	Symbol	Min	Max	Units
VIN without external 3.3V bias	V_{IN}	3.6	17	V
VIN with external 3.3V bias		2.9	17	V
Output Voltage	V_{OUT}	0.6	5.5	V
External VCC bias	V_{CC_EXT}	3.12	3.6	V
Enable voltage	V_{EN}	3.6		V
Junction Temperature Range	T_{OJ}	-40	+125	°C

THERMAL INFORMATION(4)

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is obtained in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	46.6	°C/W
Junction-to- Case (Top) Thermal Resistance	$\theta_{JC(top)}$	22.8	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$\theta_{JC(Bottom)}$	1.05	°C/W

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) Devices are ESD sensitive. Handling precaution is recommended.

(3) The device is not guaranteed to function outside its operating conditions.

(4) θJA is measured in the natural convection at TA = 25°C on a Four-layer Evaluation Board. θJC(top) is measured at the top of the package. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions

ELECTRICAL SPECIFICATIONS

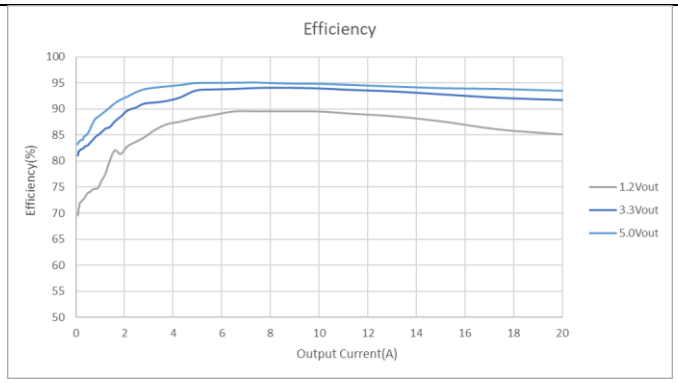
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply						
VIN Shutdown Current	Isd	T_J = 25°C, V_{EN} = 0V		5	15	uA
VIN Quiescent Current	I_Q	T_J = 25°C, V_{EN} = 2V, non-switching		1050	1300	uA
Enable						
EN Threshold Voltage	V_{ENH}	EN Rising	1.17	1.22	1.27	V
	V_{ENL}	EN Falling	0.97	1.02	1.07	V
EN Hysteresis	ΔV_{EN}			200		mV
EN Pull-Down Current	I_{ENDN}	T_J = 25°C, V_{EN} = 2V		0.5	5	uA
VFB Voltage						
FB Voltage	VFB	T_J = -40°C to +125°C	0.594	0.6	0.606	V
Start-up						
Internal fixed soft-start time	t_{SS}	VOUT rising from 0 V to 100% of final setpoint, $C_{SS/REFIN}$ = 1nF		1	1.5	ms
SS/REFIN Charge Current	$I_{SS/REFIN\_CHG}$	$V_{SS/REFIN}$ = 0V		45		uA
SS/REFIN Discharge Current	$I_{SS/REFIN\_DISCHG}$	$V_{SS/REFIN}$ = 1V		12		uA
Switching Frequency						
Switching Frequency	fSW	R_{MODE} = 0Ω , IOUT = 0A, FCCM, VOUT = 1V	480	600	720	kHz
		R_{MODE} = 30.1kΩ, IOUT = 0A, FCCM, VOUT = 1V	680	800	920	kHz
		R_{MODE} = 60.4kΩ, IOUT = 0A, FCCM, VOUT = 1V	850	1000	1150	kHz
Internal MOSFET						
High Side ON Resistance	$R_{DS(ON)\_H}$	T_J = 25°C, VCC = 3V		9		mOhm
Low Side ON Resistance	$R_{DS(ON)\_L}$	T_J = 25°C, VCC = 3V		2.5		mOhm
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	T_J = 25°C			50	ns
Minimum Off-Time	t_{OFF_MIN}	T_J = 25°C			210	ns
Current Limit						
Current Limit Voltage Threshold	V_{LIM}	T_J = 25°C, valley current	1.15	1.2	1.25	V
I_{CS} to I_{OUT} Ratio	G_{CS}	IOUT ≥ 2A	9	10	11	uA/A
Low-Side MOSFET Current Limit Threshold	I_{LIM_L}	T_J = 25°C, valley current, R_{TRIP} = 5kΩ		24		A

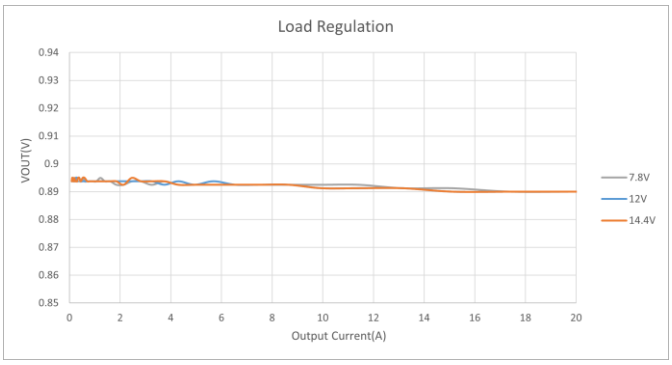
VIN = 12V, T_J = –40°C to 125°C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Low-Side MOSFET Negative Current Limit Threshold	I_{LIM_NEG}	T_J = 25°C, valley current		-10		A
UVLO						
Input UVLO Rising Threshold	V_{UVLOH}	VIN rising, VCC_EXT = 3.3V	2.6	2.7	2.9	V
Input UVLO Hysteresis	ΔV_{UVLO}			500		mV
LDO Output						
LDO Output Voltage	VCC	Load=1mA		3.0		V
VCC Rising Threshold	V_{CC_UVLOH}	VCC rising		2.8		V
VCC Hysteresis	ΔV_{CC_UVLO}	VCC hysteresis		300		mV
VCC Load Regulation		Load=25mA		0.5		%
LDO Output Current Limit	I_{LIM_LDO}			100		mA
Overvoltage and Undervoltage Protections						
Output UVP Threshold	V_{UVP}	UVP detection	77	80	83	%VFB
Output OVP Threshold	V_{OVP}	OVP detection	113	116	119	%VFB
Power Good						
PGOOD Threshold	V_{TH_PGLH1}	VFB rising threshold, PGOOD from low to high (GOOD)	89.5	92.5	95.5	%VFB
	V_{TH_PGHL1}	VFB rising threshold, PGOOD from high to low (FAULT)	113	116	119	%VFB
	V_{TH_PGLH2}	VFB falling threshold, PGOOD from low to high (GOOD)	104	108	112	%VFB
	V_{TH_PGHL2}	VFB falling threshold, PGOOD from high to low (FAULT)	77	80	83	%VFB
PGOOD Output Low Voltage	$V_{PG\_L\_100}$	VIN= 0V, VCC= 0V, VEN= 0V, PGOOD pulled up to 3.3 V through a 100kΩ resistor		650	850	mV
	$V_{PG\_L\_10}$	VIN= 0V, VCC= 0V, VEN= 0V, PGOOD pulled up to 3.3 V through a 10kΩ resistor		800	1000	mV
PGOOD Delay		VTH_PGLH1, PGOOD from low to high (GOOD)		0.8		ms
Over Temperature Protection						
Thermal Shutdown Threshold	T_{SD}			160		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			30		°C
Output Discharge						
Output discharge resistance	R_{DISCHG}	VEN = 0V or Protection		100		Ω

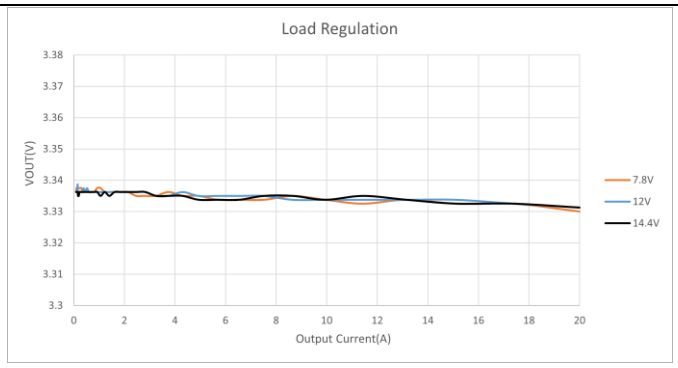
TYPICAL PERFORMANCE AND OPERATING CHARACTERISTICS



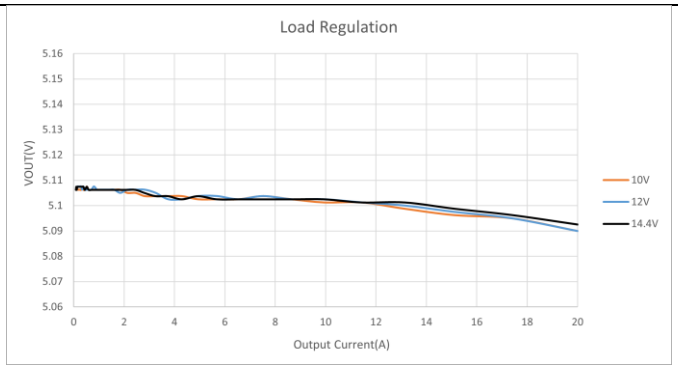
Vin=12V, Fsw=800kHz, DCM Mode, without external bias



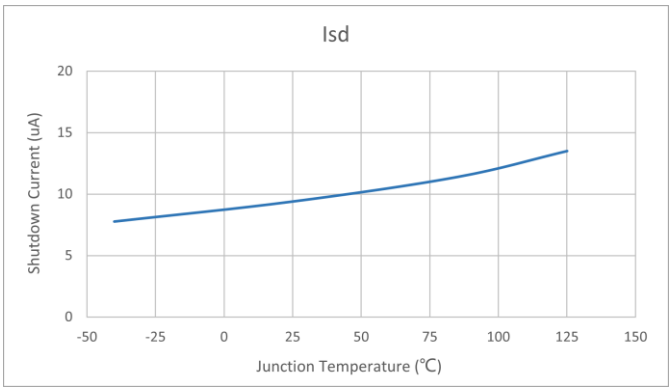
Output voltage vs. output current



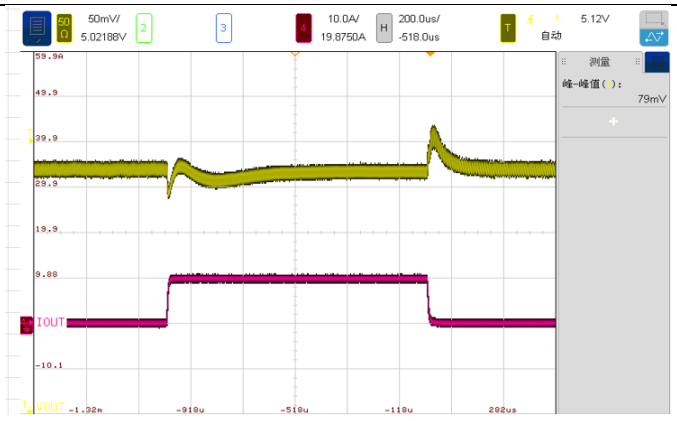
Output voltage vs. output current



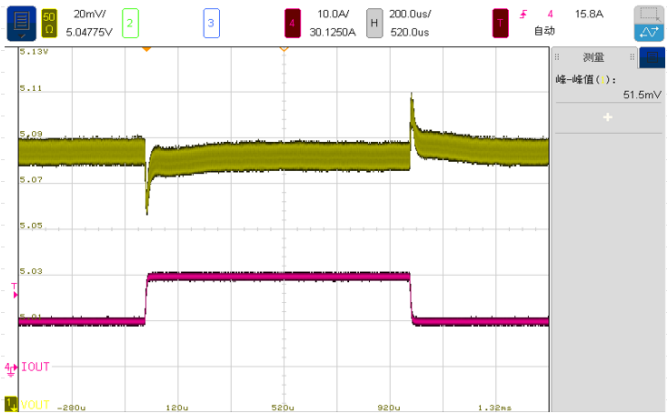
Output voltage vs. output current



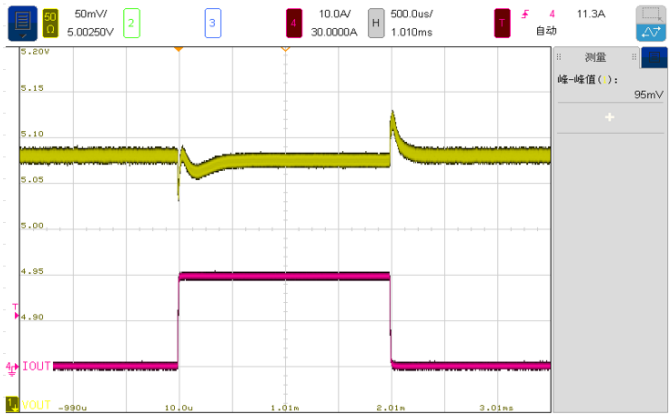
Shutdown current vs. junction temperature



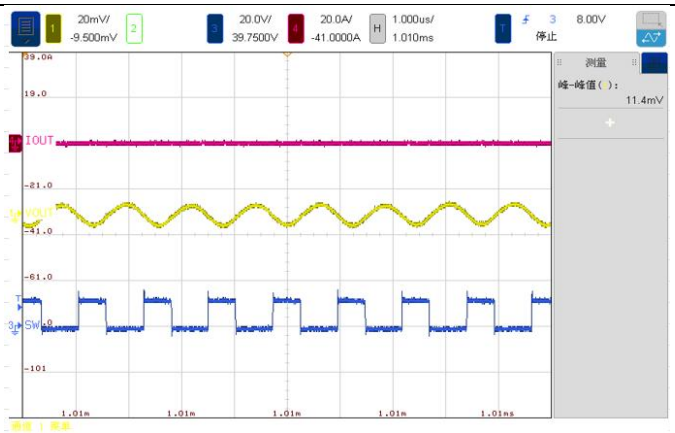
Vin=12V, V_O=5V, I_O=0A to 10A, Fsw=800kHz, L=560nH, CO=22uF×8, DCM Mode



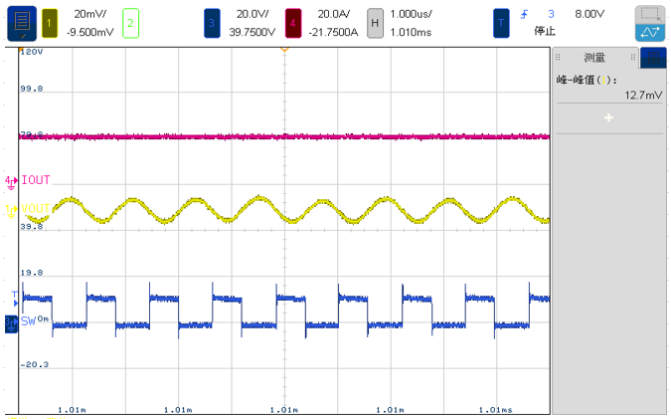
Vin=12V, V_O=5V, I_O=10A to 20A, Fsw=800kHz, L=560nH, CO=22uF×8, DCM Mode



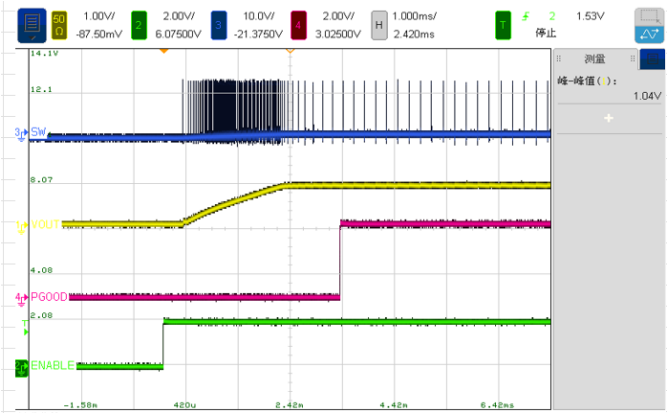
Vin=12V, V_O=5V, I_O=0A to 20A, Fsw=800kHz, L=560nH, CO=22uF×8, DCM Mode



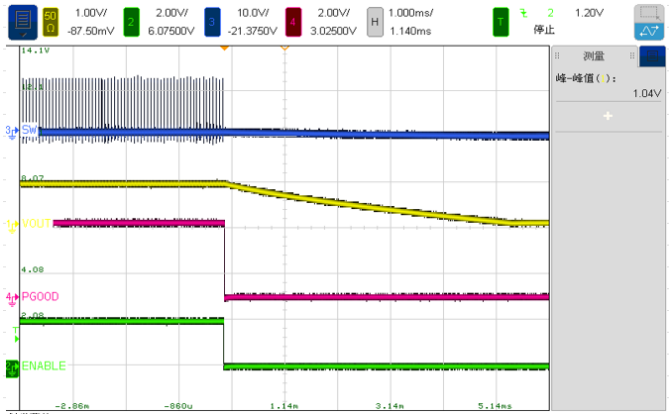
Vin=12V, V_O=5V, I_O=0A, Fsw=800kHz, L=560nH, CO=22uF×8, FCCM Mode



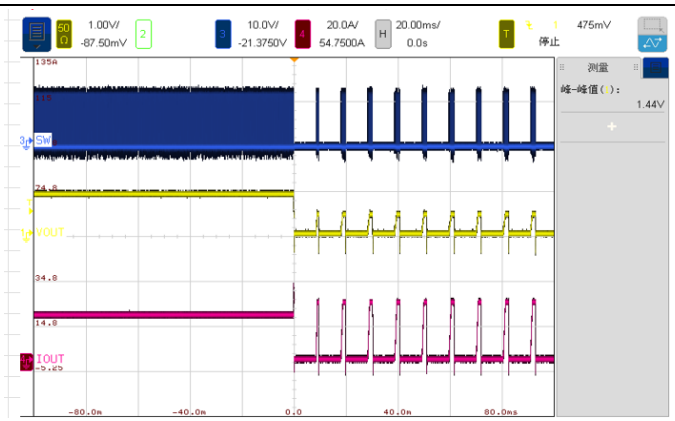
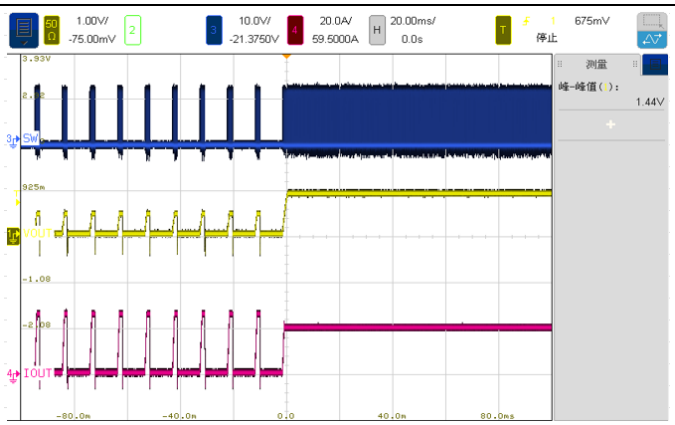
Vin=12V, V_O=5V, I_O=20A, Fsw=800kHz, L=560nH, CO=22uF×8, FCCM Mode



Enable on



Enable off

	
Short circuit entry	Short circuit recovery

OPERATION

The XPC2452 is a high efficiency synchronous stepdown converter that utilizes the proprietary Constant On-Time control architecture. The ultrafast COT control enables the use of small capacitance to reduce the overall BOM cost and save PCB space.

During normal operation, the high-side MOSFET turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the high-side MOSFET turns off, the low-side MOSFET turns on. Due to the output capacitor ESR, the voltage ripple on the output has similar shape to the inductor current. Through the feedback resistor network, this voltage ripple is compared with the internal reference. When the minimum off-time one-shot (180ns, max.) has timed out and the inductor current is below the current-limit threshold, the one-shot is triggered again if the feedback voltage falls below the internal VFB (0.6V, typ.).

The XPC2452 supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). The COT architecture also features excellent transient response, further improving the output variation during high-frequency load transient when the load is suddenly increased.

The conventional COT controller implements the on time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. However, even with defined input and output voltages, a fixed On-time means that frequency has to increase at higher load levels to compensate for the power losses in the MOSFETs and Inductor. The XPC2452 control further adds a frequency locked loop system, which slowly adjusts the On-time to compensate the power losses without influencing the fast transient behavior of the COT topology.

Power and Bias Supply

The VIN pins on the XPC2452 are used to supply voltage to the drain terminal of the internal HSFET. These pins also supply bias voltage for an internal regulator that generates 3V at VCC. The voltage on VCC pin is used for internal chip bias and gate drive for the LSFET. The gate drive for the HSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins, which is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains the C_{BOOT} voltage sufficient to turn on the HSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is higher than the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VCC rail that can pull a current higher than the internal LDO's current limit from the VCC, the VCC drops below the UVLO falling threshold and thereby shutting down the XPC2452 output.

Enable, Start-Up, Shutdown and UVLO

The XPC2452 implements Under-Voltage Lock Out protection (UVLO) to prevent operation without fully turning on the internal power MOSFETs. The UVLO monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device stops switching. The UVLO is non-latching protection.

The EN pin is provided to control the device turn-on and turn-off. When EN pin voltage is above the turn-on threshold (V_{ENH}), the device starts switching and when the EN pin voltage falls below the turn-off threshold (V_{ENL}) it stops switching. If the EN pin is floating, the XPC2452 internally pulls down the EN pin continuously.

When the EN pin voltage rises above the enable threshold voltage, and VCC rises above the V_{CC_UVLOH}, the device enters its start-up sequence and initiates a soft-start ramp of the output voltage. An internal soft start ramp 1ms (typ.) limits the ramp rate of the output voltage to prevent excessive input current during start up. If a longer ramp time is desired, the capacitors can be placed from SS/REFIN pin to the AGND and VSNS-.

The soft-start time and the required external capacitor can be calculated through equation as below.

$$C_{SS}=\frac{tss(ms)\times 45(uA)}{0.6V}$$

A minimum capacitor value of 22nF is required at the SS/REFIN pin. The SS/REFIN capacitor must use the VSNS– pin for its ground. When the V_{EN} is lower than V_{ENL}, the SS/REFIN pin voltage discharges to VSNS-.

Figure 1 below shows the typical power-up sequence of the device. When the VIN and EN pins voltage crosses the UVLO rising threshold and EN rising threshold, and once the voltage on the VCC pin reaches the UVLO rising threshold, the device will start switching if the voltage difference between the SS/REFIN pin and FB pin is equal to 100mV (i.e. VSS/REFIN−VFB= 100mV, typ.) after setting detection is completed. The SS/REFIN pin should never be left unconnected for soft start control. After the VFB rises above the power-good high threshold (92.5% of the VREF, typ.), the PGOOD pin will be in high impedance after a delay time of tPGDLY_LH (0.8ms, typ.).

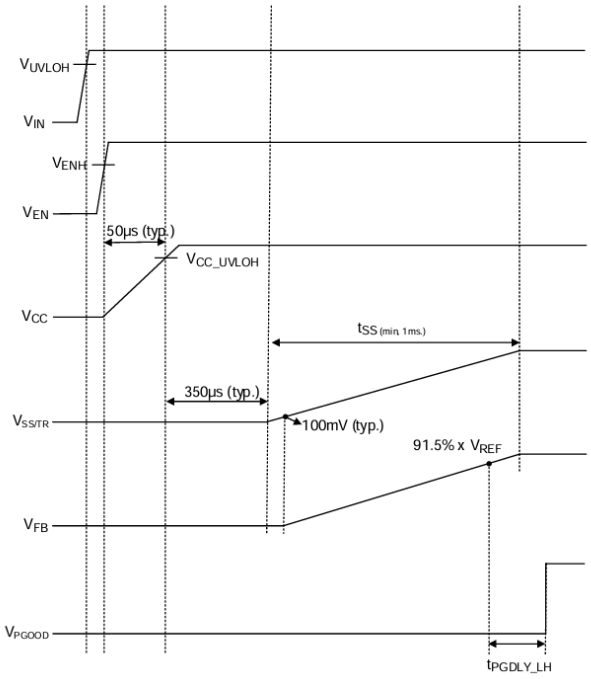


Figure 1. Power Up Sequence

Pre-Bias

If there is a residual voltage on output voltage before startup, both of internal HSFET and LSFET are prohibited switching until the soft start ramp is higher than feedback voltage. When soft-start ramp crosses above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated point.

Minimum On-time and Minimum Off-time

The constraint on operating duty cycle is the minimum controllable on-time and off-time. The minimum on-time, which is 50ns (max.), is the smallest duration of time in which the high-side MOSFET can be in its "ON" state. In continuous mode operation, the minimum duty cycle can be estimated ideally without resistive drop as follows:

$$VIN(max) \leq \frac{VOUT}{fSW(max) \times tON\_MIN(max)}$$

Where t_{ON_MIN} is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

The minimum off-time (t_{OFF_MIN}) is the smallest amount of time that the XPC2452 is capable of turning on the low-side MOSFET, tripping the current comparator and turning the power switch back off. The minimum off-time limit imposes a maximum duty cycle of tON /(tON + tOFF_MIN). Below equation shows the minimum off-time calculation that considers the loss terms,

$$VIN(min) \geq \left[\frac{VOUT + IOUT\_MAX \times (\mathrm{RDSON\_L} + \mathrm{DCR})}{1 - tOFF\_MIN(max) \times fSW(max)}\right] + \mathrm{IOUT\_MAX} \times (RDSON\_H - RDSON\_L)$$

where the minimum off-time of the XPC2452 is 180ns (max), RDS(ON)_H is the high-side MOSFET on resistance, RDS(ON)_L is the low-side MOSFET on resistance and DCR is the DC resistance of inductor.

Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This is detected by internal zero current-detect circuitry utilizing the low-side MOSFET $R_{DS(ON)\_L}$ to sense the inductor current. The low-side MOSFET is turned off when the inductor current drops to zero, resulting in power saving mode (PSM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the feedback voltage falls below the internal VFB.
PSM operation maintains high efficiency at light load, while setting MODE to FCCM operation helps meet tight voltage regulation accuracy requirements.

Power-Good Output

The XPC2452 features an open-drain power-good indication which can be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal VFB. During soft-start, VPGOOD is actively held low and only allowed to become high after soft-start is finished. If VFB rises above the V_{TH_PGLH1} (92.5% of the VFB, typ.), the PGOOD pin will be in high impedance and VPGOOD will be held high after a certain delay elapsed. When VFB falls below the PGOOD low threshold V_{TH_PGHL2} (80% of the VFB, typ.) or exceeds V_{TH_PGHL1} (116% of the VFB, typ.), the PGOOD pin will be pulled low. For VFB higher than V_{TH_PGHL1}, PGOOD can be pulled high again if VFB drops back to the PGOOD high threshold V_{TH_PGLH2} (108% of the VFB, typ.). Once being started-up, if any internal protection is triggered, PGOOD pin will be pulled low to GND. The internal open-drain pull-down device will pull the VPGOOD low. This is to prevent false flag operation for short excursions in output voltage, such as during line and load transients. The power-good indication profile is shown in Figure 2.

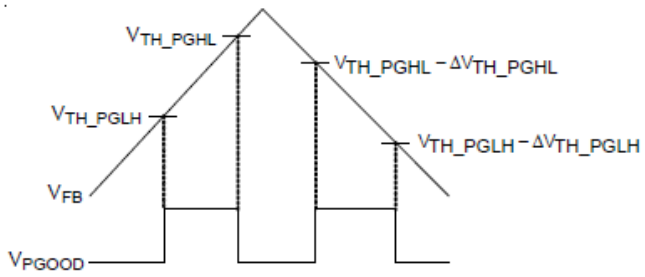


Figure 2. The Logic of PGOOD

Over-Current Protection (OCP)

The XPC2452 features cycle-by-cycle current-limit protection on both the high-side and the low-side

MOSFETs. The protection prevents the device from the catastrophic damage in output short circuit, overcurrent or inductor saturation. The high-side MOSFET peak current-limit protects the inductor current from increasing abnormally, even over the inductor saturation current rating. The high-side MOSFET peak current limit threshold (I_{LIM_H}) is typically 27A. The inductor current through the high-side MOSFET will be measured after a certain amount of delay when the high-side MOSFET is turned on. If an overcurrent condition occurs, the converter will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current from exceeding the I_{LIM_H}. The low-side MOSFET valley current-limit protection is achieved by measuring the inductor current through the low-side MOSFET and mirrored to TRIP pin with the ratio of G_{CS} by using a resistor during the low-side on time. Once the inductor current through the low-side MOSFET is above the low-side MOSFET valley current limit threshold (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the I_{LIM_L}. That is another on-time can only be triggered when the inductor current goes below the I_{LIM_L}. The XPC2452 provides the programmable a cycle-by cycle valley current limit for low-side MOSFET switch by TRIP pin.

$$RTRIP(\Omega) = \frac{VLIM}{GCS \times \left\{ ILIM - \frac{(VIN - VOUT) \times VOUT}{VIN} \times \frac{1}{2 \times L \times fSW} \right\}}$$

Where V_{LIM} =1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (A).

Output Undervoltage Protection

The XPC2452 includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage VFB. If VFB drops below the undervoltage protection threshold V_{UVP} (80% of the VFB, typ.), the UV comparator will go high to turn off both the internal high-side and low-side MOSFETs. When the UVP condition remains for a period of time, a soft-start sequence for auto-recovery will be initiated. If the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and resumes normal operation when overload or short-circuit is removed.

Negative Current Limit

The XPC2452 also monitors inductor current during the "ON" state of the low-side MOSFET to prevent large negative current flowing through the low-side MOSFET. Once the negative current exceeds the low side MOSFET negative current limit threshold ILIM_NEG (−10A, typ.), the device turns off the low-side MOSFET and turns on the high-side MOSFET for the on-time determined by VIN, VOUT and f_{SW}. After the high-side MOSFET on-time expires, the low-side MOSFET turns on again. This behavior can keep the valley of negative current at I_{LIM_NEG} to protect low-side MOSFET. The appropriate inductance should be chosen to avoid the I_{LIM_NEG} being triggered.

Output Overvoltage Protection

The XPC2452 includes an output overvoltage protection (OVP) circuit to limit the output voltage and minimize output voltage overshoot. If the VFB goes above 116% of the VFB, the high-side MOSFET will be latched off and the PGOOD pin keeps low until the VCC or EN is recycled. In the meantime, if the overvoltage condition still exists, the low-side MOSFET remains on to discharge output voltage until the low-side MOSFET valley current reaches the negative current limit threshold (I_{LIM_NEG}). Once reaching the I_{LIM_NEG} the low-side MOSFET is turned off temporarily around 700ns before the low-side FET is turned on again. The XPC2452 repeats in this cycle until the output voltage brings down when the VFB goes below 50% of the VREF, the low-side MOSFET continues to turn on.
Once OVP condition being removed, the XPC2452 returns to normal operation automatically.

Output Voltage Discharge

When the XPC2452 is disabled by EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (70Ω, typ.) connected to ground. This function prevents the reverse current flowing from the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

Over-Temperature Protection (OTP)

The XPC2452 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD} (160°C, typ.). Once the junction temperature cools down by a thermal shutdown hysteresis ΔT_{SD} (30°C, typ.), the XPC2452 will resume normal operation with a complete soft-start. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Mode Selection, Switching Frequency

The XPC2452 offers three different switching frequencies of 600kHz, 800kHz and 1000kHz by setting the MODE pin voltage. Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductors and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage. Furthermore, XPC2452 can also offer two modes which are force continuous-conduction mode (FCCM) and power saving mode (PSM) for light load condition to improve efficiency. The mode and operation frequency configuration can be set by users to connect the resistor to the AGND pin or VCC pin, according to Table 1.

Table 1. Mode Pin Selection

Mode Pin Connections	Light Load Mode	Switching frequency (kHz)
Short to VCC	PSM	600
243KΩ ±10% to AGND	PSM	800
121KΩ ±10% to AGND	PSM	1000
Short to AGND	FCCM	600
30.1KΩ ±10% to AGND	FCCM	800
60.4KΩ ±10% to AGND	FCCM	1000

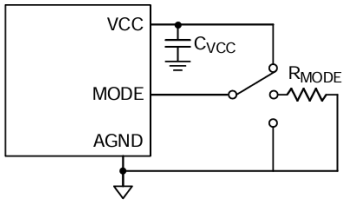
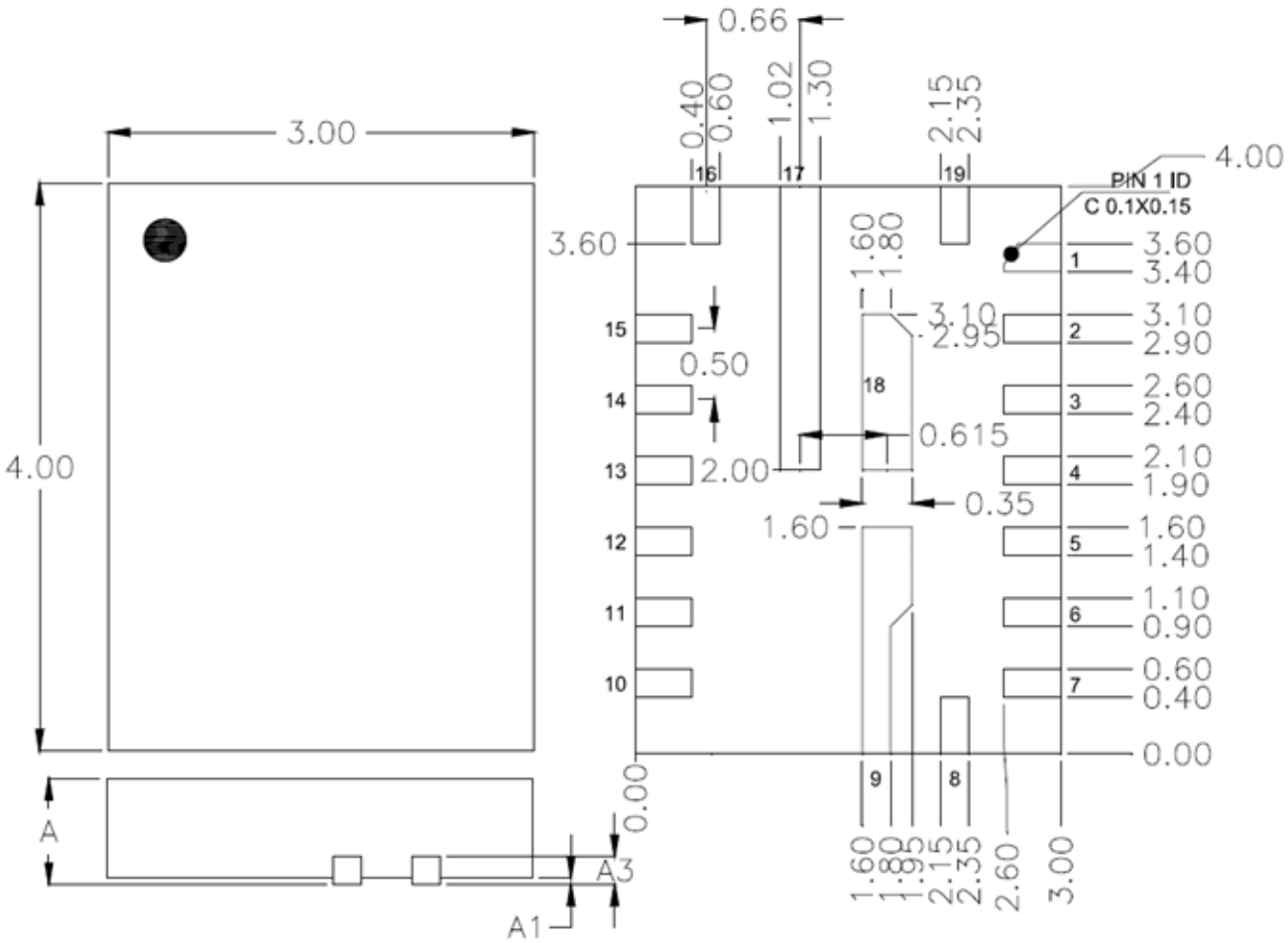


Figure 3. Mode Connection

PHYSICAL DIMENSIONS

Table:Chip Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

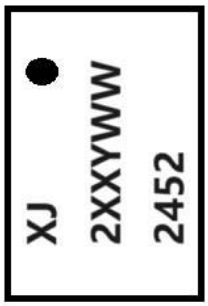
Tolerance
±0.050

MARKING AND REEL INFORMATION

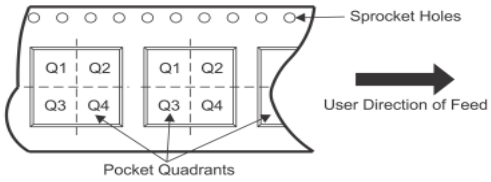
Package Marking & PQ information

XPC2452Q19R Marking

Format:



Pin 1 located in Q1 direction in T&R



Remark:

Font: Arial

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: Assembly location code: 2

b) 2nd & 3rd digit: Assembly lot number

XX means serial number for traceability, either of the 2 characters can be replaced by "0-9, A-Z, a-z"

c) 4th digit: Year code:

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week base on XinJi's calendar.

2. Line2: Product Name Code:

Product Name	P/N Code	Remark
XPC2452Q19R	2452	

3. Packing: 3K/reel