Mobile LPDDR3 SDRAM

MT52L256M16D1, MT52L128M32D1, MT52L256M32D2 MT52L512M32D4, MT52L128M64D2, MT52L256M64D4 MT52L384M32D3

Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 800–10 MHz (data rate range: 1600–20 Mb/s/pin)
- 8*n* prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK/CK# edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 8
- Per-bank refresh for concurrent operation
- Temperature-compensated self refresh (TCSR)
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- On-die termination (ODT)

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	Write Latency	Read Latency
-125	800	1600	6/9	12
-15	667	1333	6/8	10

Options

Options	Marking
• $V_{DD1}/V_{DD2}/V_{DDIN}$: 1.8V/1.2V/1.2V	L
• Array configuration	
– 256 Meg x 16	256M16
– 128 Meg x 32	128M32
– 256 Meg x 32	256M32
– 384 Meg x 32	384M32
– 512 Meg x 32	512M32
– 128 Meg x 64	128M64
– 256 Meg x 64	256M64
• Device configuration	
– 1 die in package	D1
– 2 die in package	D2
– 3 die in package	D3
– 4 die in package	D4
• FBGA “green” package	
– 178-ball FBGA (11mm x 11.5mm)	EL
– 178-ball FBGA (11mm x 11.5mm)	EM
– 178-ball FBGA (11mm x 11.5mm)	ET
– 216-ball FBGA (12mm x 12mm)	LH
– 216-ball FBGA (12mm x 12mm)	LV
– 216-ball FBGA (12mm x 12mm)	LP
– 216-ball FBGA (15mm x 15mm)	LR
– 216-ball FBGA (15mm x 15mm)	LT
– 253-ball FBGA (11.5mm x 11.5mm)	EN
– 253-ball FBGA (11.5mm x 11.5mm)	ER
– 256-ball FBGA (14mm x 14mm)	LS
– 256-ball FBGA (14mm x 14mm)	LU
• Speed grade, cycle time	
– 1.25ns @ RL = 12	-125
– 1.5ns @ RL = 10	-15
• Operating temperature range	
– From –30°C to +85°C	WT
– From –40°C to +105°C	AT
• Revision	:A

Table 2: Configuration Addressing – Single-Channel Package

Architecture		256 Meg x 16	128 Meg x 32	256 Meg x 32	384 Meg x 32	512 Meg x 32
Die per package		1	1	2	3	4
Die per rank	CS0#	1	1	1	1	2
	CS1#	0	0	1	2	2
Ranks (CS#) per channel		1	1	2	2	2
Die configuration per rank (CS#)	CS0#	32 Meg x 16 x 8 banks	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks x 2
	CS1#	N/A	N/A	16 Meg x 32 x 8 banks	32 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks x 2
Row addressing		16K A[13:0]	16K A[13:0]	16K A[13:0]	16K A[13:0]	16K A[13:0]
Column addressing	CS0#	2K A[10:0]	1K A[9:0]	1K A[9:0]	1K A[9:0]	2K A[10:0]
	CS1#	N/A	N/A	1K A[9:0]	2K A[10:0]	2K A[10:0]

Note: 1. A channel is a complete LPDRAM interface, including command/address, and data pins.

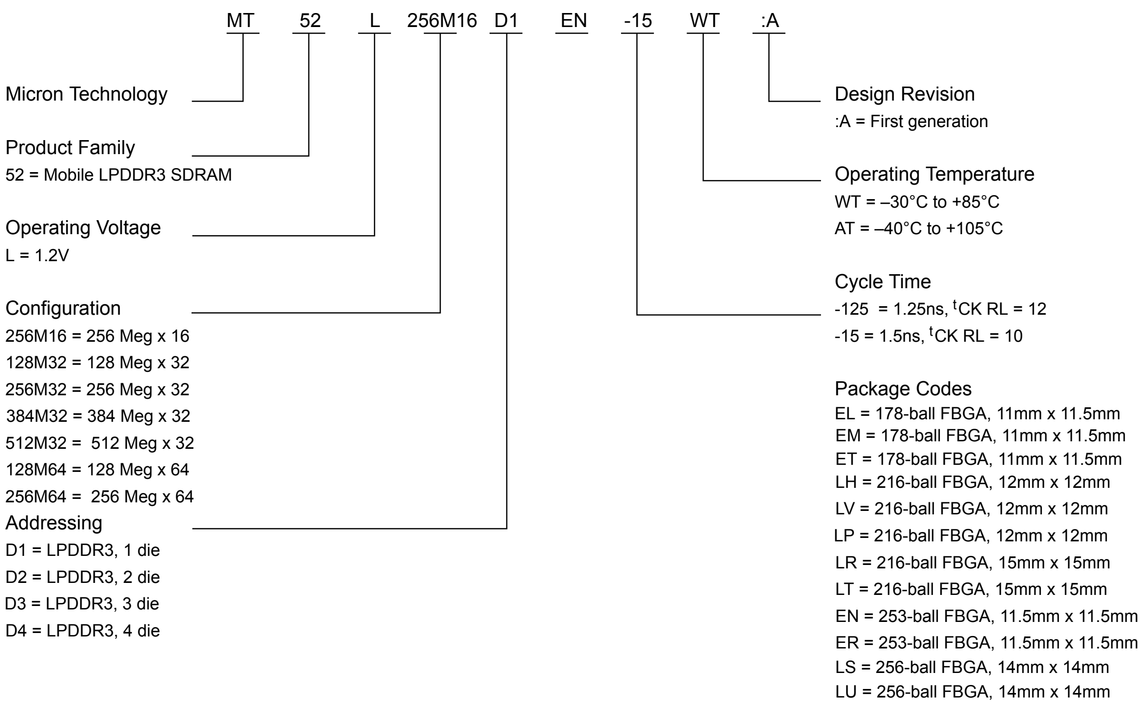
Table 3: Configuration Addressing – Dual-Channel Package

Architecture		128 Meg x 64	256 Meg x 64
Die per package		2	4
Ranks (CS#) per channel	A	1	2
	B	1	2
Die per rank	CS0#	1 ChA, 1 ChB	1 ChA, 1 ChB
	CS1#	0	1 ChA, 1 ChB
Die configuration per rank (CS#)	CS0#	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks
	CS1#	N/A	16 Meg x 32 x 8 banks
Row addressing		16K A[13:0]	16K A[13:0]
Column addressing	CS0#	1K A[9:0]	1K A[9:0]
	CS1#	N/A	1K A[9:0]

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Part Numbering

Figure 1: Marketing Part Number Chart



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Package Codes and Descriptions

Table 4: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
EL	178	1	1	11 x 11.5 x 0.8 (0.8 x 0.65 pitch)	SDP	SAC305
EM	178	2	1	11 x 11.5 x 0.9 (0.8 x 0.65 pitch)	DDP	SAC305
ET	178	2	1	11 x 11.5 x 1.2 (0.8 x 0.65 pitch)	QDP	SAC305
LH	216	1	1 (Chan B only)	12 x 12 x 0.65 (0.4 pitch)	SDP	SAC305
LV	216	2	1 (Chan B only)	12 x 12 x 0.75 (0.4 pitch)	DDP	SAC305
LP	216	2	1 (Chan B only)	12 x 12 x 0.82 (0.4 pitch)	3DP	SAC305
LR	216	1 – DDP 2 – QDP	2	15 x 15 x 0.8 (0.5 pitch)	DDP/QDP	SAC305
LT	216	2	2	15 x 15 x 1.0 (0.5 pitch)	QDP	SAC305
EN	253	1	2	11.5 x 11.5 x 0.9 (0.5 pitch)	DDP	LF35 (w/OSP)
ER	253	2	2	11.5 x 11.5 x 1.2 (0.5 pitch)	QDP	LF35 (w/OSP)
LS	256	1	2	14 x 14 x 0.75 (0.4 pitch)	DDP	SAC305
LU	256	2	2	14 x 14 x 1.0 (0.4 pitch)	QDP	SAC305

Notes:
1. SDP = Single-die package, DDP = Dual-die package, 3DP = 3-die package, QDP = Quad-die package.
2. Solder ball material: LF35 with Cu OSP ball pads (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni)
   SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)

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General Description

The 4Gb Mobile Low-Power DDR3 SDRAM (LPDDR3) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" and "CA" include all BA and CA pins, respectively, used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 5: 256 Meg x 16 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-15	-125	
I_{DD01}	V_{DD1}	15	15	mA
I_{DD02}	V_{DD2}	70	70	
$I_{DD0,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD2P1}	V_{DD1}	600	600	µA
I_{DD2P2}	V_{DD2}	800	800	
$I_{DD2P,in}$	$V_{DDCA} + V_{DDQ}$	70	70	
I_{DD2PS1}	V_{DD1}	600	600	µA
I_{DD2PS2}	V_{DD2}	800	800	
$I_{DD2PS,in}$	$V_{DDCA} + V_{DDQ}$	70	70	
I_{DD2N1}	V_{DD1}	2	2	mA
I_{DD2N2}	V_{DD2}	28	28	
$I_{DD2N,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD2NS1}	V_{DD1}	2	2	mA
I_{DD2NS2}	V_{DD2}	7	7	
$I_{DD2NS,in}$	$V_{DDCA} + V_{DDQ}$	3	3.5	
I_{DD3P1}	V_{DD1}	1.2	1.2	mA
I_{DD3P2}	V_{DD2}	8	8	mA
$I_{DD3P,in}$	$V_{DDCA} + V_{DDQ}$	150	150	µA
I_{DD3PS1}	V_{DD1}	1.2	1.2	mA
I_{DD3PS2}	V_{DD2}	8	8	mA
$I_{DD3PS,in}$	$V_{DDCA} + V_{DDQ}$	150	150	µA
I_{DD3N1}	V_{DD1}	2	2	mA
I_{DD3N2}	V_{DD2}	30	35	
$I_{DD3N,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD3NS1}	V_{DD1}	2	2	mA
I_{DD3NS2}	V_{DD2}	7	8	
$I_{DD3NS,in}$	$V_{DDCA} + V_{DDQ}$	3	3.5	
I_{DD4R1}	V_{DD1}	5	5	mA
I_{DD4R2}	V_{DD2}	235	250	
$I_{DD4R,in}$	V_{DDCA}	8	10	
I_{DD4W1}	V_{DD1}	10	10	mA
I_{DD4W2}	V_{DD2}	235	250	
$I_{DD4W,in}$	$V_{DDCA} + V_{DDQ}$	30	34	

Table 5: 256 Meg x 16 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-15	-125	
I_{DD51}	V_{DD1}	40	40	mA
I_{DD52}	V_{DD2}	150	150	
$I_{DD5,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD5PB1}	V_{DD1}	5	5	mA
I_{DD5PB2}	V_{DD2}	40	40	
$I_{DD5PB,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD5AB1}	V_{DD1}	5	5	mA
I_{DD5AB2}	V_{DD2}	40	40	
$I_{DD5AB,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD61}	V_{DD1}	1000	1000	μA
I_{DD62}	V_{DD2}	3200	3200	
$I_{DD6,in}$	$V_{DDCA} + V_{DDQ}$	70	70	
I_{DD81}	V_{DD1}	25	25	μA
I_{DD82}	V_{DD2}	100	100	
$I_{DD8,in}$	$V_{DDCA} + V_{DDQ}$	100	100	

Table 6: 128 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade		Unit
		-15	-125	
I_{DD01}	V_{DD1}	15	15	mA
I_{DD02}	V_{DD2}	70	70	
$I_{DD0,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD2P1}	V_{DD1}	600	600	µA
I_{DD2P2}	V_{DD2}	800	800	
$I_{DD2P,in}$	$V_{DDCA} + V_{DDQ}$	70	70	
I_{DD2PS1}	V_{DD1}	600	600	µA
I_{DD2PS2}	V_{DD2}	800	800	
$I_{DD2PS,in}$	$V_{DDCA} + V_{DDQ}$	70	70	
I_{DD2N1}	V_{DD1}	2	2	mA
I_{DD2N2}	V_{DD2}	28	28	mA
$I_{DD2N,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD2NS1}	V_{DD1}	2	2	
I_{DD2NS2}	V_{DD2}	7	7	mA
$I_{DD2NS,in}$	$V_{DDCA} + V_{DDQ}$	3	3.5	
I_{DD3P1}	V_{DD1}	1.2	1.2	mA
I_{DD3P2}	V_{DD2}	8	8	mA
$I_{DD3P,in}$	$V_{DDCA} + V_{DDQ}$	150	150	µA
I_{DD3PS1}	V_{DD1}	1.2	1.2	mA
I_{DD3PS2}	V_{DD2}	8	8	mA
$I_{DD3PS,in}$	$V_{DDCA} + V_{DDQ}$	150	150	µA
I_{DD3N1}	V_{DD1}	2	2	
I_{DD3N2}	V_{DD2}	30	35	mA
$I_{DD3N,in}$	$V_{DDCA} + V_{DDQ}$	8	10	
I_{DD3NS1}	V_{DD1}	2	2	mA
I_{DD3NS2}	V_{DD2}	7	8	
$I_{DD3NS,in}$	$V_{DDCA} + V_{DDQ}$	3	3.5	
I_{DD4R1}	V_{DD1}	5	5	mA
I_{DD4R2}	V_{DD2}	235	250	
$I_{DD4R,in}$	V_{DDCA}	8	10	
I_{DD4W1}	V_{DD1}	10	10	mA
I_{DD4W2}	V_{DD2}	235	250	
$I_{DD4W,in}$	$V_{DDCA} + V_{DDQ}$	30	34	
I_{DD51}	V_{DD1}	40	40	mA
I_{DD52}	V_{DD2}	150	150	
$I_{DD5,in}$	$V_{DDCA} + V_{DDQ}$	8	10	

Table 6: 128 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

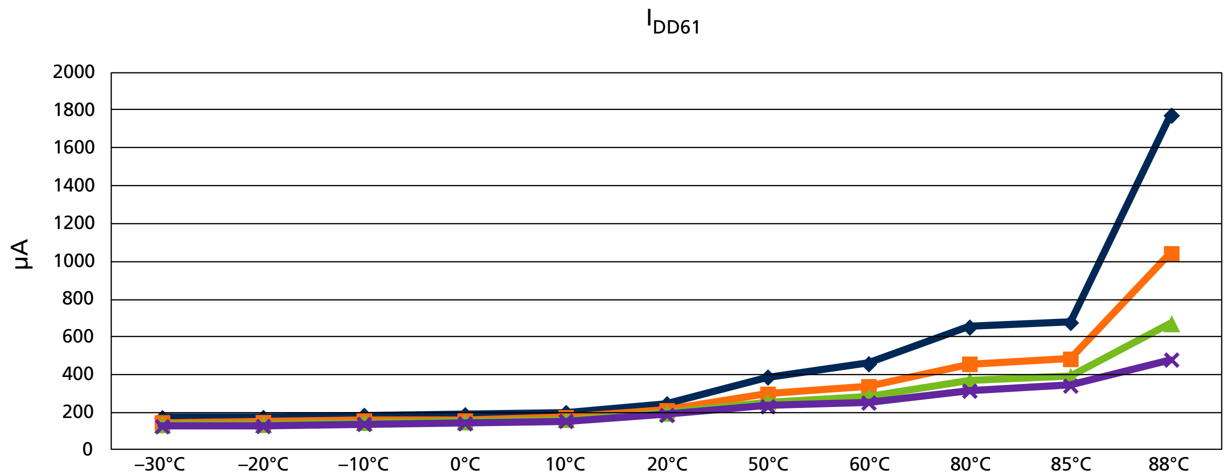
Parameter	Supply	Speed Grade		Unit
		-15	-125	
I_{DD5PB1}	V_{DD1}	5	5	mA
I_{DD5PB2}	V_{DD2}	40	40	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	8	10	
I_{DD5AB1}	V_{DD1}	5	5	mA
I_{DD5AB2}	V_{DD2}	40	40	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	8	10	
I_{DD61}	V_{DD1}	1000	1000	µA
I_{DD62}	V_{DD2}	3200	3200	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	70	70	
I_{DD81}	V_{DD1}	25	25	µA
I_{DD82}	V_{DD2}	100	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	100	100	

Table 7: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

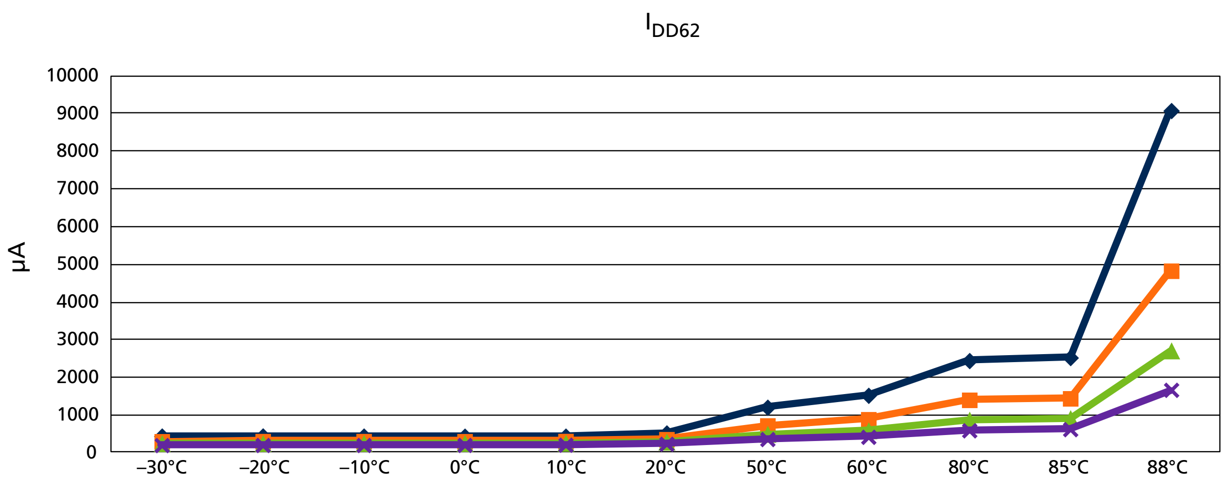
PASR	Supply	Value	Unit
Full array	V_{DD1}	1000	µA
	V_{DD2}	3200	
	V_{DDi}	70	
1/2 array	V_{DD1}	950	
	V_{DD2}	2700	
	V_{DDi}	70	
1/4 array	V_{DD1}	900	
	V_{DD2}	2400	
	V_{DDi}	70	
1/8 array	V_{DD1}	850	
	V_{DD2}	2000	
	V_{DDi}	70	

Figure 2: Typical Self Refresh Current vs. Temperature – I_{DD61}



	–30°C	–20°C	–10°C	0°C	10°C	20°C	50°C	60°C	80°C	85°C	88°C
Full array	170.1	171.2	182.5	185.7	197.5	244.2	385.8	456.1	650.4	675.3	1773
Half array	145.4	146.2	157.4	159.2	172.3	209.4	296.5	336.5	455.8	482.15	1041
Quarter array	131.7	133	143.9	146.7	159.7	193.1	253	280.2	365.3	387.5	667
Eighth array	124.9	126.3	137.5	140.6	153.2	185	230.9	250.6	313.5	340.2	478.2

Figure 3: Typical Self Refresh Current vs. Temperature – I_{DD62}



	–30°C	–20°C	–10°C	0°C	10°C	20°C	50°C	60°C	80°C	85°C	88°C
Full array	439.9	441.8	439.1	435.9	437.1	521.6	1203.8	1519.5	2441.1	2521.4	9073.2
Half array	300	303.7	303.6	301.5	305.8	354.9	718.9	884	1400.1	1438.8	4824.4
Quarter array	233	234.6	235.8	235.7	241	274.4	479.9	573.3	854.3	895.9	2693.1
Eighth array	199.2	201.8	201.1	202.8	208.4	234.4	359.6	418.7	590.6	621.5	1621.2

Package Block Diagrams

Figure 4: Single Rank, Single Channel Package Block Diagram

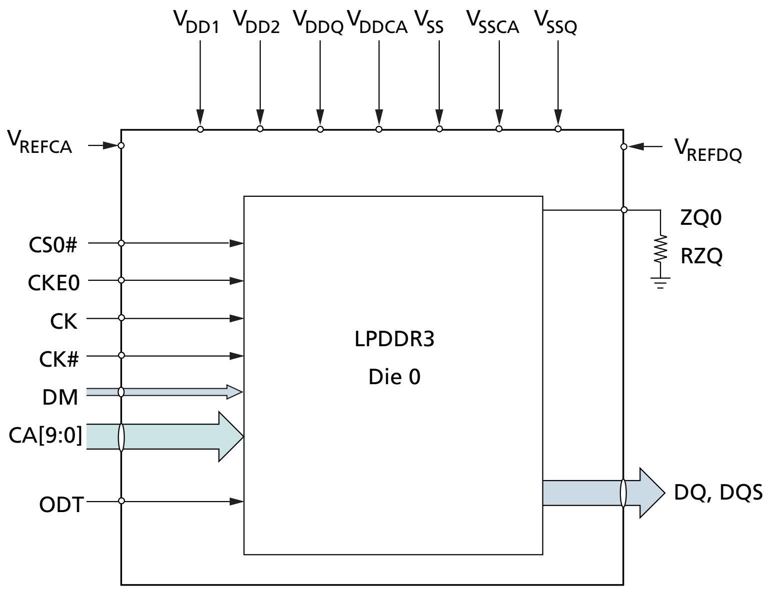


Figure 5: Dual Rank, Single Channel Package Block Diagram

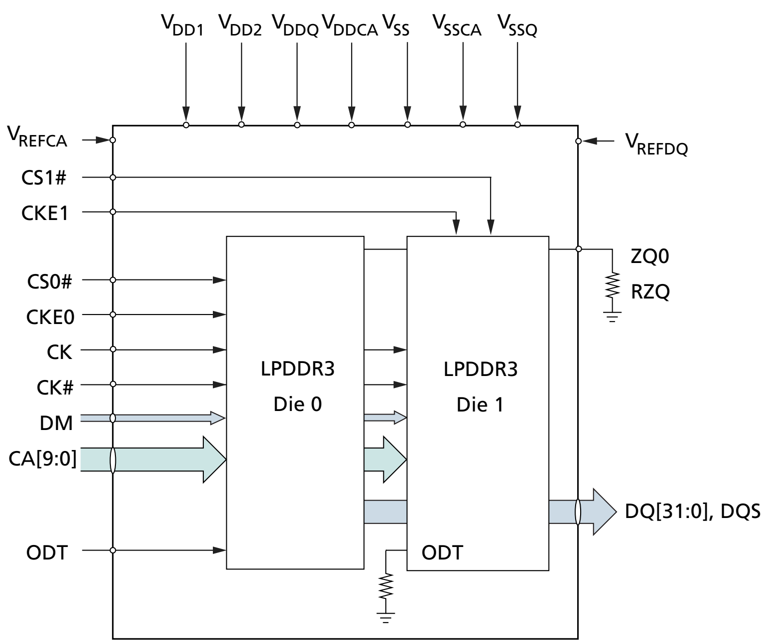


Figure 6: Single Rank, Dual Channel Package Block Diagram

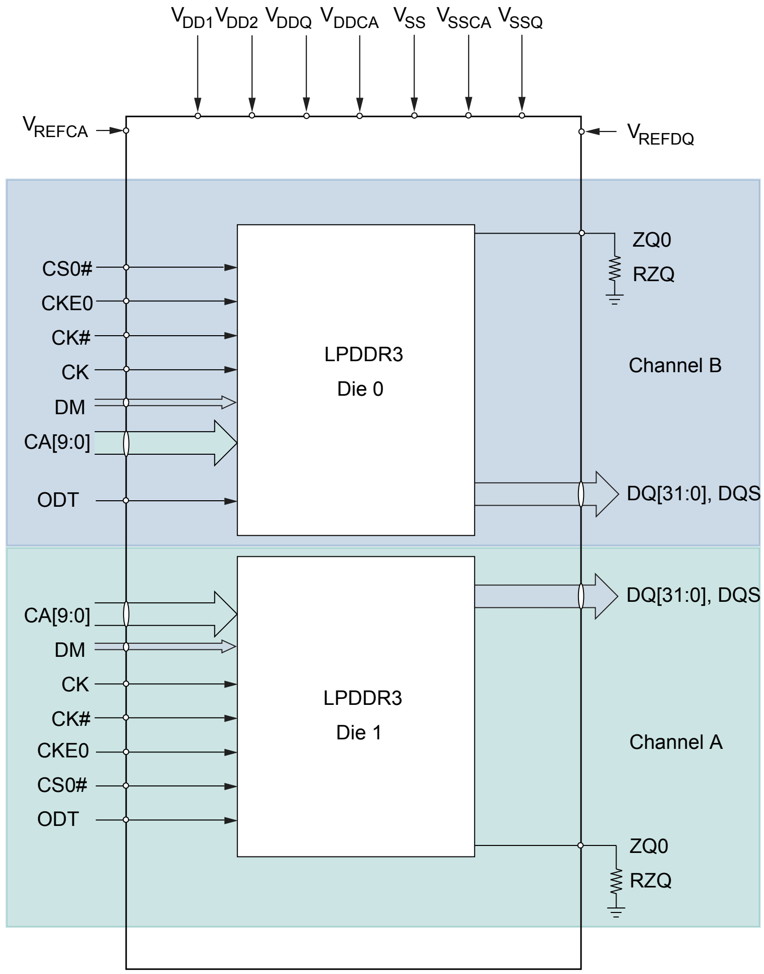


Figure 7: Dual Rank, Single Channel Package Block Diagram

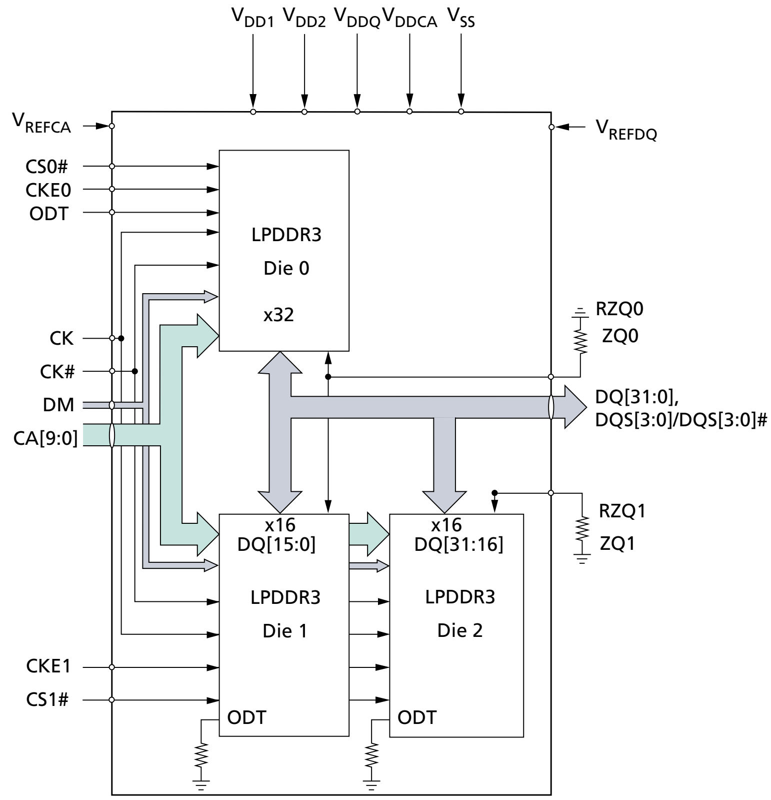


Figure 8: Dual Rank, Dual Channel Package Block Diagram

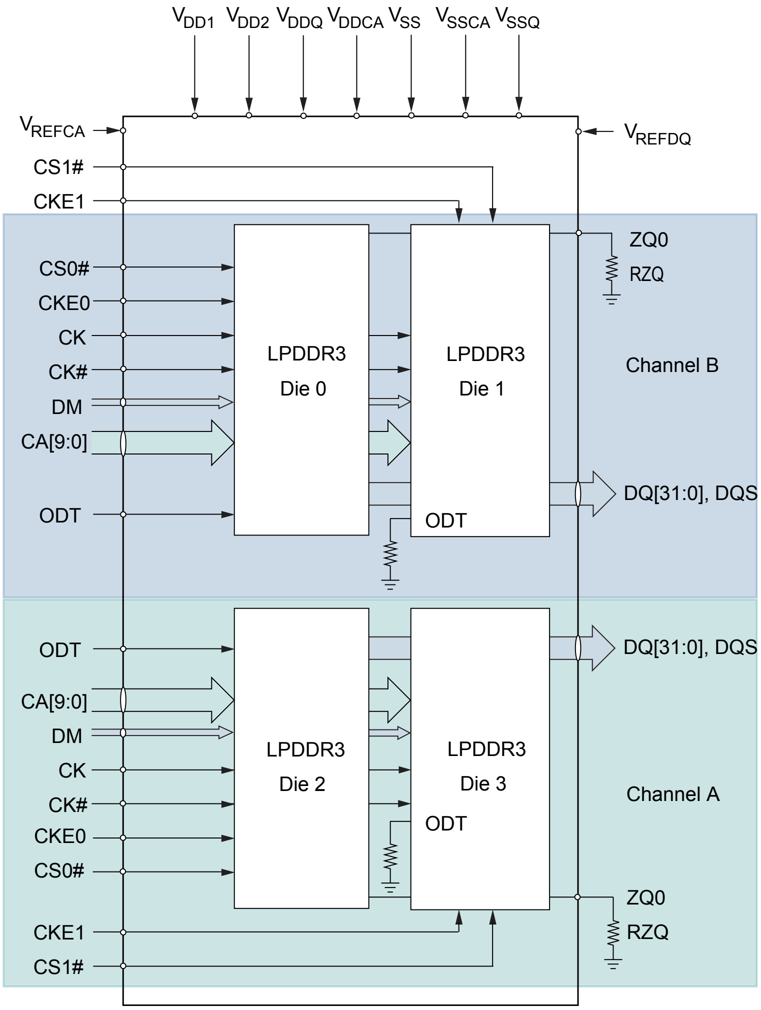
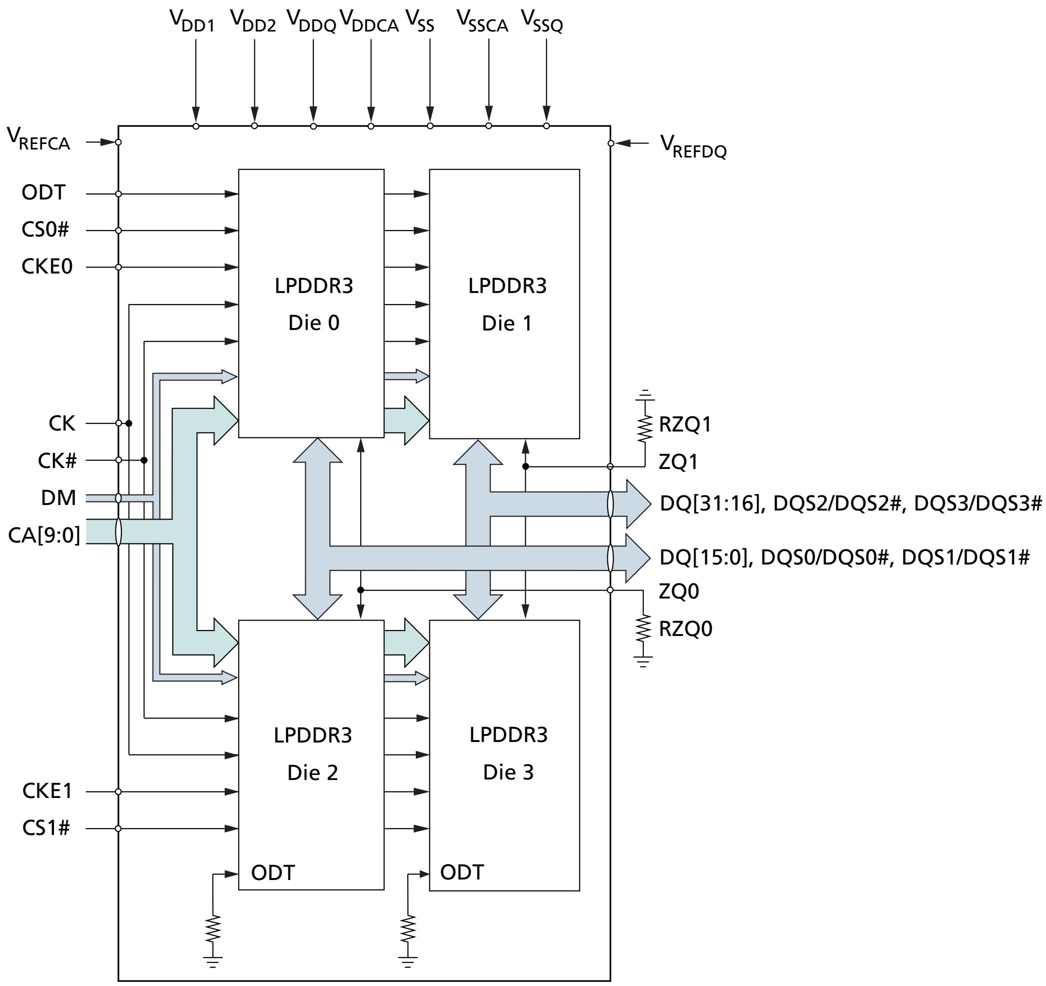
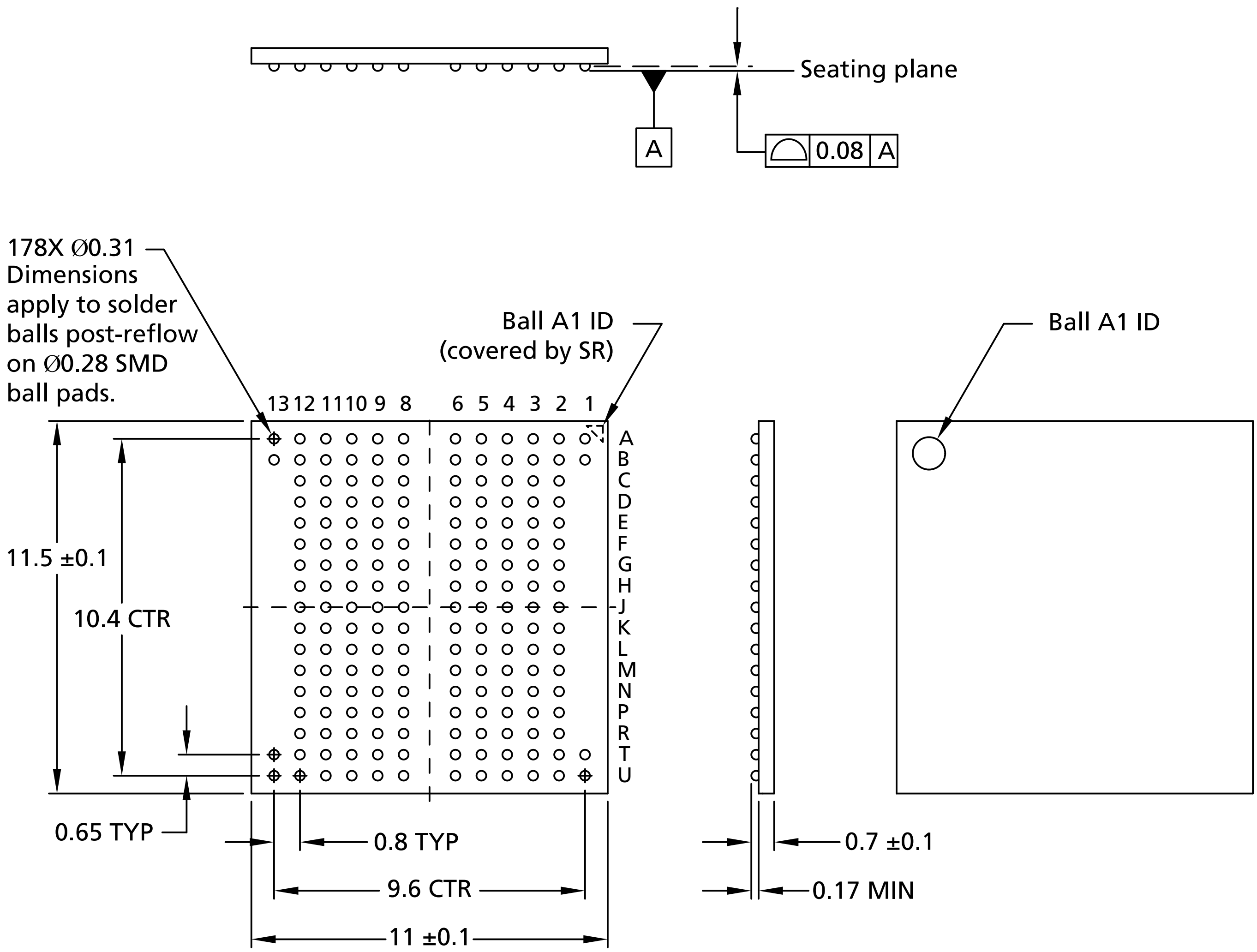


Figure 9: Dual Rank, Single Channel Package Block Diagram



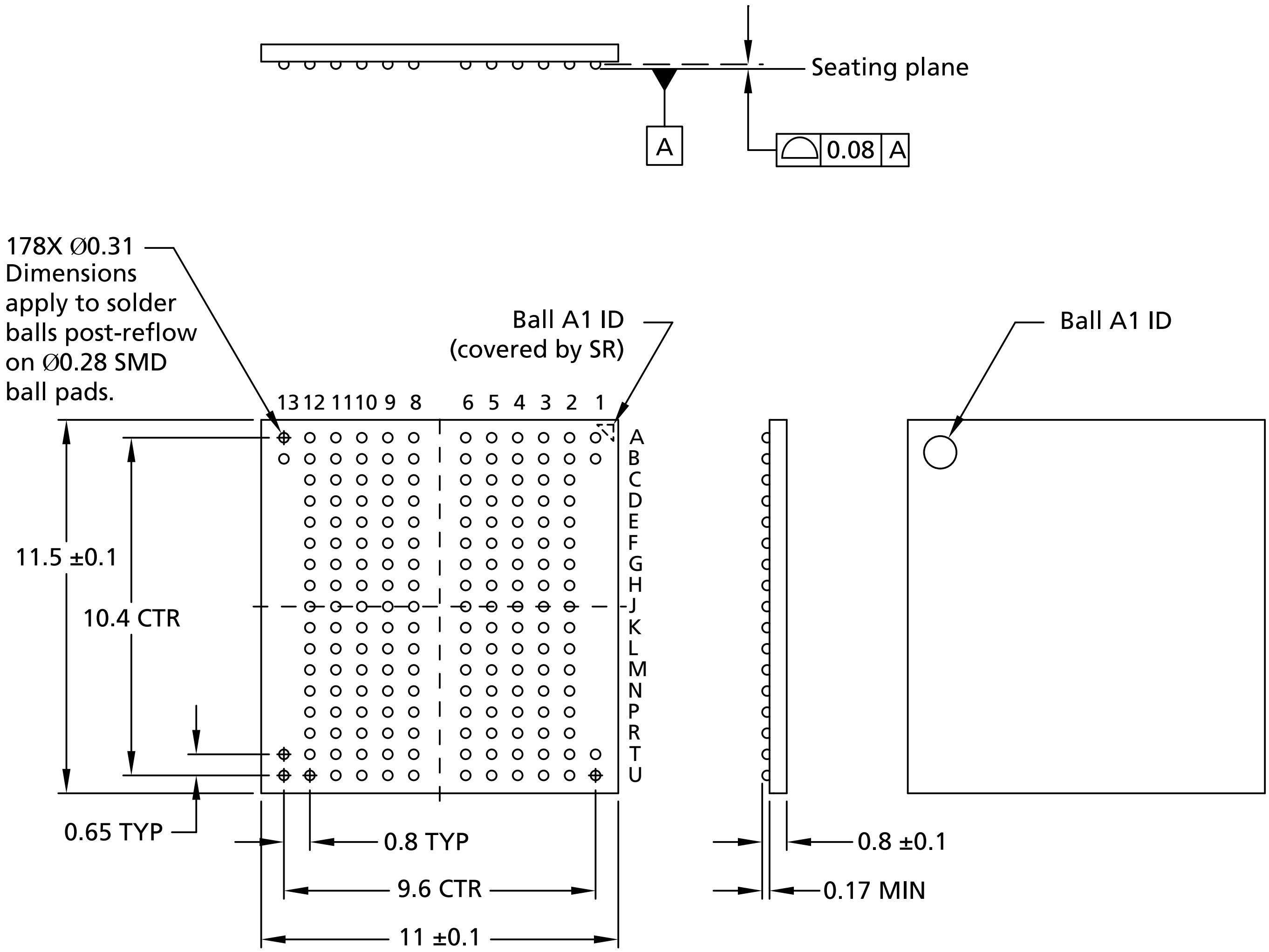
Package Dimensions

Figure 10: 178-Ball WFBGA – 11mm x 11.5mm (Package Code EL)



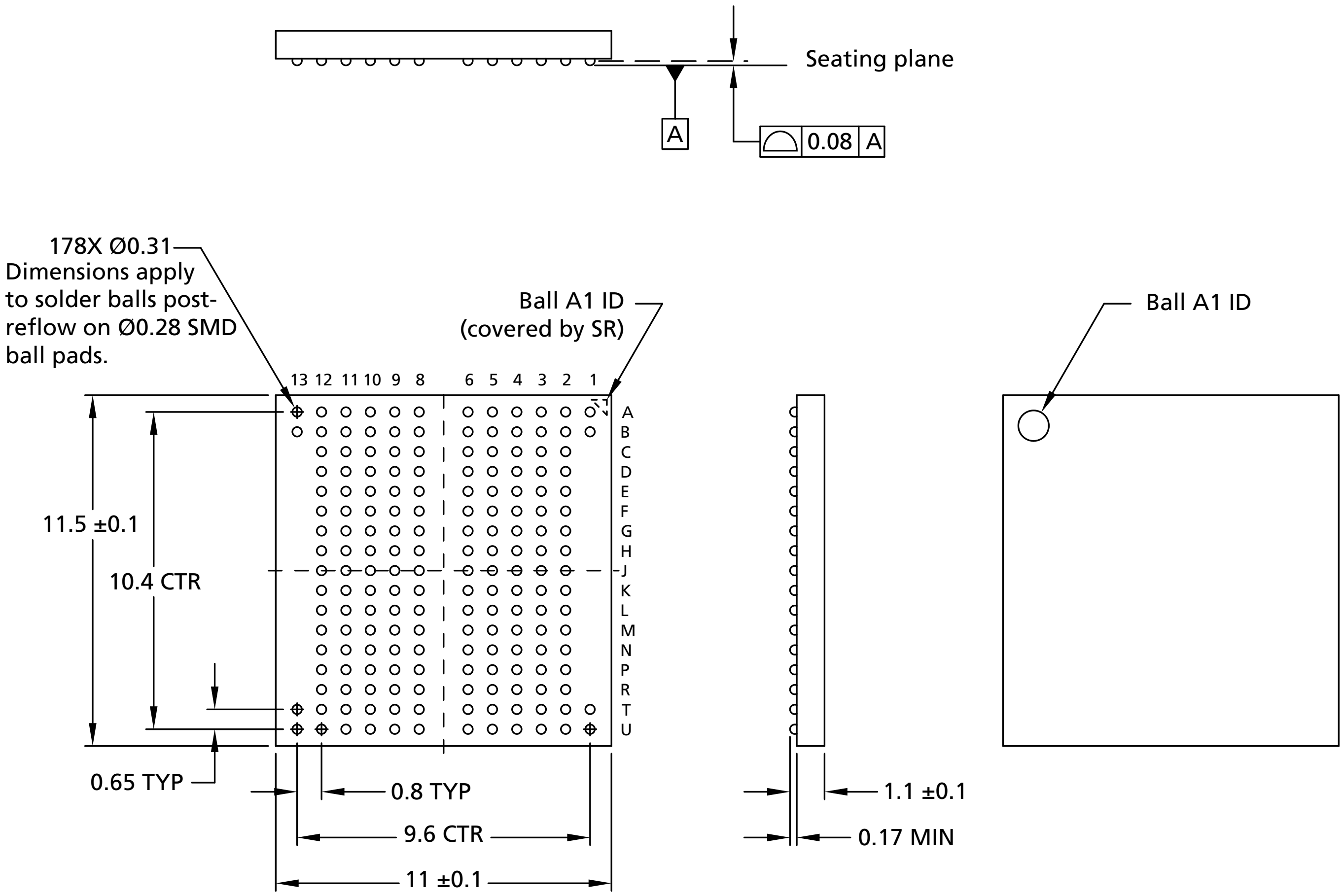
Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 11: 178-Ball VFBGA – 11mm x 11.5mm (Package Code EM)



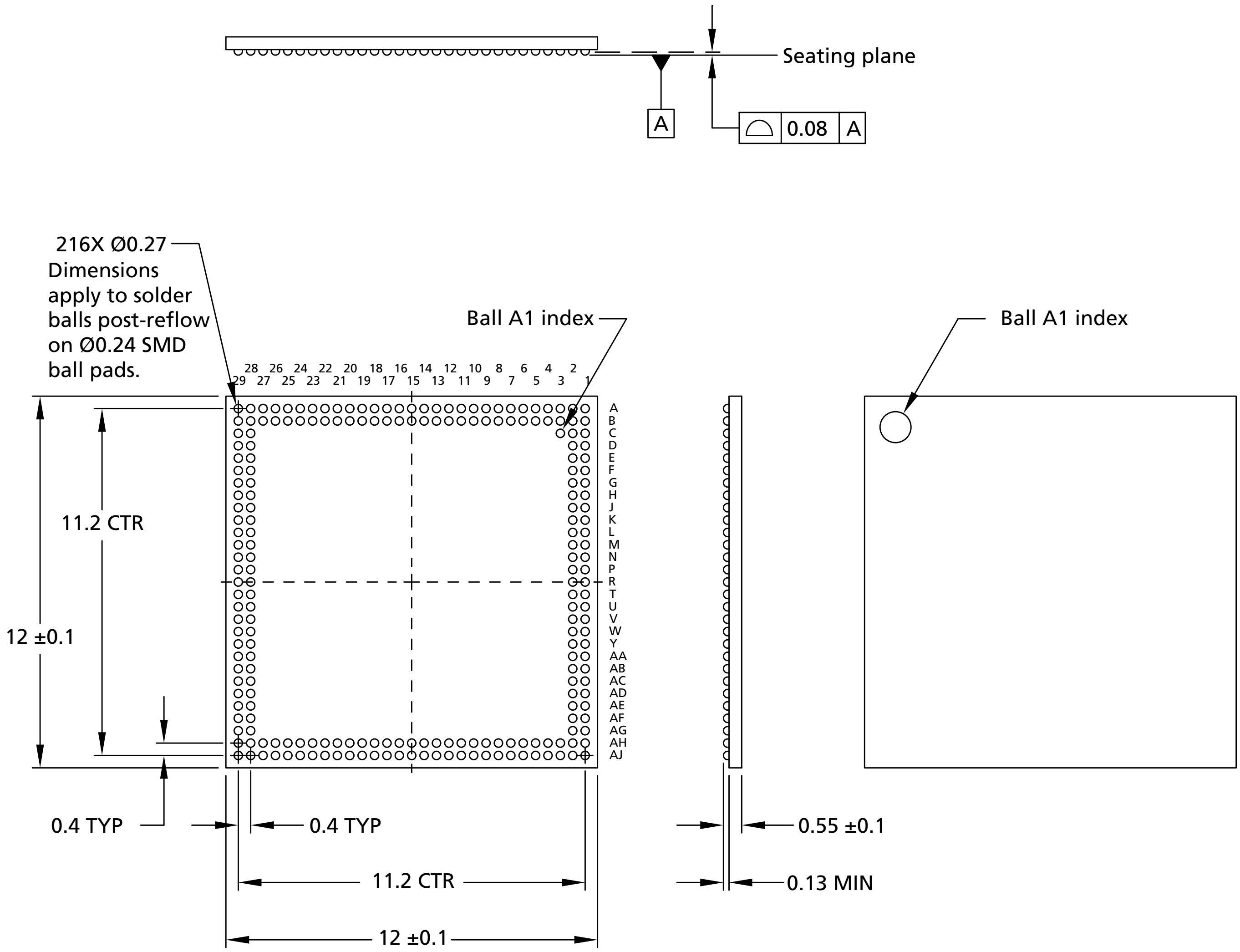
Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 12: 178-Ball VFBGA – 11mm x 11.5mm (Package Code ET)



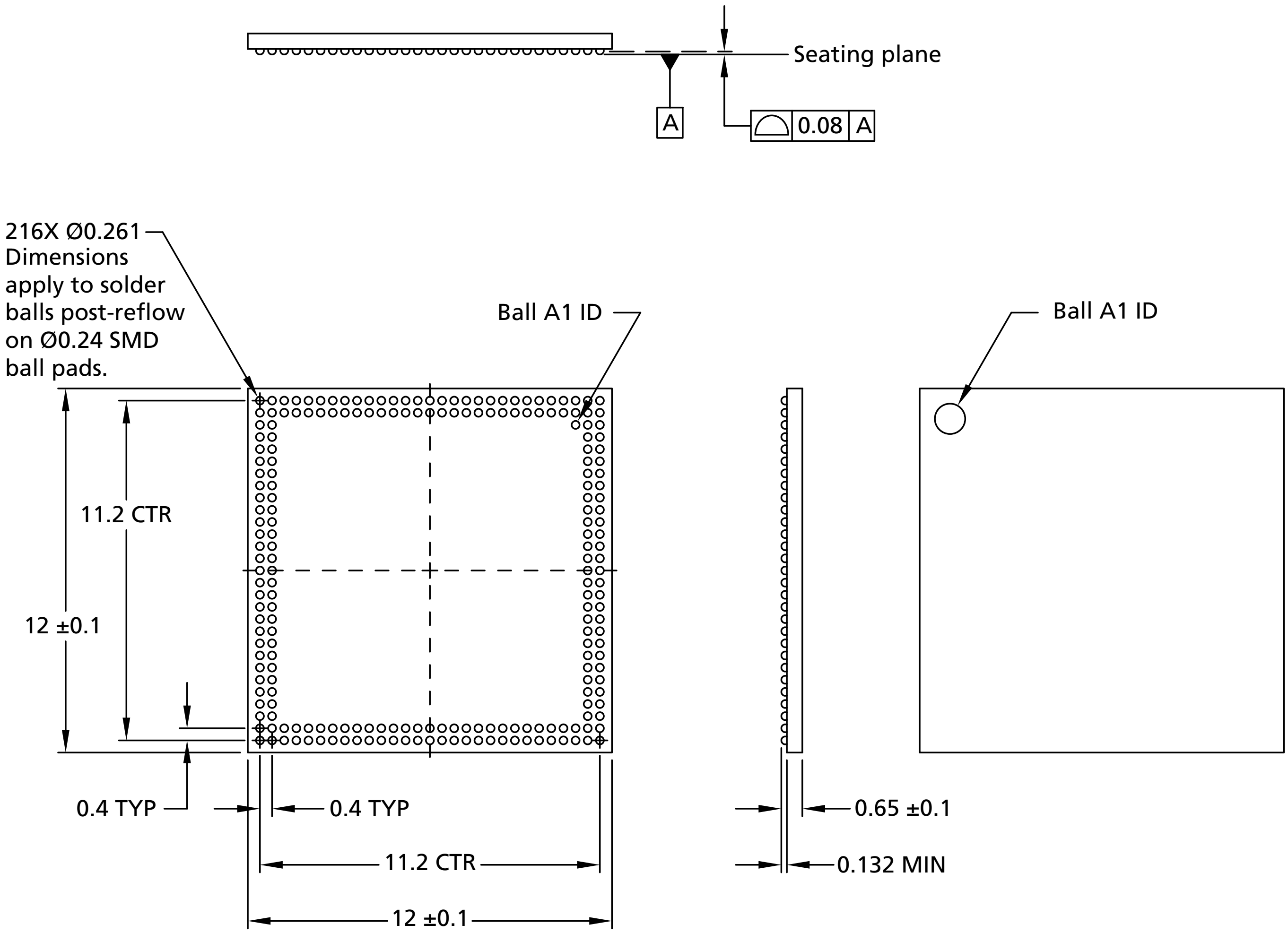
Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 13: 216-Ball UFBGA – 12mm x 12mm (Package Code LH)



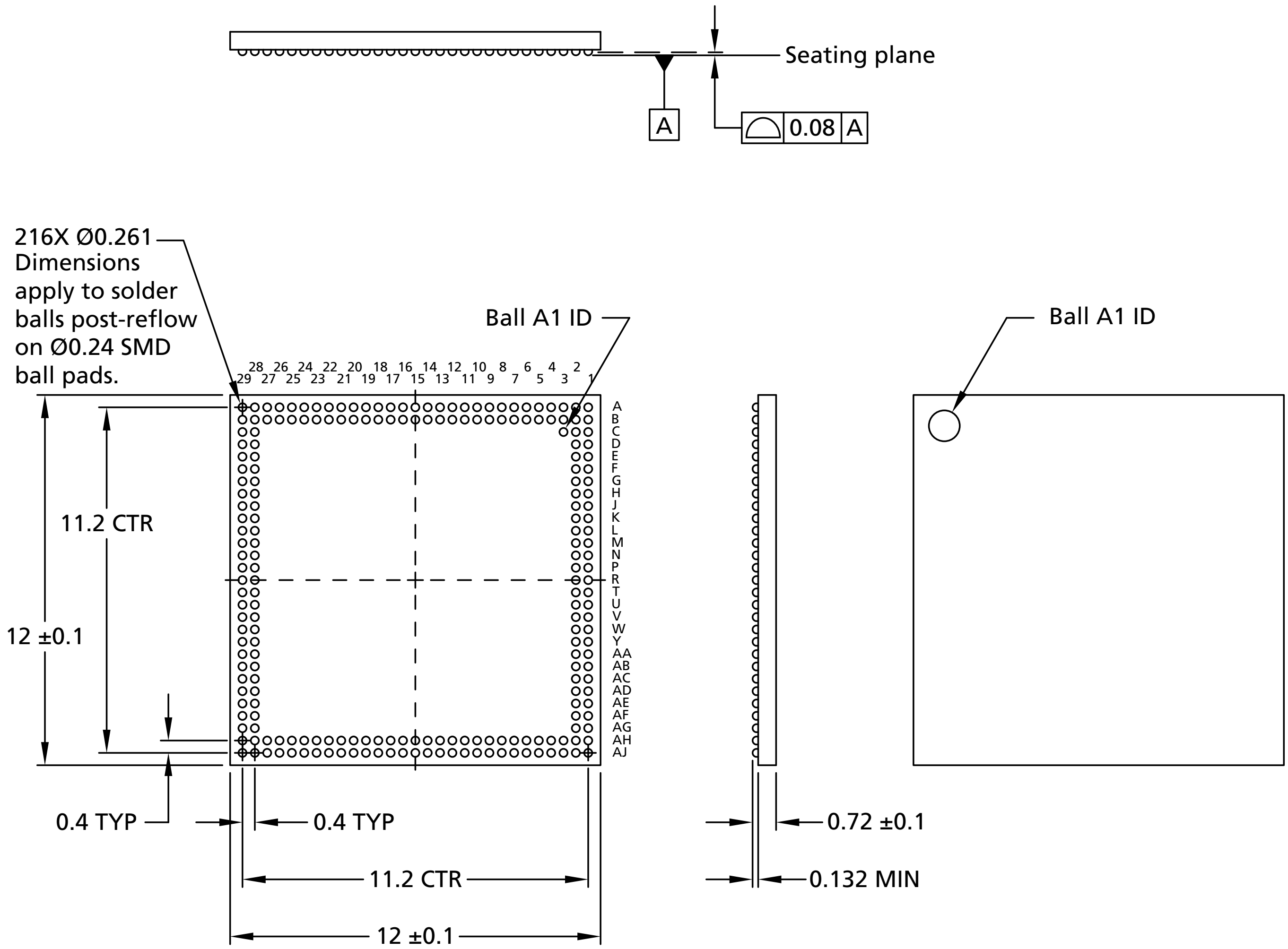
Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 14: 216-Ball WFBGA – 12mm x 12mm (Package Code LV)



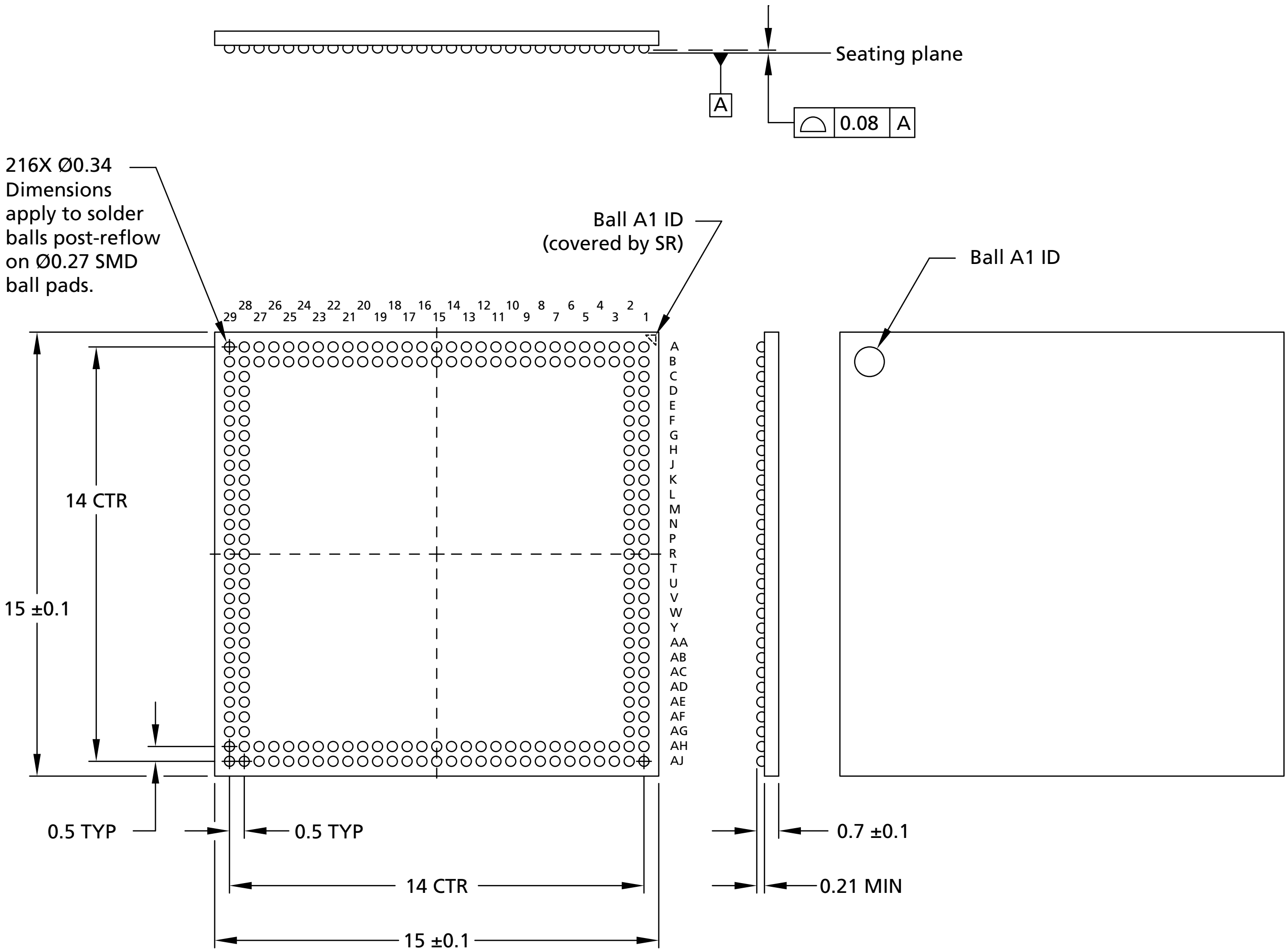
Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 15: 216-Ball VFBGA – 12mm x 12mm (Package Code LP)



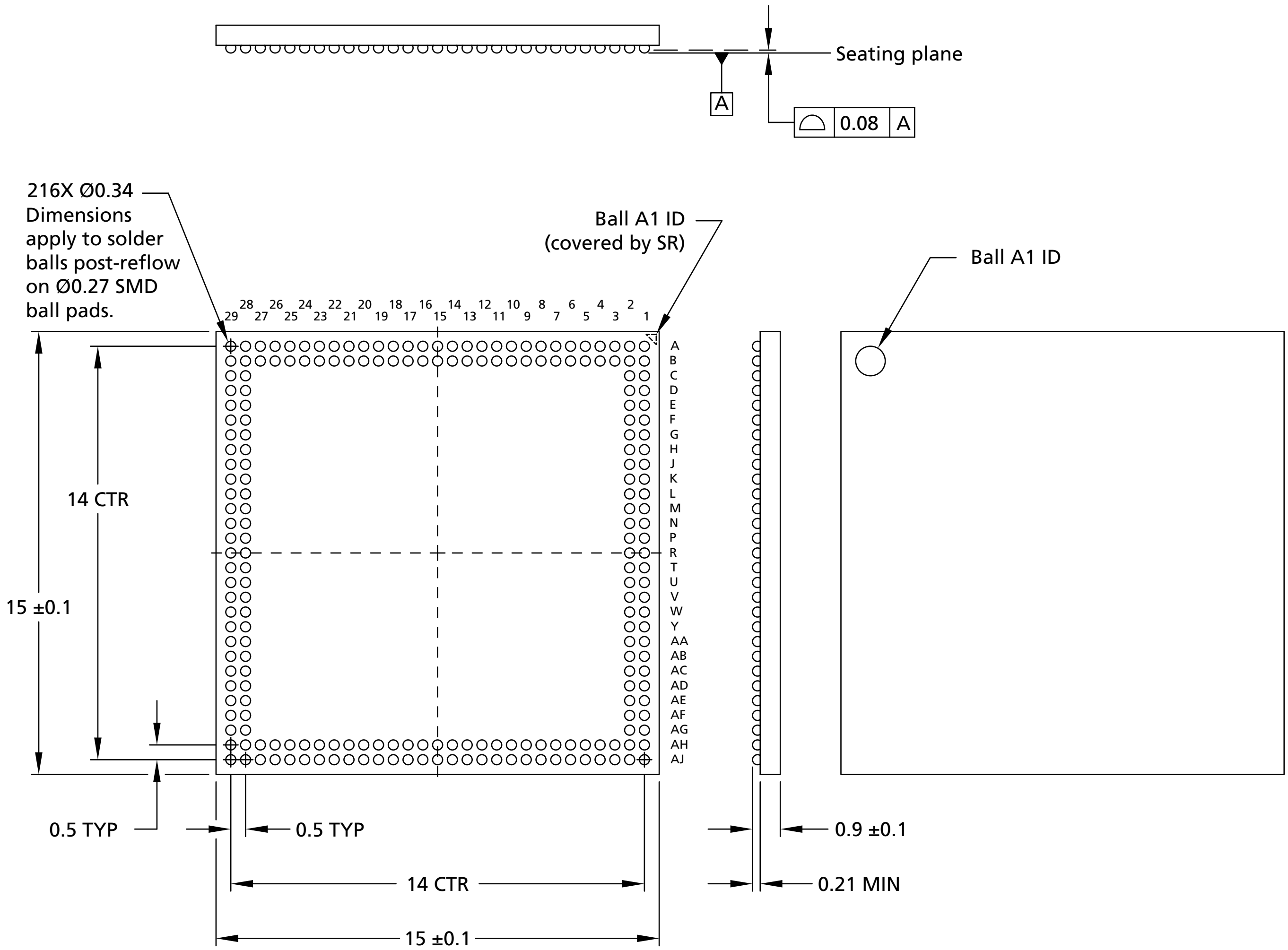
Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 16: 216-Ball WFBGA – 15mm x 15mm (Package Code LR)



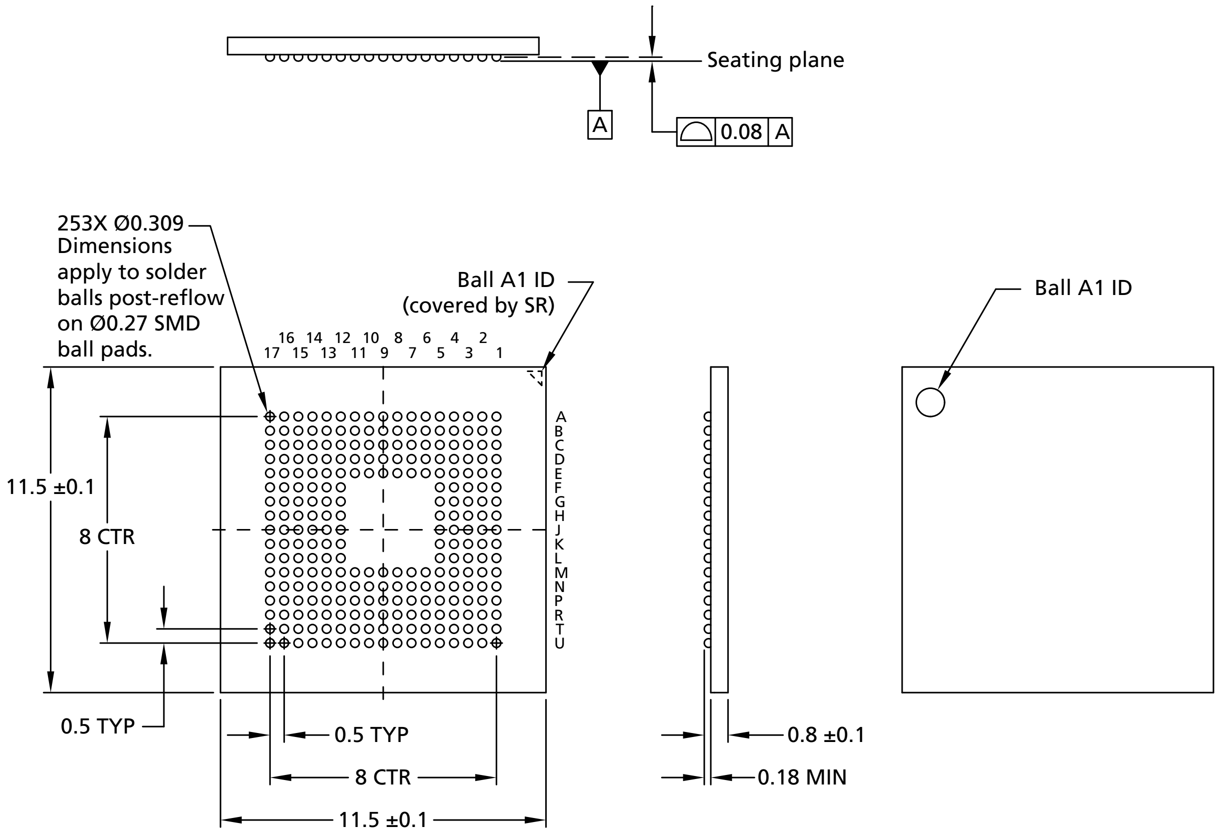
Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 17: 216-Ball VFBGA – 15mm x 15mm (Package Code LT)



Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

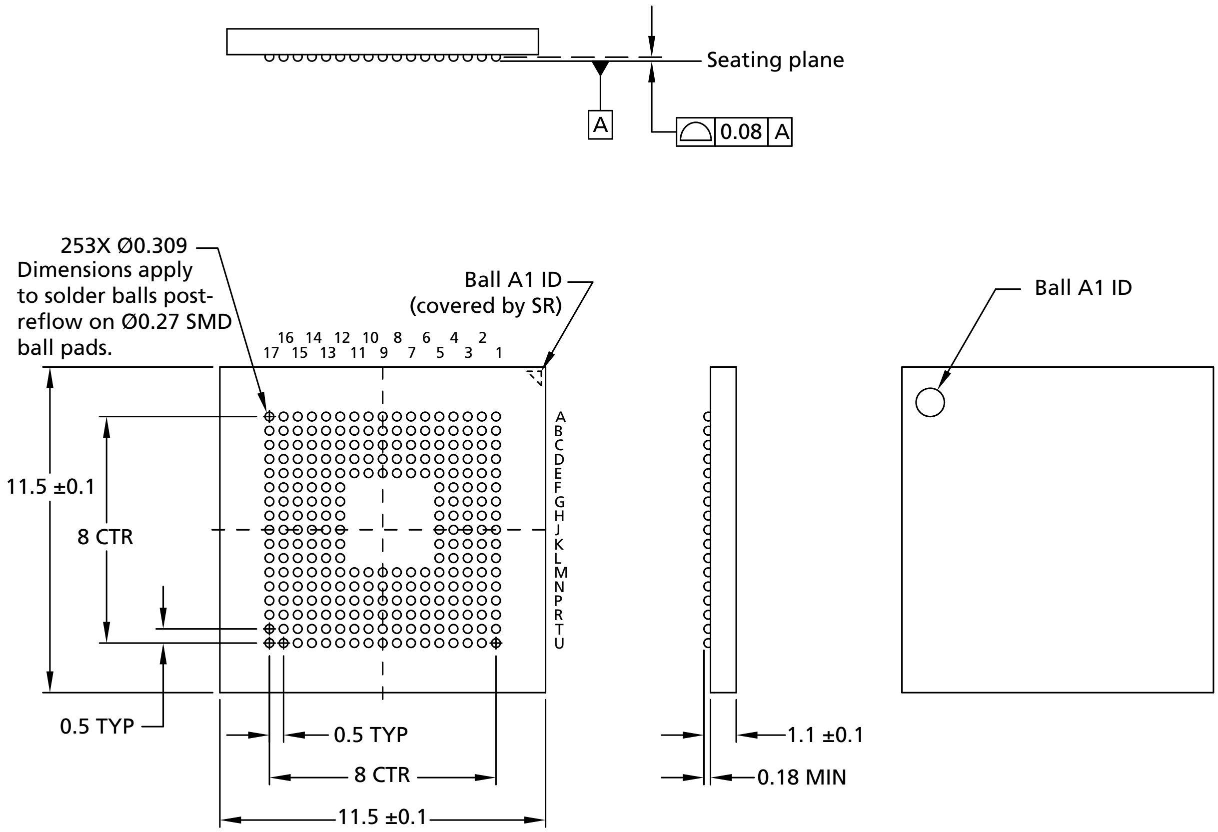
Figure 18: 253-Ball VFBGA – 11.5mm x 11.5mm (Package Code EN)



Notes: 1. All dimensions are in millimeters.

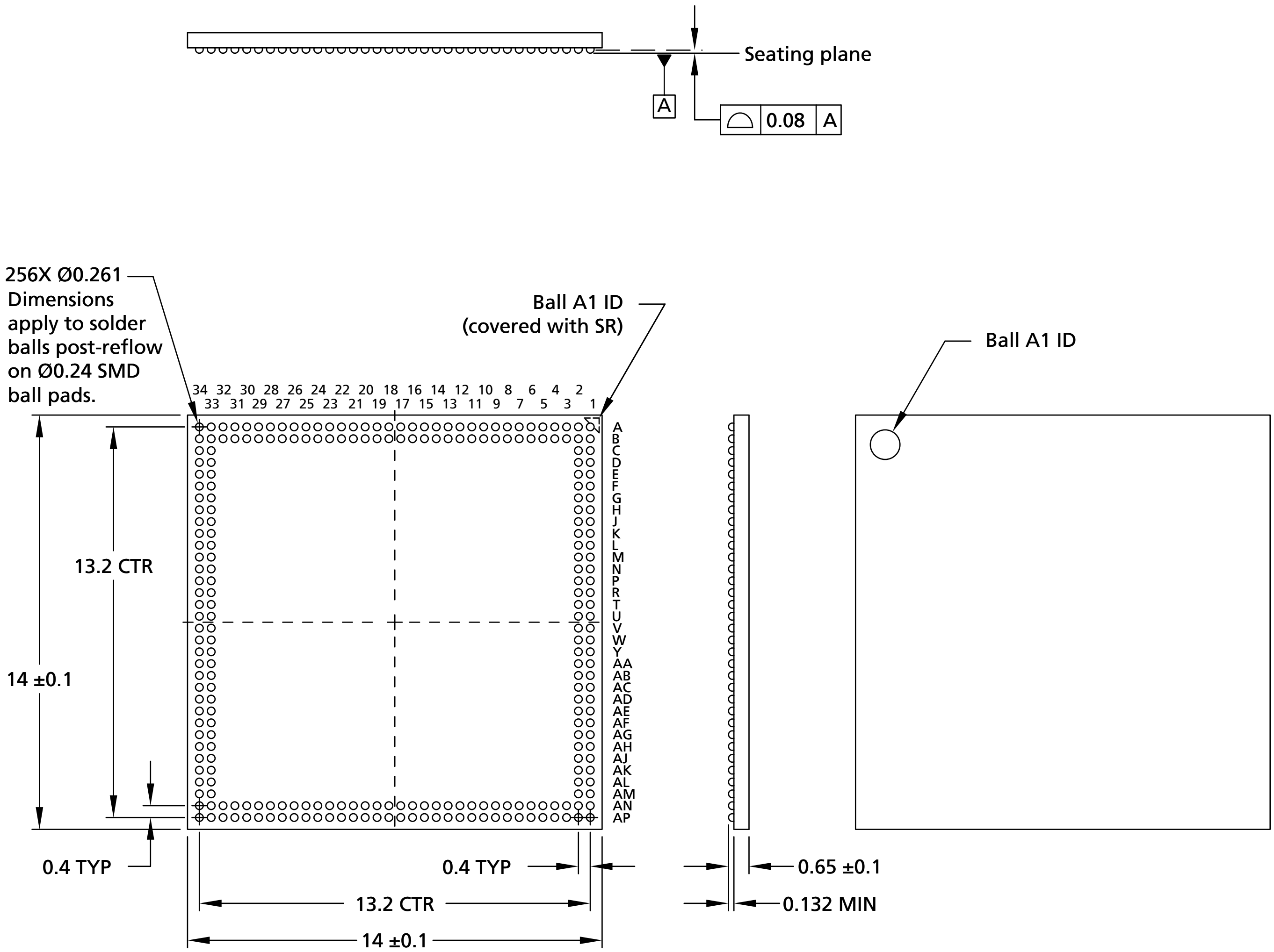
2. Solder ball composition: LF35 (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).

Figure 19: 253-Ball TFBGA – 11.5mm x 11.5mm (Package Code ER)



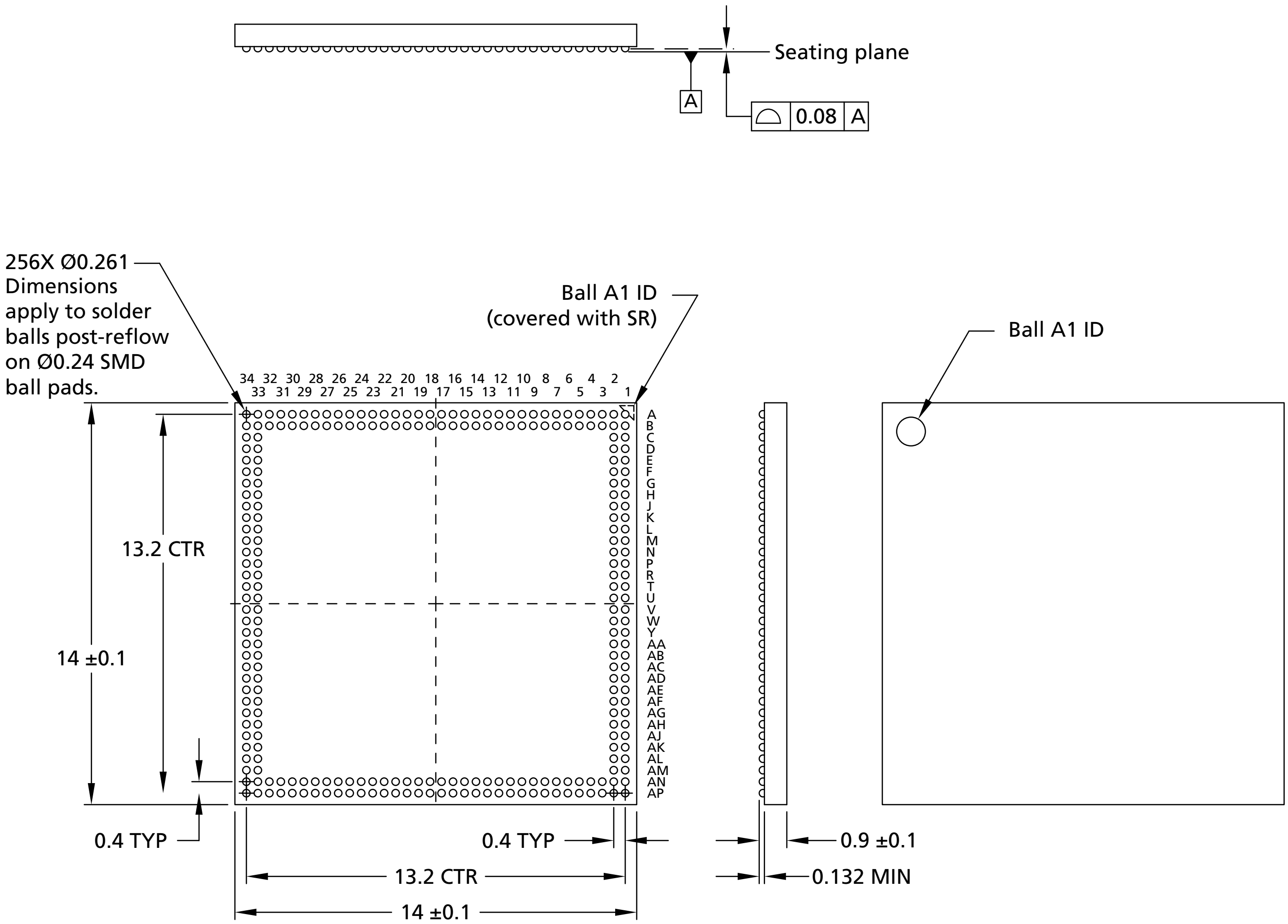
Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: LF35 (98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni).

Figure 20: 256-Ball WFBGA – 14mm x 14mm (Package Code LS)



Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 21: 256-Ball VFBGA – 14mm x 14mm (Package Code LU)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Ball Assignments

Figure 22: 178-Ball Single-Channel Discrete FBGA – 11mm x 11.5mm

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DNU	DNU	V_{DD1}	V_{DD1}	V_{DD1}	V_{DD1}		V_{DD2}	V_{DD2}	V_{DD1}	V_{DDQ}	DNU	DNU
B	DNU	V_{SS}	ZQ0	ZQ1	V_{SS}	V_{SSQ}		DQ31/ NC	DQ30/ NC	DQ29/ NC	DQ28/ NC	V_{SSQ}	DNU
C		CA9	V_{SSCA}	NC	V_{SS}	V_{SSQ}		DQ27/ NC	DQ26/ NC	DQ25/ NC	DQ24/ NC	V_{DDQ}	
D		CA8	V_{SSCA}	V_{DD2}	V_{DD2}	V_{DD2}		DM3/ NC	DQ15	DQS3/ NC	DQS3#/ NC	V_{SSQ}	
E		CA7	CA6	V_{SS}	V_{SS}	V_{SSQ}		V_{DDQ}	DQ14	DQ13	DQ12	V_{DDQ}	
F		V_{DDCA}	CA5	V_{SSCA}	V_{SS}	V_{SSQ}		DQ11	DQ10	DQ9	DQ8	V_{SSQ}	
G		V_{DDCA}	V_{SSCA}	V_{SSCA}	V_{DD2}	V_{SSQ}		DM1	V_{SSQ}	DQS1	DQS1#	V_{DDQ}	
H		V_{SS}	V_{DDCA}	V_{REFCA}	V_{DD2}	V_{DD2}		V_{DDQ}	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{DD2}	
J		CK#	CK	V_{SSCA}	V_{DD2}	V_{DD2}		ODT	V_{DDQ}	V_{DDQ}	V_{REFDQ}	V_{SS}	
K		V_{SS}	CKE0	CKE1	V_{DD2}	V_{DD2}		V_{DDQ}	NC	V_{SSQ}	V_{DDQ}	V_{DD2}	
L		V_{DDCA}	CS0#	CS1#	V_{DD2}	V_{SS}		DM0	V_{SSQ}	DQS0	DQS0#	V_{DDQ}	
M		V_{DDCA}	CA4	V_{SSCA}	V_{SS}	V_{SSQ}		DQ4	DQ5	DQ6	DQ7	V_{SSQ}	
N		CA2	CA3	V_{SS}	V_{SS}	V_{SSQ}		V_{DDQ}	DQ1	DQ2	DQ3	V_{DDQ}	
P		CA1	V_{SSCA}	V_{DD2}	V_{DD2}	V_{DD2}		DM2/ NC	DQ0	DQS2/ NC	DQS2#/ NC	V_{SSQ}	
R		CA0	NC	V_{SS}	V_{SS}	V_{SSQ}		DQ20/ NC	DQ21/ NC	DQ22/ NC	DQ23/ NC	V_{DDQ}	
T	DNU	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SSQ}		DQ16/ NC	DQ17/ NC	DQ18/ NC	DQ19/ NC	V_{SSQ}	DNU
U	DNU	DNU	V_{DD1}	V_{DD1}	V_{DD1}	V_{DD1}		V_{DD2}	V_{DD2}	V_{DD1}	V_{DDQ}	DNU	DNU

Top View (ball down)

LPDDR Supply Ground

Note: 1. For x16 devices, the upper byte DQ pins become NC.

Figure 23: 216-Ball Channel B-Only FBGA – 12mm x 12mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	V_{SS}	V_{DD2}	NC	NC	V_{SS}	NC	NC	V_{SS}	NC	V_{SS}	NC	NC	V_{SS}	V_{DD1}	V_{DD2}	NC	NC	NC	NC	NC	V_{DDQ}	NC	NC	NC	NC	NC	V_{SS}	DNU
B	V_{SS}	NC	NC	V_{DDQ}	NC	NC	V_{DDQ}	NC	V_{DDQ}	NC	NC	NC	V_{DDQ}	V_{SS}	NC	V_{DD2}	NC	V_{DDQ}	NC	NC	V_{SS}	NC	NC	V_{SS}	V_{DDQ}	NC	NC	NC	V_{SS}
C	V_{DD1}	DQ16																										V_{DD1}	V_{DD2}
D	DQ17	V_{DDQ}																										NC	V_{DDQ}
E	DQ18	DQ19																										V_{SS}	NC
F	V_{SS}	DQ20																										NC	V_{DDQ}
G	DQ21	V_{DDQ}																										NC	NC
H	DQ22	DQ23																										V_{SS}	NC
J	V_{SS}	V_{DDQ}																										V_{DDQ}	NC
K	DQS2#	DQS2																										NC	NC
L	DM2	DQ0																										NC	V_{SS}
M	DQ1	V_{SS}																										V_{DDQ}	NC
N	DQ2	V_{DD1}																										NC	NC
P	V_{SS}	V_{SS}																										V_{DD2}	V_{DD1}
R	V_{DD1}	V_{REFDQb}																										V_{SS}	CA0
T	V_{DD2}	V_{DD2}																										V_{DDCA}	CA1
U	V_{DDQ}	DQ3																										V_{REFCAb}	CA2
V	DQ4	V_{SS}																										V_{SS}	CA3
W	DQ6	DQ5																										CA4	CS1a#
Y	V_{DDQ}	DQ7																										CS0#	CKE1
AA	DQS0	DQS0#																										V_{SS}	CKE0
AB	DM0	V_{SS}																										CK	CK#
AC	V_{DDQ}	DM1																										V_{DDCA}	CA5
AD	DQS1#	DQS1																										CA7	CA6
AE	DQ8	V_{SS}																										CA8	V_{DDCA}
AF	DQ9	V_{DDQ}																										V_{SS}	CA9
AG	DQ10	DQ11																										V_{DD2}	ZQ0
AH	V_{SS}	V_{DD1}	V_{DD2}	DQ13	V_{SS}	DQ15	DM3	DQS3	V_{DDQ}	DQ26	DQ27	V_{DDQ}	DQ30	V_{SS}	V_{DD2}	NC	NC	V_{SS}	NC	NC	NC	V_{DDCA}	NC	NC	NC	NC	NC	V_{DD1}	V_{SS}
AJ	DNU	V_{SS}	DQ12	V_{DDQ}	DQ14	V_{DDQ}	V_{SS}	DQS3#	DQ24	DQ25	V_{SS}	DQ28	DQ29	DQ31	V_{DD1}	V_{SS}	ZQ1/NC[2]	NC	V_{DDCA}	NC	NC	V_{SS}	NC	NC	NC	V_{DDCA}	NC	V_{SS}	DNU

Top View (ball down)

Channel B | Supply | Ground

Notes:
1. For single-channel packages, the following balls become NC for the unused channel: CS#, CKE, CA, DQ, DQS, DQS#, DM, ODT, ZQ, V_{REFDQ}, and V_{REFCA}.
2. ZQ1 for 3DP; NC for all other configurations.

Figure 24: 216-Ball PoP Dual-Channel FBGA – 15mm x 15mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	DNU	V_{SS}	V_{DD2}	DQ30	DQ29	V_{SS}	DQ26	DQ25	V_{SS}	DQS3#	V_{SS}	DQ15	DQ13	V_{SS}	DQ11	DQ10	V_{SS}	DQ8	DM1	V_{REFDQa}	V_{SS}	V_{DDQ}	V_{SS}	DQS0	DQ7	DQ6	DQ4	V_{SS}	DNU	A
B	V_{SS}	RFU	DQ31	V_{DDQ}	DQ28	DQ27	V_{DDQ}	DQ24	V_{DDQ}	DQS3	DM3	DQ14	V_{DDQ}	DQ12	V_{DD2}	V_{DDQ}	DQ9	DQS1	DQS1#	ODT	V_{DD2}	RFU	DM0	DQS0#	V_{DDQ}	DQ5	DQ3	V_{DD1}	V_{SS}	B
C	V_{DD1}	DQ16																										DQ2	V_{DD2}	C
D	DQ17	V_{DDQ}																										DQ1	V_{DDQ}	D
E	DQ18	DQ19																										V_{SS}	DQ0	E
F	V_{SS}	DQ20																										DM2	V_{DDQ}	F
G	DQ21	V_{DDQ}																										DQS2	DQS2#	G
H	DQ22	DQ23																										V_{SS}	DQ23	H
J	V_{SS}	V_{DDQ}																										V_{DDQ}	DQ22	J
K	DQS2#	DQS2																										DQ20	DQ21	K
L	DM2	DQ0																										DQ19	V_{SS}	L
M	DQ1	V_{SS}																										V_{DDQ}	DQ18	M
N	DQ2	DQ3																										DQ16	DQ17	N
P	V_{DDQ}	V_{DD2}																										V_{DD2}	V_{DD1}	P
R	DQ4	V_{SS}																										V_{SS}	CA0	R
T	DQ6	DQ5																										V_{DDCA}	CA1	T
U	DQS0	DQ7																										V_{REFCAb}	CA2	U
V	DQS0#	DM0																										V_{SS}	CA3	V
W	V_{DDQ}	RFU																										CA4	CS1#	W
Y	V_{SS}	V_{REFDQb}																										CS0#	CKE1	Y
AA	V_{SS}	V_{DD2}																										V_{SS}	CKE0	AA
AB	V_{DD2}	ODT																										CK	CK#	AB
AC	V_{DDQ}	DM1																										V_{DDCA}	CA5	AC
AD	DQS1#	DQS1																										CA7	CA6	AD
AE	DQ8	V_{SS}																										CA8	V_{DDCA}	AE
AF	DQ9	V_{DDQ}																										V_{SS}	CA9	AF
AG	DQ10	DQ11																										RFU	ZQ	AG
AH	V_{SS}	V_{DD1}	V_{DD2}	DQ13	V_{SS}	DQ15	DM3	DQS3	V_{DDQ}	DQ26	DQ27	V_{DDQ}	DQ30	V_{SS}	V_{DD2}	V_{REFCAa}	CA9	V_{SS}	CA7	CA6	CK#	V_{DDCA}	CKE0	CS0#	CA3	CA2	CA1	V_{DD2}	V_{SS}	AH
AJ	DNU	V_{SS}	DQ12	V_{DDQ}	DQ14	V_{DDQ}	V_{SS}	DQS3#	DQ24	DQ25	V_{SS}	DQ28	DQ29	DQ31	V_{DD1}	RFU	ZQ	CA8	V_{DDCA}	CA5	CK	V_{SS}	CKE1	CS1#	CA4	V_{DDCA}	CA0	V_{SS}	DNU	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Top View (ball down)

Channel A Channel B Supply Ground

Figure 25: 253-Ball Dual-Channel Discrete FBGA – 11.5mm x 11.5mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDCA}	V_{DD2}	V_{SS}	V_{DDCA}	V_{REFCAa}	V_{DD2}	V_{SS}	V_{DDQ}	V_{SS}	V_{DD1}	V_{DD1}	NC	A
B	V_{SS}	V_{DD1}	V_{SS}	V_{SS}	CA0	CA3	CS1#	CK	V_{DDCA}	CA7	ZQ0	V_{DDQ}	DQ28	DQ29	DQ30	DQ31	V_{DD2}	B
C	V_{SS}	V_{SS}	V_{DD2}	V_{SS}	CA1	CA4	CKE0	CK#	CA5	CA8	ZQ1	V_{DDQ}	DQ24	DQ25	DQ26	DQ27	V_{DD2}	C
D	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CA2	CS0#	CKE1	RFU	CA6	CA9	RFU	V_{SS}	DQ15	DM3	DQS3#	DQS3	V_{SS}	D
E	V_{DDCA}	ZQ0	ZQ1	RFU	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DQ11	DQ12	DQ13	DQ14	V_{DDQ}	E
F	V_{SS}	CA7	CA8	CA9	V_{SS}							V_{SS}	DM1	DQ8	DQ9	DQ10	V_{SS}	F
G	V_{SS}	V_{DDCA}	CA5	CA6	V_{SS}							V_{DDQ}	DQS1#	DQS1	V_{SS}	V_{SS}	V_{DDQ}	G
H	V_{DD2}	CK#	CK	RFU	V_{SS}							V_{SS}	ODT0	DM0	V_{SS}	V_{DD2}	V_{REFDQb}	H
J	V_{REFCAb}	CS1#	CKE0	CKE1	V_{SS}							RFU	DQS0#	DQS0	DQ6	DQ7	V_{SS}	J
K	V_{DDCA}	CA3	CA4	CS0#	V_{SS}							V_{DDQ}	DQ2	DQ3	DQ4	DQ5	V_{DDQ}	K
L	V_{DD2}	CA0	CA1	CA2	V_{SS}							V_{SS}	DQ23	DM2	DQ0	DQ1	V_{DDQ}	L
M	V_{SS}	V_{DDQ}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}	RFU	V_{DDQ}	V_{SS}	V_{DDQ}	DQ21	DQ22	DQS2#	DQS2	V_{SS}	M
N	V_{DDQ}	DQ19	DQ23	DQ0	DQ4	DM0	DQS0#	ODT0	DQS1#	DQ13	DQ24	DQ25	V_{SS}	DQ18	DQ19	DQ20	V_{SS}	N
P	V_{SS}	DQ18	DQ22	DM2	DQ3	DQ7	DQS0	DM1	DQS1	DQ12	DM3	DQ26	DQ29	V_{SS}	DQ16	DQ17	V_{DDQ}	P
R	V_{DD1}	DQ17	DQ21	DQS2#	DQ2	DQ6	V_{SS}	V_{SS}	DQ9	DQ11	DQ15	DQS3#	DQ28	DQ31	V_{DD2}	V_{SS}	V_{SS}	R
T	V_{DD1}	DQ16	DQ20	DQS2	DQ1	DQ5	V_{SS}	V_{DD2}	DQ8	DQ10	DQ14	DQS3	DQ27	DQ30	V_{SS}	V_{DD1}	V_{SS}	T
U	NC	V_{DD2}	V_{DD2}	V_{SS}	V_{DDQ}	V_{SS}	V_{DDQ}	V_{REFDQa}	V_{SS}	V_{DDQ}	V_{DDQ}	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	NC	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Top View (ball down)

Channel A   Channel B   Supply   Ground

Figure 26: 256-Ball PoP FBGA – 14mm x 14mm

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
A	DNU	DNU	V_{DD2}	DQ30	DQ28	DQ27	V_{DDQ}	DQ24	DQS3	V_{DDQ}	V_{DD2}	DQ15	V_{DDQ}	DQ12	DQ11	V_{DDQ}	DQ8	DQS1	V_{DDQ}	V_{DD2}	ODT	V_{REFDQa}	V_{DDQ}	DQS0#	DQ7	V_{DDQ}	DQ4	DQ3	V_{DDQ}	DQ0	V_{DDQ}	V_{DD2}	DNU	DNU
B	DNU	V_{SS}	V_{DD1}	DQ31	DQ29	V_{SS}	DQ26	DQ25	V_{SS}	DQS3#	DM3	V_{SS}	DQ14	DQ13	V_{SS}	DQ10	DQ9	V_{SS}	DQS1#	DM1	V_{SS}	DM0	DQS0	V_{SS}	DQ6	DQ5	V_{SS}	DQ2	DQ1	V_{SS}	DM2	V_{DD1}	V_{SS}	DNU
C	V_{DD2}	V_{DD1}																															DQS2#	V_{DDQ}
D	DQ17	DQ16																															V_{SS}	DQS2
E	DQ19	DQ18																															DQ22	DQ23
F	DQ20	V_{SS}																															DQ21	V_{DDQ}
G	V_{DDQ}	DQ21																															V_{SS}	DQ20
H	DQ23	DQ22																															DQ18	DQ19
J	DQS2	V_{SS}																															DQ16	DQ17
K	V_{DDQ}	DQS2#																															V_{SS}	V_{DDQ}
L	V_{DD2}	DM2																															V_{DD1}	V_{DD2}
M	DQ0	V_{SS}																															V_{SS}	V_{SS}
N	V_{DDQ}	DQ1																															CA0	V_{DDCA}
P	DQ3	DQ2																															CA2	CA1
R	DQ4	V_{SS}																															V_{SS}	V_{DD2}
T	V_{DDQ}	DQ5																															CA4	CA3
U	DQ7	DQ6																															CS1#	CS0#
V	DQS0#	V_{SS}																															CKE1	CKE0
W	V_{DDQ}	DQS0																															V_{SS}	V_{DDCA}
Y	V_{REFDQb}	DM0																															CK#	CK
AA	ODT	V_{SS}																															V_{REFCAb}	V_{DD2}
AB	V_{DD2}	DM1																															V_{SS}	V_{DDCA}
AC	V_{DDQ}	DQS1#																															CA6	CA5
AD	DQS1	V_{SS}																															V_{SS}	CA7
AE	DQ8	DQ9																															CA8	V_{DDCA}
AF	V_{DDQ}	DQ10																															ZQ0	CA9
AG	DQ11	V_{SS}																															RFU	ZQ1
AH	DQ12	DQ13																															V_{DD1}	V_{DD2}
AJ	V_{DDQ}	DQ14																															V_{SS}	V_{SS}
AK	DQ15	V_{SS}																															DNU	DNU
AL	V_{DDQ}	DM3																															DNU	DNU
AM	V_{DD2}	V_{DD1}																															DNU	DNU
AN	DNU	V_{SS}	DQS3#	V_{SS}	DQ25	DQ26	V_{SS}	DQ29	DQ31	V_{SS}	V_{DD1}	RFU	ZQ0	CA8	V_{SS}	CA6	V_{SS}	V_{REFCAa}	CK#	V_{SS}	CKE1	CS1#	CA4	V_{SS}	CA2	CA0	V_{SS}	V_{DD1}	V_{SS}	DNU	DNU	DNU	DNU	DNU
AP	DNU	DNU	V_{DDQ}	DQS3	DQ24	V_{DDQ}	DQ27	DQ28	DQ30	V_{DDQ}	V_{DD2}	ZQ1	CA9	V_{DDCA}	CA7	CA5	V_{DDCA}	V_{DD2}	CK	V_{DDCA}	CKE0	CS0#	CA3	V_{DD2}	CA1	V_{DDCA}	V_{SS}	V_{DD2}	V_{SS}	DNU	DNU	DNU	DNU	DNU

Top View (ball down)

Channel A | Channel B | Supply | Ground

Ball Descriptions

Table 8: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK, CK#	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS#[1:0]	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0], DQS#[3:0]	I/O	**Data strobe:** Bdirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS#[3:0] is DQS for each of the four data bytes, respectively.
ODT	Input	**On-die termination:** Enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Functional Description

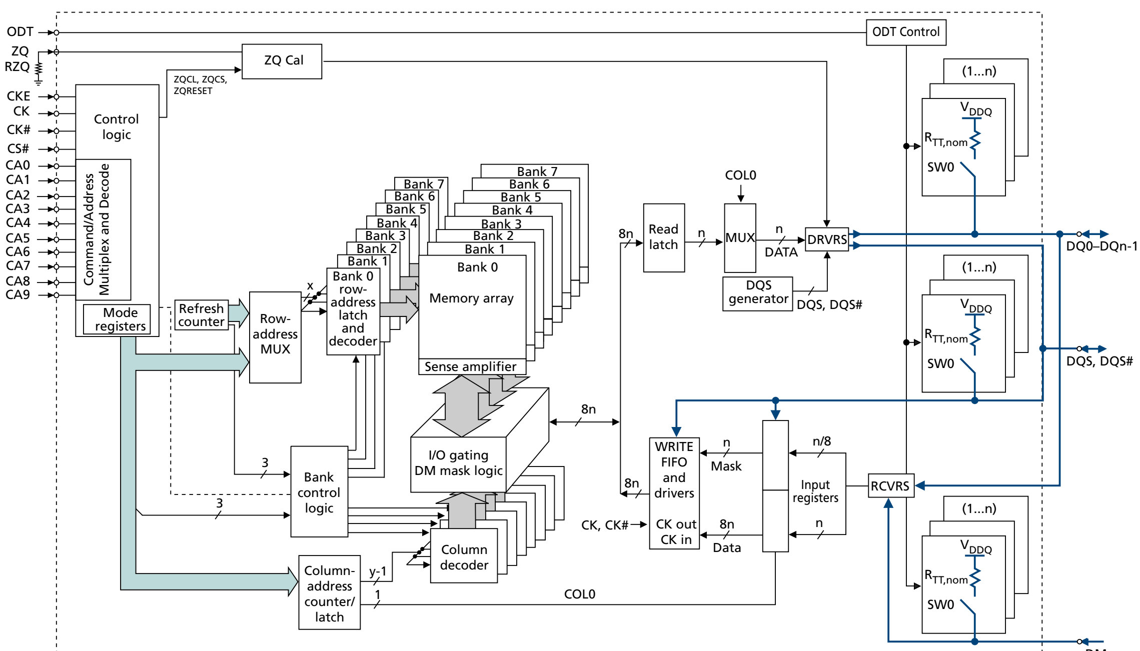
Mobile LPDDR3 is a high-speed SDRAM internally configured as an 8-bank memory device. LPDDR3 uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR3 uses a double data rate architecture on the DQ pins to achieve high- speed operation. The double data rate architecture is essentially an 8*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for LPDDR3 effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

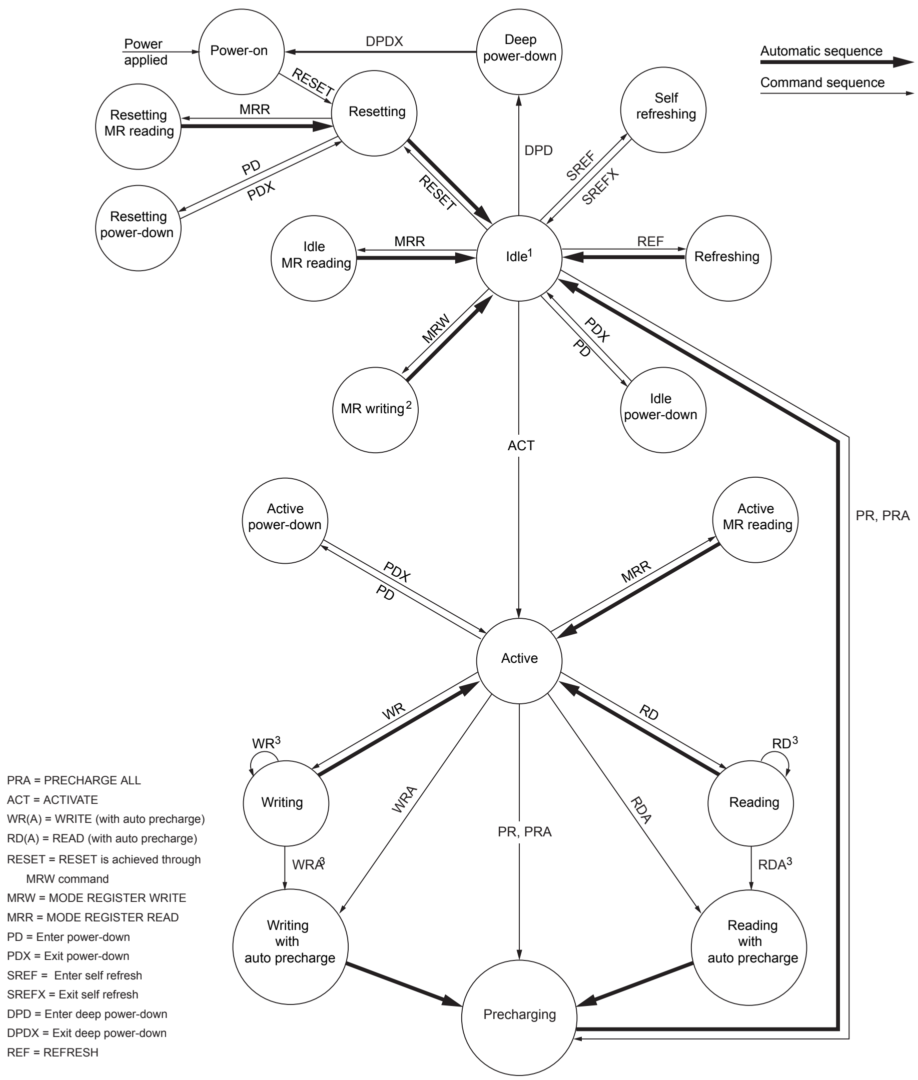
Figure 27: Functional Block Diagram



Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

Figure 28: Simplified State Diagram



Notes:
1. All banks are precharged in the idle state.
2. In the case of using MRW to enter CA training mode or write leveling mode, the state machine will not automatically return to the idle state. In these cases, an additional MRW command is required to exit either operating mode and return to the idle state. See the CA Training Mode or Write Leveling Mode sections.
3. Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before a transition can occur.

Power-Up and Initialization

The device must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp: While applying power (after Ta), CKE must be held LOW, and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

Following completion of the of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table below.

Table 9: Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2} - 200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV
	V_{REF} must always be less than all other supply voltages

Notes:
1. Ta is the point when any power supply first reaches 300mV.
2. Noted conditions apply between Ta and power-down (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
5. The voltage difference between any V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Beginning at Tb, CKE must remain LOW for at least ^{t}INIT1, after which CKE can be asserted HIGH. The clock must be stable at least ^{t}INIT2 prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (^{t}IS, ^{t}IH) with respect to the first rising clock edge and to subsequent falling and rising edges.

If any MRRs are issued, the clock period must be within the range defined for ^{t}CKb. MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least ^{t}INIT3 (Td). The ODT input signal may be in an undefined state until ^{t}IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal must be statically held either LOW or HIGH. The ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^{t}ZQINIT.

2. RESET Command: After ^{t}INIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RE-

SET command. Wait at least ^{t}INIT4 while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during ^{t}INIT4.

3. MRRs and Device Auto Initialization (DAI) Polling: After ^{t}INIT4 is satisfied (Te), only MRR commands and POWER-DOWN ENTRY/EXIT commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down). MRR commands are only valid at this time if the CA bus does not need to be trained. CA training may only begin after time Tf. Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured.

The MRR command is used to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of ^{t}INIT5 or until the DAI bit is set before proceeding.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than ^{t}INIT5 after the RESET command. The controller must wait at least ^{t}INIT5 or until the DAI bit is set before proceeding.

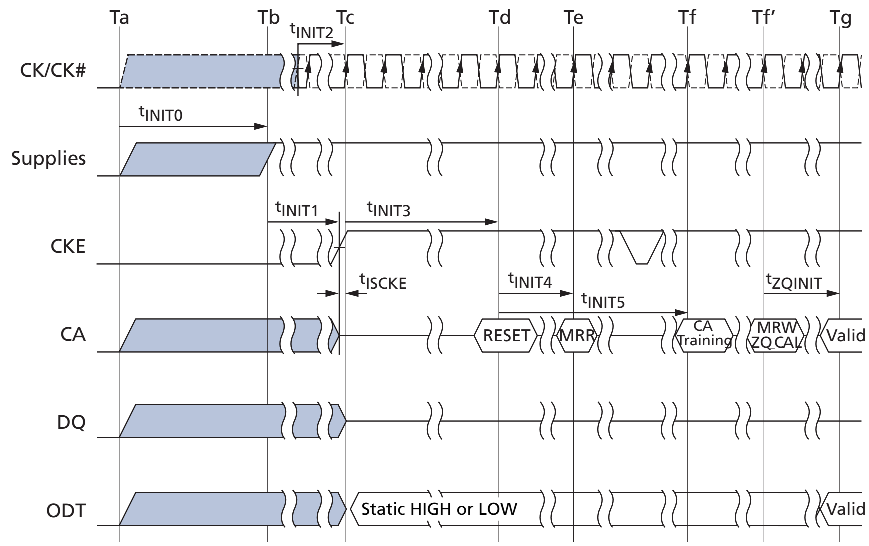
4. ZQ Calibration: If CA training is not required, the MRW INITIALIZATION CALIBRATION (ZQ_CAL) command can be issued to the memory (MR10) after Tf. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA training. After the completion of CA training (Tf'), the MRW INITIALIZATION CALIBRATION (ZQ_CAL) command can be issued to the memory.

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after ^{t}ZQINIT.

5. Normal Operation: After^{t}ZQINIT (Tg), MRW commands must be used to properly configure the memory (for example, output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the Input Clock Frequency Changes and Clock Stop Events section.

Figure 29: Voltage Ramp and Initialization Sequence



Notes: 1. High-Z on the CA bus indicates a valid NOP.
2. For ^{t}INIT values, see the Initialization Timing Parameters table.

Table 10: Initialization Timing Parameters

Note:

The ^{t}INIT0 maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding ^{t}INIT0 MAX, please contact the factory.

Parameter	Min	Max	Unit	Comment
^{t}INIT0	–	20	ms	Maximum voltage ramp time
^{t}INIT1	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
^{t}INIT2	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
^{t}INIT3	200	–	μs	Minimum idle time after first CKE assertion
^{t}INIT4	1	–	μs	Minimum idle time after RESET command
^{t}INIT5	–	10	μs	Maximum duration of device auto initialization
^{t}ZQINIT	1	–	μs	ZQ initial calibration
^{t}CKb	18	100	ns	Clock cycle time during boot

Initialization After Reset (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW; all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 11: Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2} - 200mV
	V_{DD1} must be greater than V_{DDCA} - 200mV
	V_{DD1} must be greater than V_{DDQ} - 200mV
	V_{REF} must always be less than all other supply voltages

Notes: 1. The voltage difference between any V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.
2. For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met.

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 12: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	^{t}POFF	–	2	sec

Mode Register Definition

For LPDDR3, a set of mode registers is used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. An "R" in the access column of the table indicates read-only; a "W" indicates write-only; "R/W" indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 13: Mode Register Assignments

Notes 1–5 apply to entire table

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RL3	WL-B	RFU	RZQI		RFU		DAI	Go to MR0
1	01h	Device feature 1	W	*n*WR (for AP)			RFU		BL			Go to MR1
2	02h	Device feature 2	W	WR Lev	WL Select	RFU	*n*WRE	RL and WL				Go to MR2
3	03h	I/O config-1	W	RFU				DS				Go to MR3
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate			Go to MR4
5	05h	Basic config-1	R	Manufacturer ID								Go to MR5
6	06h	Basic config-2	R	Revision ID1								Go to MR6
7	07h	Basic config-3	R	Revision ID2								Go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		Go to MR8
9	09h	Test mode	W	Vendor-specific test mode								Go to MR9
10	0Ah	I/O calibration	W	Calibration code								Go to MR10
11	0Bh	ODT	W	RFU					PD ctl	DQ ODT		Go to MR11
12–15	0Ch≈0Fh	Reserved	–	RFU								Go to MR12
16	10h	PASR_Bank	W	PASR bank mask								Go to MR16
17	11h	PASR_Seg	W	PASR segment mask								Go to MR17
18–31	12h–1Fh	Reserved	–									Go to MR18–MR30
32	20h	DQ calibration pattern A	R	See Data Calibration Pattern Description								Go to MR32
33–39	21h≈27h	Do not use	–									Go to MR33
40	28h	DQ calibration pattern B	R	See Data Calibration Pattern Description								Go to MR40
41	29h	CA training 1	W	See MRW - CA Training Mode								Go to MR41
42	2Ah	CA training 2	W	See MRW - CA Training Mode								Go to MR42
43–47	2Bh≈2Fh	Do not use	–									Go to MR43
48	30h	CA training 3	W	See MRW - CA Training Mode								
49–62	31h≈3Eh	Reserved	–	RFU								Go to MR48
63	3Fh	RESET	W	X								Go to MR63
64–255	40h≈FFh	Reserved	–	RFU								Go to MR64

Notes: 1. RFU bits must be set to 0 during MRW.
2. RFU bits must be read as 0 during MRR.

3. For READs to a write-only or RFU register, DQS is toggled and undefined data is returned.
4. RFU mode registers must not be written.
5. WRITEs to read-only registers must have no impact on the functionality of the device.

Table 14: MR0 Device Feature 0 (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL-B	RFU	RZQI		RFU		DAI

Table 15: MR0 Op-Code BIt Definitions

Register Information	Tag	Type	OP	Definition
Device auto initialization status	DAI	Read-only	OP0	0b: DAI complete 1b: DAI in progress
Built-in self-test for RZQ information	RZQI[1]	Read-only	OP[4:3]	00b: RZQ self-test not supported 01b: ZQ pin can connect to V_{DDCA} or float 10b: ZQ pin can short to GND 11b: ZQ pin self-test completed, no error condition detected (ZQ pin must not float; connect to V_{DD} or short to GND
WL Set B option support	WL-B	Read-only	OP[6]	0b: Device does not support WL Set B 1b: Device supports WL Set B
RL3 option support	RL3	Read-only	OP[7]	0b: Device does not support RL= 3, *n*WR = 3, WL = 1 1b: Device supports RL = 3, *n*WR = 3, WL = 1 for frequencies ≤166 MHz

Notes:
1. RZQI will be set upon completion of the MRW ZQ INITIALIZATION CALIBRATION command.
2. If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3] = 01 or OP[4:3] = 10 might indicate a ZQ pin asSembly error.
3. In the case of a possible assembly error, the device will default to factory trim settings for R_{ON} and will ignore ZQ CALIBRATION commands. In either case, the system may not function as intended.
4. If the ZQ self-test returns a value of 11b, it indicates that the device has detected a resistor connection to the ZQ pin. However, that result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limit of 240Ω ±1%.

Table 16: MR1 Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
*n*WR (for AP)			RFU		BL		

Table 17: MR1 Op-Code Bit Definitions

Feature	Type	OP	Definition	Notes
BL	Write-only	OP[2:0]	011b: BL8 (default) All others: Reserved	
*n*WR	Write-only	OP[7:5]	If *n*WR (MR2 OP[4]) = 0 001b: *n*WR = 3 100b: *n*WR = 6 110b: *n*WR = 8 111b: *n*WR = 9 If *n*WR (MR2 OP[4]) = 1 000b: *n*WR = 10 (default) 001b: *n*WR = 11 010b: *n*WR = 12 All others: Reserved	1

Note: 1. The programmed value in the *n*WR register is the number of clock cycles that determine when to start the internal precharge operation for a WRITE burst with AP enabled. It is determined by RU (^{t}WR/^{t}CK).

Table 18: Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0b	0b	0b	8	0	1	2	3	4	5	6	7
0b	1b	0b		2	3	4	5	6	7	0	1
1b	0b	0b		4	5	6	7	0	1	2	3
1b	1b	0b		6	7	0	1	2	3	4	5

Note: 1. C0 input is not present on CA bus; it is implied zero.

Table 19: MR2 Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Sel	RFU	*n*WRE	RL and WL			

Table 20: MR2 Op-Code Bit Definitions

Feature	Type	OP	Definition
RL and WL	Write-only	OP[3:0]	If OP[6] = 0 (default, WL Set A)
			0001b: RL3/WL1 (≤166 MHz) 0100b: RL6/WL3 (≤400 MHz) 0110b: RL8/WL4 (≤533 MHz) 0111b: RL9/WL5 (≤600 MHz) 1000b: RL10/WL6 (≤667 MHz, default) 1001b: RL11/WL6 (≤733 MHz) 1010b: RL12/WL6 (≤800 MHz) All others: Reserved If OP[6] = 1 (WL Set B) 0001b: RL3/WL1 (≤166 MHz) 0100b: RL6/WL3 (≤400 MHz) 0110b: RL8/WL4 (≤533 MHz) 0111b: RL9/WL5 (≤600 MHz) 1000b: RL10/WL8 (≤667 MHz, default) 1001b: RL11/WL9 (≤733 MHz) 1010b: RL12/WL9 (≤800 MHz) All others: Reserved
*n*WRE	Write-only	OP[4]	0b: Enable *n*WRE programming ≤9
			1b: Enable *n*WRE programming >9 (default)
WL select	Write-only	OP[6]	0b: Use WL Set A (default)
			1b: Use WL Set B
WR Lev	Write-only	OP[7]	0b: Disable write leveling (default)
			1b: Enable write leveling

Table 21: MR3 I/O Configuration 1 (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

Table 22: MR3 Op-Code Bit Definitions

Feature	Type	OP	Definition
DS	Write-only	OP[3:0]	0001b: 34.3Ω typical 0010b: 40Ω typical (default) 0011b: 48Ω typical 0100b: Reserved for 60Ω typical 0110b: Reserved for 80Ω typical 1001b: 34.3Ω pull-down, 40Ω pull-up (240Ω termination) 1010b: 40Ω pull-down, 48Ω pull-up (240Ω termination) 1011b: 34.3Ω pull-down, 48Ω pull-up (120Ω termination) All others: Reserved

Table 23: MR4 Device Temperature (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM refresh rate		

Table 24: MR4 Op-Code Bit Definitions

Notes 1–8 apply to entire table

Feature	Type	OP	Definition
SDRAM refresh rate	Read-only	OP[2:0]	000b: SDRAM low temperature operating limit exceeded 001b: 4 × ^{t}REFI, 4 × ^{t}REFIpb, 4 × ^{t}REFW 010b: 2 × ^{t}REFI, 2 × ^{t}REFIpb, 2 × ^{t}REFW 011b: 1 × ^{t}REFI, 1 × ^{t}REFIpb, 1 × ^{t}REFW (≤85˚C) 100b: Reserved 101b: 0.25 × ^{t}REFI, 0.25 × ^{t}REFIpb, 0.25 × ^{t}REFW, no AC timing derating 110b: 0.25 × ^{t}REFI, 0.25 × ^{t}REFIpb, 0.25 × ^{t}REFW, timing derating required 111b: SDRAM high-temperature operating limit exceeded
Temperature update flag (TUF)	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4 1b: OP[2:0] value has changed since last read of MR4

Notes:
1. A mode register read from MR4 will reset OP7 to 0.
2. OP7 is reset to 0 at power-up.
3. If OP2 = 1, the device temperature is greater than 85˚C.
4. OP7 is set to 1 if OP[2:0] has changed at any time since the last MR4 read.
5. The device might not operate properly when OP[2:0] = 000b or 111b.
6. For the specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.
7. LPDDR3 devices must be derated by adding 1.875ns to the following core timing parameters: ^{t}RCD, ^{t}RC, ^{t}RAS, ^{t}RP, and ^{t}RRD. The ^{t}DQSCK parameter must be derated as specified in the AC Timing table. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in the Temperature Sensor section.

Table 25: MR5 Basic Configuration 1 (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 26: MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b: Micron
			All others: Reserved

Table 27: MR6 Basic Configuration 2 (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Note: 1. MR6 is vendor-specific.

Table 28: MR6 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID1	Read-only	OP[7:0]	0000 0000b: Die revision A

Table 29: MR7 Basic Configuration 3 (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Table 30: MR7 Op-Code Bit Definitions

Feature	Type	OP	Definition
Revision ID2	Read-only	OP[7:0]	0000 0000b: Die revision A

Note: 1. MR7 is vendor-specific.

Table 31: MR8 Basic Configuration 4 (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 32: MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	11b: LPDDR3 All other states reserved

Table 32: MR8 Op-Code Bit Definitions (Continued)

Feature	Type	OP	Definition
Density	Read-only	OP[5:2]	0110b: 4Gb 0111b: 8Gb 1000b: 16Gb 1001b: 32Gb All others: Reserved
I/O width	Read-only	OP[7:6]	00b: x32 01b: x16 All others: Reserved

Table 33: MR9 Test Mode (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific test mode							

Table 34: MR10 Calibration (MA[7:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration code							

Table 35: MR10 Op-Code Bit Definitions

Notes 1–4 apply to entire table

Feature	Type	OP	Definition
Calibration code	Write-only	OP[7:0]	0xFF: CALIBRATION command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ reset All others: Reserved

Notes:
1. The device ignores calibration commands when a reserved value is written into MR10.
2. See AC Timing table for the calibration latency.
3. If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see MRW ZQ CALIBRATION Command) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
4. Devices that do not support calibration ignore the ZQ CALIBRATION command.

Table 36: MR[11] ODT Control (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved					PD CTL	DQ ODT	

Table 37: MR11 Op-Code Bit Definitions

Feature	Type	OP	Definition
DQ ODT	Write-only	OP[1:0]	00b: Disable (default) 01b: Reserved 10b: RZQ/2 11b: RZQ/1
PD control	Write-only	OP[2]	00b: ODT disabled by DRAM during power-down (default) 01b: ODT enabled by DRAM during power-down

Table 38: MR[12:15] Reserved (MA[7:0] = 0Ch–0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved							

Table 39: MR16 PASR Bank Mask (MA[7:0] = 010h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR bank mask							

Table 40: MR16 Op-Code Bit Definitions

Feature	Type	OP	Definition
Bank[7:0] mask	Write-only	OP[7:0]	0b: Refresh enable to the bank = unmasked (default) 1b: Refresh blocked = masked

Table 41: MR17 PASR Segment Mask (MA[7:0] = 011h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR segment mask							

Table 42: MR17 PASR Segment Mask Definitions

Feature	Type	OP	Definition
Segment[7:0] mask	Write-only	OP[7:0]	0b: Refresh enable to the segment = unmasked (default)
			1b: Refresh blocked = masked

Table 43: MR17 PASR Row Address Ranges in Masked Segments

Segment	OP	Segment Mask	4Gb	8Gb/16Gb	32Gb
			R[13:11]	R[14:12]	TBD
0	0	XXXXXXX1	000b		

Table 43: MR17 PASR Row Address Ranges in Masked Segments (Continued)

Segment	OP	Segment Mask	4Gb R[13:11]	8Gb/16Gb R[14:12]	32Gb TBD
1	1	XXXXXX1X	001b		
2	2	XXXXX1XX	010b		
3	3	XXXX1XXX	011b		
4	4	XXX1XXXX	100b		
5	5	XX1XXXXX	101b		
6	6	X1XXXXXX	110b		
7	7	1XXXXXXX	111b		

Note: 1. X = "Don't Care" for the designated segment.

Table 44: MR63 RESET (MA[7:0] = 3Fh) – MRW Only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFCh							

Note: 1. For additional information on MRW RESET, see the Mode Register Write (MRW) section.

Table 45: Reserved Mode Registers

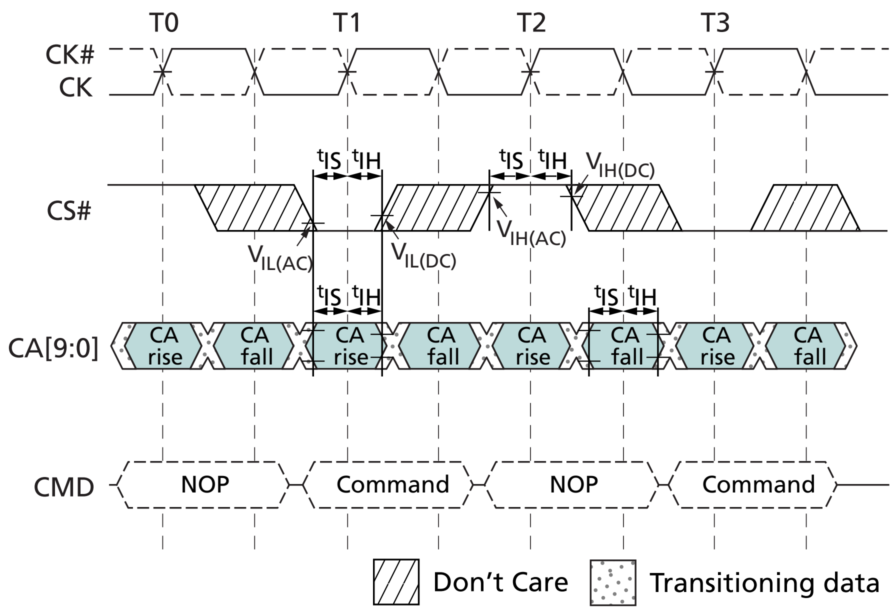
Mode Register	MA	Address	Restriction	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR[12:15]	MA[7:0]	0Bh-0Fh	Reserved	Reserved							
MR[18:31]		12h–1Fh	Reserved								
MR32		20h	DQ calibration pattern A								
MR[33:39]		21h–27h	DNU								
MR40		28h	DQ calibration pattern B								
MR41		29h	CA training 1								
MR42		2Ah	CA training 2								
MR[43:47]		2Bh–2Fh	DNU								
MR48		30h	CA training 3								
MR[49:62]		31h–3Eh	Reserved								
MR[64:255]		40h–FFh	Reserved								

Note: 1. DNU = Do not use; RVU = Reserved for vendor use.

Commands and Timing

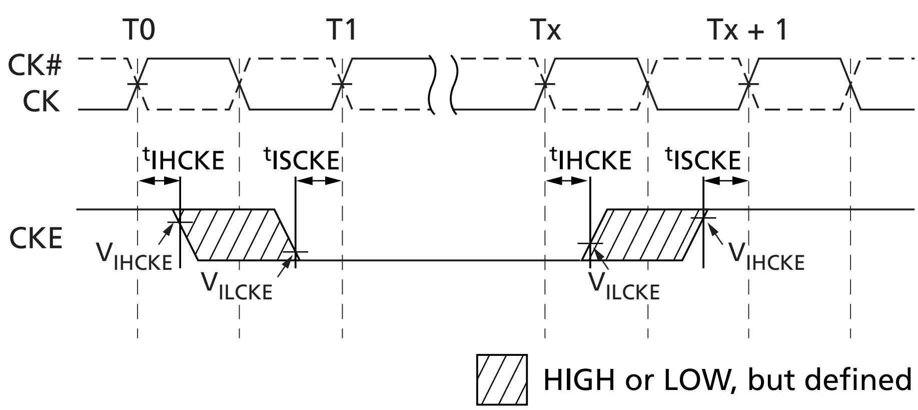
The setup and hold timings, shown in the figures below, apply for all commands.

Figure 30: Command and Input Setup and Hold



Note: 1. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see the Power-Down section.

Figure 31: CKE Input Setup and Hold



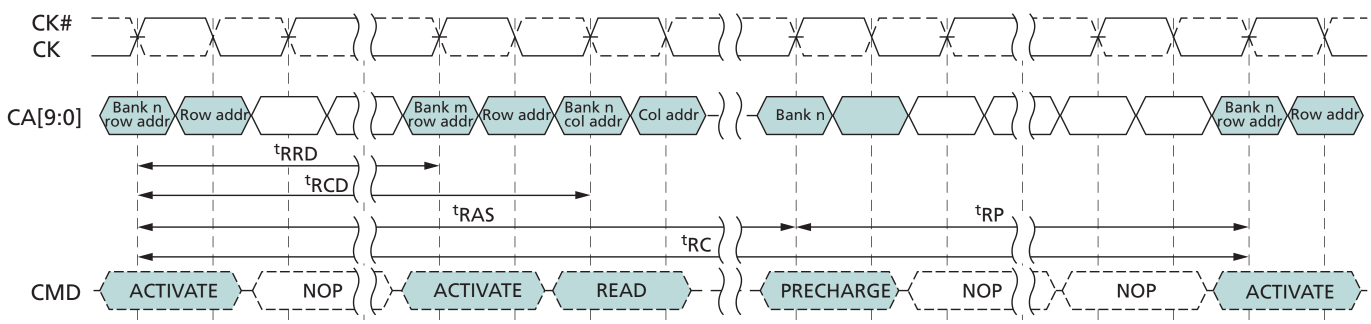
Notes: 1. After CKE is registered LOW, the CKE signal level is maintained below V_{ILCKE} for ^tCKE specification (LOW pulse width).

2. After CKE is registered HIGH, the CKE signal level is maintained above V_{IHCKE} for ^tCKE (HIGH pulse width).

ACTIVATE

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at ^{t}RCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (^{t}RC). The minimum time interval between ACTIVATE commands to different banks is ^{t}RRD.

Figure 32: ACTIVATE Command



Note: 1. A PRECHARGE ALL command uses ^{t}RPab timing, and a single-bank PRECHARGE command uses ^{t}RPpb timing. In this figure, ^{t}RP denotes either an all-bank PRECHARGE or a single-bank PRECHARGE.

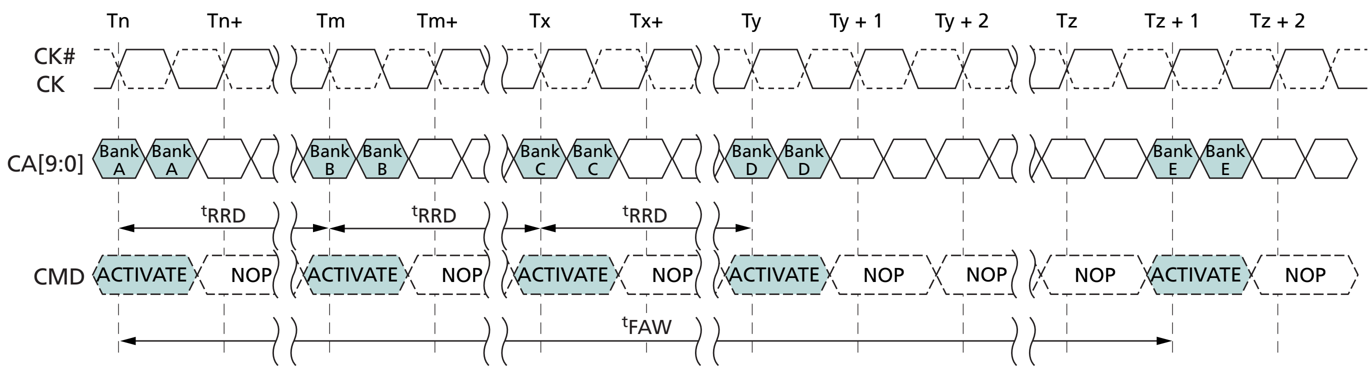
8-Bank Device Operation

Certain restrictions must be taken into consideration when operating 8-bank devices; one restricts the number of sequential ACTIVATE commands that can be issued and one provides additional RAS precharge time for a PRECHARGE ALL command.

The 8-Bank Device Sequential Bank Activation Restriction: No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling ^{t}FAW window. The number of clocks in a ^{t}FAW period depends on the clock frequency, which may vary. If the clock frequency is not changed over this period, convert to clocks by dividing ^{t}FAW[ns] by ^{t}CK[ns] and then rounding up to the next integer value. As an example of the rolling window, if RU(^{t}FAW/^{t}CK) is 10 clocks, and an ACTIVATE command is issued in clock *n*, no more than three further ACTIVATE commands can be issued at or between clock $n + 1$ and $n + 9$. REFpb also counts as bank activation for purposes of ^{t}FAW. If the clock is changed during the ^{t}FAW period, the rolling ^{t}FAW window may be calculated in clock cycles by adding together the time spent in each clock period. The ^{t}FAW requirement is met when the previous *n* clock cycles exceeds the ^{t}FAW time.

The 8-Bank Device PRECHARGE ALL Provision: ^{t}RP for a PRECHARGE ALL command must equal ^{t}RPab, which is greater than ^{t}RPpb.

Figure 33: ^{t}FAW Timing



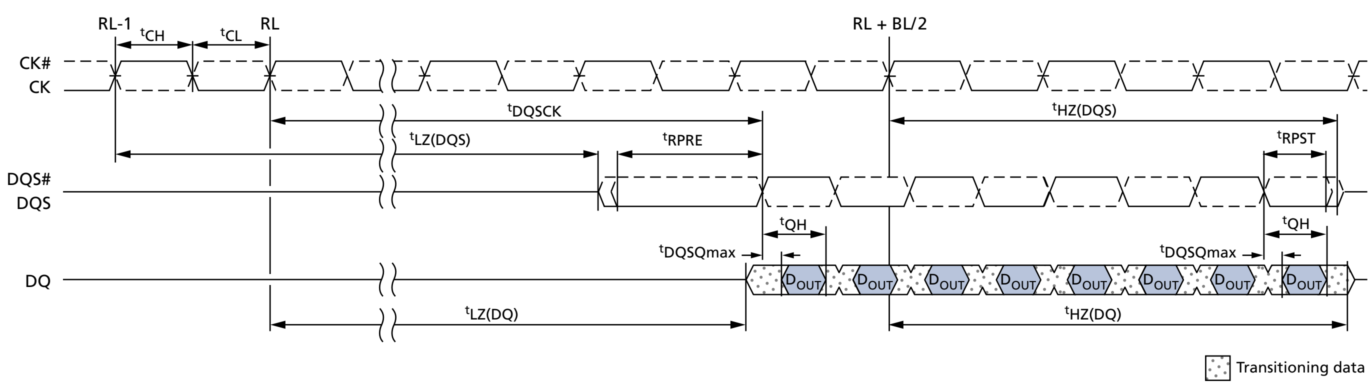
Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles. Burst interrupts are not allowed.

Burst READ Command

The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid data is available RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW ^{t}RPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 34: READ Output Timing



Note: 1. ^{t}DQSCK can span multiple clock periods.

Figure 35: Burst READ – RL = 12, BL = 8, ^{t}DQSCK > ^{t}CK

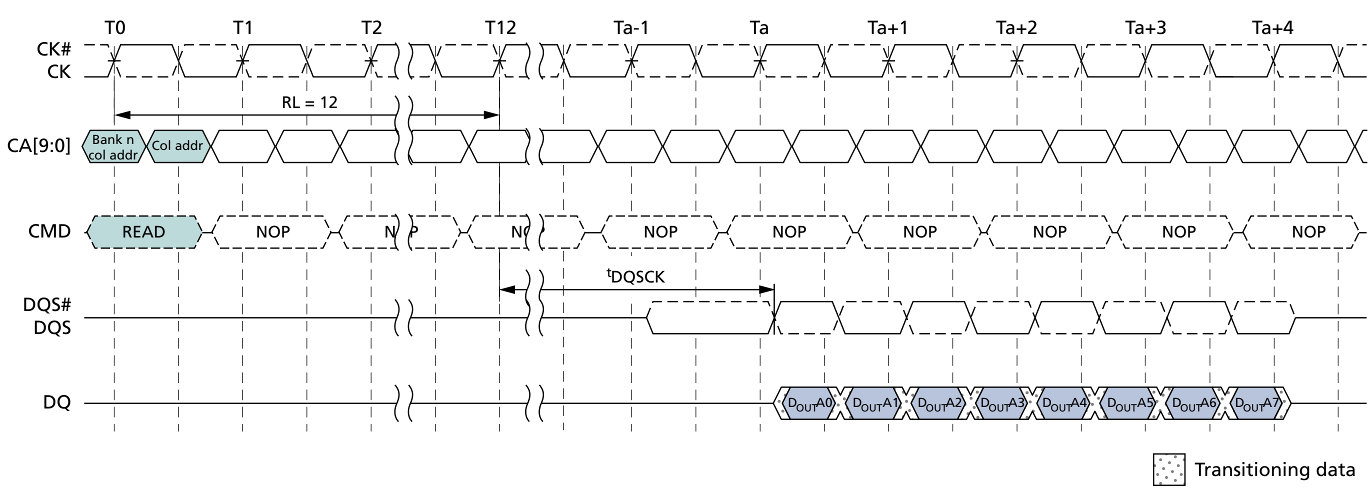


Figure 36: Burst READ – RL = 12, BL = 8, $^tDQSCK < ^tCK$

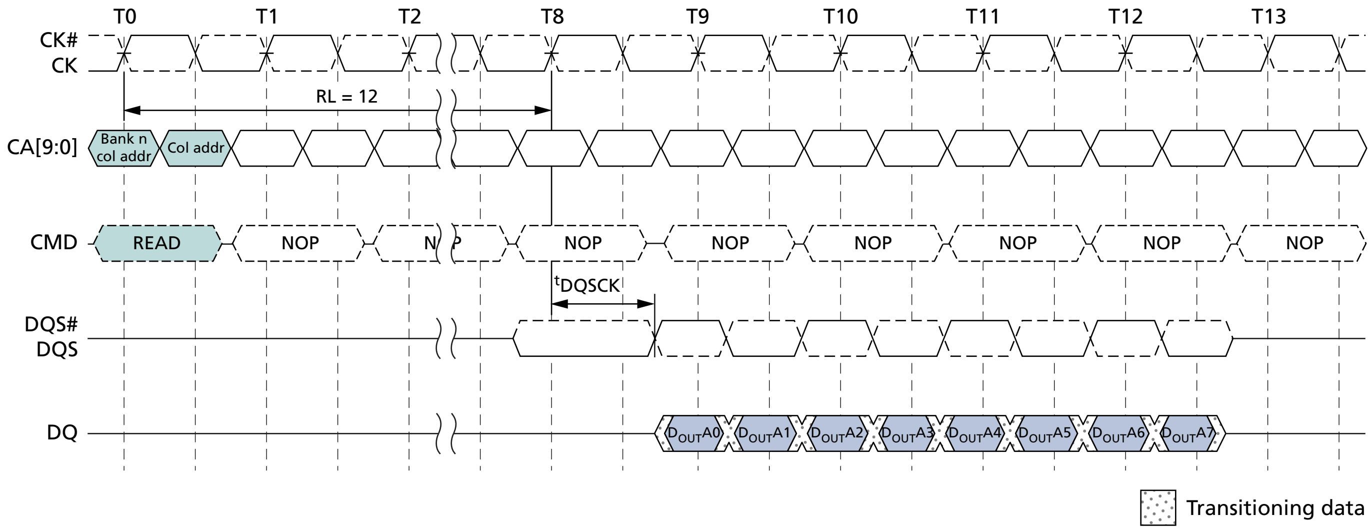
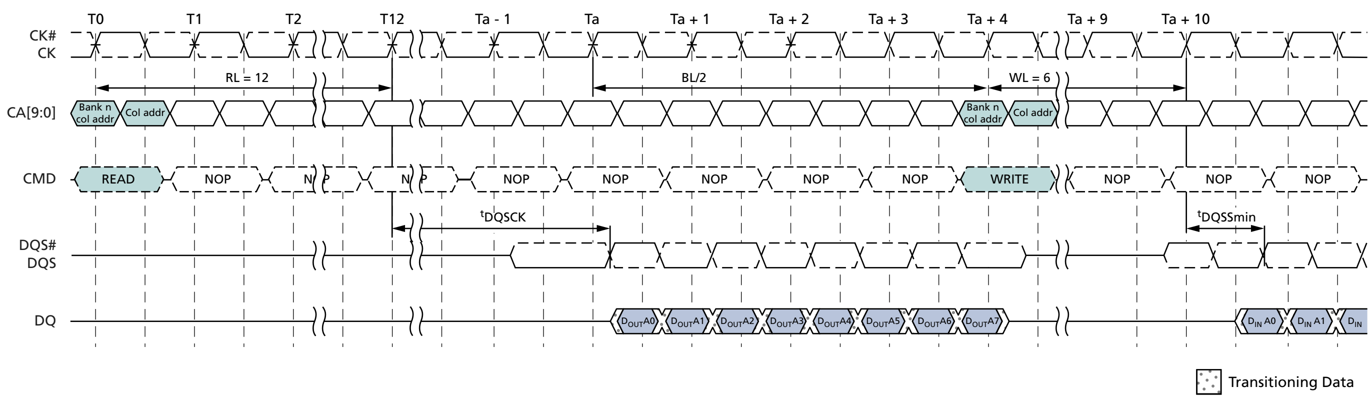
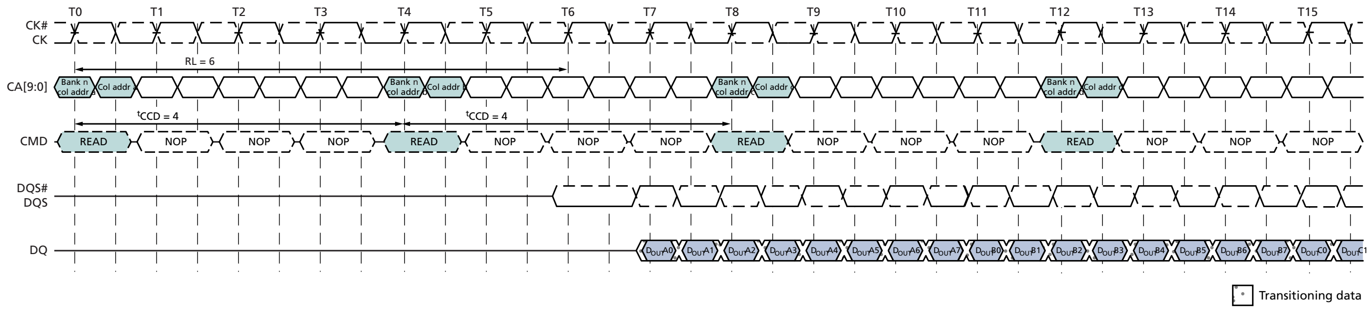


Figure 37: Burst READ Followed by Burst WRITE – RL = 12, WL = 6, BL = 8



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU($^tDQSCK(MAX)/^tCK$) + BL/2 + 1 - WL clock cycles.

Figure 38: Seamless Burst READ – RL = 6, BL = 8, ^{t}CCD = 4

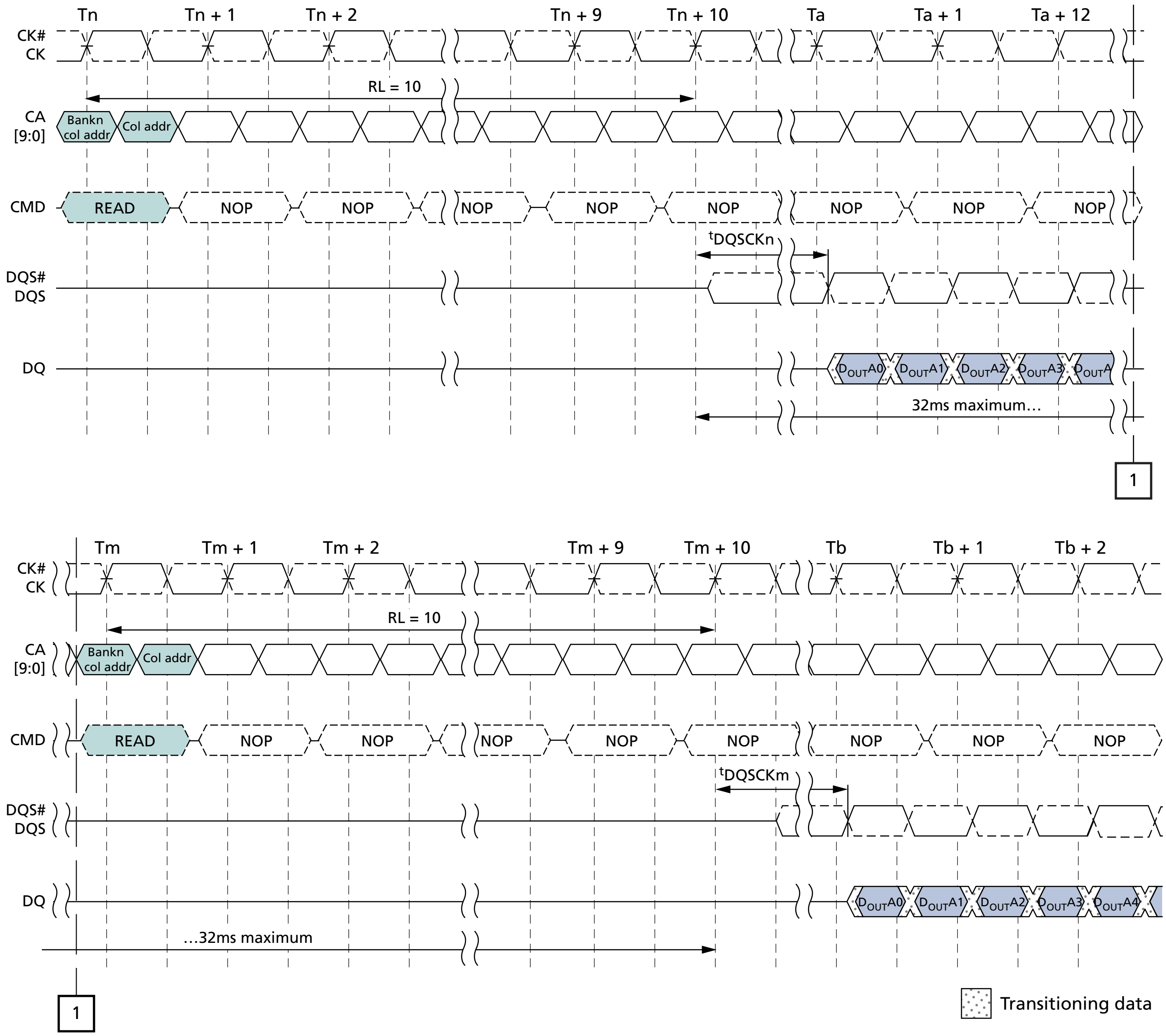


The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

^{t}DQSCK Delta Timing

To allow the system to track variations in ^{t}DQSCK output across multiple clock cycles, three parameters are provided: ^{t}DQSCKDL (delta long), ^{t}DQSCKDM (delta medium), and ^{t}DQSCKDS (delta short). Each of these parameters defines the change in ^{t}DQSCK over a short, medium, or long rolling window, respectively. The definition for each ^{t}DQSCK-delta parameter is shown in the figures below.

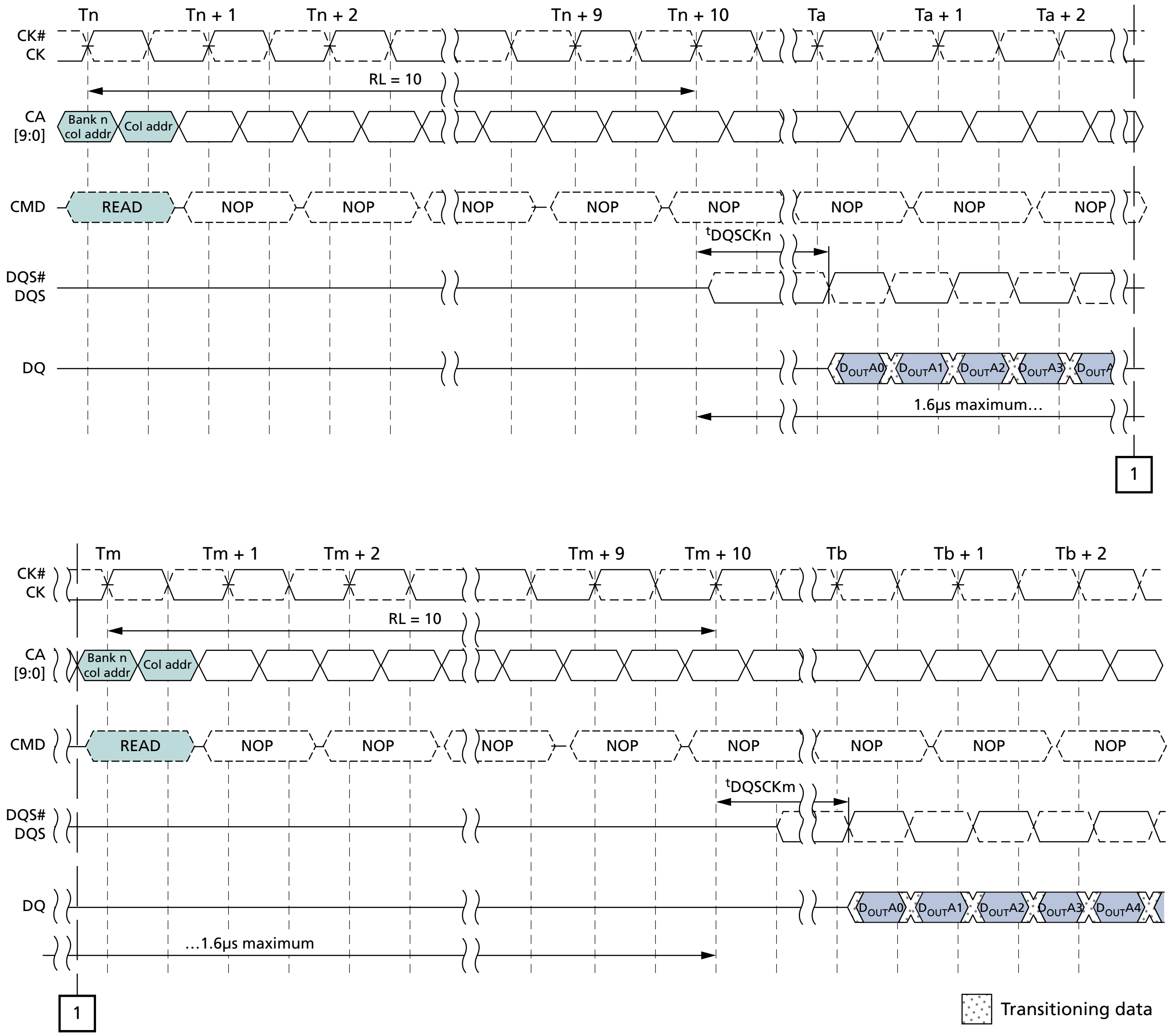
Figure 39: ^{t}DQSCKDL Timing



Notes: 1. ^{t}DQSCKDL = (^{t}DQSCKn - ^{t}DQSCKm).

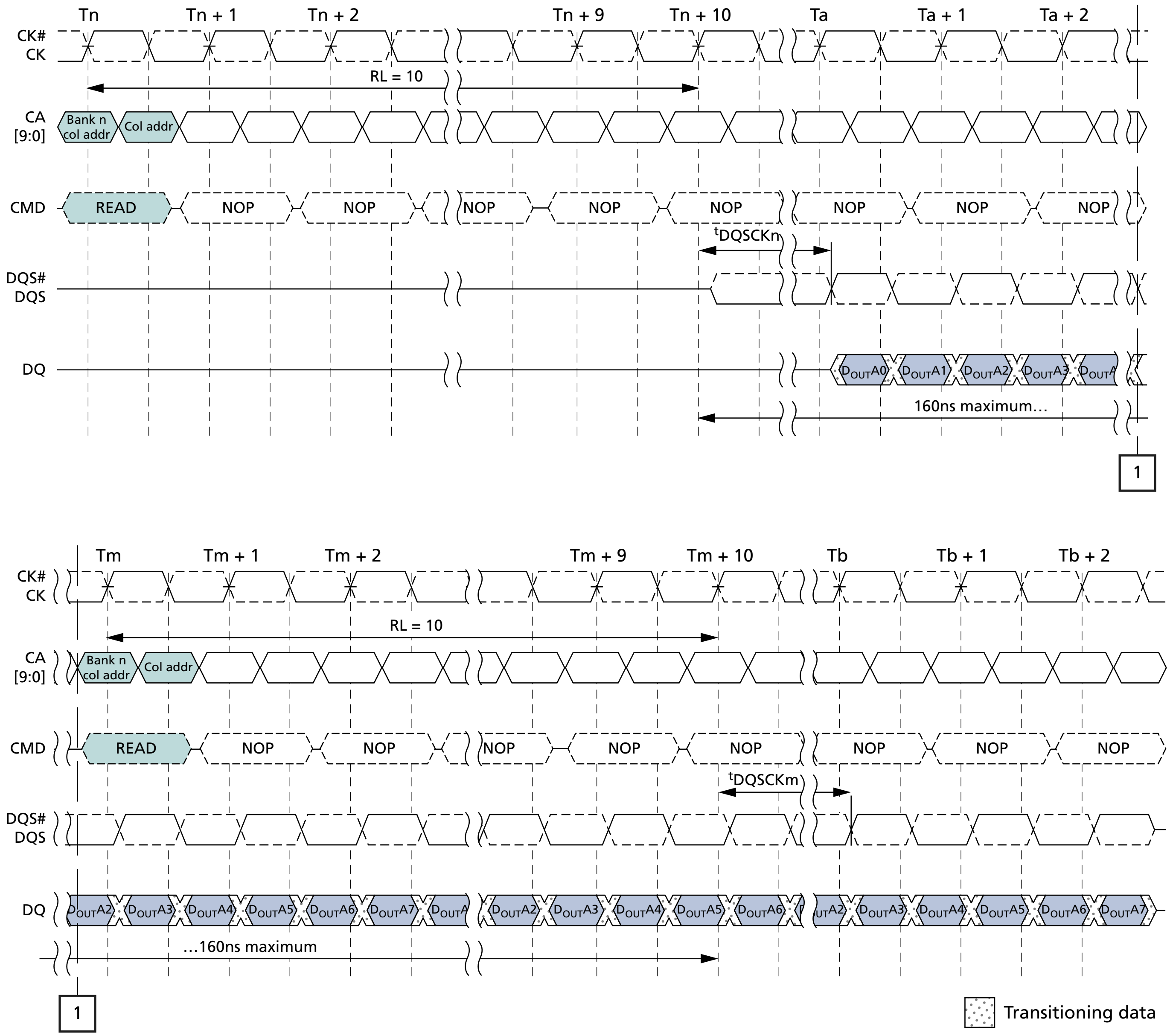
2. ^{t}DQSCKDL (MAX) is defined as the maximum of ABS (^{t}DQSCKn - ^{t}DQSCKm) for any (^{t}DQSCKn, ^{t}DQSCKm) pair within any 32ms rolling window.

Figure 40: ^{t}DQSCKDM Timing



Notes:
1. ^{t}DQSCKDM = (^{t}DQSCK*n* - ^{t}DQSCK*m*).
2. ^{t}DQSCKDM (MAX) is defined as the maximum of ABS (^{t}DQSCK*n* - ^{t}DQSCK*m*) for any (^{t}DQSCK*n*, ^{t}DQSCK*m*) pair within any 1.6µs rolling window.

Figure 41: ^{t}DQSCKDS Timing



Notes:
1. ^{t}DQSCKDS = (^{t}DQSCK*n* - ^{t}DQSCK*m*).
2. ^{t}DQSCKDS (MAX) is defined as the maximum of ABS (^{t}DQSCK*n* - ^{t}DQSCK*m*) for any (^{t}DQSCK*n*, ^{t}DQSCK*m*) pair for READs within a consecutive burst, within any 160ns rolling window.

Burst WRITE Command

The burst WRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the ^{t}DQSS delay is measured. The first valid data must be driven WL × ^{t}CK + ^{t}DQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signals (DQS/DQS#) must be driven as shown in Figure 44 (page 68). The burst cycle data bits must be applied to the DQ pins ^{t}DS prior to the associated edge of the DQS and held valid until ^{t}DH after that edge. Burst data is sampled on successive edges of the DQS until the burst length is completed. After a burst WRITE operation, ^{t}WR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 42: Data Input (WRITE) Timing

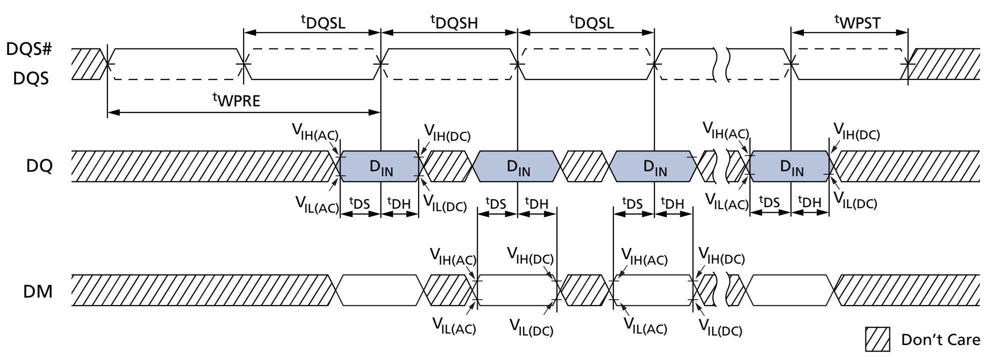


Figure 43: Burst WRITE

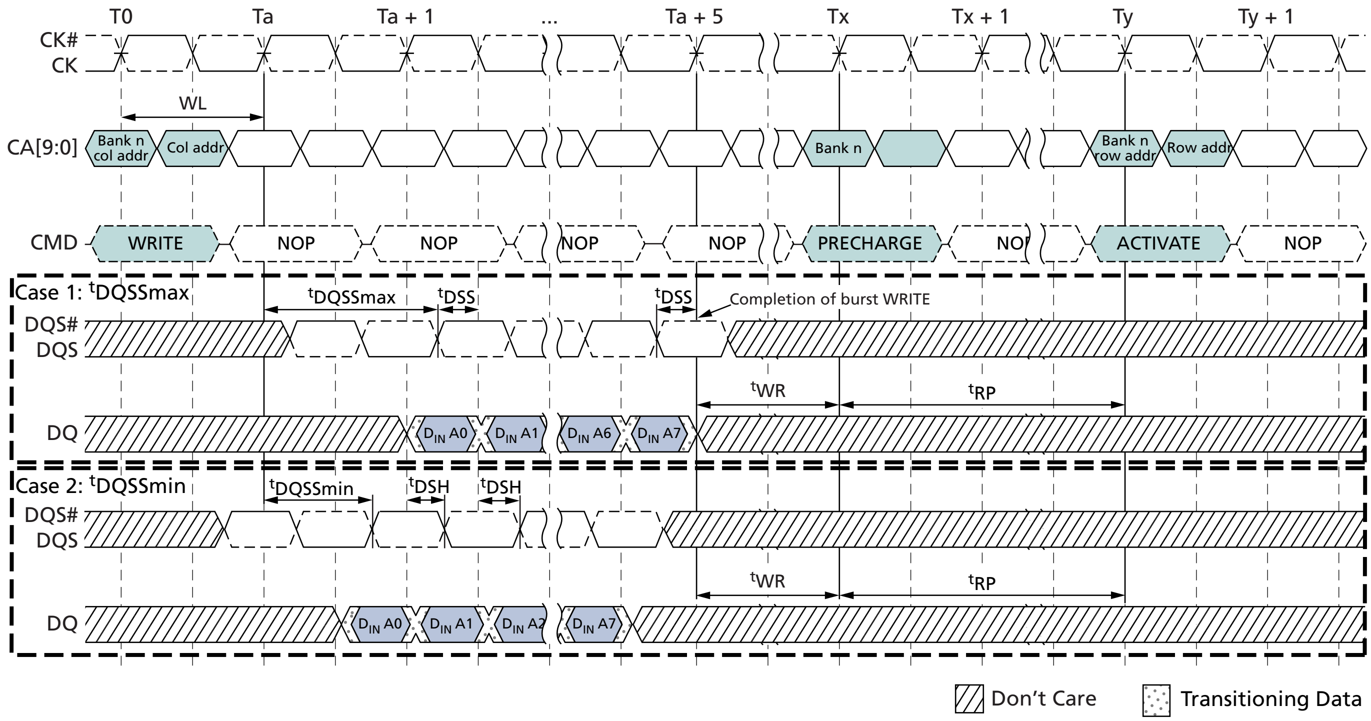


Figure 44: Method for Calculating ^{t}WPRE Transitions and Endpoints

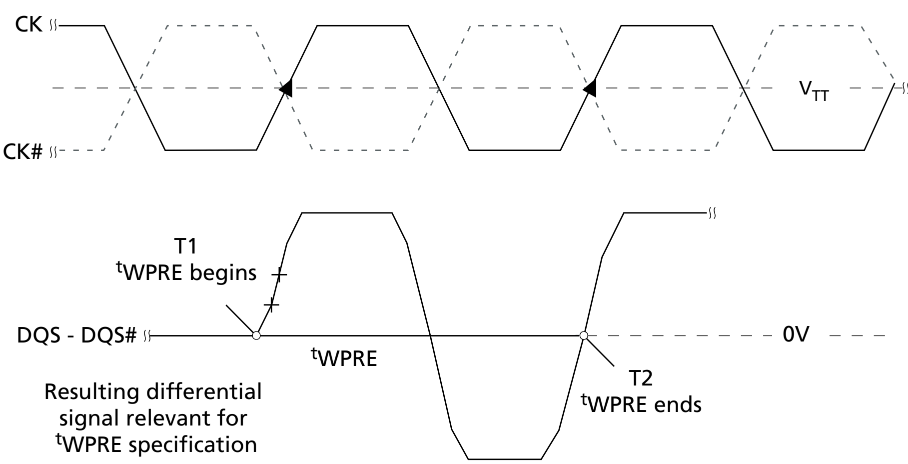


Figure 45: Method for Calculating ^tWPST Transitions and Endpoints

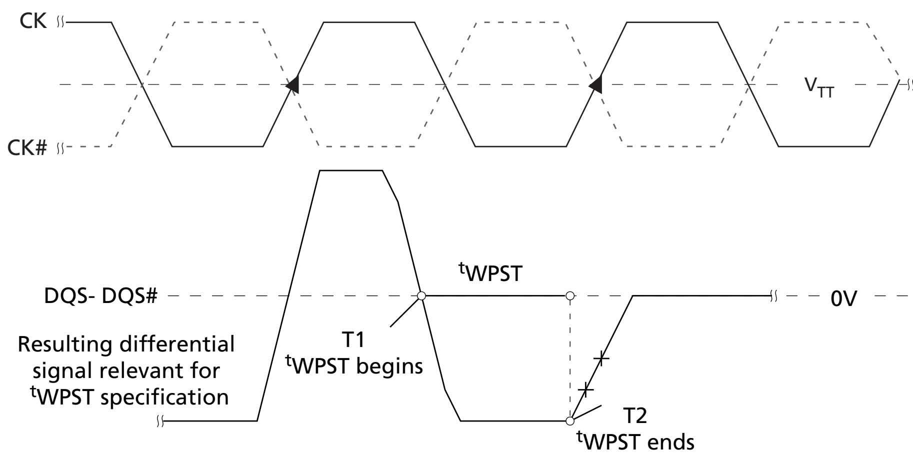
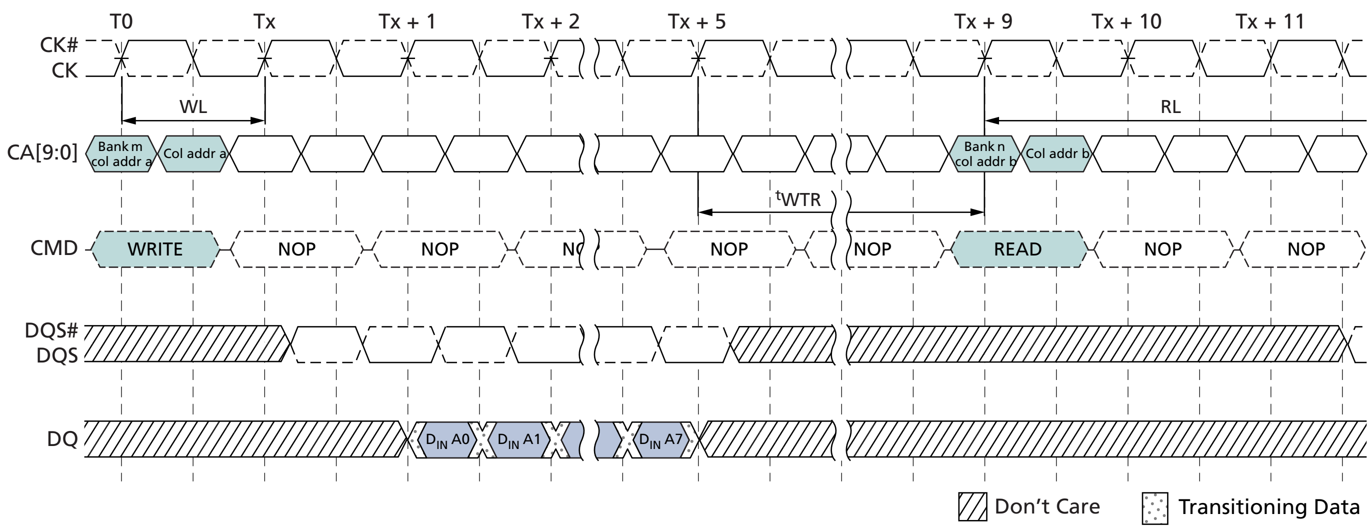
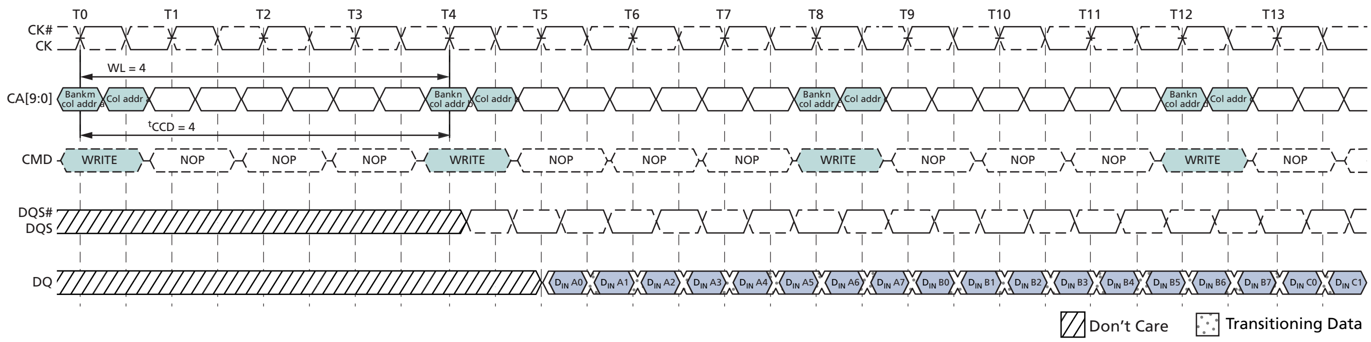


Figure 46: Burst WRITE Followed by Burst READ



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU($^tWTR/^tCK$)].
2. ^tWTR starts at the rising edge of the clock after the last valid input data.

Figure 47: Seamless Burst WRITE – WL = 4, BL = 8, ^tCCD = 4



Note: 1. The seamless burst WRITE operation is supported by enabling a WRITE command every four clocks for BL = 8 operation. This operation is supported for any activated bank.

Write Data Mask

LPDDR3 devices support one write data mask (DM) pin for each data byte (DQ), which is consistent with LPDDR2 devices. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

Figure 48: Data Mask Timing

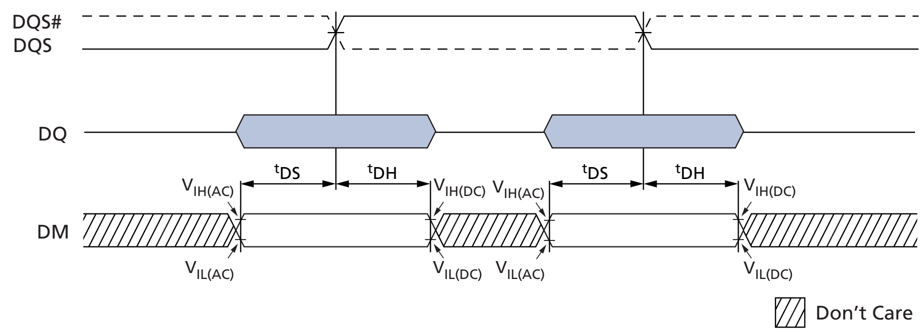
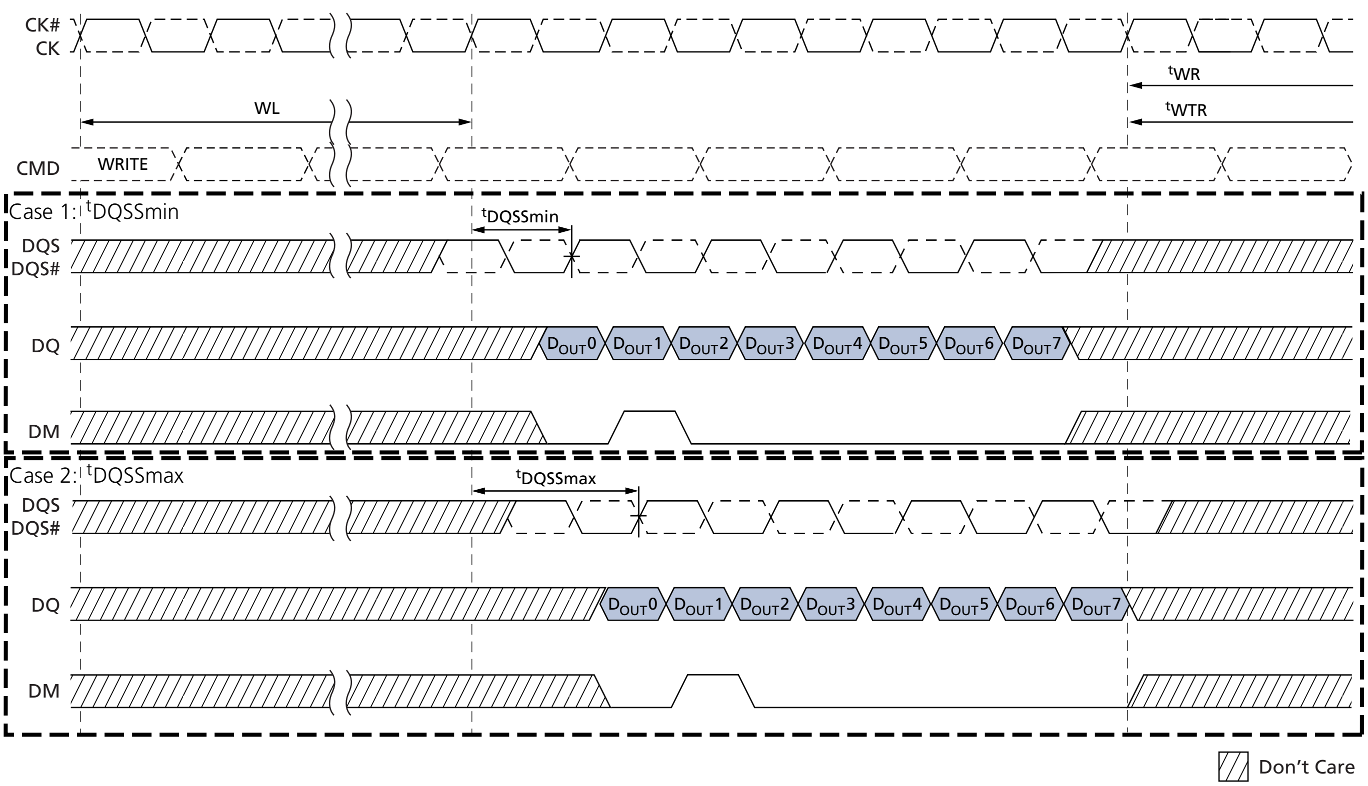


Figure 49: Write Data Mask – Second Data Bit Masked



PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access ^{t}RPab after an all-bank PRECHARGE command is issued, or ^{t}RPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row precharge time (^{t}RP) for an all bank PRECHARGE (^{t}RPab) will be longer than the row precharge time for a single-bank PRECHARGE (^{t}RPpb). ACTIVATE to PRECHARGE timing is shown in the ACTIVATE Command figure.

Table 46: Bank Selection for PRECHARGE by Address Bits

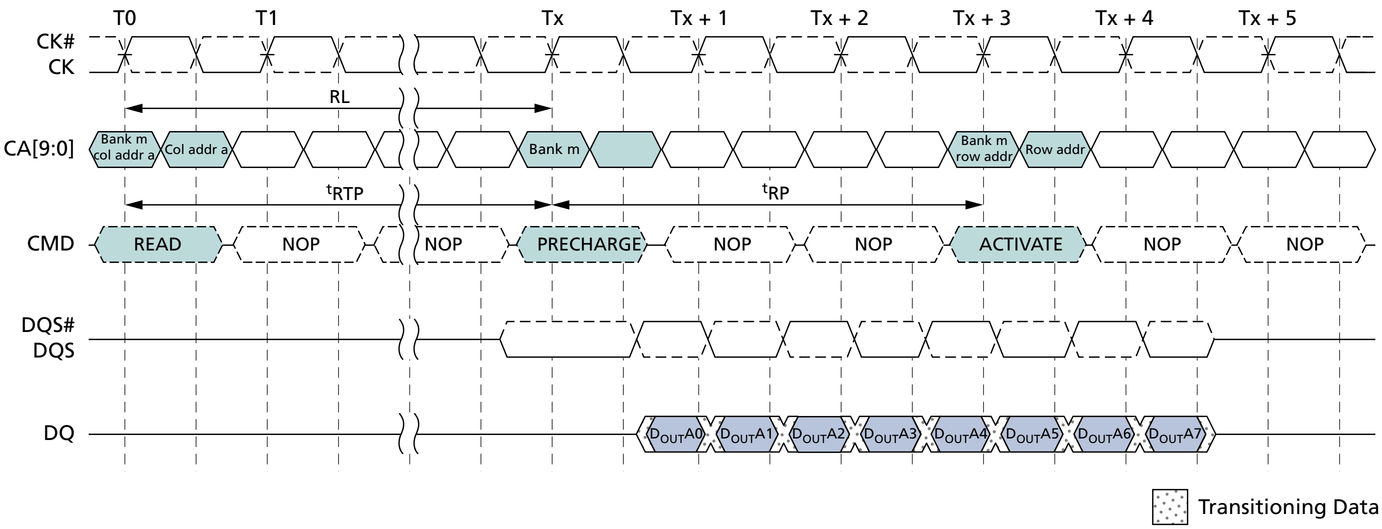
AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-Bank Device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don't Care	Don't Care	Don't Care	All banks

Burst READ Operation Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (^{t}RP) has elapsed. A PRECHARGE command cannot be issued until after ^{t}RAS is satisfied.

For LPDDR3 devices, the minimum READ-to-PRECHARGE time (^{t}RTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. ^{t}RTP begins BL/2 - 4 clock cycles after the READ command. For LPDDR3 READ-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

Figure 50: Burst READ Followed by PRECHARGE – BL = 8, RU(^{t}RTP(MIN)/^{t}CK) = 2



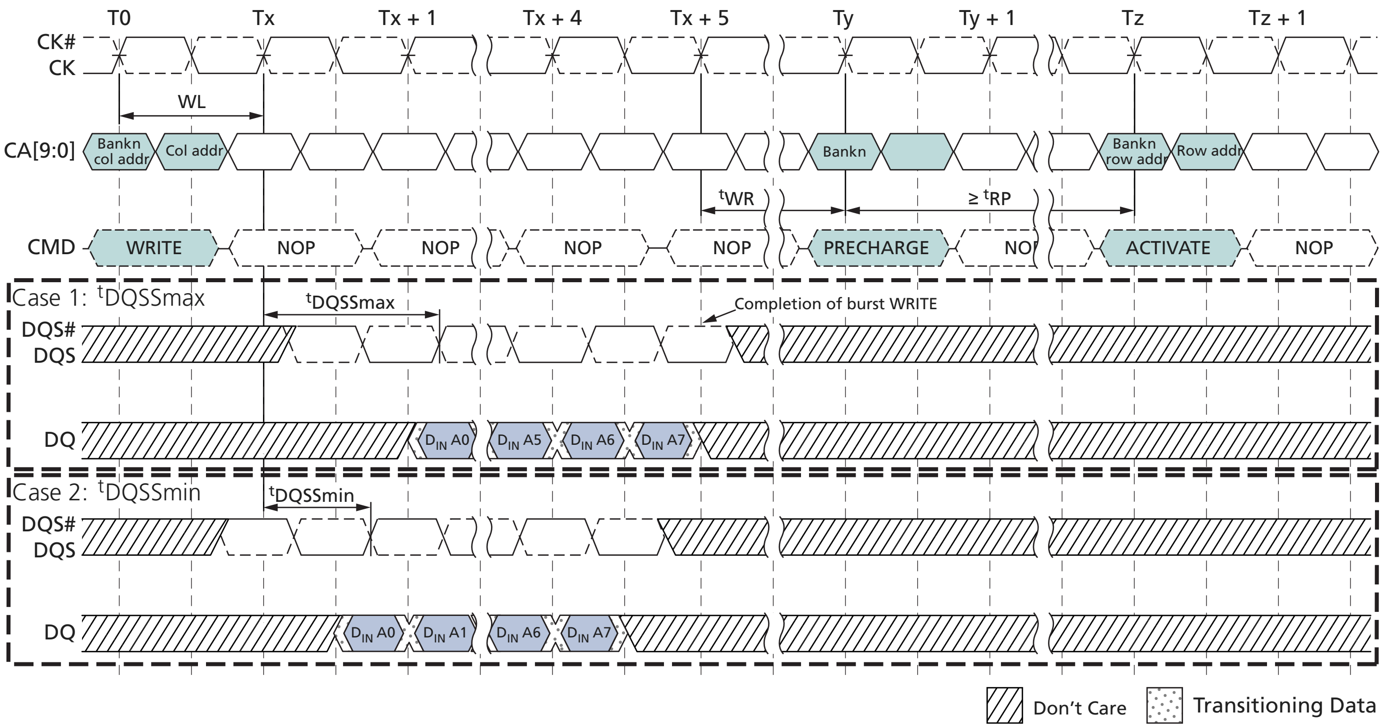
Burst WRITE Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (^{t}WR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the ^{t}WR delay. For LPDDR3 WRITE-to-PRECHARGE timings, see the PRECHARGE and Auto Precharge Clarification table.

LPDDR3 devices write data to the array in prefetch multiples (prefetch = 8). An internal WRITE operation can begin only after a prefetch group has been completely latched, so ^{t}WR starts at prefetch bondaries.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(^{t}WR/^{t}CK) clock cycles.

Figure 51: Burst WRITE Followed by PRECHARGE – BL = 8



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed, and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

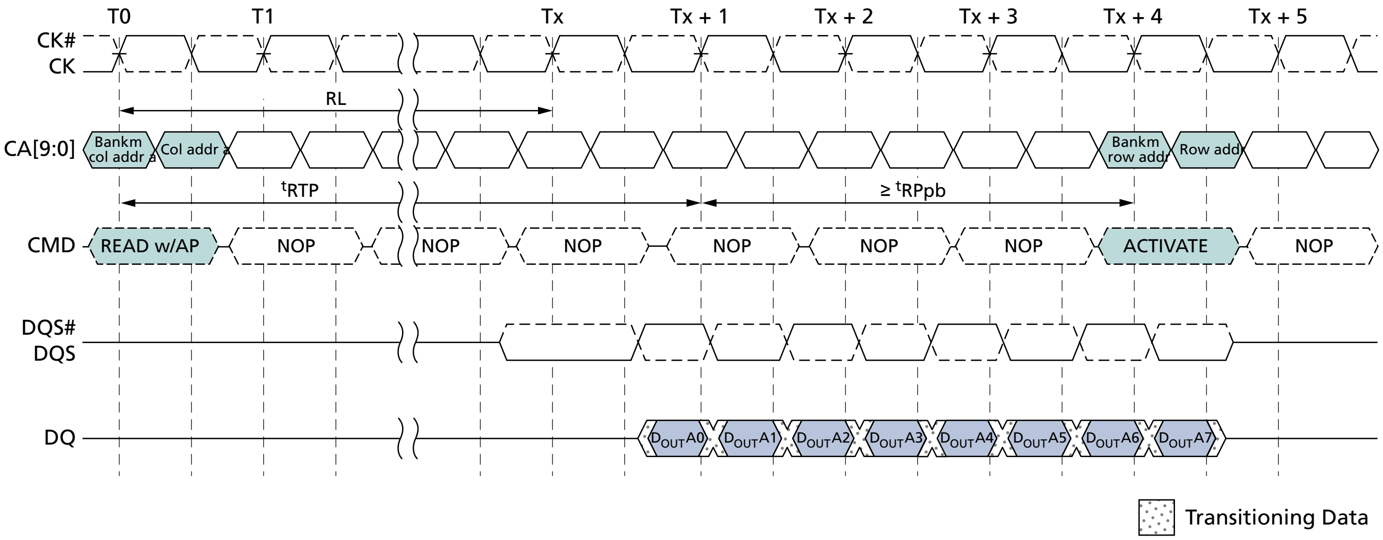
Burst READ with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged. LPDDR3 devices start an auto precharge on the rising edge of the clock BL/2 or BL/2 - 4 + RU(^{t}RTP/^{t}CK) clock cycles later than the READ with auto precharge command, whichever is greater. For LPDDR3 auto precharge calculations, see the PRECHARGE and Auto Precharge Clarification table.

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

- The RAS precharge time (^tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (^tRC) from the previous bank activation has been satisfied.

Figure 52: LPDDR3 – Burst READ with Auto Precharge



Burst WRITE with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge ^tWR cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

- The RAS precharge time (^tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (^tRC) from the previous bank activation has been satisfied.

Figure 53: Burst WRITE with Auto Precharge – BL = 8

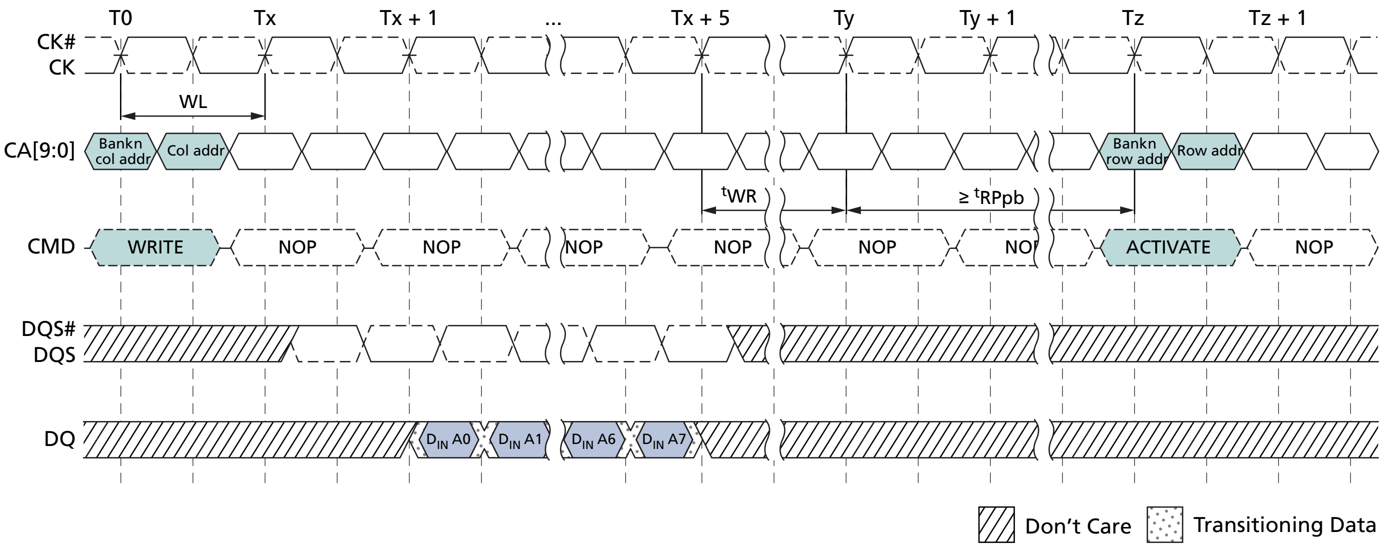


Table 47: PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
READ	PRECHARGE to same bank as READ	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1
	PRECHARGE ALL	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1
READ w/AP	PRECHARGE to same bank as READ w/AP	BL/2 + MAX (4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1, 2
	PRECHARGE ALL	BL/2 + MAX(4, RU(^{t}RTP/^{t}CK)) - 4	CLK	1
	ACTIVATE to same bank as READ w/AP	BL/2 + MAX(4, RU(^{t}RTP/^{t}CK)) - 4 + RU(^{t}RPpb/ ^{t}CK)	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCKmax/^{t}CK) - WL + 1	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	BL/2	CLK	3
WRITE	PRECHARGE to same bank as WRITE	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1, 2
	PRECHARGE ALL	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	CLK	1
	ACTIVATE to same bank as WRITE w/AP	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RPpb/^{t}CK)	CLK	1
	WRITE or WRITE w/AP (same bank)	Illegal	CLK	3
	WRITE or WRITE w/AP (different bank)	BL/2	CLK	3
	READ or READ w/AP (same bank)	Illegal	CLK	3
	READ or READ w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	CLK	3
PRECHARGE	PRECHARGE to same bank as PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1

Table 47: PRECHARGE and Auto Precharge Clarification (Continued)

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
PRECHARGE ALL	PRECHARGE	1	CLK	1
	PRECHARGE ALL	1	CLK	1

Notes:
1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command—either a one-bank PRECHARGE or PRECHARGE ALL—issued to that bank. The PRECHARGE period is satisfied after ^{t}RP, depending on the latest PRECHARGE command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

REFRESH Command

The REFRESH command is initiated with CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCab has been satisfied after the prior REFab command
- ^{t}RFCpb has been satisfied after the prior REFpb command
- ^{t}RP has been satisfied after the prior PRECHARGE command to that bank
- ^{t}RRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (^{t}RFCpb); however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCpb must be satisfied before issuing a REFab command
- ^{t}RFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- ^{t}RRD must be satisfied before issuing an ACTIVATE command to a different bank
- ^{t}RFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met (see the REFRESH Command Scheduling Separation Requirements table):

- ^{t}RFCab has been satisfied following the prior REFab command
- ^{t}RFCpb has been satisfied following the prior REFpb command
- ^{t}RP has been satisfied following the prior PRECHARGE commands

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- ^{t}RFCab latency must be satisfied before issuing an ACTIVATE command
- ^{t}RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 48: REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From	To	Notes
^{t}RFCab	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
^{t}RFCpb	REFpb	REFab	
		ACTIVATE command to same bank as REFpb	
		REFpb	
^{t}RRD	REFpb	ACTIVATE command to a different bank than REFpb	
	ACTIVATE	REFpb	1
		ACTIVATE command to a different bank than the prior ACTIVATE command	

Note: 1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited. REFpb is supported only if it affects a bank that is in the idle state.

LPDDR3 devices provide significant flexibility in scheduling REFRESH commands as long as the required boundary conditions are met (see the ^{t}SRF Definition figure). In the most straightforward implementations, a REFRESH command should be scheduled every ^{t}REFI. In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for example, to enable a period in which no refresh is required. In the extreme (such as LPDDR3 4Gb), the user can choose to issue a refresh burst of 8192 REFRESH commands at the maximum supported rate (limited by ^{t}REFBW), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: ^{t}REFW - (R/8) × ^{t}REFBW = ^{t}REFW - R × 4 × ^{t}RFCab.

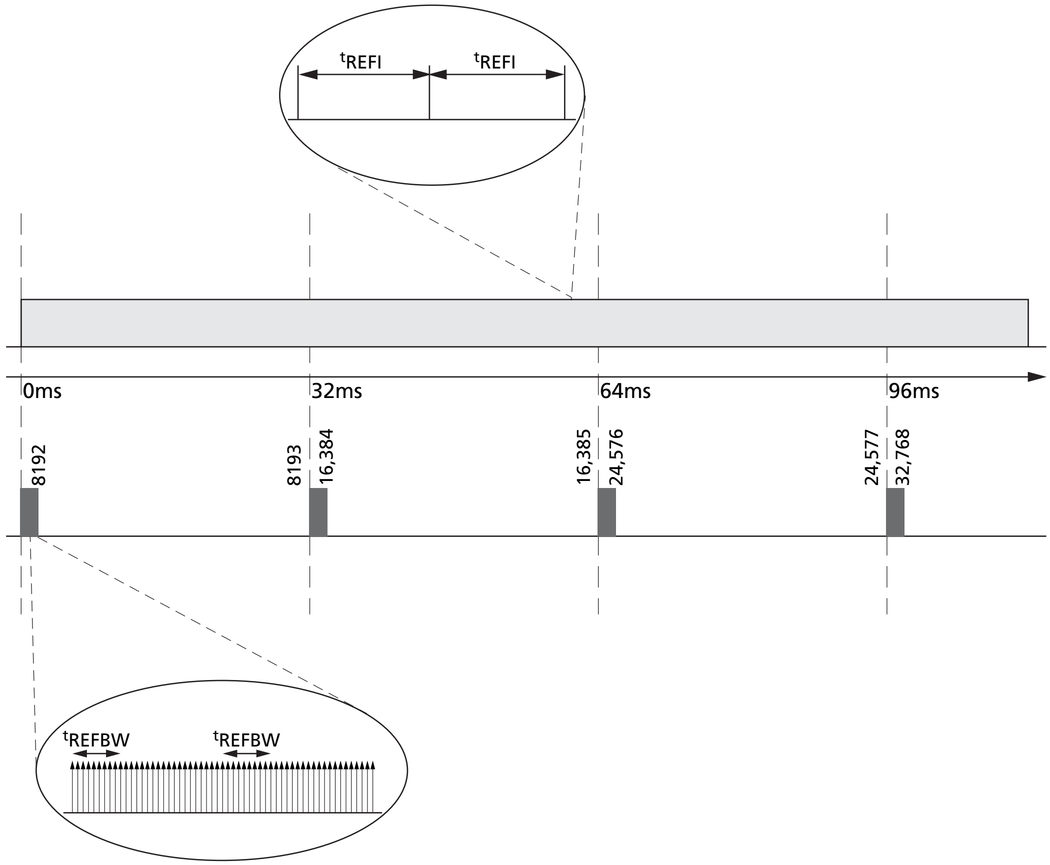
For example, a 4Gb device at T_C ≤ 85˚C can be operated without a refresh for up to 32ms - 8192 × 4 × 130ns ≈ 28ms.

Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in *every* rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in the Supported Transition from Repetitive REFRESH Burst figure. If this transition occurs immediately after the burst refresh phase, all rolling ^{t}REFW intervals will meet the minimum required number refreshes.

A nonsupported transition is shown in the Nonsupported Transition from Repetitive REFRESH Burst figure. In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling ^{t}REFW intervals, the minimum number of REFRESH commands is not satisfied.

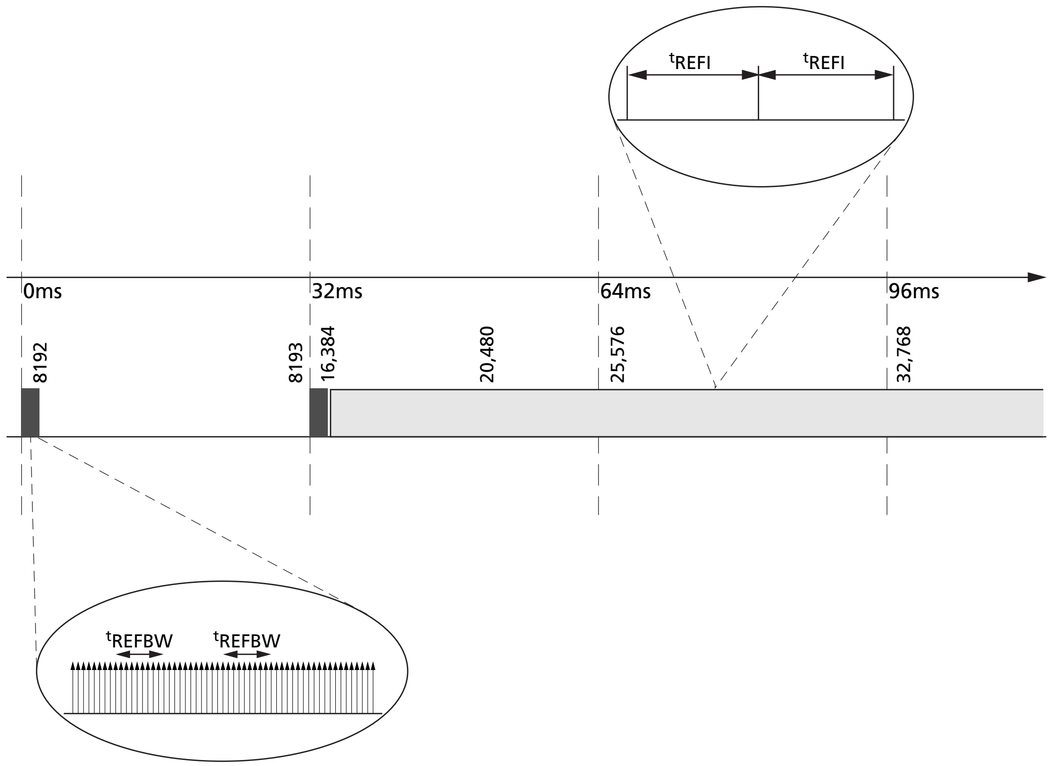
Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed-refresh pattern must be assumed. Micron recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see the Recommended Self Refresh Entry and Exit figure).

Figure 54: Regular Distributed-Refresh Pattern



Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
2. As an example, in a 4Gb LPDDR3 device at $T_C \leq 85^\circ C$, the distributed-refresh pattern has one REFRESH command per 3.9µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 28ms without any REFRESH command.

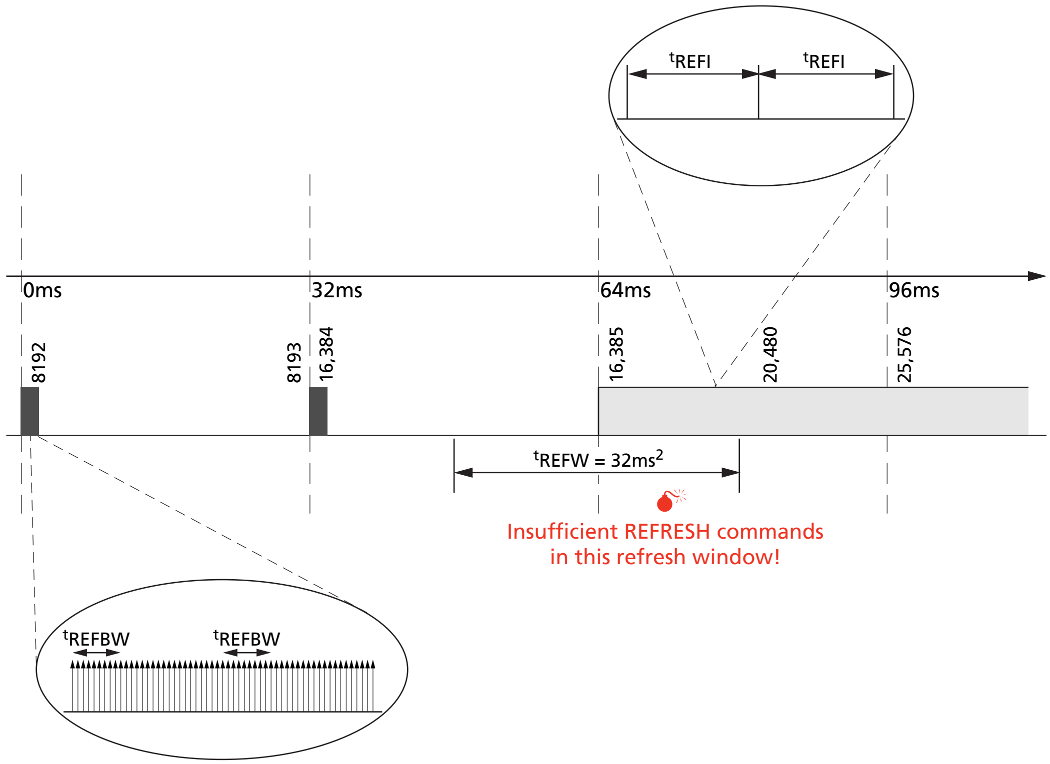
Figure 55: Supported Transition from Repetitive REFRESH Burst



Notes: 1. Shown with subsequent REFRESH pause to regular distributed-refresh pattern.

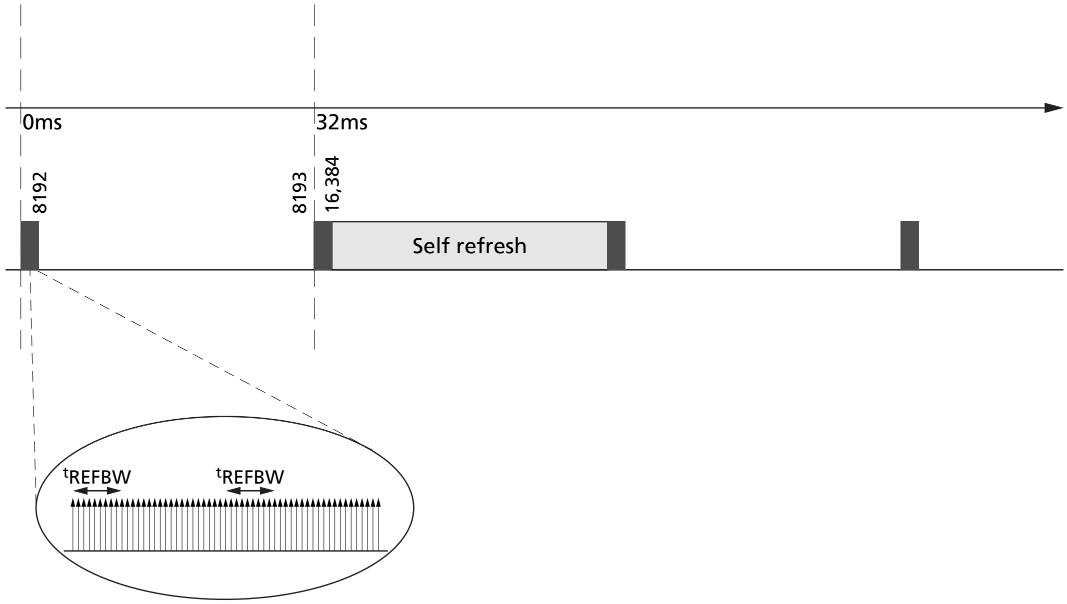
2. As an example, in a 4Gb LPDDR3 device at $T_C \leq 85$˚C, the distributed-refresh pattern has one REFRESH command per 3.9µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 28ms without any REFRESH command.

Figure 56: Nonsupported Transition from Repetitive REFRESH Burst



Notes:
1. Shown with subsequent REFRESH pause to regular distributed-refresh pattern.
2. There are only ≈ 4096 REFRESH commands in the indicated ^tREFW window. This does not provide the required minimum number of REFRESH commands (R).

Figure 57: Recommended Self Refresh Entry and Exit



Note: 1. In conjunction with a burst/pause refresh pattern.

REFRESH Requirements

1. Minimum Number of REFRESH Commands

LPDDR3 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (^{t}REFW = 32 ms @ MR4[2:0] = 011 or $T_C \leq 85$˚C). For actual values per density and the resulting average refresh interval (^{t}REFI), see the Refresh Requirement Parameters (Per Density) table.

For ^{t}REFW and ^{t}REFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) and the MR4 Op-Code Bit Definitions tables.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REFab commands can be issued in any rolling ^{t}REFBW (^{t}REFBW = 4 × 8 × ^{t}RFCab). This condition does not apply if REFpb commands are used.

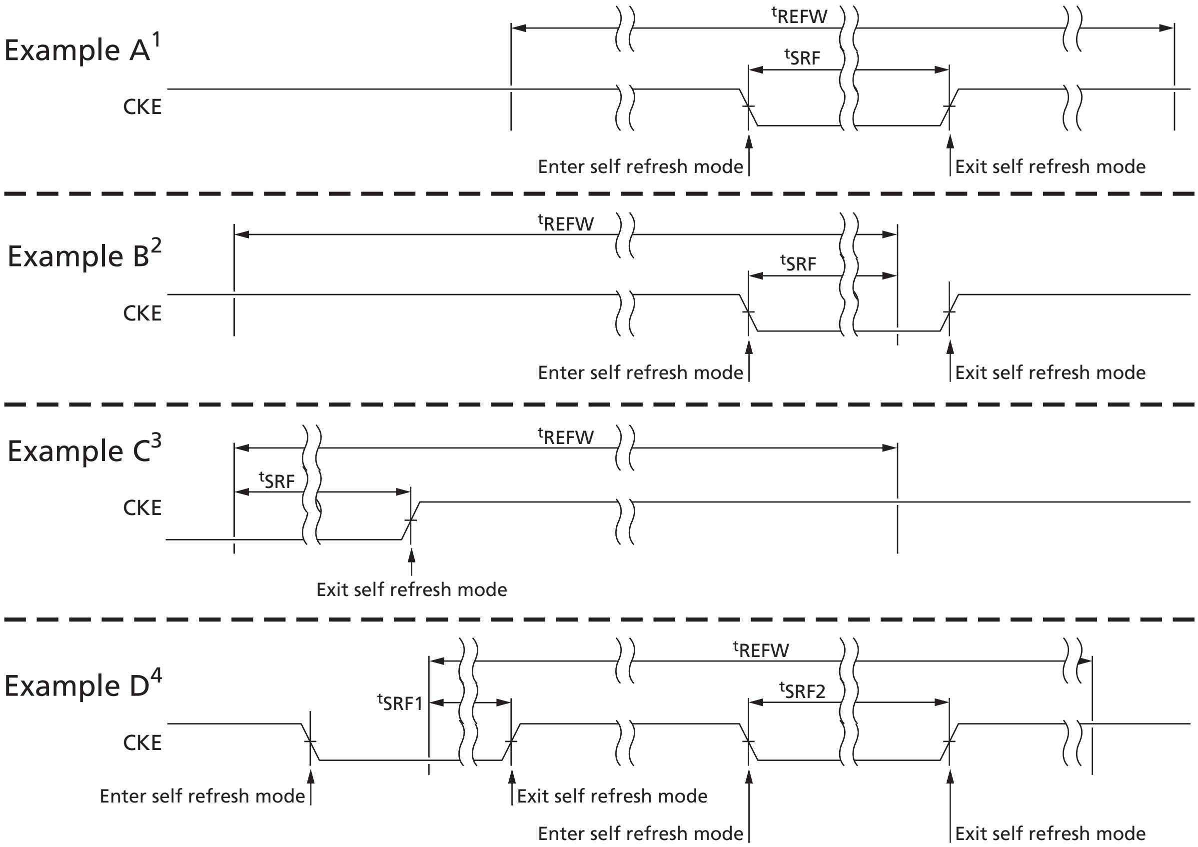
3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

$$R' = RU\left(\frac{^tSRF}{^tREFI}\right) = R - RU\left(R \times \frac{^tSRF}{^tREFW}\right)$$

Where RU represents the round-up function.

Figure 58: ^{t}SRF Definition



Notes:
1. Time in self refresh mode is fully enclosed in the refresh window (^{t}REFW).
2. At self refresh entry.
3. At self refresh exit.
4. Several intervals in self refresh during one ^{t}REFW interval. In this example, ^{t}SRF = ^{t}SRF1 + ^{t}SRF2.

Figure 59: All-Bank REFRESH Operation

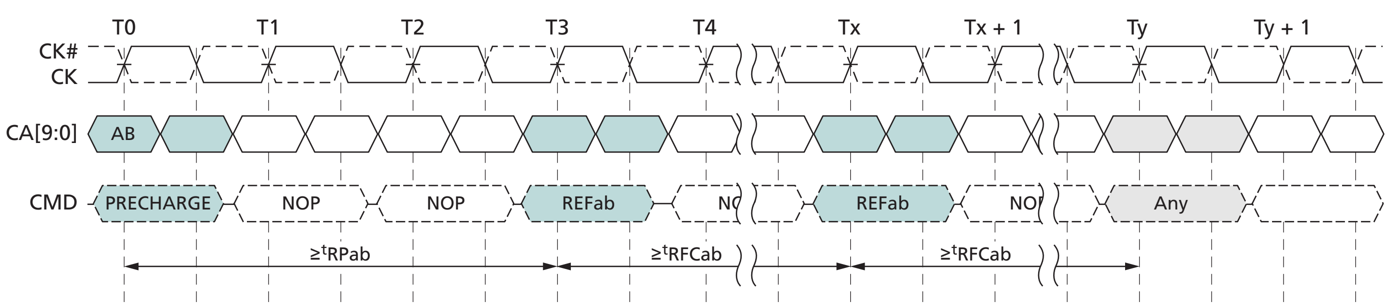
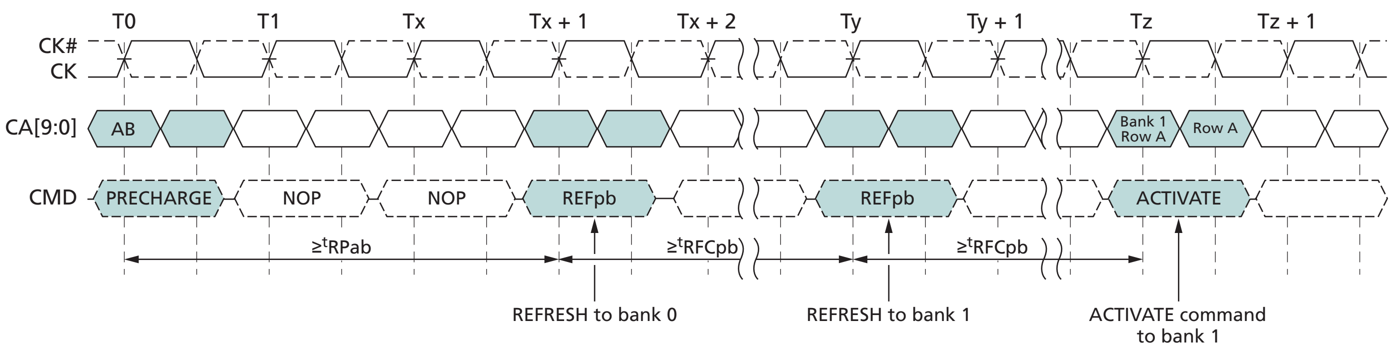


Figure 60: Per-Bank REFRESH Operation



Notes:
1. In the beginning of this example, the REFpb bank counter points to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the ^{t}RFCpb period.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered-down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress.

To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW; this timing period is defined as ^{t}CPDED. CKE LOW will result in deactivation of input receivers after ^{t}CPDED has expired. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.

Mobile LPDDR3 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range. See the I_{DD} Specification Parameters and Operating Conditions table for details.

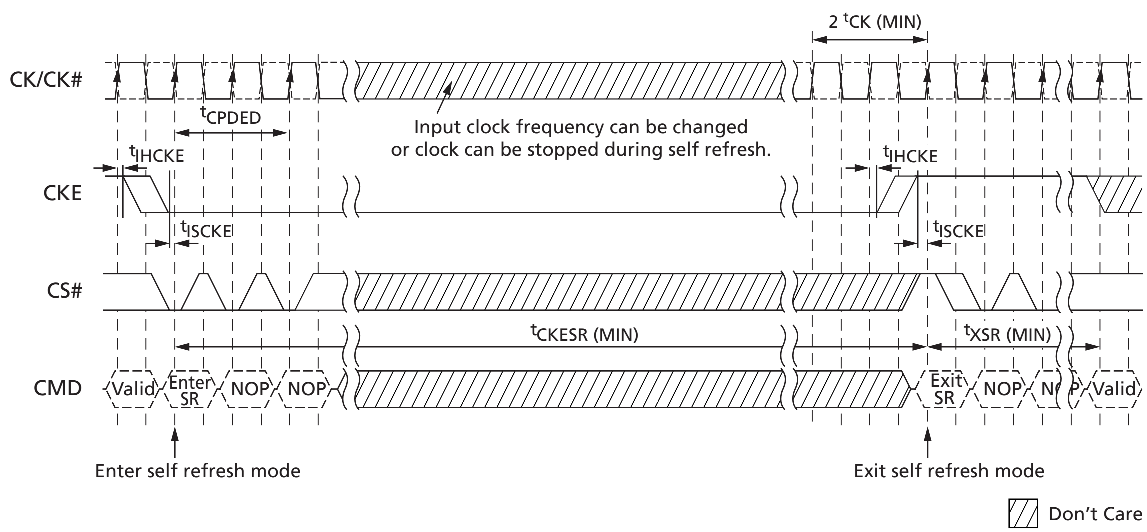
After the device has entered self refresh mode, all external signals other than CKE are “Don’t Care.” For proper SELF REFRESH operation, power supply pins (V_{DD1}, V_{DD2}, V_{DDQ}, and V_{DDCA}) must be at valid levels. V_{DDQ} can be turned off during self refresh. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting self refresh, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions). V_{REFDQ} can be at any level between 0 and V_{DDQ}; V_{REFCA} can be at any level between 0 and V_{DDCA} during self refresh.

Before exiting self refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (see the AC and DC Logic Input Measurement Levels for Single-Ended Signals section). After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during ^{t}CKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least ^{t}CKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (^tXSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout ^tXSR. NOP commands must be registered on each rising clock edge during ^tXSR. For the description of ODT operation and specifications during self-refresh entry and exit, see "On Die Termination" section.

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

Figure 61: SELF REFRESH Operation



Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
2. The device must be in the all-banks-idle state prior to entering self refresh mode.
3. ^tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after ^tXSR is satisfied. NOPs must be issued during ^tXSR.

Partial-Array Self Refresh (PASR) – Bank Masking

LPDDR3 SDRAMs comprise eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks. For bank-masking bit assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank-mask register, a REFRESH operation to the entire bank is blocked, and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as "unmasked." When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the segment mask bits.

Partial-Array Self Refresh – Segment Masking

Programming segment-mask bits is similar to programming bank-mask bits. Eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment-mask bits up to eight bits.

When the mask bit to an address range (represented as a segment) is programmed as "masked," a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment-masking scheme can be used in place of or in combination with a bank-masking scheme. Each segment mask bit setting is applied across all banks. For segment-masking bit assignments, see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables.

Table 49: Bank- and Segment-Masking Example

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
Segment 0	0	–	M	–	–	–	–	–	M
Segment 1	0	–	M	–	–	–	–	–	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	–	M	–	–	–	–	–	M
Segment 4	0	–	M	–	–	–	–	–	M
Segment 5	0	–	M	–	–	–	–	–	M
Segment 6	0	–	M	–	–	–	–	–	M
Segment 7	1	M	M	M	M	M	M	M	M

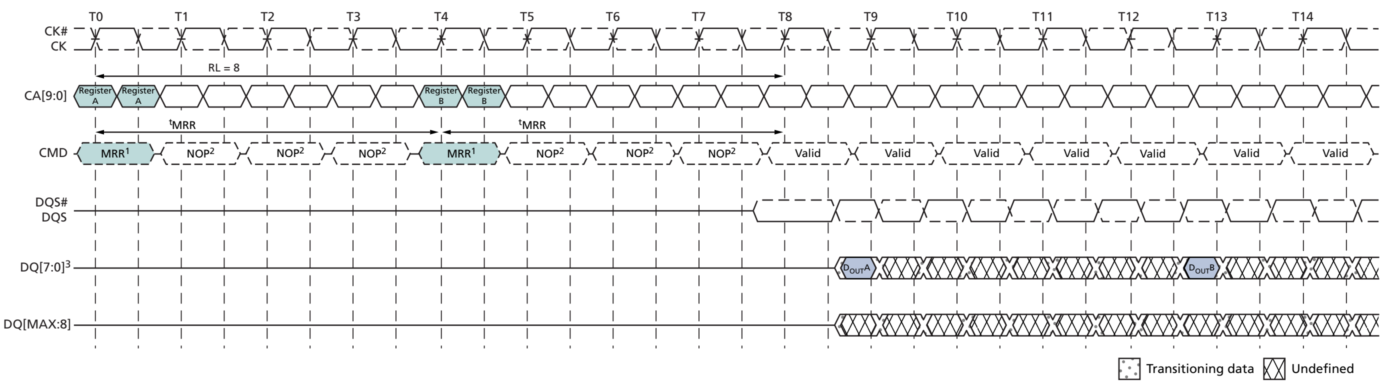
Note: 1. This table provides values for an eight-bank device with REFRESH operations masked to banks 1 and 7 and to segments 2 and 7.

MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × ^{t}CK + ^{t}DQSCK + ^{t}DQSQ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the Data Calibration Pattern Description table. All DQS are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period is ^{t}MRR.

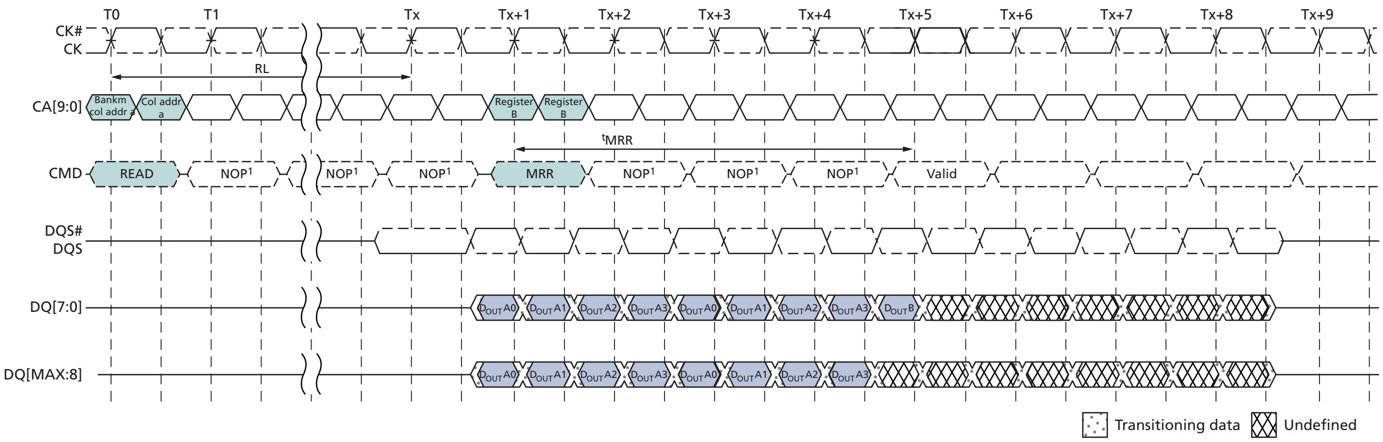
Figure 62: MRR Timing



Notes: 1. MRRs to DQ calibration registers MR32 and MR40 are described in the DQ Calibration section.
2. Only the NOP command is supported during ^{t}MRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum MRR to write latency is RL + RU(^{t}DQSCKmax/^{t}CK) + 8/2 + 1 - WL clock cycles.
5. Minimum MRR to MRW latency is RL + RU(^{t}DQSCKmax/^{t}CK) + 8/2 + 1 clock cycles.
6. In this example, RL = 8 for illustration purposes only.

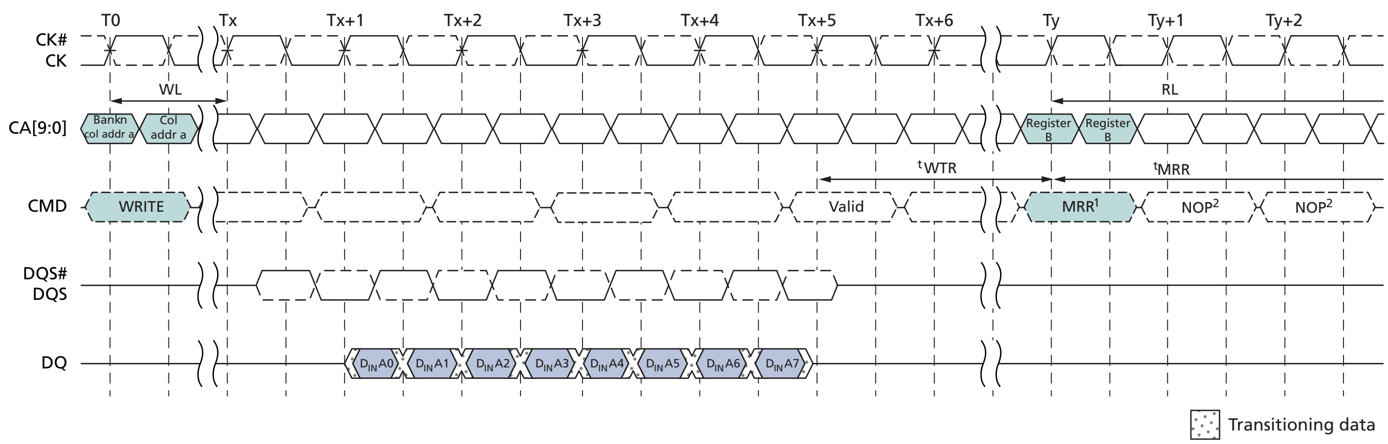
After a prior READ command, the MRR command must not be issued before BL/2 clock cycles have completed. Following a WRITE command, the MRR command must not be issued before WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK) clock cycles have completed, as READ bursts and WRITE bursts must not be truncated my MRR.

Figure 63: READ to MRR Timing



Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Only the NOP command is supported during ^{t}MRR.

Figure 64: Burst WRITE Followed by MRR

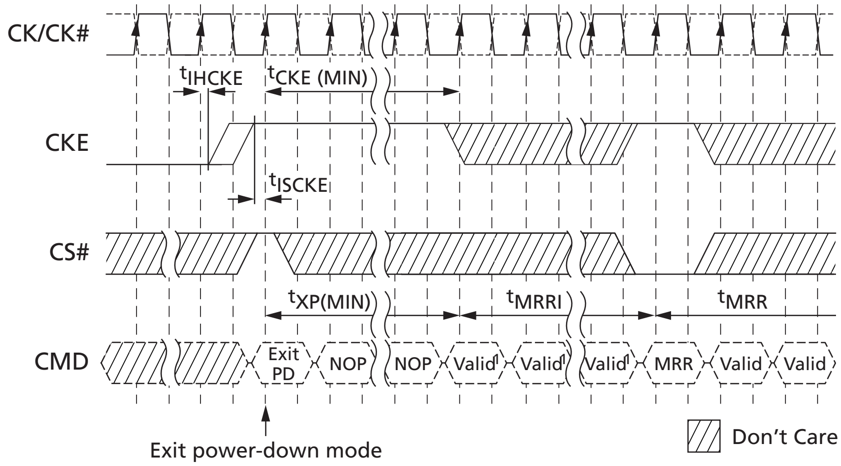


Notes:
1. The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(^{t}WTR/^{t}CK)].
2. Only the NOP command is supported during ^{t}MRR.

MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, ^{t}MRRI, is required prior to issuing the MODE REGISTER READ (MRR) command. This additional time (equivalent to ^{t}RCD) is required in order to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from the idle power-down state.

Figure 65: MRR After Idle Power-Down Exit



Note: 1. Any valid command except MRR.

Temperature Sensor

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see the Operating Temperature Range table).

Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than ^{t}TSI.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see the Operating Temperature Range table). For example, T_{CASE} could be above 85°C when MR4[2:0] equals 011b.

To ensure proper operation using the temperature sensor, applications must accommodate the following table.

Table 50: Temperature Sensor Definitions and Operating Conditions

Parameter	Description	Symbol	Min/Max	Value	Unit
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C	TempGradient	MAX	System-dependent	°C/s
MR4 READ interval	Time period between MR4 READs from the system	ReadInterval	MAX	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of MR4	^{t}TSI	MAX	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	MAX	System-dependent	ms

Table 50: Temperature Sensor Definitions and Operating Conditions (Continued)

Parameter	Description	Symbol	Min/Max	Value	Unit
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	MAX	2	°C

These devices accommodate the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

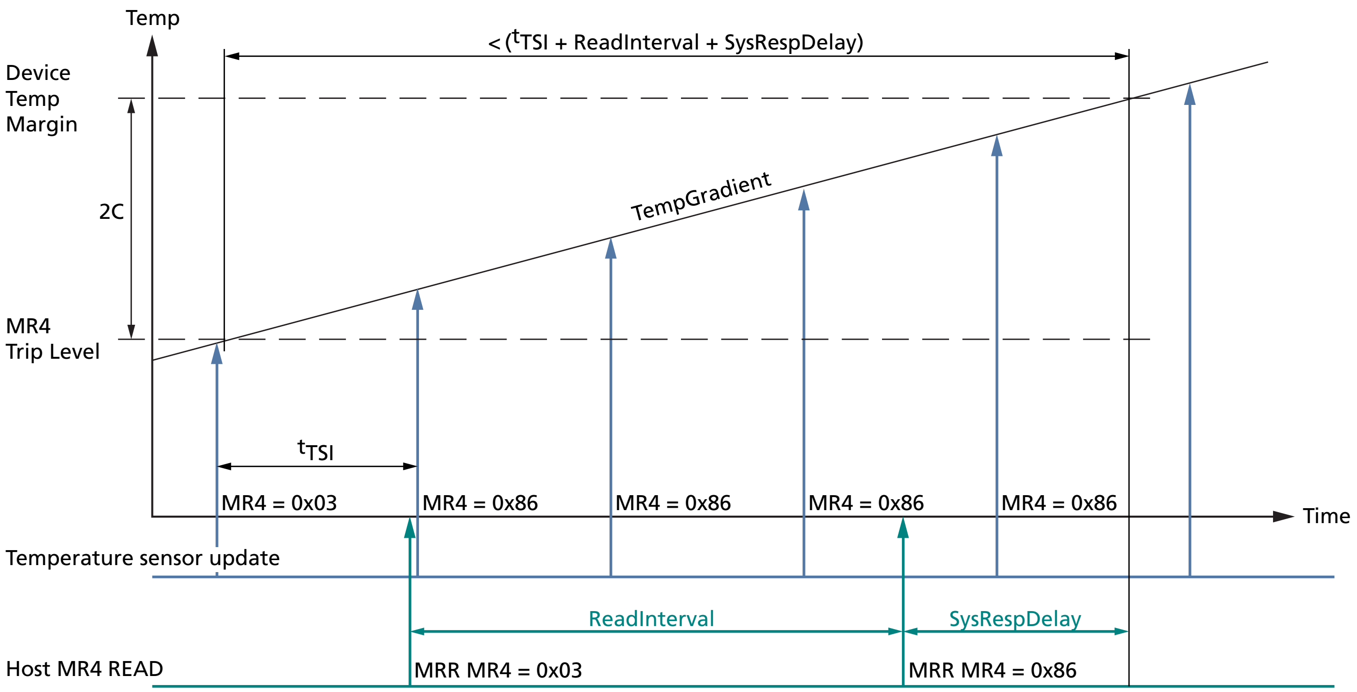
$$\text{TempGradient} \times (\text{ReadInterval} + {}^t\text{TSI} + \text{SysRespDelay}) \leq 2°\text{C}$$

For example, if TempGradient is 10˚C/s, and the SysRespDelay is 1ms:

$$\frac{10°\text{C}}{\text{s}} \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2°\text{C}$$

In this case, ReadInterval must not exceed 183ms.

Figure 66: Temperature Sensor Timing



DQ Calibration

LPDDR3 devices feature a DQ calibration function that outputs one of two predefined system timing calibration patterns. An MRR operation to MR32 (pattern A) or and MRR operation to MR40 (pattern B) will return the specified pattern on DQ0 and DQ8—for x32 devices, on DQ0, DQ8, DQ16 and DQ24.

For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

Figure 67: MR32 and MR40 DQ Calibration Timing

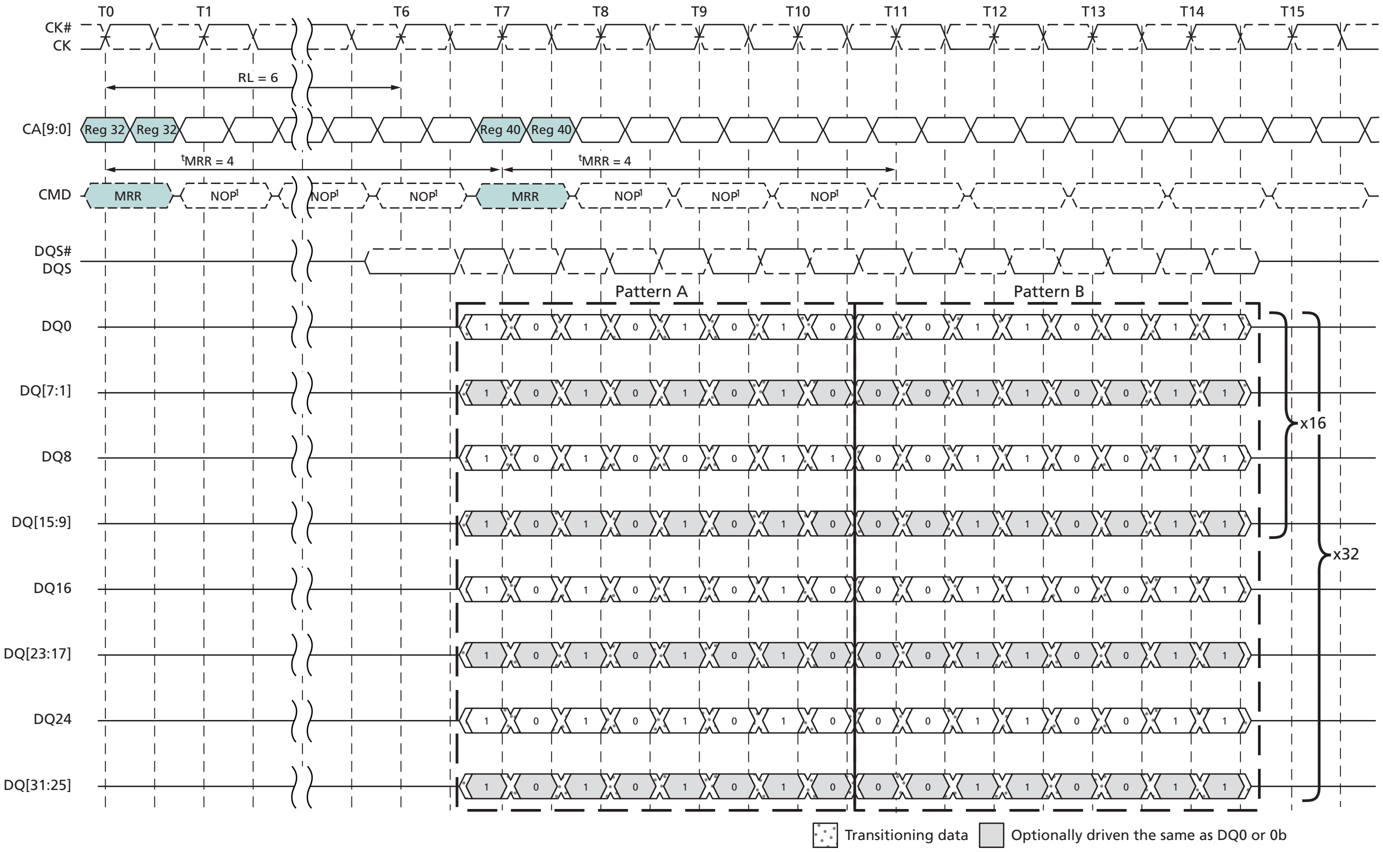


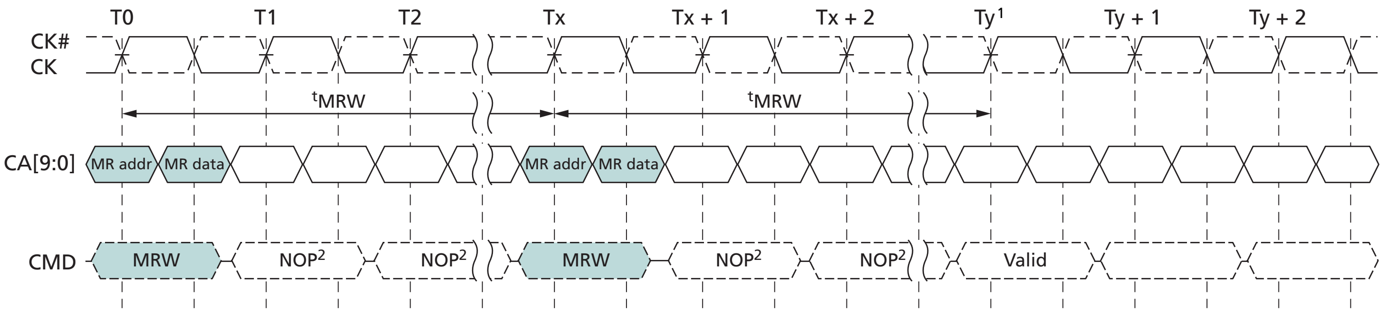
Table 51: Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7	
Pattern A	MR32	1	0	1	0	1	0	1	0	Reads to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	0	0	1	1	Reads to MR40 return DQ calibration pattern B

MODE REGISTER WRITE (MRW)

The MRW command is used to write configuration data to the mode registers. The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f–CA0f, CA9r–CA4r. The data to be written to the mode register is contained in CA9f–CA2f. The MRW command period is defined by ^{t}MRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.

Figure 68: MODE REGISTER WRITE Timing



Notes: 1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during ^{t}MRW.

MRW

MRW can be issued only when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

Table 52: Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	All banks idle
	MRW (RESET)	Resetting, device auto initialization	All banks idle
Bank(s) active	MRR	Reading mode register, bank(s) idle	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

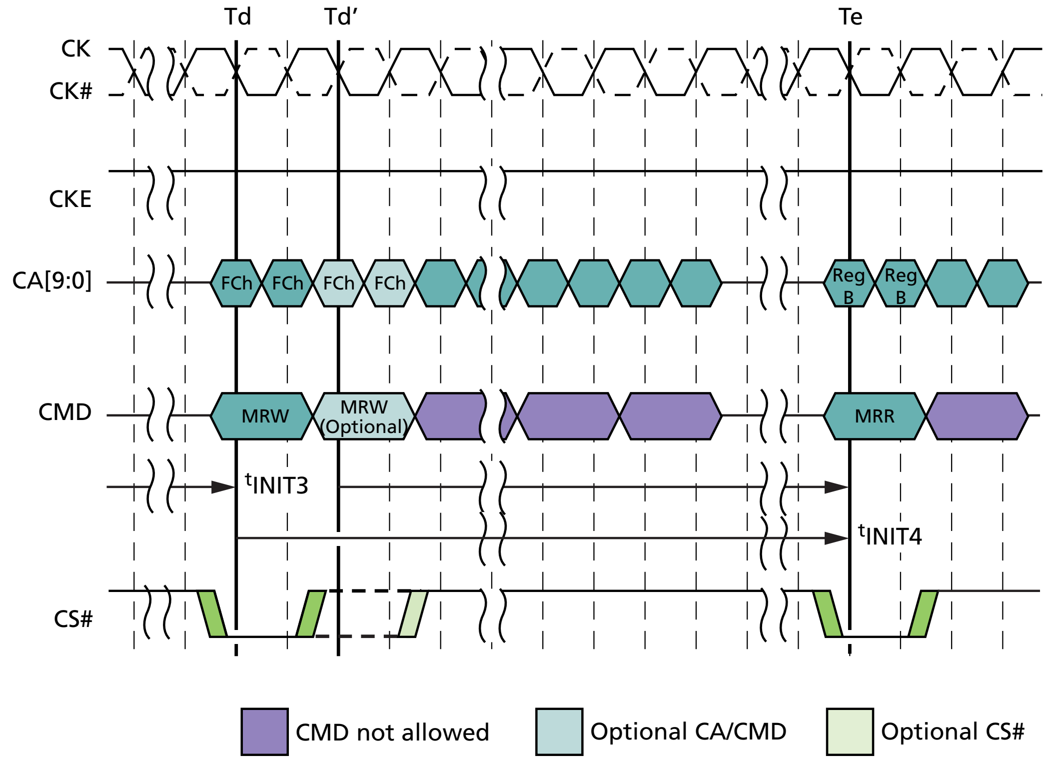
MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see the Voltage Ramp and Device Initialization section). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete, and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA training may be necessary to ensure setup and hold timings. As the MRW RESET command is required prior to CA Training, an alternate MRW RESET command with an op-code of 0xFCh should be used. This encoding ensures that no transitions occur on the CA bus. Prior to CA training, it is recommended to hold the CA bus stable for one cycle prior to, and one cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.

For MRW RESET timing, see the figure below and see the Voltage Ramp and Initialization Sequence figure.

Figure 69: MODE REGISTER WRITE Timing for MRW RESET



Note: 1. Optional MRW RESET command and optional CS# assertion are allowed. When the optional MRW RESET command is used, ^{t}INIT4 starts at Td'.

MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR3 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: ^{t}ZQINIT, ^{t}ZQRESET, ^{t}ZQCL, and ^{t}ZQCS. ^{t}ZQINIT is used for initialization calibration; ^{t}ZQRESET is used for resetting ZQ to the default output impedance; ^{t}ZQCL is used for long calibration(s); and ^{t}ZQCS is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of ±15%. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15%. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

ZQRESET resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within ^{t}ZQCS for all speed bins, assuming the maximum sensitivities specified in the Output Driver Sensitivity Definition and Output Driver Temperature and Voltage Sensitivity tables are met. The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate ($T_{driftrate}$) and voltage drift rate ($V_{driftrate}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ_{correction}}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where T_{sens} = MAX ($dR_{ON}dT$) and V_{sens} = MAX ($dR_{ON}dV$) define temperature and voltage sensitivities.

For example, if T_{sens} = 0.75%/˚C, V_{sens} = 0.20%/mV, $T_{driftrate}$ = 1˚C/sec, and $V_{driftrate}$ = 15 mV/sec, then the interval between ZQCS commands is calculated as:

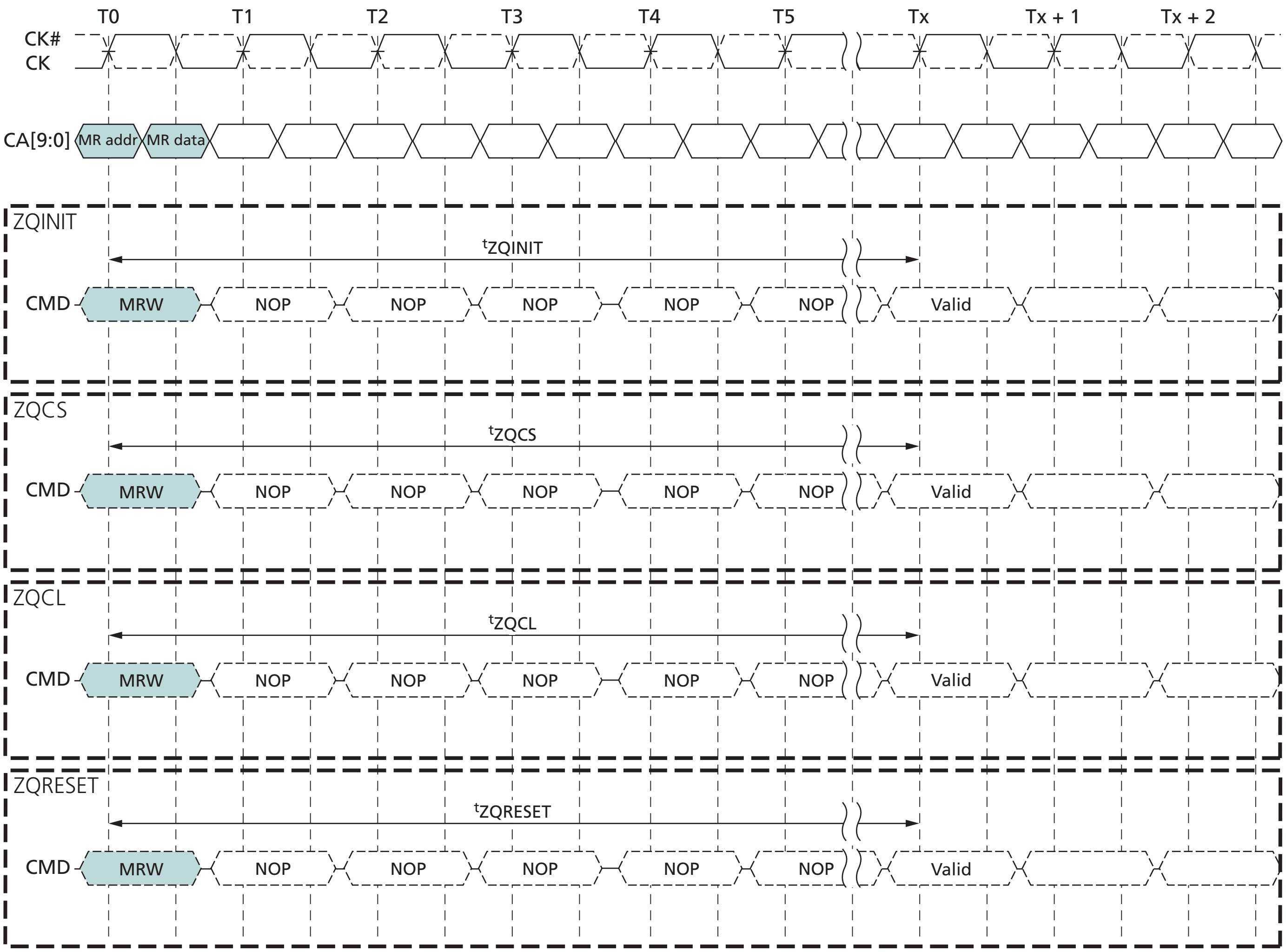
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ calibration command can be issued only when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods (^tZQINIT, ^tZQCL, or ^tZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor among devices, the controller must prevent ^tZQINIT, ^tZQCS, and ^tZQCL overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to V_{DDCA}. In this situation, the device must ignore ZQ calibration commands, and the device will use the default calibration settings.

Figure 70: ZQ Timings



Notes:
1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240Ω (±1% tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device, or one resistor can be shared among multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Input/Output Capacitance table).

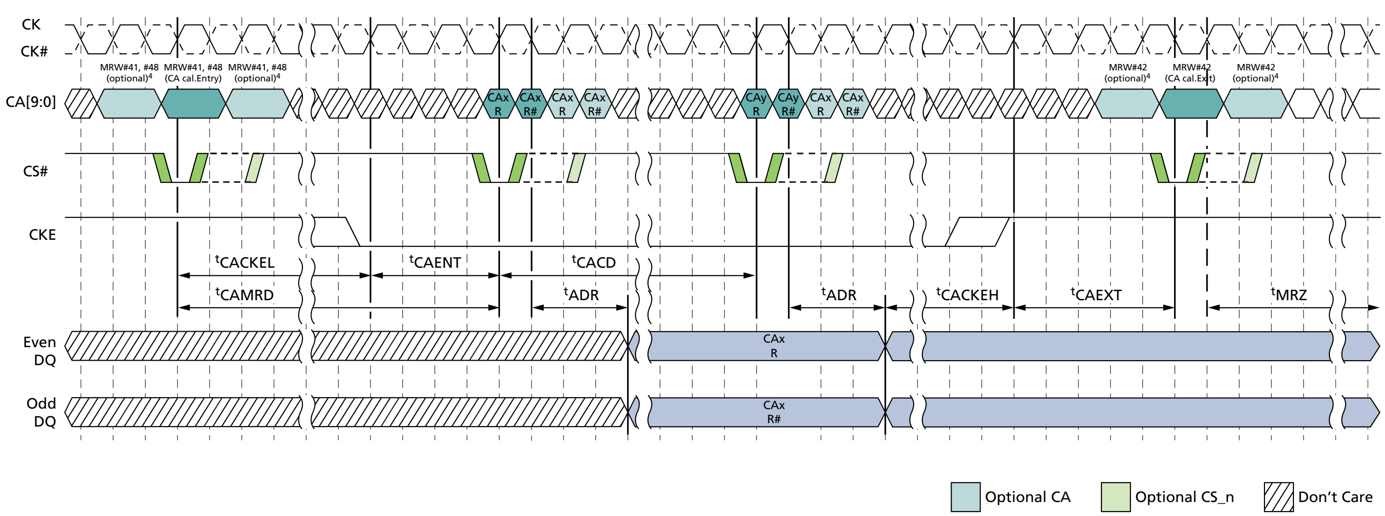
MRW – CA Training Mode

Because CA inputs operate as double data rate, it may be difficult for the memory controller to satisfy CA input setup/hold timings at higher frequency. A CA training mechanism is provided.

CA Training Sequence

1. CA training mode entry: MODE REGISTER WRITE command to MR41
2. CA training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see the CA Training Mode Enable (MR41 (29H, 0010 1001b) OP=A4H (1010 0100b)) table)
3. CA to DQ mapping change: MODE REGISTER WRITE command to MR48
4. Additional CA training session: Calibrate remaining CA pins (CA4 and CA9) (see the CA Training Mode Enable (MR48 (30H, 0011 0000b) OP=C0H (1100 0000b)) table)
5. CA training mode exit: MODE REGISTER WRITE command to MR42

Figure 71: CA Training Timing



Notes:
1. Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.
2. CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Both MR41 and MR48 training sequences must be completed before exiting the training mode (MR42). To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command. (See the steps in the CA Training Sequence section for details.)
3. Because data-out control is asynchronous and will be an analog delay from when all the CA data is available, ^{t}ADR and ^{t}MRZ are defined from the falling edge of CK.

4. It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA TRAINING ENTRY command to ensure setup and hold timings on the CA bus.
5. Optional MRW 41, 48, 42 commands and the CA CALIBRATION command are allowed. To complement these optional commands, optional CS# assertions are also allowed. All timing must comprehend these optional CS# assertions: a) ^{t}ADR starts at the falling clock edge after the last registered CS# assertion; b) ^{t}CACD, ^{t}CACKEL, and ^{t}CAMRD start with the rising clock edge of the last CS# assertion; c) ^{t}CAENT and ^{t}CAEXT need to be met by the first CS# assertion; and d) ^{t}MRZ will be met after the falling clock edge following the first CS# assertion with exit (MRW #42) command.

The LPDDR3 SDRAM device may not properly recognize a MODE REGISTER WRITE command at normal operation frequency before CA training is finished. Special encodings are provided for CA training mode enable/disable.

MR41 and MR42 encodings are selected so that rising-edge and falling-edge values are the same. The device will recognize MR41 and MR42 at normal operation frequency even before CA timing adjustments have been made. Calibration data will be output through DQ pins. CA to DQ mapping is described in the CA to DQ mapping (CA training mode enabled with MR41) table.

After timing calibration with MR41 is finished, issue MRW to MR48 and calibrate the remaining CA pins (CA4 and CA9) using (DQ0/DQ1and DQ8/DQ9) as calibration data output pins (see the CA to DQ mapping (CA training mode is enabled with MR48) table).

Table 53: CA Training Mode Enable (MR41 (29H, 0010 1001b), OP = A4H (1010 0100b))

Clock Edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	H	L	L	H	L	H
CK falling edge	L	L	L	L	H	L	L	H	L	H

Table 54: CA Training Mode Disable (MR42 (2AH, 0010 1010b), OP = A8H(1010 1000b))

Clock Edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	L	H	L	H	L	H
CK falling edge	L	L	L	L	L	H	L	H	L	H

Table 55: CA to DQ Mapping (CA Training Mode Enabled with MR41)

Clock Edge	CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8
CK rising edge	DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14
CK falling edge	DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15

Note: 1. Other DQs must have valid output (either HIGH or LOW).

Table 56: CA Training Mode Enable (MR48 (30H, 0011 0000b), OP = C0H (1100 0000b))

Clock Edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK rising edge	L	L	L	L	L	L	L	L	H	H

Table 56: CA Training Mode Enable (MR48 (30H, 0011 0000b), OP = C0H (1100 0000b)) (Continued)

Clock Edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CK falling edge	L	L	L	L	L	L	L	L	H	H

Table 57: CA to DQ Mapping (CA Training Mode Enabled with MR48)

Clock Edge	CA4	CA9
CK rising edge	DQ0	DQ8
CK falling edge	DQ1	DQ9

Note: 1. Other DQs must have valid output (either HIGH or LOW).

MRW - Write Leveling Mode

To improve signal-integrity performance, the LPDDR3 SDRAM provides a write-leveling feature to compensate for timing skew, affecting timing parameters such as ^{t}DQSS, ^{t}DSS, and ^{t}DSH.

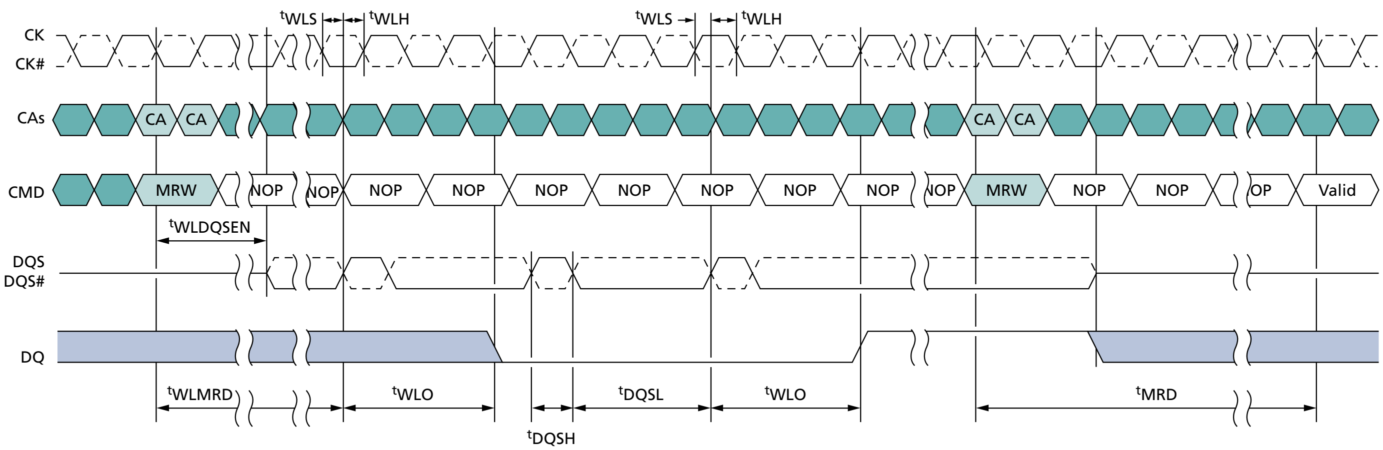
The memory controller uses the write-leveling feature to receive feedback from the SDRAM, enabling it to adjust the clock-to-data strobe signal relationship for each DQS/DQS# signal pair. The memory controller performing the leveling must have an adjustable delay setting on the DQS/DQS# signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signal delay established through this exercise ensures the ^{t}DQSS specification can be met.

All data bits carry the leveling feedback to the controller (DQ[15:0] for x16 configuration, DQ[31:0] for x32 configuration). All DQS signals must be leveled independently.

The LPDDR3 SDRAM enters into write-leveling mode when mode register MR2[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only NOP commands are allowed, or a MRW command to exit the write-leveling operation. Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2[7] is reset LOW.

The controller drives DQS LOW and DQS# HIGH after a delay of ^{t}WLDQSEN. After time ^{t}WLMRD, the controller provides DQS signal input, which is used by the DRAM to sample the clock signal driven from the controller. The delay time ^{t}WLMRD (MAX) is controller-dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time ^{t}WLO. The controller samples this information and either increments or decrements the DQS and/or DQS# delay settings and launches the next DQS/DQS# pulse. The sample time and trigger time are controller-dependent. After the following DQ/DQS# transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. The following figure describes the timing for the write-leveling operation.

Figure 72: Write-Leveling Timing



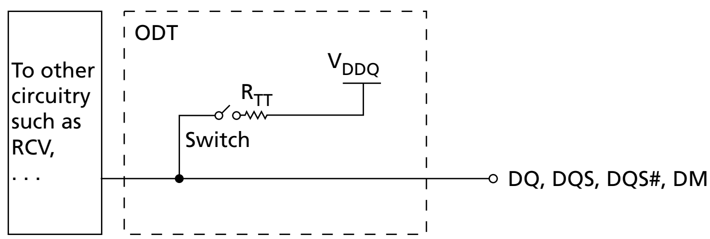
On-Die Termination (ODT)

On-die termination (ODT) is a feature that enables the device to enable/disable and turn on/off termination resistance for each DQ, DQS, DQS#, and DM signal via the ODT control pin. ODT is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the internal termination resistance for any or all DRAM devices. The ODT pin directly controls ODT operation and is not sampled by the clock.

ODT is turned off and not supported in self refresh and deep power-down modes. The device will also disable termination during READ operations. ODT operation can be enabled optionally during power-down mode via a mode register. Note that if ODT is enabled during power-down mode, V_{DDQ} may not be turned off during power down. The DRAM will also disable termination during READ operations.

A simple functional representation of the ODT feature is shown below.

Figure 73: Functional Representation of On-Die Termination



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of R_{TT} (ODT termination resistance value) is determined by the settings of several mode register bits. The ODT pin will be ignored if MR11 is programmed to disable ODT, in self refresh, in deep power-down, in CKE power-down (mode register option), and during READ operations.

ODT Mode Register

ODT mode is enabled if MR11[1:0] are non-zero. In this case, the value of R_{TT} is determined by the settings of those bits. ODT mode is disabled if MR11[1:0] are zero. MR11[2] determines whether ODT, if enabled through MR11[1:0], will operate during power-down mode.

Asychronous ODT

When enabled, the ODT feature is controlled asynchronously based on the status of the ODT pin. ODT is off under any of the following conditions:

- ODT is disabled through MR11[1:0]
- Device is performing a READ operation (READ or MRR)
- Device is in power-down mode and MR11[2] is zero
- Device is in self refresh or deep power-down mode
- Device is in CA training mode

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin ^{t}ODToff, ^{t}ODTon.

Minimum R_{TT} turn-on time (^{t}ODTon,min) is the point in time when the device termination circuit leaves High-Z state and ODT resistance begins to turn on. Maximum R_{TT} turn-on time (^{t}ODTon,max) is the point in time when ODT resistance is fully on. ^{t}ODTon,min and ^{t}ODTon,max are measured from ODT pin HIGH.

Minimum R_{TT} turn-off time (^{t}ODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (^{t}ODToff,max) is the point in time when the on-die termination has reached High-Z. ^{t}ODToff,min and ^{t}ODToff,max are measured from ODT pin LOW.

ODT During READ Operations (READ or MRR)

During READ operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT mode is enabled).

ODT During Power-Down

When MR11[2] is zero, termination control through the ODT pin will be disabled when the DRAM enters power-down. After a power-down entry is registered, termination will be disabled within a time window specified by ^{t}ODTd,min,max. ODT pin control is resumed when power-down is exited (if ODT mode is enabled). Between the POWER-DOWN EXIT command and until ^{t}XP is satisfied, termination will transition from disabled to control by the ODT pin. When ^{t}XP is satisfied, the ODT pin is used to control termination.

Minimum R_{TT} disable time (^{t}ODTd,min) is the point in time when the device termination circuit is no longer controlled by the ODT pin. Maximum ODT disable time (^{t}ODTd,max) is the point in time when ODT will be in High-Z.

When MR11[2] is enabled and MR11[1:0] are non-zero, ODT operation is supported during CKE power-down with ODT control through the ODT pin.

ODT During Self Refresh

The device disables the ODT function during self refresh. After a SELF REFRESH command is registered, termination will be disabled within a time window specified by ^{t}ODTd,min,max. During self refresh exit, ODT control through the ODT pin is resumed (if ODT mode is enabled). Between the SELF REFRESH EXIT command and until ^{t}XSR is satisfied, termination will transition from disabled to control by the ODT pin. When ^{t}XSR is satisfied, the ODT pin is used to control termination.

ODT During Deep Power-Down

The device disables the ODT function during deep power-down. After a DEEP POWER-DOWN command is registered, termination will be disabled within a time window specified by ^{t}ODTd,min,max.

ODT During CA Training and Write Leveling

During CA training mode, the device will disable ODT and ignore the state of the ODT control pin. For ODT operation during write leveling mode, refer to the DRAM Termination Function in Write Leveling Mode table for termination activation and deactivation for DQ and DQS/DQS#. If ODT is enabled, the ODT pin must be HIGH in write leveling mode.

Table 58: DRAM Termination Function in Write Leveling Mode

ODT pin	DQS/DQS# Termination	DQ Termination
De-asserted	OFF	OFF
Asserted	ON	OFF

Table 59: ODT States Truth Table

	Write	Read/DQ Calibration	ZQ Calibration	CA Training	Write Leveling
DQ termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS termination	Enabled	Disabled	Disabled	Disabled	Enabled

Figure 74: Asynchronous ODT Timing – RL = 12

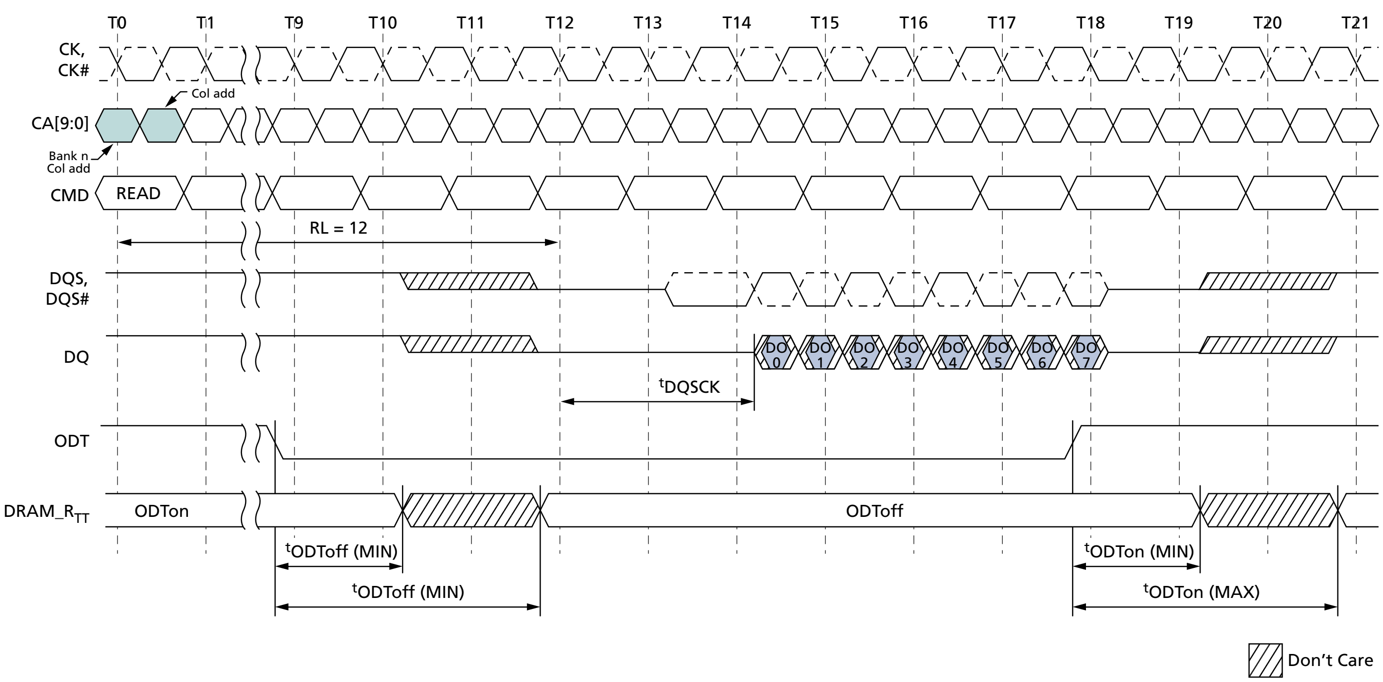
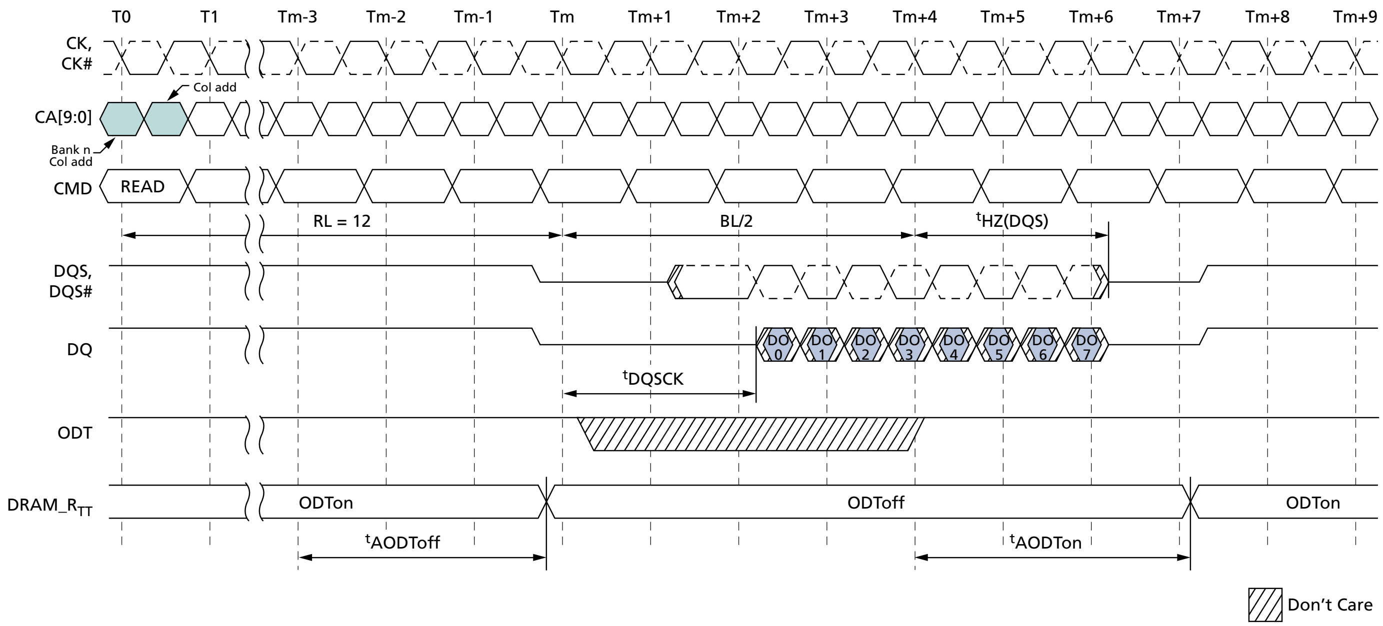


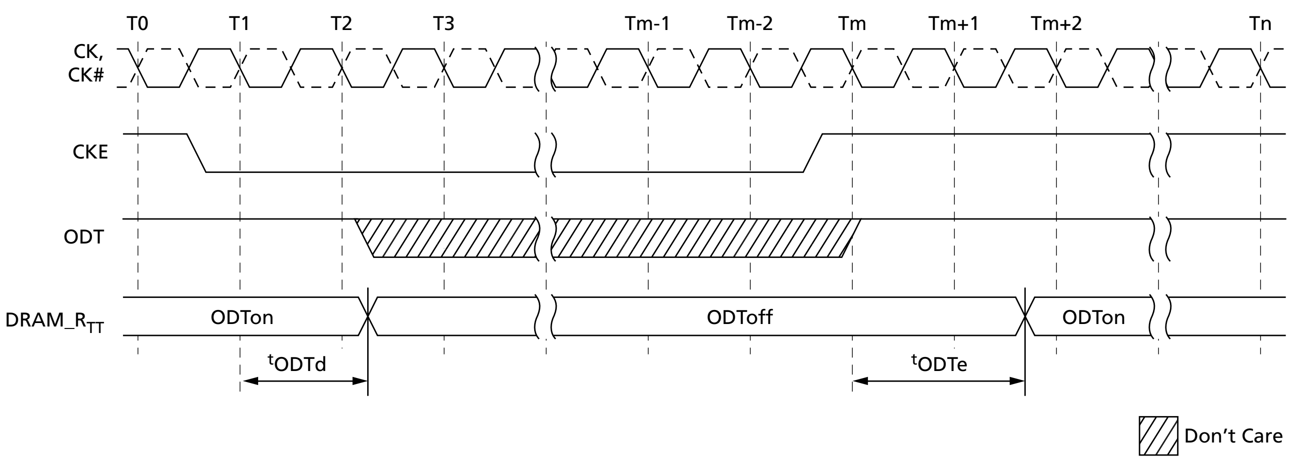
Figure 75: Automatic ODT Timing During READ Operation – RL = *m*



Notes: 1. The automatic R_{TT} turn-off delay, $^tAODToff$, is referenced from the rising edge of RL - 2 clock at T_{m-2}.

2. The automatic R_{TT} turn-on delay, ^tAODTon, is referenced from the rising edge of RL + BL/2 clock at T_{m+4}.

Figure 76: ODT Timing During Power-Down, Self Refresh, Deep Power-Down Entry/Exit



Note: 1. Upon exiting of deep power-down mode, a complete power-up initialization sequence is required.

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS# is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following the POWER-DOWN command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE, AUTO PRECHARGE, or REFRESH are in progress, but the power-down I_{DD} specification is not applied until such operations are complete.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW. this timing period is defined as t_{CPDED}. CKE LOW results in deactivation of input receivers after t_{CPDED} has expired. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until ^{t}CKE is satisfied, and V_{REFCA} must be maintained at a valid level during power-down.

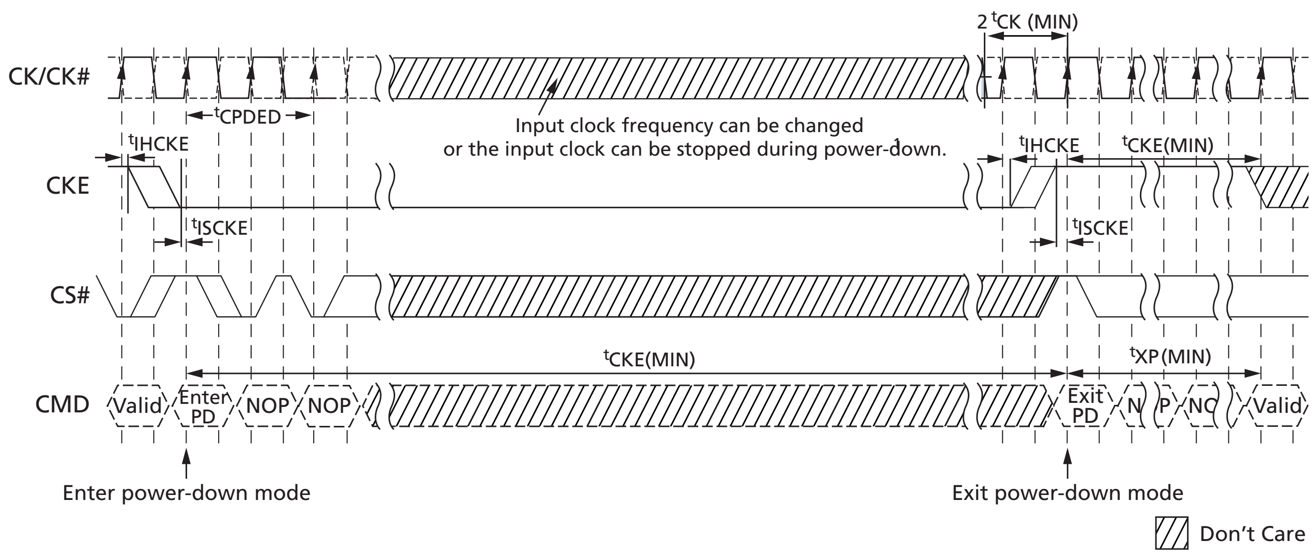
V_{DDQ} can be turned off during power-down. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting power-down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see the AC and DC Operating Conditions section).

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the REFRESH Command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until ^{t}CKE is satisfied. A valid, executable command can be applied with power-down exit latency ^{t}XP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing table.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when a row is active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see the On-Die Termination section.

Figure 77: Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use and that prior to power-down exit, a minimum of two stable clocks complete.

Figure 78: CKE Intensive Environment

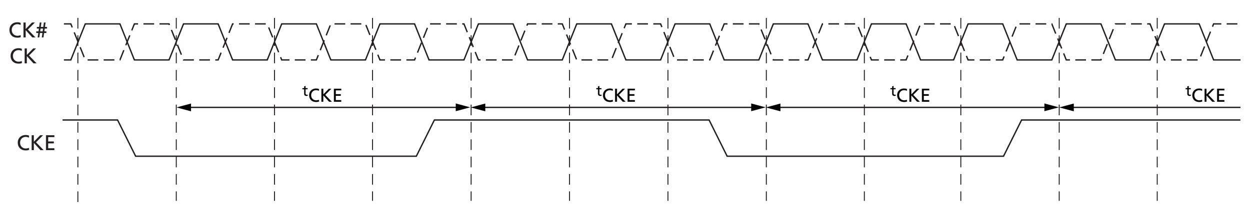
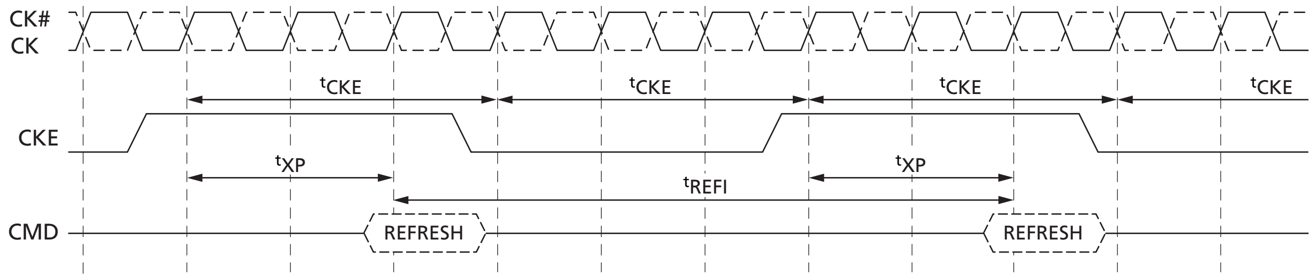
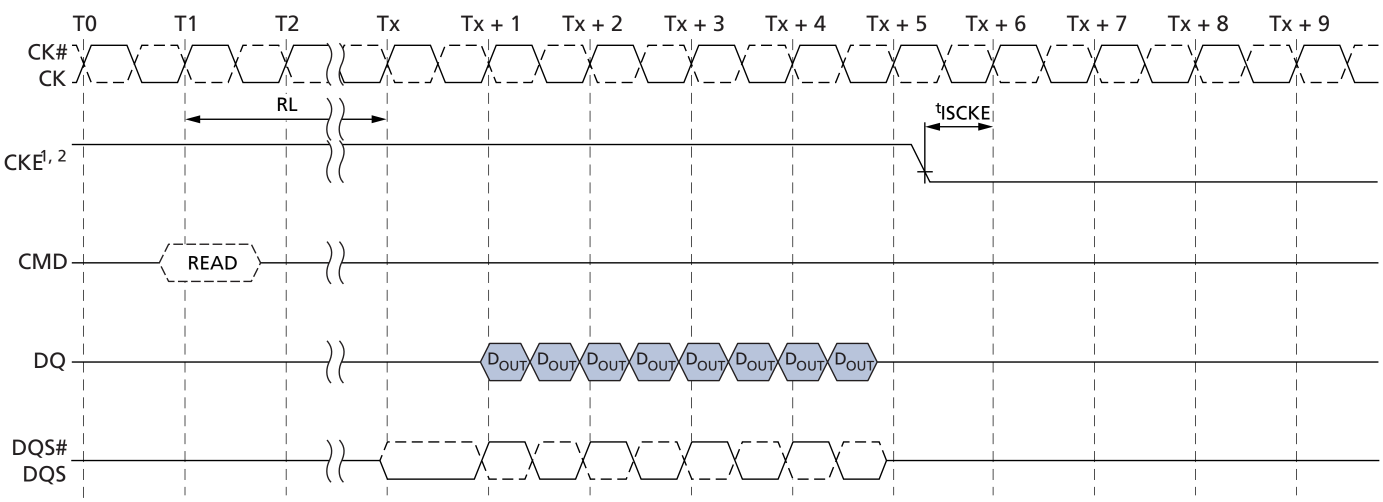


Figure 79: REFRESH-to-REFRESH Timing in CKE Intensive Environments



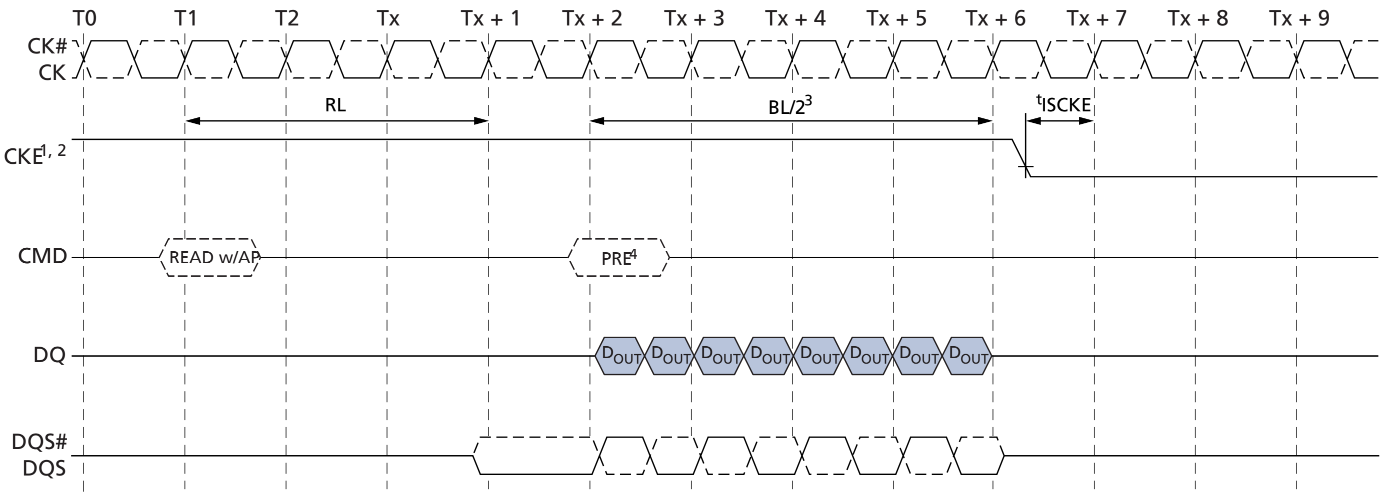
Note: 1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure 80: READ to Power-Down Entry



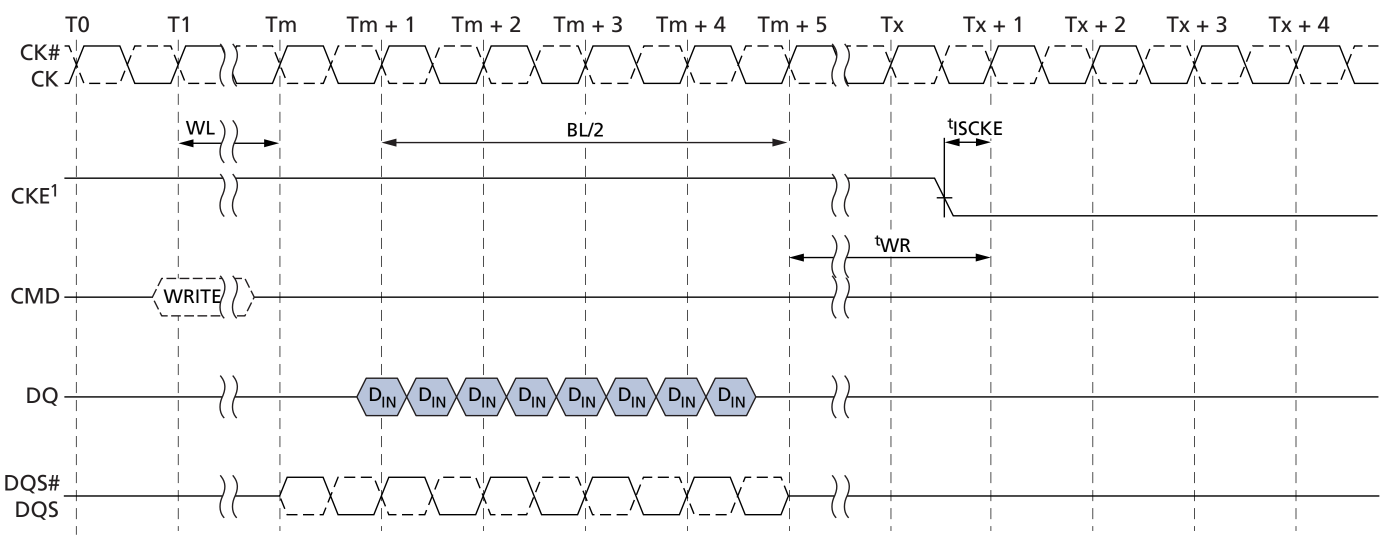
Notes: 1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at {RL + RU[tDQSCK(MAX)/tCK] + BL/2 + 1} clock cycles after the clock on which the READ command is registered.

Figure 81: READ with Auto Precharge to Power-Down Entry



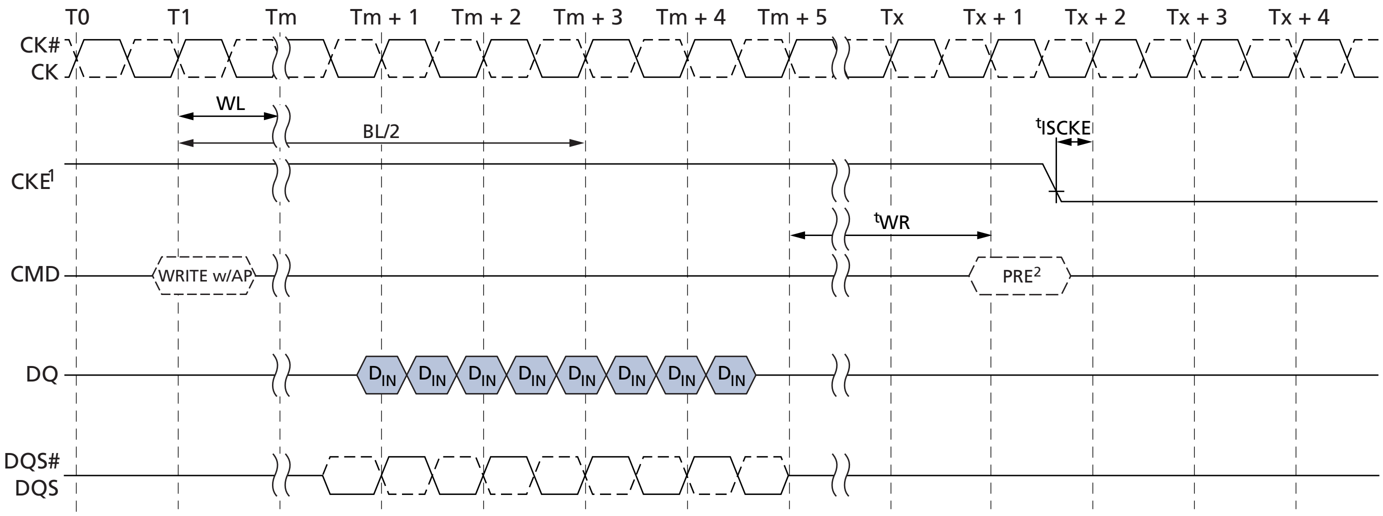
Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at [RL + RU(^{t}DQSCK/^{t}CK) + BL/2 + 1] clock cycles after the clock on which the READ command is registered.
3. BL/2 with ^{t}RTP = 7.5ns and ^{t}RAS (MIN) is satisfied.
4. Start internal PRECHARGE.

Figure 82: WRITE to Power-Down Entry



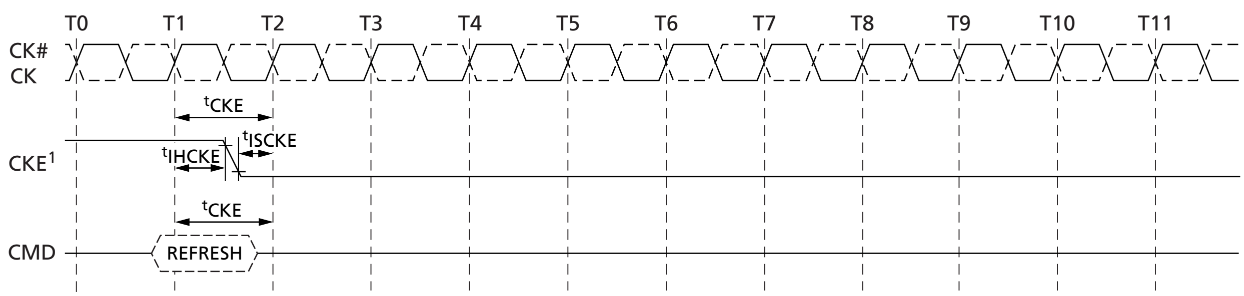
Note:
1. CKE can be registered LOW at [WL + 1 + BL/2 + RU(^{t}WR/^{t}CK)] clock cycles after the clock on which the WRITE command is registered.

Figure 83: WRITE with Auto Precharge to Power-Down Entry



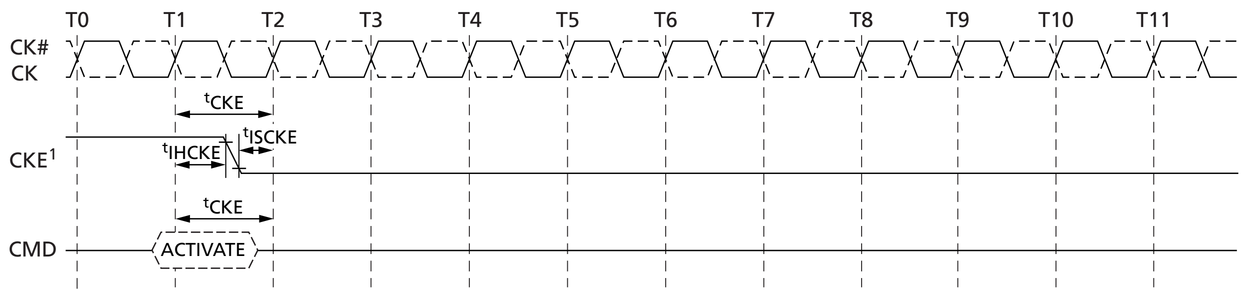
Notes: 1. CKE can be registered LOW at [WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) + 1] clock cycles after the WRITE command is registered.
2. Start internal PRECHARGE.

Figure 84: REFRESH Command to Power-Down Entry



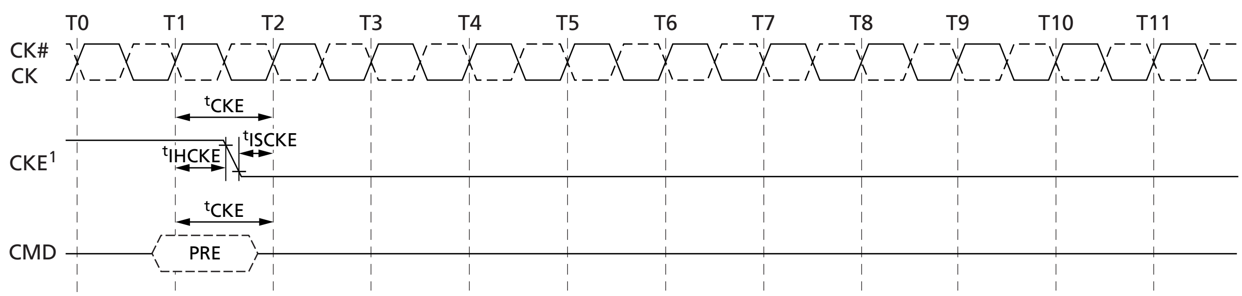
Note: 1. CKE can go LOW ^{t}IHCKE after the clock on which the REFRESH command is registered.

Figure 85: ACTIVATE Command to Power-Down Entry



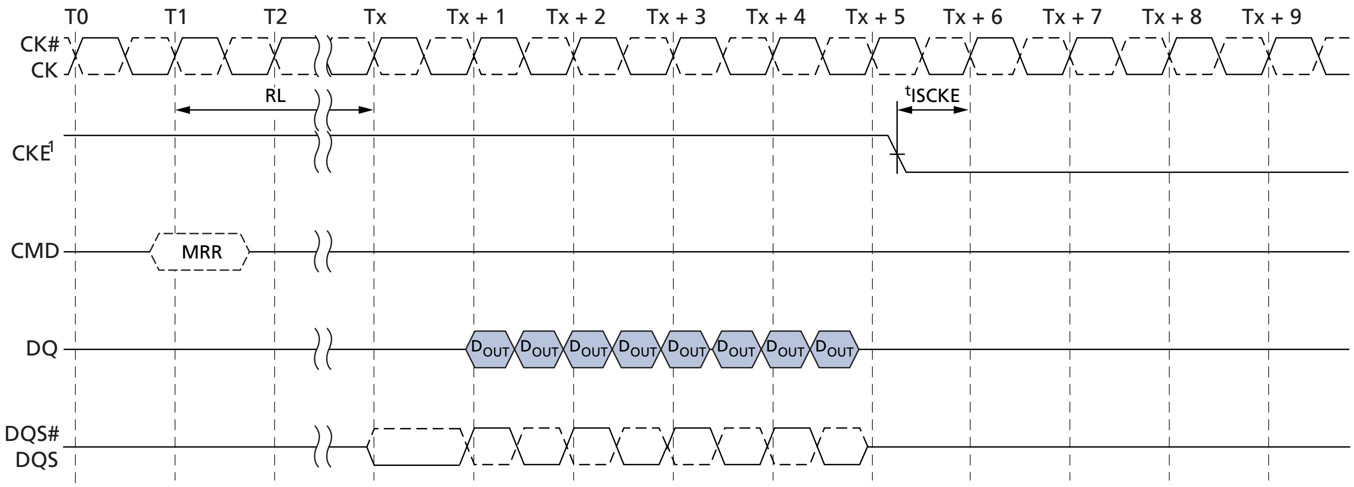
Note: 1. CKE can go LOW at ^{t}IHCKE after the clock on which the ACTIVATE command is registered.

Figure 86: PRECHARGE Command to Power-Down Entry



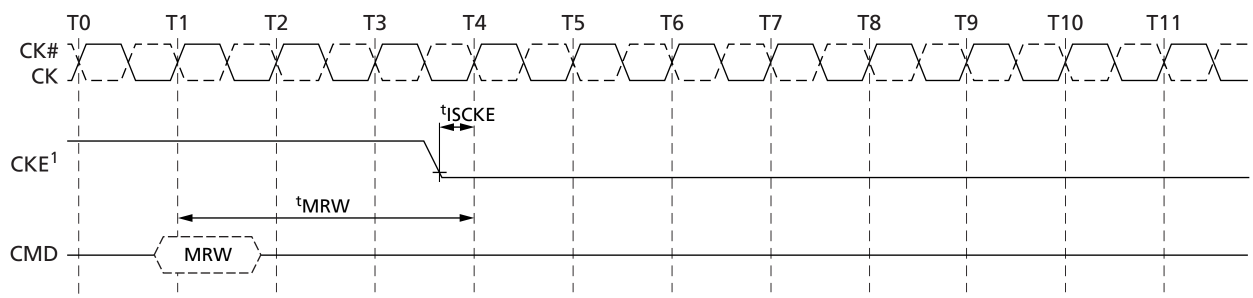
Note: 1. CKE can go LOW ^{t}IHCKE after the clock on which the PRECHARGE command is registered.

Figure 87: MRR Power-Down Entry



Note: 1. CKE can be registered LOW at [RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1] clock cycles after the clock on which the MRR command is registered.

Figure 88: MRW Command to Power-Down Entry



Note: 1. CKE can be registered LOW ^{t}MRW after the clock on which the MRW command is registered.

Deep Power-Down

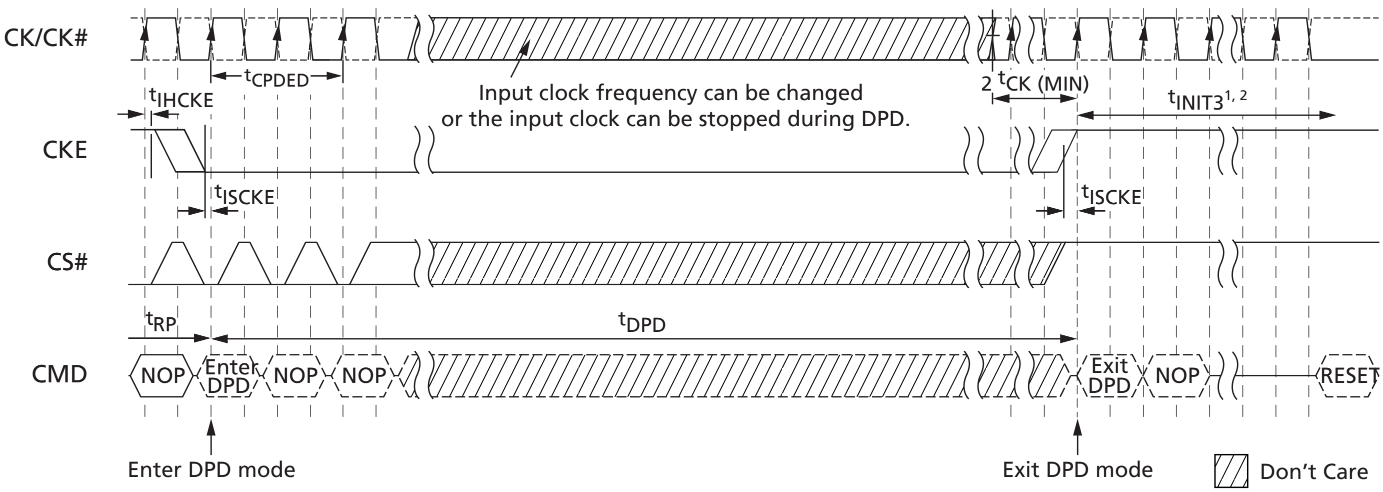
Deep power-down (DPD) is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. All banks must be in the idle state with no activity on the data bus prior to entering DPD mode. During DPD, CKE must be held LOW. The contents of the device will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW; this timing period is defined as ^{t}CPDED. CKE LOW will result in deactivation of command and address receivers after ^{t}CPDED has expired. V_{REFDQ} can be at any level between 0 and V_{DDQ}, and V_{REFCA} can be at any level between 0 and V_{DDCA}

during DPD. All power supplies, including V_{REF}, must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

DPD mode is exited when CKE is registered HIGH while meeting ^{t}ISCKE, and the clock must be stable. The device must be fully reinitialized using the power-up initialization sequence. For a description of ODT operation and specifications during DPD entry and exit, see the ODT During Deep Power-Down section.

Figure 89: Deep Power-Down Entry and Exit Timing



Notes:
1. The initialization sequence can start at any time after Tx + 1.
2. ^{t}INIT3 and Tx + 1 refer to timings in the initialization sequence. For details, see the Mode Register Definition section.

Input Clock Frequency Changes and Stop Events

Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, the device supports input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, ^{t}RCD and ^{t}RP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, ^{t}CK (MIN) and ^{t}CK (MAX) must be met for each clock cycle.

After the input clock frequency changes and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, and so on. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, the device supports input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands have completed, including any associated data bursts, prior to changing the frequency
- Related timing conditions, ^{t}RCD, ^{t}WR, ^{t}WRA, ^{t}RP, ^{t}MRW, and ^{t}MRR, etc., are met
- CS# must be held HIGH
- Only REFab or REFpb commands can be in process

The device is ready for normal operation after the clock satisfies ^{t}CH(abs) and ^{t}CL(abs) for a minimum of 2 × ^{t}CK + ^{t}XP.

After the input clock frequency changes, ^{t}CK (MIN) and ^{t}CK (MAX) must be met for each clock cycle.

After the input clock frequency changes, additional MRW commands may be required to set the WR, RL, and so on. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

NO OPERATION (NOP) Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle n when the CKE level is constant for clock cycle n - 1 and clock cycle n. A NOP command has two possible encodings:

1. CS# HIGH at the clock rising edge n.

2. CS# LOW with CA0, CA1, CA2 HIGH at the clock rising edge n.

The NOP command does not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Table 60: Command Truth Table

Notes 1–11 apply to all parameters and conditions

	Command Pins			CA Pins										
	CKE													CK
Command	CK(*n*-1)	CK(*n*)	CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	Edge
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	
				MA6	MA7	X								
REFRESH (per bank)	H	H	L	L	L	H	L	X						
				X										
REFRESH (all banks)	H	H	L	L	L	H	H	X						
				X										
Enter self refresh	H	L	L	L	L	H	X							
				X										
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	
				AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	
				AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	
				X										
Enter DPD	H	L	L	H	H	L	X							
				X										
NOP	H	H	L	H	H	H	X							
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							
NOP	H	H	H	X										
Maintain PD, SREF, DPD [4]	L	L	X	X										

Table 60: Command Truth Table (Continued)

Notes 1–11 apply to all parameters and conditions

Command	Command Pins			CA Pins										CK Edge
	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(*n*-1)	CK(*n*)												
Enter power-down	H	L	H	X										↑
Exit PD, SREF, DPD	L	H	H	X										↑

Notes:
1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses (BA) determine which bank will be operated upon.
3. AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
4. X indicates a “Don’t Care” state, with a defined logic level, either HIGH (H) or LOW (L). For PD, SREF and DPD, CS#, CK and CK# can be floated after t_{CPDED} has been met and until the required exit procedure is initiated as described in their respective entry/exit procedures.
5. Self refresh exit and DPD exit are asynchronous.
6. V_{REF} must be between 0 and V_{DDQ} during self refresh and DPD operation.
7. CAxr refers to command/address bit “x” on the rising edge of clock.
8. CAxf refers to command/address bit “x” on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. The least significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.
11. AB HIGH during a PRECHARGE command indicates that an all-bank precharge will occur. In this case, bank address is a "Don't Care."

Table 61: CKE Truth Table

Notes 1–5 apply to all parameters and conditions; L = LOW; H = HIGH; X = “Don’t Care”

Current State	CKE*n*-1	CKE*n*	CS#	Command *n*	Operation *n*	Next State	Notes
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, 7
Idle power-down	L	L	X	X	Maintain idle power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9

Table 61: CKE Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions; L = LOW; H = HIGH; X = “Don’t Care”

Current State	CKE*n*-1	CKE*n*	CS#	Command *n*	Operation *n*	Next State	Notes
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank(s) active	H	L	H	NOP	Enter active power-down	Active power-down	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down	
	H	L	L	Enter self refresh	Enter self refresh	Self refresh	
	H	L	L	DPD	Enter deep power-down	Deep power-down	
Resetting	H	L	H	NOP	Enter resetting power-down	Resetting power-down	
Other states	H	H	Refer to the command truth table				

Notes:
1. Current state = the state of the device immediately prior to clock edge *n*.
2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
3. CKE*n* = the logic state of CKE at clock rising edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
4. CS# = the logic state of CS# at the clock rising edge *n*.
5. Command *n* = the command registered at clock edge *n*, and operation *n* is a result of command *n*.
6. Power-down exit time (^tXP) must elapse before any command other than NOP is issued.
7. The clock must toggle at least twice prior to the ^tXP period.
8. Upon exiting the resetting power-down state, the device will return to the idle state if $^tINIT5$ has expired.
9. The DPD exit procedure must be followed as described in Deep Power-Down.
10. Self refresh exit time (^tXSR) must elapse before any command other than NOP is issued.
11. The clock must toggle at least twice prior to the ^tXSR time.

Table 62: Current State Bank *n* to Command to Bank *n* Truth Table

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (per bank)	Begin to refresh	Refreshing (per bank)	6
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	7
	MRW	Load value to mode register	MR writing	7
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	7, 8
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9, 10

Table 62: Current State Bank *n* to Command to Bank *n* Truth Table (Continued)

Notes 1–5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Notes
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	9
Reading	READ	Select column and start new read burst	Reading	11, 12
	WRITE	Select column and start write burst	Writing	11, 12, 13
Writing	WRITE	Select column and start new write burst	Writing	11, 12
	READ	Select column and start read burst	Reading	11, 12, 14
Power-on	MRW RESET	Begin device auto initialization	Resetting	7, 9
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:
1. Values in this table apply when both CKE*n* -1 and CKE*n* are HIGH, and after ^{t}XSR or ^{t}XP has been met, if the previous state was power-down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

State	Definition
Idle	The bank or banks have been precharged, and ^{t}RP has been met.
Active	A row in the bank has been activated, and ^{t}RCD has been met. No data bursts or accesses, and no register accesses, are in progress.
Reading	A READ burst has been initiated with auto precharge disabled, and has not yet terminated.
Writing	A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated.

4. The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in the table: Current State Bank *n* to Command to Bank *m*.

State	Starts with...	Ends when...	Notes
Precharging	Registration of a PRECHARGE command	^{t}RP is met	After ^{t}RP is met, the bank is in the idle state.
Row activating	Registration of an ACTIVATE command	^{t}RCD is met	After ^{t}RCD is met, the bank is in the active state.
READ with AP enabled	Registration of a READ command with auto precharge enabled	^{t}RP is met	After ^{t}RP is met, the bank is in the idle state.
WRITE with AP enabled	Registration of a WRITE command with auto precharge enabled	^{t}RP is met	After ^{t}RP is met, the bank is in the idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

State	Starts with...	Ends when...	Notes
Refreshing (per bank)	Registration of a REFRESH (per bank) command	^tRFCpb is met	After ^tRFCpb is met, the bank is in the idle state.
Refreshing (all banks)	Registration of a REFRESH (all banks) command	^tRFCab is met	After ^tRFCab is met, the device is in the all banks idle state.
Idle MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the device is in the all banks idle state.
Active MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	^tMRW is met	After ^tMRW is met, the device is in the all banks idle state.
Precharging all	Registration of a PRECHARGE ALL command	^tRP is met	After ^tRP is met, the device is in the all banks idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, ^tRP still applies.
11. A command other than NOP should not be issued to the same bank while a READ or WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued only after the completion of the READ burst.
14. A READ command can be issued only after completion of the WRITE burst.

Table 63: Current State Bank *n* to Command to Bank *m* Truth Table

Notes 1–6 apply to all parameters and conditions

Current State of Bank *n*	Command to Bank *m*	Operation	Next State for Bank *m*	Notes
Any	NOP	Continue previous operation	Current state of bank *m*	
Idle	Any	Any command supported to bank *m*	–	
Row activating, active, or precharging	ACTIVATE	Select and activate row in bank *m*	Active	6
	READ	Select column and start READ burst from bank *m*	Reading	7
	WRITE	Select column and start WRITE burst to bank *m*	Writing	7
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
	MRR	READ value from mode register	Idle MR reading or active MR reading	9, 10, 11

Table 63: Current State Bank *n* to Command to Bank *m* Truth Table (Continued)

Notes 1–6 apply to all parameters and conditions

Current State of Bank *n*	Command to Bank *m*	Operation	Next State for Bank *m*	Notes
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank *m*	Reading	7
	WRITE	Select column and start WRITE burst to bank *m*	Writing	7, 12
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank *m*	Reading	7, 13
	WRITE	Select column and start WRITE burst to bank *m*	Writing	7
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
Reading with auto precharge	READ	Select column and start READ burst from bank *m*	Reading	7, 14
	WRITE	Select column and start WRITE burst to bank *m*	Writing	7, 12, 14
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
Writing with auto precharge	READ	Select column and start READ burst from bank *m*	Reading	7, 13, 14
	WRITE	Select column and start WRITE burst to bank *m*	Writing	7, 14
	ACTIVATE	Select and activate row in bank *m*	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
Power-on	MRW RESET	Begin device auto initialization	Resetting	15, 16
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:
1. This table applies when:
   1a. the previous state was self refresh or power-down;
   1b. after ^tXSR or ^tXP has been met;
   1c. *and* both CKE*n* -1 and CKE*n* are HIGH
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

State	Condition	And...	And...
Idle	The bank has been pre-charged	^tRP is met	
Active	A row in the bank has been activated	^tRCD is met	No data bursts/accesses and no register accesses are in progress.

State	Condition	And...	And...
Reading	A READ burst has been initiated with auto precharge disabled	The READ has not yet terminated	
Writing	A WRITE burst has been initiated with auto precharge disabled	The WRITE has not yet terminated	

4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.
5. The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

State	Starts with...	Ends when...	Notes
Idle MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the device is in the all banks idle state.
Resetting MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the device is in the all banks idle state.
Active MR reading	Registration of the MRR command	^tMRR is met	After ^tMRR is met, the bank is in the active state.
MR writing	Registration of the MRW command	^tMRW is met	After ^tMRW is met, the device is in the all banks idle state.

6. ^tRRD must be met between the ACTIVATE command to bank *n* and any subsequent ACTIVATE command to bank *m*.
7. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
8. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is supported in the row-activating state.
10. MRR is supported in the precharging state.
11. The next state for bank *m* depends on the current state of bank *m* (idle, row-activating, precharging, or active).
12. A WRITE command can be issued only after the completion of the READ burst.
13. A READ command can be issued only after the completion of the WRITE burst.
14. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks, provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
15. Not bank-specific; requires that all banks are idle and no bursts are in progress.
16. RESET command is achieved through the MODE REGISTER WRITE command.

Table 64: DM Truth Table

Functional Name	DM	DQ	Notes
Write enable	L	Valid	1
Write inhibit	H	X	1

Note: 1. Used to mask write data; provided simultaneously with the corresponding input data.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 65: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	–0.4	2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	–0.4	1.6	V	1
V_{DDCA} supply voltage relative to V_{SSCA}	V_{DDCA}	–0.4	1.6	V	1, 2
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.4	1.6	V	1, 3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	1.6	V	
Storage temperature	T_{STG}	–55	+125	˚C	4

Notes:
1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. $V_{REFCA} \leq 0.6 \leq V_{DDCA}$; however, V_{REFCA} may be $\geq V_{DDCA}$, provided that $V_{REFCA} \leq$ 300mV.
3. $V_{REFDQ} \leq 0.6 \leq V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$, provided that $V_{REFDQ} \leq$ 300mV.
4. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Input/Output Capacitance

Table 66: Input/Output Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	LPDDR3 1600-1333		Unit	Notes
		Min	Max		
Input capacitance, CK and CK#	C_{CK}	0.7	1.4	pF	2, 3
Input capacitance delta, CK and CK#	C_{DCK}	0	0.15	pF	2, 3, 4
Input capacitance, all other input-only pins	C_I	0.7	1.3	pF	2, 3, 5
Input capacitance delta, all other input-only pins	C_{DI}	–0.20	0.20	pF	2, 3, 6
Input/output capacitance, DQ, DM, DQS, DQS#	C_{IO}	1.0	1.8	pF	2, 3, 7, 8
Input/output capacitance delta, DQS, DQS#	C_{DDQS}	0	0.2	pF	2, 3, 8, 9
Input/output capacitance delta, DQ, DM	C_{DIO}	–0.25	0.25	pF	2, 3, 8, 10
Input/output capacitance, ZQ	C_{ZQ}	0	2.0	pF	2, 3

Notes:
1. T_C = –40˚C to +105˚C; V_{DDQ} = 1.14–1.3V; V_{DDCA} = 1.14–1.3V; V_{DD1} = 1.7–1.95V; V_{DD2} = 1.14–1.3V.
2. This parameter applies to die devices only (does not include package capacitance).
3. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring in-

put capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, and V_{SSQ} applied; all other pins are left floating.

4. Absolute value of CK - CK#.
5. C_I applies to CS#, CKE, and CA[9:0].
6. $C_{DI} = C_I - 0.5 \times (CK + CK\#)$.
7. DM loading matches DQ and DQS.
8. MR3 I/O configuration DS OP[3:0] = 0001b (34.3Ω typical).
9. Absolute value of CDQS and CDQS#.
10. $C_{DIO} = C_{IO} - 0.5 \times (CDQS + CDQS\#)$ in byte-lane.

Electrical Specifications – I_{DD} Specifications and Conditions

The following definitions and conditions are used in the I_{DD} measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)max}$
- HIGH: $V_{IN} \geq V_{IH(DC)min}$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table 67: Switching for CA Input Signals

	CK (Rising)/ CK# (Falling)	CK (Falling)/ CK# (Rising)	CK (Rising)/ CK# (Falling)	CK (Falling)/ CK# (Rising)	CK (Rising)/ CK# (Falling)	CK (Falling)/ CK# (Rising)	CK (Rising)/ CK# (Falling)	CK (Falling)/ CK# (Rising)
Cycle	N		N + 1		N + 2		N + 3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:
1. CS# must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 68: Switching for I_{DD4R}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	HLH	LHLLHLH	L
Rising	H	L	N + 4	Read_Rising	HLH	LHLLHLH	H
Falling	H	L	N + 4	Read_Falling	HHL	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 7	NOP	HLH	LHLHLHL	L

Notes: 1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4R}.

Table 69: Switching for I_{DD4W}

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	LLH	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N + 1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	LLL	LLLLLLL	L
Rising	H	H	N + 2	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 2	NOP	LLL	LLLLLLL	H
Rising	H	H	N + 3	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 3	NOP	LLH	LHLLHLH	L
Rising	H	L	N + 4	Write_Rising	LLH	LHLLHLH	H
Falling	H	L	N + 4	Write_Falling	HHL	HHHHHHH	H
Rising	H	H	N + 5	NOP	HHH	HHHHHHH	H
Falling	H	H	N + 5	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 6	NOP	HHH	HHHHHHH	L
Falling	H	H	N + 6	NOP	HHH	HHHHHHH	L
Rising	H	H	N + 7	NOP	HHH	HHHHHHH	H

Table 69: Switching for I_{DD4W} (Continued)

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Falling	H	H	N + 7	NOP	LLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The noted pattern (N, N + 1...) is used continuously during I_{DD} measurement for I_{DD4W}.

Table 70: I_{DD} Specification Parameters and Operating Conditions

Notes 1–3 apply for all values

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: ^tCK = ^tCK (MIN); ^tRC = ^tRC (MIN); CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	$I_{DD0,in}$	V_{DDCA}, V_{DDQ}	5
Idle power-down standby current: ^tCK = ^tCK (MIN); CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	$I_{DD2P,in}$	V_{DDCA}, V_{DDQ}	5
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDCA}, V_{DDQ}	5
Idle non-power-down standby current: ^tCK = ^tCK (MIN); CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDCA}, V_{DDQ}	5
Idle non-power-down standby current with clock stopped: CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDCA}, V_{DDQ}	5
Active power-down standby current: ^tCK = ^tCK (MIN); CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDCA}, V_{DDQ}	5
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	
	$I_{DD3PS22}$	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	5

Table 70: I_{DD} Specification Parameters and Operating Conditions (Continued)

Notes 1–3 apply for all values

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current: $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	5
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	5
Operating burst READ current: $^tCK = {}^tCK$ (MIN); CS# is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	6
Operating burst WRITE current: $^tCK = {}^tCK$ (MIN); CS# is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	5
All-bank REFRESH burst current: $^tCK = {}^tCK$ (MIN); CKE is HIGH between valid commands; $^tRC = {}^tRFCab$ (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	$I_{DD5,in}$	V_{DDCA}, V_{DDQ}	5
All-bank REFRESH average current: $^tCK = {}^tCK$ (MIN); CKE is HIGH between valid commands; $^tRC = {}^tREFI$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	5
Per-bank REFRESH average current: $^tCK = {}^tCK$ (MIN); CKE is HIGH between valid commands; $^tRC = {}^tREFI/8$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	5
Self refresh current (–40˚C to +85˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	7
	I_{DD62}	V_{DD2}	7
	$I_{DD6,in}$	V_{DDCA}, V_{DDQ}	5, 7
Self refresh current (+85˚C to +105˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD6ET1}	V_{DD1}	7, 8
	I_{DD6ET2}	V_{DD2}	7, 8
	$I_{DD6ET,in}$	V_{DDCA}, V_{DDQ}	5, 7, 8

Table 70: I_{DD} Specification Parameters and Operating Conditions (Continued)

Notes 1–3 apply for all values

Parameter/Condition	Symbol	Power Supply	Notes
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD81}	V_{DD1}	8
	I_{DD82}	V_{DD2}	8
	$I_{DD8,in}$	V_{DDCA}, V_{DDQ}	5, 8, 9

Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.
4. ODT disabled: MR11[2:0] = 000b.
5. Measured currents are the summation of V_{DDQ} and V_{DDCA}.
6. Guaranteed by design with output reference load and $R_{ON} = 40\Omega$.
7. This is the general definition that applies to full-array SELF REFRESH.
8. I_{DD6ET} and I_{DD8} are typical values, are sampled only, and are not tested.
9. CKE must be ≤ V_{ILCKE}.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 71: Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit
V_{DD1}[1]	1.70	1.80	1.95	Core power 1	V
V_{DD2}	1.14	1.20	1.30	Core power 2	V
V_{DDCA}	1.14	1.20	1.30	Input buffer power	V
V_{DDQ}	1.14	1.20	1.30	I/O buffer power	V

Note: 1. V_{DD1} uses significantly less power than V_{DD2}.

Table 72: Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current: For CA, CKE, CS#, CK, CK#; Any input 0V ≤ V_{IN} ≤ V_{DDCA}; (All other pins not under test = 0V)	I_I	–2	2	µA	1
V_{REF} supply leakage current: V_{REFDQ} = V_{DDQ}/2, or V_{REFCA} = V_{DDCA}/2; (All other pins not under test = 0V)	I_{VREF}	–1	1	µA	2

Notes:
1. Although DM is for input only, the DM leakage must match the DQ and DQS/DQS# output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Table 73: Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
WT temperature range	T_{CASE}[1]	–30	+85	°C
AT temperature range		–40	+105	°C

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the operating temperature range. For example, T_{CASE} could be above +85°C when the temperature sensor indicates a temperature of less than +85°C.

AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 74: Single-Ended AC and DC Input Levels for CA and CS# Inputs

Parameter	Symbol	Min	Max	Unit	Notes
AC input logic HIGH	$V_{IHCA(AC)}$	V_{REF} + 0.150	Note 2	V	1, 2
AC input logic LOW	$V_{ILCA(AC)}$	Note 2	V_{REF} - 0.150	V	1, 2
DC input logic HIGH	$V_{IHCA(DC)}$	V_{REF} + 0.100	V_{DDCA}	V	1
DC input logic LOW	$V_{ILCA(DC)}$	V_{SSCA}	V_{REF} - 0.100	V	1
Reference voltage for CA and CS# inputs	$V_{REFCA(DC)}$	0.49 × V_{DDCA}	0.51 × V_{DDCA}	V	3, 4

Notes:
1. For CA and CS# input-only pins. $V_{REF} = V_{REFCA(DC)}$.
2. See figure: Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFCA} could prevent V_{REFCA} from deviating more than ±1% V_{DDCA} from $V_{REFCA(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately V_{DDCA}/2 ±12mV.

Table 75: Single-Ended AC and DC Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Notes
CKE input HIGH level	V_{IHCKE}	0.65 × V_{DDCA}	Note 1	V	1
CKE input LOW level	V_{ILCKE}	Note 1	0.35 × V_{DDCA}	V	1

Note:
1. See figure: Overshoot and Undershoot Definition.

Table 76: Single-Ended AC and DC Input Levels for DQ and DM

Parameter	Symbol	Min	Max	Unit	Notes
AC input logic HIGH	$V_{IHDQ(AC)}$	V_{REF} + 0.150	Note 2	V	1, 2
AC input logic LOW	$V_{ILDQ(AC)}$	Note 2	V_{REF} - 0.150	V	1, 2
DC input logic HIGH	$V_{IHDQ(DC)}$	V_{REF} + 0.100	V_{DDQ}	V	1
DC input logic LOW	$V_{ILDQ(DC)}$	V_{SSQ}	V_{REF} - 0.100	V	1
Reference voltage for DQ and DM inputs	$V_{REFDQ(DC)}$	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	3, 4
Reference voltage for DQ and DM inputs (DQ ODT enabled)	$V_{REFDQ(DC)}$ DQODT,enabled	V_{ODTR}/2 - 0.01 × V_{DDQ}	V_{ODTR}/2 + 0.01 × V_{DDQ}	V	3, 4, 5

Notes:
1. For DQ input-only pins. $V_{REF} = V_{REFDQ(DC)}$.
2. See figure: Overshoot and Undershoot Definition.
3. The AC peak noise on V_{REFDQ} could prevent V_{REFDQ} from deviating more than ±1% V_{DDQ} from $V_{REFDQ(DC)}$ (for reference, approximately ±12mV).
4. For reference, approximately V_{DDQ}/2 ±12mV.
5. The nominal mode register programmed values for R_{ODT} and the nominal controller output impedance R_{ON} are used for the calculation of V_{ODTR}:

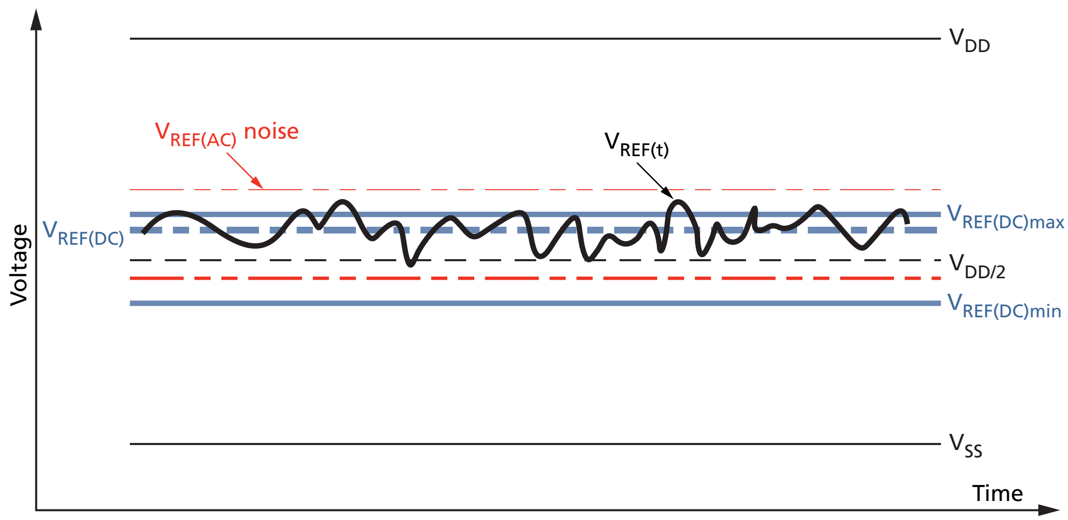
$$V_{OTDR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

For testing purposes, a controller R_{ON} value of 50Ω is used.

V_{REF} Tolerances

The DC tolerance limits and AC noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are shown below. This figure shows a valid reference voltage $V_{REF}(t)$ as a function of time. V_{DD} is used in place of V_{DDCA} for V_{REFCA}, and V_{DDQ} for V_{REFDQ}. $V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (for example, 1 second), and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA}, also over a very long period of time (for example, 1 second). This average must meet the MIN/MAX requirements in the table: Single-Ended AC and DC Input Levels for CA and CS# Inputs. Additionally, $V_{REF}(t)$ can temporarily deviate from $V_{REF(DC)}$ by no more than ±1% V_{DD}. $V_{REF}(t)$ cannot track noise on V_{DDQ} or V_{DDCA} if doing so would force V_{REF} outside these specifications.

Figure 90: V_{REF} DC Tolerance and V_{REF} AC Noise Limits



The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{REF}.

V_{REF} DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When V_{REF} is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

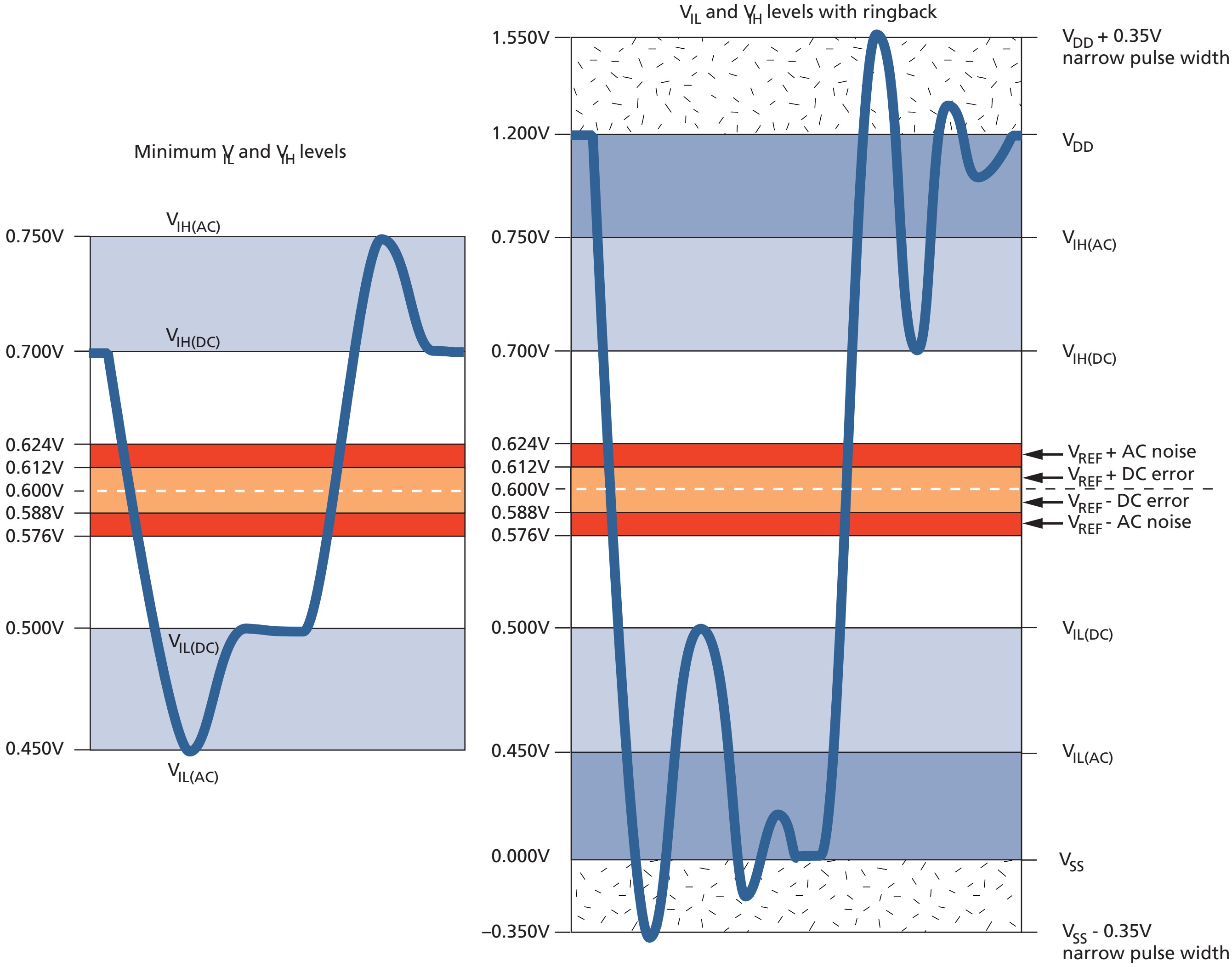
- V_{REF} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}), *and*
- the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF} (see the table: Single-Ended AC and DC Input Levels for DQ and DM).

System timing and voltage budgets must account for V_{REF} deviations outside this range.

The setup/hold specification and derating values must include time and voltage associated with V_{REF} AC noise. Timing and voltage effects due to AC noise on V_{REF} up to the specified limit (±1% V_{DD}) are included in device timings and associated deratings.

Input Signal

Figure 91: LPDDR3-1600 to LPDDR3-1333 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, CK#, and CS#, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, DQS#, and ODT, V_{DD} stands for V_{DDQ}.
3. For CA[9:0], CK, CK#, and CS#, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, DQS#, and ODT, V_{SS} stands for V_{SSQ}.

AC and DC Logic Input Measurement Levels for Differential Signals

Figure 92: Differential AC Swing Time and ^{t}DVAC

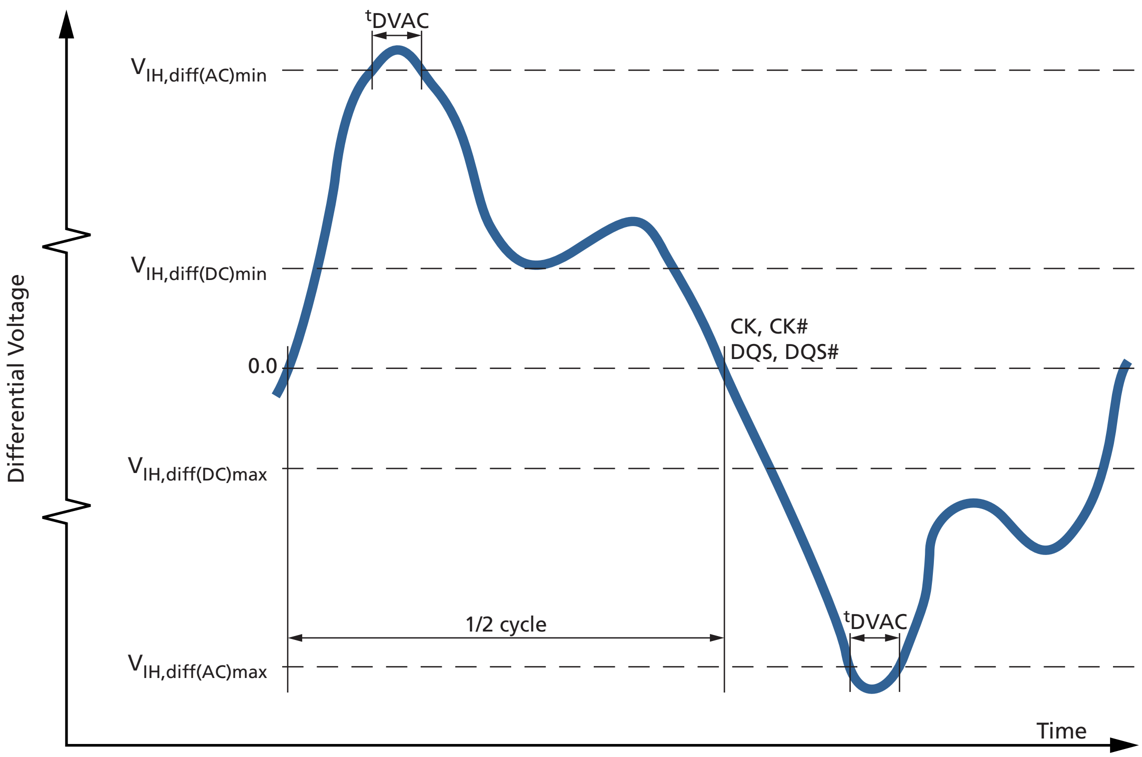


Table 77: Differential AC and DC Input Levels

For CK and CK#, $V_{REF} = V_{REFCA(DC)}$; For DQS and DQS#, $V_{REF} = V_{REFDQ(DC)}$

Parameter	Symbol	LPDDR3-1600 to LPDDR3-800		Unit	Notes
		Min	Max		
Differential input HIGH AC	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	V	2
Differential input LOW AC	$V_{IL,diff(AC)}$	Note 1	$2 \times (V_{REF} - V_{IL(AC)})$	V	2
Differential input HIGH DC	$V_{IH,diff(DC)}$	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	V	3
Differential input LOW DC	$V_{IL,diff(DC)}$	Note 1	$2 \times (V_{REF} - V_{IL(DC)})$	V	3

Notes:
1. These values are not defined; however, the single-ended signals CK, CK#, DQS, and DQS# must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (see figure: Overshoot and Undershoot Definition).
2. For CK and CK#, use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS and DQS#, use $V_{IH}/V_{IL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. Used to define a differential signal slew rate.

Table 78: CK/CK# and DQS/DQS# Time Requirements Before Ringback (^tDVAC)

Slew Rate (V/ns)	^tDVAC (ps) @ $V_{IH}/V_{IL,diff(AC)}$ = 300mV1333Mbps		^tDVAC (ps) @ $V_{IH}/V_{IL,diff(AC)}$ = 300mV1600Mbps	
	Min	Max	Min	Max
>8.0	58	–	48	–
8.0	58	–	48	–
7.0	56	–	46	–
6.0	53	–	43	–
5.0	50	–	40	–
4.0	45	–	35	–
3.0	37	–	27	–
<30.0	37	–	27	–

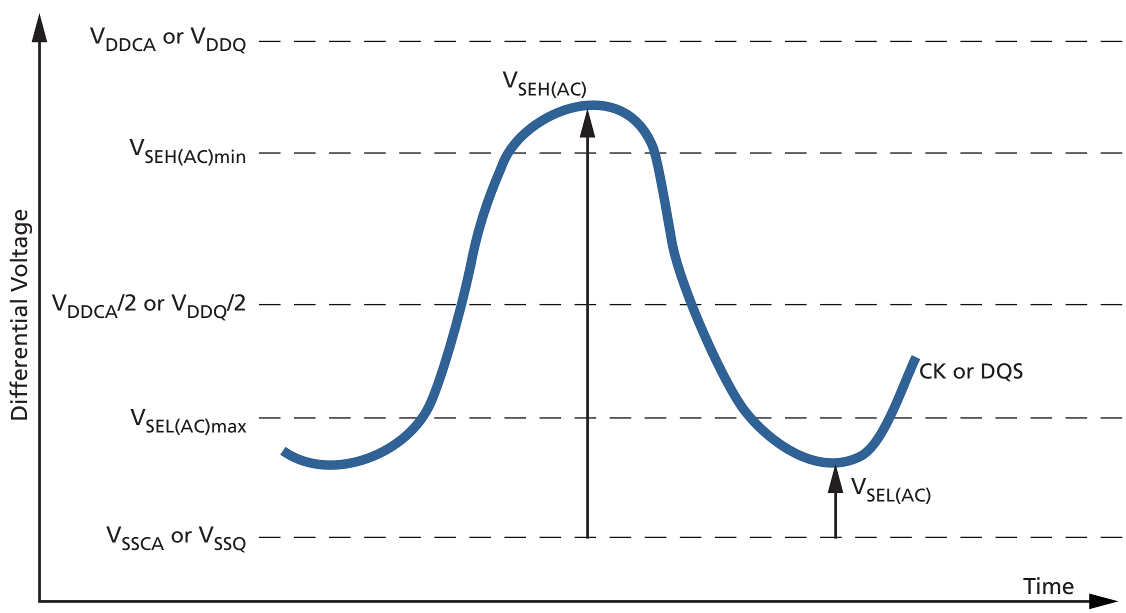
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, CK#, DQS, and DQS#) must also comply with certain requirements for single-ended signals.

CK and CK# must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle. DQS, DQS# must meet $V_{SEH(AC)min}/V_{SEL(AC)max}$ in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.

Figure 93: Single-Ended Requirements for Differential Signals



Note: While CA and DQ signal requirements are referenced to V_{REF}, the single-ended components of differential signals also have a requirement with respect to $V_{DDQ}/2$ for DQS, and $V_{DDCA}/2$ for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)max}$ or $V_{SEH(AC)min}$ has no bearing on timing; however, this requirement adds a restriction on the common mode characteristics of these signals (see tables: Single-Ended AC and DC Input Levels for CA and CS# Inputs; Single-Ended AC and DC Input Levels for DQ and DM).

Table 79: Single-Ended Levels for CK, CK#, DQS, DQS#

Parameter	Symbol	LPDDR3-1600 to LPDDR3-800		Unit	Notes
		Min	Max		
Single-ended HIGH level for strobes	$V_{SEH(AC)}$	$(V_{DDQ}/2) + 0.150$	Note 1	V	2, 3
Single-ended HIGH level for CK, CK#		$(V_{DDCA}/2) + 0.150$	Note 1	V	2, 3
Single-ended LOW level for strobes	$V_{SEL(AC)}$	Note 1	$(V_{DDQ}/2) - 0.150$	V	2, 3
Single-ended LOW level for CK, CK#		Note 1	$(V_{DDCA}/2) - 0.150$	V	2, 3

Notes:
1. These values are not defined; however, the single-ended signals CK, CK#, DQS[3:0], and DQS#[3:0] must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot (see figure: Overshoot and Undershoot Definition).
2. For CK and CK#, use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and DQS#[3:0]), use $V_{IH}/V_{IL(AC)}$ of DQ.
3. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times, as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK, CK#, DQS, and DQS#) must meet the specifications in the table above. The differential input crosspoint voltage (V_{IX}) is measured from the actual crosspoint of the true signal and its and complement to the midlevel between V_{DD} and V_{SS}.

Figure 94: V_{IX} Definition

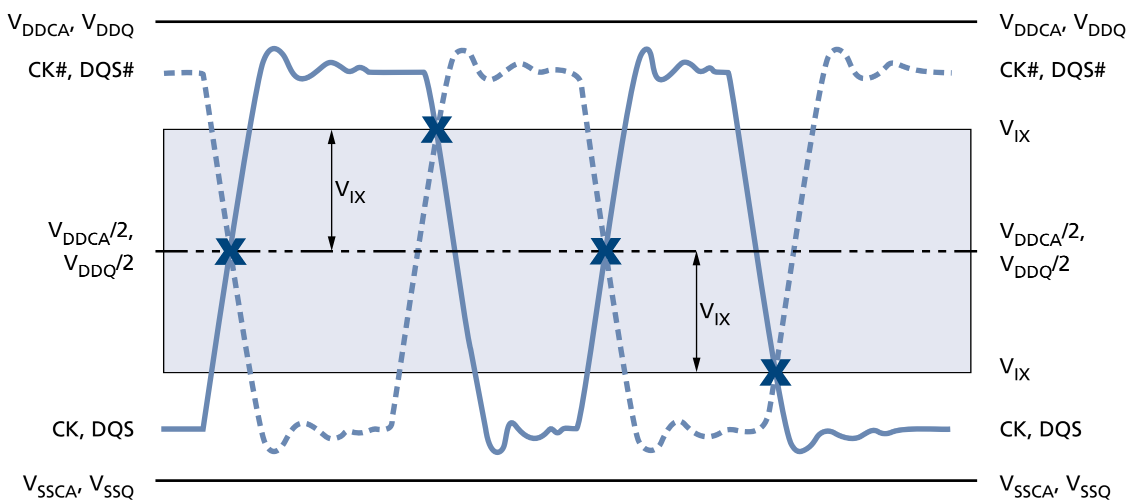


Table 80: Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#)

Parameter	Symbol	Min	Max	Unit	Notes
Differential input crosspoint voltage relative to $V_{DDCA}/2$ for CK and CK#	$V_{IXCA(AC)}$	–120	120	mV	1, 2
Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS and DQ#	$V_{IXDQ(AC)}$	–120	120	mV	1, 2

Notes:
1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK and CK#, $V_{REF} = V_{REFCA(DC)}$. For DQS and DQS#, $V_{REF} = V_{REFDQ(DC)}$.

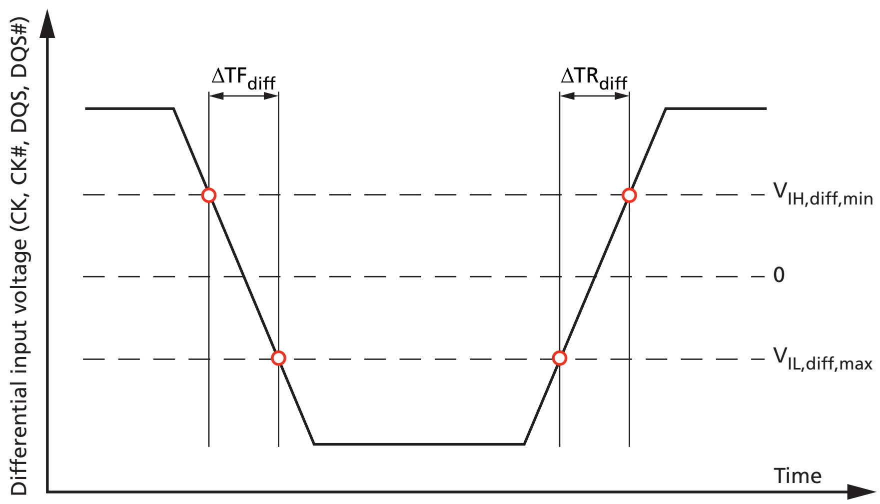
Input Slew Rate

Table 81: Differential Input Slew Rate Definition

Description	Measured[1]		Defined By
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$(V_{IH,diff,min} - V_{IL,diff,max}) / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$(V_{IH,diff,min} - V_{IL,diff,max}) / \Delta TF_{diff}$

Note: 1. The differential signals (CK/CK# and DQS/DQS#) must be linear between these thresholds.

Figure 95: Differential Input Slew Rate Definition for CK, CK#, DQS, and DQS#



Output Characteristics and Operating Conditions

Table 82: Single-Ended AC and DC Output Levels

Parameter	Symbol	Value	Unit	Notes
AC output HIGH measurement level (for output slew rate)	$V_{OH(AC)}$	V_{REF} + 0.12	V	
AC output LOW measurement level (for output slew rate)	$V_{OL(AC)}$	V_{REF} - 0.12	V	
DC output HIGH measurement level (for I-V curve linearity)	$V_{OH(DC)}$	0.9 × V_{DDQ}	V	1
DC output LOW measurement level (for I-V curve linearity)	$V_{OL(DC)}$	0.1 × V_{DDQ}		2
DC output LOW measurement level (for I-V curve linearity); ODT enabled	$V_{OL(DC)ODT,enabled}$	V_{DDQ} × {0.1 + 0.9 × [R_{ON} / (R_{TT} + R_{ON})]}	V	3
Output leakage current (DQ, DM, DQS, DQS#); DQ, DQS, DQS# are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	I_{OZ}	–5 (MIN)	µA	
		5 (MAX)		
Delta output impedance between pull-up and pull-down for DQ/DM	MM_{PUPD}	–15 (MIN)	%	
		15 (MAX)		

Notes: 1. I_{OH} = –0.1mA.
2. I_{OL} = 0.1mA.
3. The minimum value is derived when using $R_{TT,min}$ and $R_{ON,max}$ (+/-30% uncalibrated, +/-15% calibrated).

Table 83: Differential AC and DC Output Levels

Parameter	Symbol	Value	Unit
AC differential output HIGH measurement level (for output SR)	$V_{OH,diff(AC)}$	0.2 x V_{DDQ}	V
AC differential output LOW measurement level (for output SR)	$V_{OL,diff(AC)}$	–0.2 x V_{DDQ}	V

Single-Ended Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 84: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 96: Single-Ended Output Slew Rate Definition

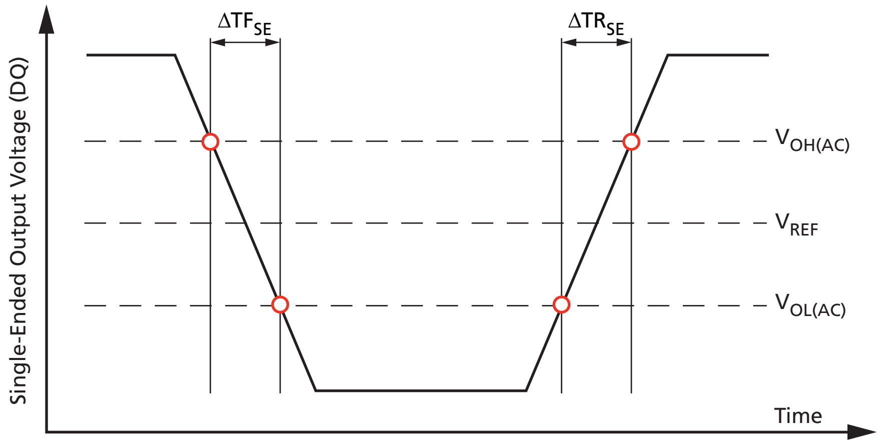


Table 85: Single-Ended Output Slew Rate

Notes 1–5 apply to all parameters conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended output slew rate (output impedance = 40Ω ±30%)	SRQ_{SE}	1.5	4.0	V/ns
Output slew-rate-matching ratio (pull-up to pull-down)	–	0.7	1.4	–

Notes:
1. Definitions: SR = slew rate; Q = query output (similar to DQ = data-in, query output); SE = single-ended signals.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one half of DQ signals per data byte driving HIGH and one half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 86: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}] / \Delta TF_{diff}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production testing.

Figure 97: Differential Output Slew Rate Definition

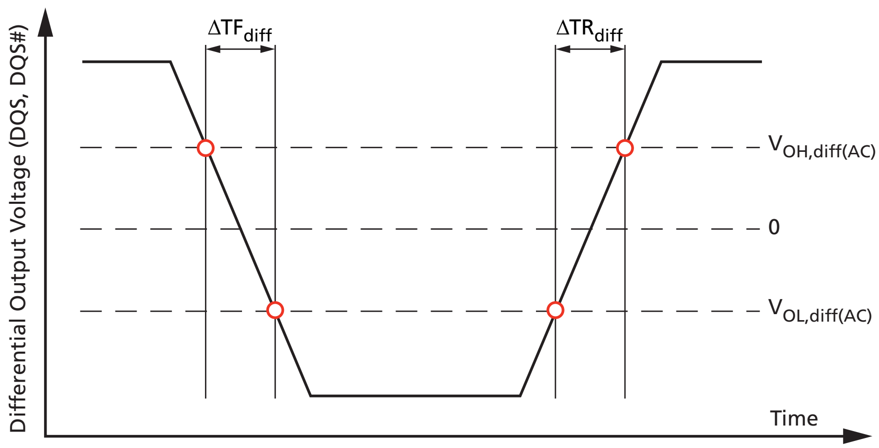


Table 87: Differential Output Slew Rate

Parameter	Symbol	Min	Max	Unit
Differential output slew rate (output impedance = 40Ω ±30%)	SRQ_{diff}	3.0	8.0	V/ns

Notes:
1. Definitions: SR = slew rate; Q = query output (similar to DQ = data-in, query output); diff = differential signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one half of DQ signals per data byte driving HIGH and one half of DQ signals per data byte driving LOW.

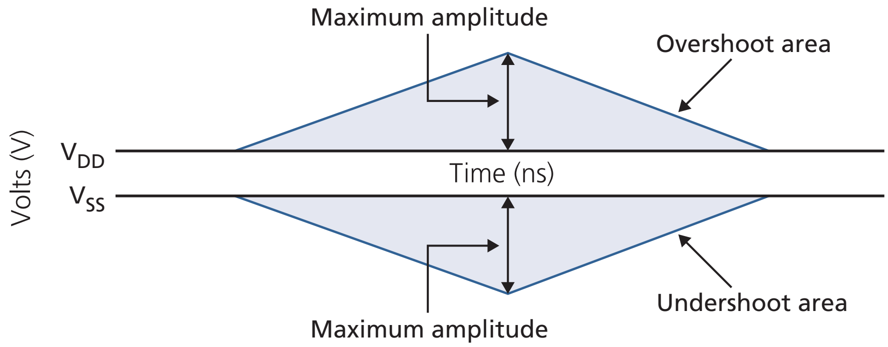
Table 88: AC Overshoot/Undershoot Specification

Applies to CA[9:0], CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM, and ODT.

Parameter	1600	1333	Unit	Notes
Maximum peak amplitude provided for overshoot area	0.35	0.35	V	
Maximum peak amplitude provided for undershoot area	0.35	0.35	V	
Maximum area above V_{DD}	0.10	0.12	V/ns	1
Maximum area below V_{SS}	0.10	0.12	V/ns	2

Notes: 1. $V_{DD} = V_{DDCA}$ for CA[9:0], CK, CK#, CS#, and CKE. V_{DD} stands for V_{DDQ} for DQ, DM, DQS, DQS#, and ODT.
2. $V_{SS} = V_{SSCA}$ for CA[9:0], CK, CK#, CS#, and CKE. V_{SS} stands for V_{SSQ} for DQ, DM, DQS, DQS#, and ODT.

Figure 98: Overshoot and Undershoot Definition

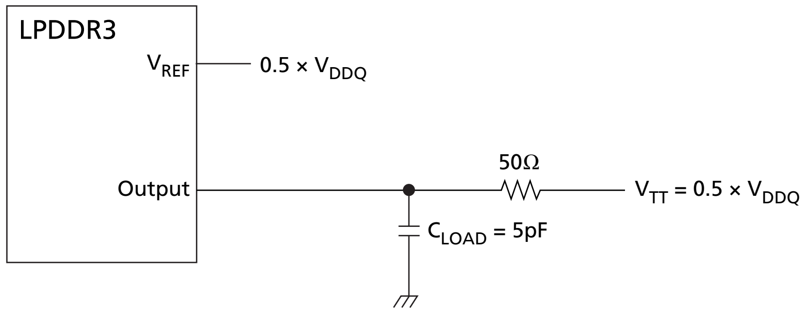


Notes: 1. $V_{DD} = V_{DDCA}$ for CA[9:0], CK, CK#, CS#, and CKE. $V_{DD} = V_{DDQ}$ for DQ, DM, DQS, DQS#, and ODT.
2. $V_{SS} = V_{SSCA}$ for CA[9:0], CK, CK#, CS#, and CKE. $V_{SS} = V_{SSQ}$ for DQ, DM, DQS, DQS#, and ODT.

HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.

Figure 99: HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note: 1. All output timing parameter values (^{t}DQSCK, ^{t}DQSQ, ^{t}HZ, ^{t}RPRE, etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance

Output driver impedance is selected by a mode register during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output drive unless specifically stated otherwise. The output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

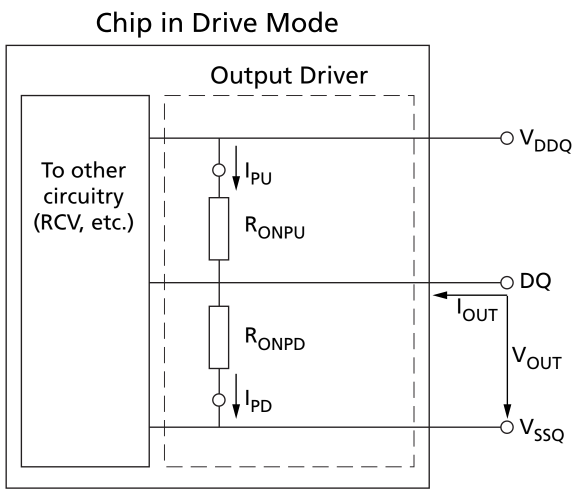
$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPD} is turned off.

$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPU} is turned off.

Figure 100: Output Driver



Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor R_{ZQ}. Typical R_{ZQ} is 240Ω.

Table 89: Output Driver DC Electrical Characteristics with ZQ Calibration

Notes 1–4 apply to all parameters and conditions

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit	Notes
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	
	R_{ON34PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	
	R_{ON40PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	
	R_{ON48PU}	0.5 × V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	
Mismatch between pull-up and pull-down	MM_{PUPD}	–	–15.00	–	15.00	%	5

Notes:
1. Applies across entire operating temperature range after calibration.
2. R_{ZQ} = 240Ω.
3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see Output Driver Temperature and Voltage Sensitivity.
4. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x V_{DDQ}.
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure R_{ONPU} and R_{ONPD}, both at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

For example, with MM_{PUPD} (MAX) = 15% and R_{ONPD} = 0.85, R_{ONPU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen.

Table 90: Output Driver Sensitivity Definition

Notes 1 and 2 apply to all parameters and conditions.

Resistor	V_{OUT}	Min	Max	Unit
R_{ONPD}	0.5 × V_{DDQ}	85 - ($dR_{ON}dT$ × |ΔT|) - ($dR_{ON}dV$ × |ΔV|)	115 - ($dR_{ON}dT$ × |ΔT|) - ($dR_{ON}dV$ × |ΔV|)	%
R_{ONPU}				

Notes:
1. ΔT = T - T (at calibration). ΔV = V - V (at calibration).
2. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production testing; they are verified by design and characterization.

Table 91: Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dR_{ONdT}	R_{ON} temperature sensitivity	0.00	0.75	%/˚C
dR_{ONdV}	R_{ON} voltage sensitivity	0.00	0.20	%/mV
dR_{TTdT}	R_{TT} temperature sensitivity	0.00	0.75	%/˚C
dR_{TTdV}	R_{TT} voltage sensitivity	0.00	0.20	%/mV

Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Table 92: Output Driver DC Electrical Characteristics Without ZQ Calibration

Notes 1 and 2 apply to all parameters and conditions.

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/7
	R_{ON34PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/7
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/6
	R_{ON40PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/6
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/5
	R_{ON48PU}	0.5 × V_{DDQ}	0.70	1.00	1.30	R_{ZQ}/5

Notes:
1. Applies across entire operating temperature range without calibration.
2. R_{ZQ} = 240Ω.

Table 93: I-V Curves

	R_{ON} = 240Ω (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current (mA) / R_{ON} (Ω)				Current (mA) / R_{ON} (Ω)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
Voltage (V)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.00	0.00	0.00	N/A	N/A	0.00	0.00	N/A	N/A
0.05	0.17	0.35	N/A	N/A	–0.17	–0.35	N/A	N/A
0.10	0.34	0.70	N/A	N/A	–0.34	–0.70	N/A	N/A
0.15	0.50	1.03	N/A	N/A	–0.50	–1.03	N/A	N/A
0.20	0.67	1.39	N/A	N/A	–0.67	–1.39	N/A	N/A
0.25	0.83	1.73	N/A	N/A	–0.83	–1.73	N/A	N/A
0.30	0.97	2.05	N/A	N/A	–0.97	–2.05	N/A	N/A
0.35	1.13	2.39	N/A	N/A	–1.13	–2.39	N/A	N/A
0.40	1.26	2.71	N/A	N/A	–1.26	–2.71	N/A	N/A
0.45	1.39	3.01	N/A	N/A	–1.39	–3.01	N/A	N/A

Table 93: I-V Curves (Continued)

	R_{ON} = 240Ω (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current (mA) / R_{ON} (Ω)				Current (mA) / R_{ON} (Ω)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
Voltage (V)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.50	1.51	3.32	N/A	N/A	–1.51	–3.32	N/A	N/A
0.55	1.63	3.63	N/A	N/A	–1.63	–3.63	N/A	N/A
0.60	1.73	3.93	2.17	2.94	–1.73	–3.93	–2.17	–2.94
0.65	1.82	4.21	N/A	N/A	–1.82	–4.21	N/A	N/A
0.70	1.90	4.49	N/A	N/A	–1.90	–4.49	N/A	N/A
0.75	1.97	4.74	N/A	N/A	–1.97	–4.74	N/A	N/A
0.80	2.03	4.99	N/A	N/A	–2.03	–4.99	N/A	N/A
0.85	2.07	5.21	N/A	N/A	–2.07	–5.21	N/A	N/A
0.90	2.11	5.41	N/A	N/A	–2.11	–5.41	N/A	N/A
0.95	2.13	5.59	N/A	N/A	–2.13	–5.59	N/A	N/A
1.00	2.17	5.72	N/A	N/A	–2.17	–5.72	N/A	N/A
1.05	2.19	5.84	N/A	N/A	–2.19	–5.84	N/A	N/A
1.10	2.21	5.95	N/A	N/A	–2.21	–5.95	N/A	N/A
1.15	2.23	6.03	N/A	N/A	–2.23	–6.03	N/A	N/A
1.20	2.25	6.11	N/A	N/A	–2.25	–6.11	N/A	N/A

Figure 101: Output Impedance = 240Ω, I-V Curves After ZQ_{RESET}

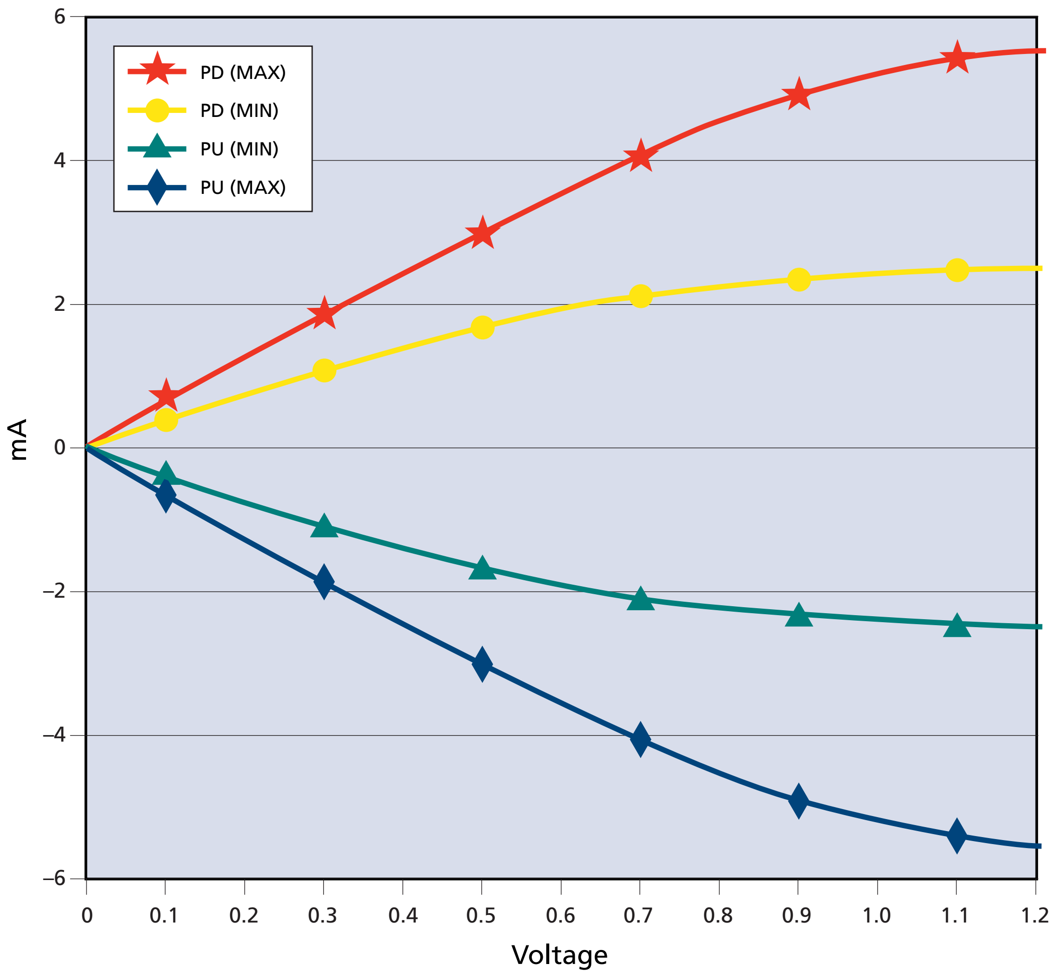
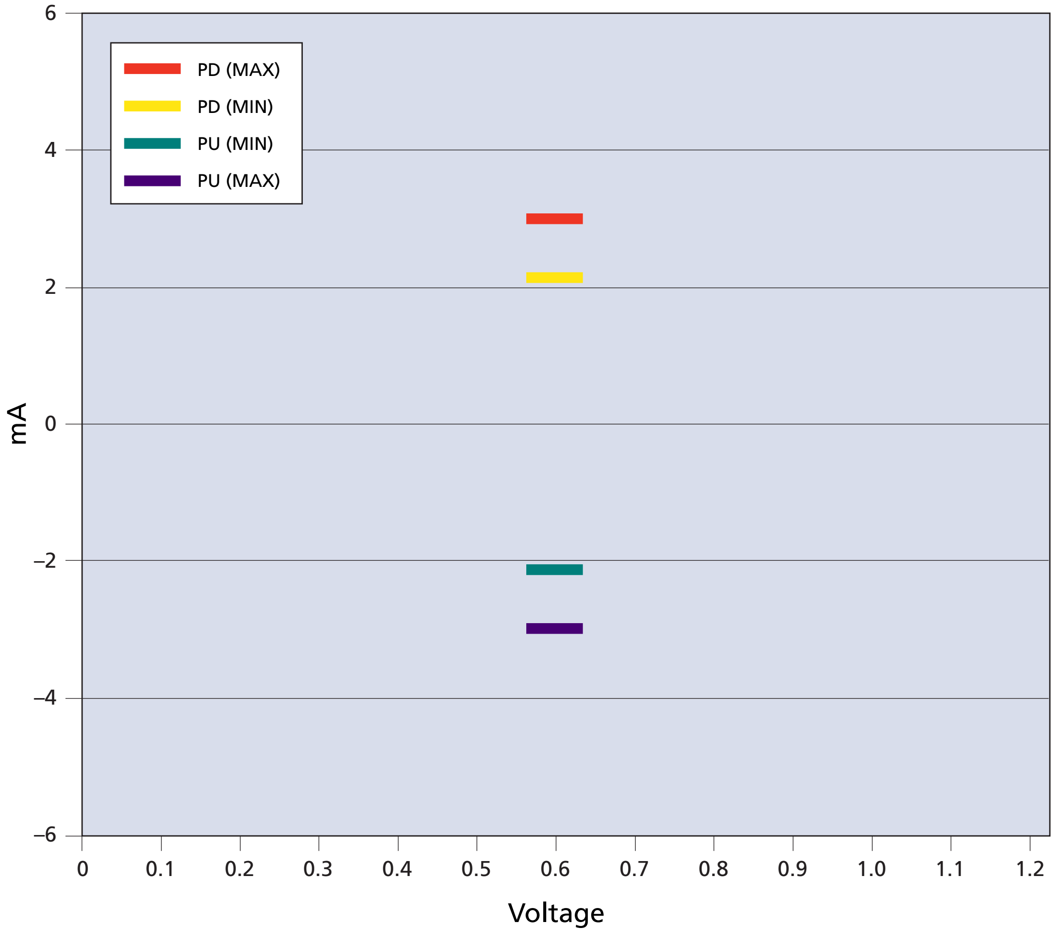


Figure 102: Output Impedance = 240Ω, I-V Curves After Calibration



ODT Levels and I-V Characteristics

ODT effective resistance, R_{TT}, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional block diagram of the on-die termination is shown in the figure below. R_{TT} is defined by the following formua: $R_{TTPU} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$

Figure 103: ODT Functional Block Diagram

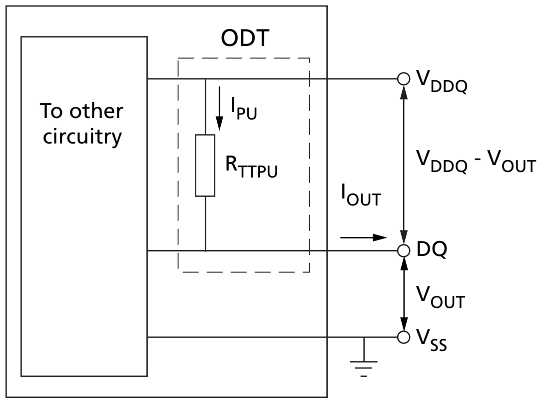


Table 94: ODT DC Electrical Characteristics (R_{ZQ} = 240Ω After Proper ZQ Calibration)

R_{TT} (Ω)	V_{OUT}	I_{OUT}	
		Min (mA)	Max (mA)
$R_{ZQ}/1$	0.6	–2.17	–2.94
$R_{ZQ}/2$	0.6	–4.34	–5.88

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 95: Definitions and Calculations

Symbol	Description	Calculation	Notes
^{t}CK(avg) and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit ^{t}CK(avg) represents the actual clock average ^{t}CK(avg) of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. ^{t}CK(avg)can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$^tCK(avg) = \left(\sum_{j=1}^{N} {^tCK_j}\right)/N$ Where N = 200	
^{t}CK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
^{t}CH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$^tCH(avg) = \left(\sum_{j=1}^{N} {^tCH_j}\right)/(N \times {^tCK(avg)})$ Where N = 200	
^{t}CL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$^tCL(avg) = \left(\sum_{j=1}^{N} {^tCL_j}\right)/(N \times {^tCK(avg)})$ Where N = 200	
^{t}JIT(per)	The single-period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).	$^tJIT(per) = \text{min/max of } \left({^tCK_i} - {^tCK(avg)}\right)$ Where i = 1 to 200	1
^{t}JIT(per),act	The actual clock jitter for a given system.		
^{t}JIT(per), allowed	The specified clock period jitter allowance.		
^{t}JIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. ^{t}JIT(cc) defines the cycle-to-cycle jitter.	$^tJIT(cc) = \text{max of } \left({^tCK_{i+1}} - {^tCK_i}\right)$	1
^{t}ERR(nper)	The cumulative error across *n* multiple consecutive cycles from ^{t}CK(avg).	$^tERR(nper) = \left(\sum_{j=i}^{i+n-1} {^tCK_j}\right) - (n \times {^tCK(avg)})$	1
^{t}ERR(nper),act	The actual cumulative error over *n* cycles for a given system.		
^{t}ERR(nper), allowed	The specified cumulative error allowance over *n* cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	$^tERR(nper),min = (1 + 0.68LN(n)) \times {^tJIT(per),min}$	2

Table 95: Definitions and Calculations (Continued)

Symbol	Description	Calculation	Notes
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	^{t}ERR(nper),max = (1 + 0.68LN(n)) × ^{t}JIT(per),max	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	^{t}JIT(duty),min = MIN((^{t}CH(abs),min – ^{t}CH(avg),min), (^{t}CL(abs),min – ^{t}CL(avg),min)) × ^{t}CK(avg) ^{t}JIT(duty),max = MAX((^{t}CH(abs),max – ^{t}CH(avg),max), (^{t}CL(abs),max – ^{t}CL(avg),max)) × ^{t}CK(avg)	

Notes: 1. Not subject to production testing.
2. Using these equations, ^{t}ERR(nper) tables can be generated for each ^{t}JIT(per),act value.

^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 96: ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min[2]/^{t}CK(avg)min	^{t}CK(avg)

Notes: 1. ^{t}CK(avg),min is expressed in ps for this table.
2. ^{t}JIT(duty),min is a negative value.

Clock Period Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^tnPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks, or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks ($^t nPARAM$), when $^tCK(avg)$ and $^tERR(^t nPARAM)$,act exceed $^tERR(^t nPARAM)$,allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{^tPARAM + {^tERR}(^tnPARAM),act - {^tERR}(^tnPARAM),allowed}{^tnPARAM} - {^tCK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks ($^t nPARAM$), clock cycle derating should be specified with $^tJIT(per)$.

For a given number of clocks ($^t nPARAM$), when $^tCK(avg)$ plus ($^tERR(^t nPARAM)$,act) exceed the supported cumulative $^tERR(^t nPARAM)$,allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^tCORE), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = RU\left\{\frac{^tPARAM + {^tERR}(^tnPARAM),act - {^tERR}(^tnPARAM),allowed}{^tCK(avg)}\right\} - {^tnPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (^tIS, ^tIH, ^tISCKE, ^tIHCKE, ^tISb, ^tIHb, ^tISCKEb, ^tIHCKEb) are measured from a command/address signal (CKE, CS, or CA[9:0]) transition edge to its respective clock signal (CK/CK#) crossing. The specification values are not affected by the $^tJIT(per)$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

^tRPRE

When the device is operated with input clock jitter, ^tRPRE must be derated by the $^tJIT(per)$,act,max of the input clock that exceeds $^tJIT(per)$,allowed,max. Output deratings are relative to the input clock:

$$^tRPRE(min,derated) = 0.9 - \left(\frac{^tJIT(per),act,max - {^tJIT(per)},allowed,max}{^tCK(avg)}\right)$$

For example, if the measured jitter into a LPDDR3-1600 device has $^tCK(avg)$ = 1250ps, $^tJIT(per)$,act,min = –92ps, and $^tJIT(per)$,act,max = +134ps, then ^tRPRE,min,derated = 0.9 - ($^tJIT(per)$,act,max - $^tJIT(per)$,allowed,max)/$^tCK(avg)$ = 0.9 - (134 - 100)/1250 = 0.8728 $^tCK(avg)$.

^{t}LZ(DQ), ^{t}HZ(DQ), ^{t}DQSCK, ^{t}LZ(DQS), ^{t}HZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where: n = 0, 1, 2, or 3; and m = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by ^{t}JIT(per).

^{t}QSH, ^{t}QSL

These parameters are affected by duty cycle jitter, represented by ^{t}CH(abs)min and ^{t}CL(abs)min. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = min [(^{t}QSH(abs)min × ^{t}CK(avg)min - ^{t}DQSQmax - ^{t}QHSmax), (^{t}QSL(abs)min × ^{t}CK(avg)min - ^{t}DQSQmax - ^{t}QHSmax)]. This minimum data valid window must be met at the target frequency regardless of clock jitter.

^{t}RPST

^{t}RPST is affected by duty cycle jitter, represented by ^{t}CL(abs). Therefore, ^{t}RPST(abs)min can be specified by ^{t}CL(abs)min. ^{t}RPST(abs)min = ^{t}CL(abs)min - 0.05 = ^{t}QSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

^{t}DS, ^{t}DH

These parameters are measured from a data signal (DM*n or* DQ*m*, where n = 0, 1, 2, 3; and m = DQ[31:0]) transition edge to its respective data strobe signal (DQS*n*, DQS*n*#: n = 0,1,2,3) crossing. The specification values are not affected by the amount of ^{t}JIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DSS, ^{t}DSH

These parameters are measured from a data strobe signal crossing (DQS*x*, DQS*x*#) to its clock signal crossing (CK/CK#). The specification values are not affected by the amount of ^{t}JIT(per)) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

^{t}DQSS

^{t}DQSS is measured from the clock signal crossing (CK/CK#) to the first latching data strobe signal crossing (DQS*x*, DQS*x*#). When the device is operated with input clock jitter, this parameter must be derated by the actual ^{t}JIT(per),act of the input clock in excess of ^{t}JIT(per),allowed.

$$^t\text{DQSS(min,derated)} = 0.75 - \left(\frac{^t\text{JIT(per),act,min} - {}^t\text{JIT(per),allowed, min}}{^t\text{CK(avg)}}\right)$$

$$^t\text{DQSS(max,derated)} = 1.25 - \left(\frac{^t\text{JIT(per),act,max} - {}^t\text{JIT(per),allowed, max}}{^t\text{CK(avg)}}\right)$$

For example, if the measured jitter into an LPDDR3-1600 device has ^{t}CK(avg) = 1250ps, ^{t}JIT(per),act,min = -92ps, and ^{t}JIT(per),act,max = +134ps, then:

^{t}DQSS,(min,derated) = 0.75 - (^{t}JIT(per),act,min - ^{t}JIT(per),allowed,min)/^{t}CK(avg) = 0.75 - (-93 + 100)/1250 = 0.7444 ^{t}CK(avg), *and*

^{t}DQSS,(max,derated) = 1.25 - (^{t}JIT(per),act,max - ^{t}JIT(per),allowed,max)/^{t}CK(avg) = 1.25 - (134 - 100)/1250 = 1.2228 ^{t}CK(avg).

Refresh Requirements

Table 97: Refresh Requirement Parameters (Per Density)

Parameter		Symbol	4Gb	8Gb	16Gb	32Gb	Unit
Number of banks		–	8			TBD	
Refresh window: T_{CASE} ≤ 85˚		^{t}REFW	32			TBD	ms
Refresh window: 1/2 rate		^{t}REFW	16			TBD	ms
Refresh window: 1/4 rate		^{t}REFW	8			TBD	ms
Required number of REFRESH commands (MIN)		R	8192			TBD	
Average time between REFRESH commands (for reference only) T_{CASE} ≤ 85˚C	REFab	^{t}REFI	3.9			TBD	µs
	REFpb	^{t}REFIpb	0.4875			TBD	µs
Refresh cycle time		^{t}RFCab	130	210	TBD	TBD	ns
Per-bank REFRESH cycle time		^{t}RFCpb	60	90	TBD	TBD	ns
Burst REFRESH window = 4 × 8 × ^{t}RFCab		^{t}REFBW	4.16	6.72	TBD	TBD	µs

Table 98: Read and Write Latencies

Parameter	LPDDR3 Data Rate							Unit
	333	800	1066	1200	1333	1466	1600	
Maximum clock frequency	166	400	533	600	667	733	800	MHz
Average clock period	6	2.5	1.875	1.67	1.5	1.36	1.25	ns
Read latency	3	6	8	9	10	11	12	^{t}CK(avg)
Write latency (set A)	1	3	4	5	6	6	6	^{t}CK(avg)
Write latency (set B)	1	3	4	5	8	9	9	^{t}CK(avg)

AC Timing

Table 99: AC Timing

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate 1333	Data Rate 1600	Unit
Maximum frequency	–	–	667	800	MHz
Clock Timing					
Average clock period	$^tCK(avg)$	MIN	1.5	1.25	ns
		MAX	100		
Average HIGH pulse width	$^tCH(avg)$	MIN	0.45		$^tCK(avg)$
		MAX	0.55		
Average LOW pulse width	$^tCL(avg)$	MIN	0.45		$^tCK(avg)$
		MAX	0.55		
Absolute clock period	$^tCK(abs)$	MIN	$^tCK(avg)$ MIN + $^tJIT(per)$ MIN		ns
Absolute clock HIGH pulse width	$^tCH(abs)$	MIN	0.43		$^tCK(avg)$
		MAX	0.57		
Absolute clock LOW pulse width	$^tCL(abs)$	MIN	0.43		$^tCK(avg)$
		MAX	0.57		
Clock period jitter (with supported jitter)	$^tJIT(per)$, allowed	MIN	–80	–70	ps
		MAX	80	70	
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	$^tJIT(cc)$, allowed	MAX	160	140	ps
Duty cycle jitter (with supported jitter)	$^tJIT(duty)$, allowed	MIN	min(($^tCH(abs)$,min - $^tCH(avg)$,min), ($^tCL(abs)$,min - $^tCL(avg)$,min)) × $^tCK(avg)$		ps
		MAX	max(($^tCH(abs)$,max - $^tCH(avg)$,max), ($^tCL(abs)$,max - $^tCL(avg)$,max)) × $^tCK(avg)$		
Cumulative errors across 2 cycles	$^tERR(2per)$, allowed	MIN	–118	–103	ps
		MAX	118	103	
Cumulative errors across 3 cycles	$^tERR(3per)$, allowed	MIN	–140	–122	ps
		MAX	140	122	
Cumulative errors across 4 cycles	$^tERR(4per)$, allowed	MIN	–155	–136	ps
		MAX	155	136	
Cumulative errors across 5 cycles	$^tERR(5per)$, allowed	MIN	–168	–147	ps
		MAX	168	147	
Cumulative errors across 6 cycles	$^tERR(6per)$, allowed	MIN	–177	–155	ps
		MAX	177	155	
Cumulative errors across 7 cycles	$^tERR(7per)$, allowed	MIN	–186	–163	ps
		MAX	186	163	
Cumulative errors across 8 cycles	$^tERR(8per)$, allowed	MIN	–193	–169	ps
		MAX	193	169	

Table 99: AC Timing (Continued)

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Cumulative errors across 9 cycles	tERR(9per), allowed	MIN	–200	–175	ps
		MAX	200	175	
Cumulative errors across 10 cycles	tERR(10per), allowed	MIN	–205	–180	ps
		MAX	205	180	
Cumulative errors across 11 cycles	tERR(11per), allowed	MIN	–210	–184	ps
		MAX	210	184	
Cumulative errors across 12 cycles	tERR(12per), allowed	MIN	–215	–188	ps
		MAX	215	188	
Cumulative errors across n = 13, 14, 15…, 19, 20 cycles	tERR(nper), allowed	MIN	tERR(nper),allowed MIN = (1 + 0.68ln(n)) × tJIT(per), allowed MIN		ps
		MAX	tERR (nper), allowed MAX = (1 + 0.68ln(n)) × tJIT(per), allowed MAX		
ZQ Calibration Parameters					
Initialization calibration time	tZQINIT	MIN	1		µs
Long calibration time	tZQCL	MIN	360		ns
Short calibration time	tZQCS	MIN	90		ns
Calibration reset time	tZQRESET	MIN	MAX (50ns, 3nCK)		ns
READ Parameters[5]					
DQS output access time from CK/CK#	tDQSCK	MIN	2500		ps
		MAX	5500		
DQSCK delta short	tDQSCKDS	MAX	265	220	ps
DQSCK delta medium	tDQSCKDM	MAX	593	511	ps
DQSCK delta long	tDQSCKDL	MAX	733	614	ps
DQS-DQ skew	tDQSQ	MAX	165	135	ps
DQS output HIGH pulse width	tQSH	MIN	tCH(abs) - 0.05		tCK(avg)
DQS output LOW pulse width	tQSL	MIN	tCL(abs) - 0.05		tCK(avg)
DQ/DQS output hold time from DQS	tQH	MIN	MIN (tQSH, tQSL)		ps
READ preamble	tRPRE	MIN	0.9		tCK(avg)
READ postamble	tRPST	MIN	0.3		tCK(avg)
DQS Low-Z from clock	tLZ(DQS)	MIN	tDQSCK (MIN) - 300		ps
DQ Low-Z from clock	tLZ(DQ)	MIN	tDQSCK (MIN) - 300		ps
DQS High-Z from clock	tHZ(DQS)	MAX	tDQSCK (MAX) - 100		ps
DQ High-Z from clock	tHZ(DQ)	MAX	tDQSCK (MAX) + (1.4 × tDQSQ (MAX))		ps
WRITE Parameters[5]					
DQ and DM input hold time (V_{REF} based)	tDH	MIN	175	150	ps

Table 99: AC Timing (Continued)

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
DQ and DM input setup time (V_{REF} based)	^tDS	MIN	175	150	ps
DQ and DM input pulse width	^tDIPW	MIN	0.35		$^tCK(avg)$
Write command to first DQS latching transition	^tDQSS	MIN	0.75		$^tCK(avg)$
		MAX	1.25		
DQS input high-level width	^tDQSH	MIN	0.4		$^tCK(avg)$
DQS input low-level width	^tDQSL	MIN	0.4		$^tCK(avg)$
DQS rising edge to CK falling edge, and DQS# falling edge to CK rising edge setup time.	^tDSS	MIN	0.2		$^tCK(avg)$
CK rising edge to DQS falling edge and CK falling edge to DQS rising edge hold time	^tDSH	MIN	0.2		$^tCK(avg)$
Write postamble	^tWPST	MIN	0.4		$^tCK(avg)$
Write preamble	^tWPRE	MIN	0.8		$^tCK(avg)$
CKE Input Parameters					
CKE minimum pulse width (HIGH and LOW pulse width)	^tCKE	MIN	MAX (7.5ns, 3nCK)		$^tCK(avg)$
CKE input setup time	^tISCKE	MIN	0.25		$^tCK(avg)$
CKE input hold time	^tIHCKE	MIN	0.25		$^tCK(avg)$
Command path disable delay	^tCPDED	MIN	2		$^tCK(avg)$
Command Address Input Parameters[5]					
Address and control input setup time	^tISCA	MIN	175	150	ps
Address and control input hold time	^tIHCA	MIN	175	150	ps
CS# input setup time	^tISCS	MIN	290	270	ps
CS# input hold time	^tIHCS	MIN	290	270	ps
Address and control input pulse width	^tIPWCA	MIN	0.35		$^tCK(avg)$
CS# input pulse width	^tIPWCS	MIN	0.7		$^tCK(avg)$
Boot Parameters (10–55 MHz)[16, 17, 18]					
Clock cycle time	^tCKb	MAX	100		ns
		MIN	18		
CKE input setup time	^tISCKEb	MIN	2.5		ns
CKE input hold time	^tIHCKEb	MIN	2.5		ns
Address and control input setup time	^tISb	MIN	1150		ps
Address and control input hold time	^tIHb	MIN	1150		ps
DQS output data access time from CK/CK#	^tDQSCKb	MIN	2		ns
		MAX	10		
Data strobe edge to output data edge	^tDQSQb	MAX	1.2		ns

Table 99: AC Timing (Continued)

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate 1333	Data Rate 1600	Unit
Mode Register Parameters					
MODE REGISTER WRITE command period	^{t}MRW	MIN	10		^{t}CK(avg)
MODE REGISTER READ command period	^{t}MRR	MIN	4		^{t}CK(avg)
Additional time after ^{t}XP has expired until the MRR command may be issued	^{t}MRRI	MIN	^{t}RCD (MIN)		ns
Core Parameters[19]					
ACTIVATE-to-ACTIVATE command period	^{t}RC	MIN	^{t}RAS + ^{t}RPab (with all-bank precharge) ^{t}RAS + ^{t}RPpb (with per-bank precharge)		ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	^{t}CKESR	MIN	MAX (15ns, 3nCK)		ns
SELF REFRESH exit to next valid command delay	^{t}XSR	MIN	MAX (^{t}RFCab + 10ns, 2nCK)		ns
Exit power-down to next valid command delay	^{t}XP	MIN	MAX (7.5ns, 3nCK)		ns
CAS-to-CAS delay	^{t}CCD	MIN	4		^{t}CK(avg)
Internal READ to PRECHARGE command delay	^{t}RTP	MIN	MAX (7.5ns, 4nCK)		ns
RAS-to-CAS delay	^{t}RCD (fast)	MIN	MAX (15ns, 3nCK)		ns
	^{t}RCD (typ)		MAX (18ns, 3nCK)		
	^{t}RCD (slow)		MAX (24ns, 3nCK)		
Row precharge time (single bank)	^{t}RPpb (fast)	MIN	MAX (15ns, 3nCK)		ns
	^{t}RPpb (typ)		MAX (18ns, 3nCK)		
	^{t}RPpb (slow)		MAX (24ns, 3nCK)		
Row precharge time (all banks)	^{t}RPpab (fast)	MIN	MAX (18ns, 3nCK)		ns
	^{t}RPpab (typ)		MAX (21ns, 3nCK)		
	^{t}RPpab (slow)		MAX (27ns, 3nCK)		
Row active time	^{t}RAS	MIN	MAX (42ns, 3nCK)		ns
		MAX	70		µs
WRITE recovery time	^{t}WR	MIN	MAX (15ns, 4nCK)		ns
Internal WRITE-to- READ command delay	^{t}WTR	MIN	MAX (7.5ns, 4nCK)		ns
Active bank A to active bank B	^{t}RRD	MIN	MAX (10ns, 2nCK)		ns
Four-bank ACTIVATE window	^{t}FAW	MIN	MAX (50ns, 8nCK)		ns
Minimum deep power-down time	^{t}DPD	MIN	500		µs

Table 99: AC Timing (Continued)

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate 1333	Data Rate 1600	Unit
ODT Parameters					
Asynchronous RTT turn-on dely from ODT input	^{t}ODTon	MIN	1.75		ns
		MAX	3.5		
Asynchronous RTT turn-off delay from ODT input	^{t}ODToff	MIN	1.75		ns
		MAX	3.5		
Automatic RTT turn-on delay after READ data	^{t}AODTon	MAX	^{t}DQSCK + 1.4 × ^{t}DQSQmax + ^{t}CK(avg,min)		ps
Automatic RTT turn-off delay after READ data	^{t}AODToff	MIN	^{t}DQSCKmin - 300		ps
RTT disable delay from power-down, self refresh, and deep power-down entry	^{t}ODTd	MAX	12		ns
RTT enable delay from power-down and self refresh exit	^{t}ODTe	MAX	12		ns
CA Training Parameters					
First CA calibration command following CA training entry	^{t}CAMRD	MIN	20		^{t}CK(avg)
First CA calibration command following CKE LOW	^{t}CAENT	MIN	10		^{t}CK(avg)
CA calibration exit command following CKE HIGH	^{t}CAEXT	MIN	10		^{t}CK(avg)
CKE LOW following CA calibration mode entry	^{t}CACKEL	MIN	10		^{t}CK(avg)
CKE HIGH following last CA calibration results	^{t}CACKEH	MIN	10		^{t}CK(avg)
Data out delay after CA training calibration command entry	^{t}ADR	MAX	20		ns
MRW CA exit command to DQ tristate	^{t}MRZ	MIN	3		ns
CA calibration command to CA calibration command delay	^{t}CACD	MIN	RU(^{t}ADR + 2 × ^{t}CK)		^{t}CK(avg)
Write Leveling Parameters					
DQS/DQS# delay after write leveling mode is programmed	^{t}WLDQSEN	MIN	25		ns
		MAX	–		
First DQS/DQS# edge after write leveling mode is programmed	^{t}WLMRD	MIN	40		ns
		MAX	–		
Write leveling output delay	^{t}WLO	MIN	0		ns
		MAX	20		

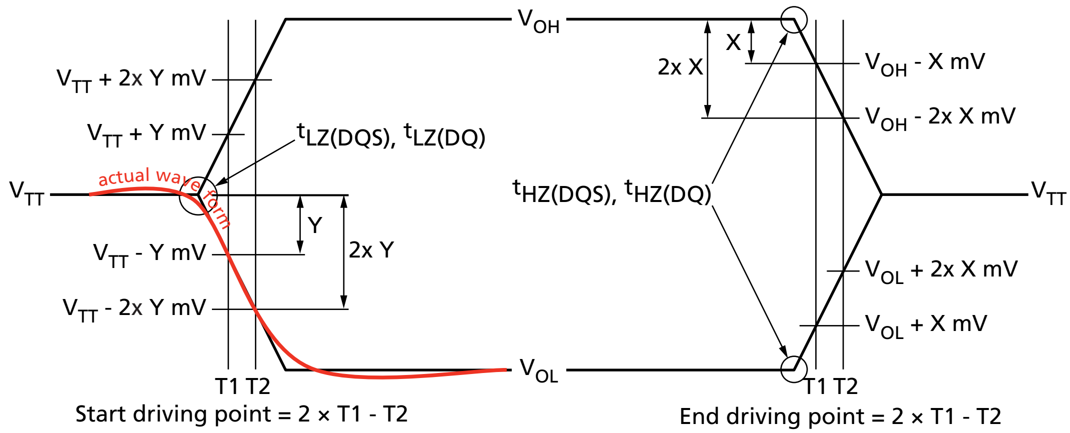
Table 99: AC Timing (Continued)

Notes 1–4 apply to all parameters and conditions

Parameter	Symbol	Min/Max	Data Rate		Unit
			1333	1600	
Write leveling hold time	^{t}WLH	MIN	205	175	ps
Write leveling setup time	^{t}WLS	MIN	205	175	ps
Mode register set command delay	^{t}MRD	MIN	MAX (14ns, 10*n*CK)		ns
		MAX	–		
Temperature Derating Parameters					
DQS output access time from CK/CK# (derated)	^{t}DQSCK	MAX	5620		ps
RAS-to-CAS delay (derated)	^{t}RCD	MIN	^{t}RCD + 1.875		ns
ACTIVATE-to- ACTIVATE command period (derated)	^{t}RC	MIN	^{t}RC + 1.875		ns
Row active time (derated)	^{t}RAS	MIN	^{t}RAS + 1.875		ns
Row precharge time (derated)	^{t}RP	MIN	^{t}RP + 1.875		ns
Active bank A to active bank B (derated)	^{t}RRD	MIN	^{t}RRD + 1.875		ns

Notes:
1. Frequency values are for reference only. Clock cycle time (^{t}CK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 2 V/ns for single-ended signals.
3. Measured with 4 V/ns differential CK/CK# slew rate and nominal V_{IX}.
4. All timing and voltage measurements are defined at the ball.
5. READ, WRITE, and input setup and hold values are referenced to V_{REF}.
6. ^{t}DQSCKDS is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. ^{t}DQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
7. ^{t}DQSCKDM is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a 1.6µs rolling window. ^{t}DQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
8. ^{t}DQSCKDL is the absolute value of the difference between any two ^{t}DQSCK measurements (in a byte lane) within a 32ms rolling window. ^{t}DQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10˚C/s. Values do not include clock jitter.
9. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). ^{t}HZ and ^{t}LZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for ^{t}RPST, ^{t}HZ(DQS) and ^{t}HZ(DQ)), or begins driving (for ^{t}RPRE, ^{t}LZ(DQS) and ^{t}LZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ) or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

Output Transition Timing



10. The parameters ^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as single-ended. The timing parameters ^{t}RPRE and ^{t}RPST are determined from the differential signal DQS/DQS#.
11. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.
12. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal.
13. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/CK# crossing.
14. CKE input hold time is measured from CK/CK# crossing to CKE reaching a HIGH/LOW voltage level.
15. Input setup/hold time for signal (CA[9:0], CS#).
16. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, ^{t}CK during boot is ^{t}CKb).
17. Mobile LPDDR3 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
18. The output skew parameters are measured with default output impedance settings using the reference load.
19. The minimum ^{t}CK column applies only when ^{t}CK is greater than 6ns.

CA and CS# Setup, Hold, and Derating

For all input signals (CA and CS#), the total required setup time (^tIS) and hold time (^tIH) is calculated by adding the data sheet ^tIS (base) and ^tIH (base) values to the Δ^tIS and Δ^tIH derating values, respectively. Example: ^tIS (total setup time) = ^tIS(base) + Δ^tIS. (See the series of tables following this section.)

The typical setup slew rate (^tIS) for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. The typical setup slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is consistently earlier than the typical slew rate line between the shaded $V_{REF(DC)}$-to-(AC) region, use the typical slew rate for the derating value (see the Typical Slew Rate and ^tVAC – ^tIS for CA and CS# Relative to Clock figure). If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see the Tangent Line – ^tIS for CA and CS# Relative to Clock figure).

The hold (^tIH) typical slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The hold (^tIH) typical slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is consistently later than the typical slew rate line between the shaded DC-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value (see the Typical Slew Rate – ^tIH for CA and CS# Relative to Clock figure). If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see the Tangent Line – ^tIH for CA and CS# Relative to Clock figure).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for a specified time, ^tVAC (see the Required Time for Valid Transition – $^tVAC > V_{IH(AC)}$ and $< V_{IL(AC)}$ table).

For slow slew rates, the total setup time could be a negative value (that is, a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the Derating Values for AC/DC-Based $^tIS/^tIH$ (AC150) table, the derating values are obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 100: CA Setup and Hold Base Values

Parameter	Data Rate		Reference
	1333	1600	
^tIS (base)	100	75	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±150mV
^tIH (base)	125	100	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±100mV

Note: 1. AC/DC referenced for 2 V/ns CA and CS# slew rate and 4 V/ns differential CK/CK# slew rate.

Table 101: CS# Setup and Hold Base Values

Parameter	Data Rate		Reference
	1333	1600	
^{t}IS (base)	215	195	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±150mV
^{t}IH (base)	240	220	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±100mV

Note: 1. AC/DC referenced for 2 V/ns CA and CS# slew rate, and 4 V/ns differential CK/CK# slew rate.

Table 102: Derating Values for AC/DC-Based ^{t}IS/^{t}IH (AC150)

Δ^{t}IS, Δ^{t}IH derating in ps

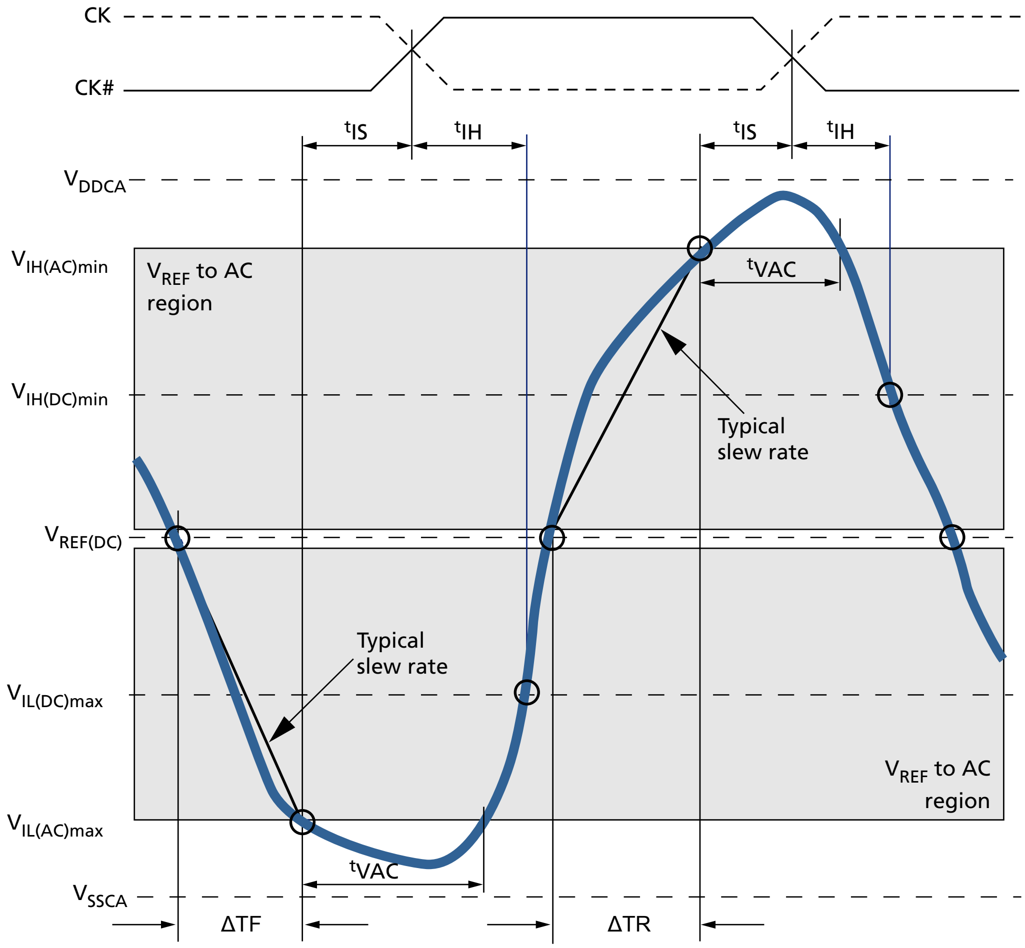
		Δ^{t}IS, Δ^{t}IH Derating in [ps] AC/DC-based AC150 Threshold -> $VIH_{(ac)} = V_{REF(dc)}$+150mV, $V_{IL(ac)} = V_{REF(dc)}$ - 150mV DC100 Threshold -> $V_{IH(dc)}$ = VREF(dc) + 100mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100mV											
		CK_t, CK_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
CA, CS# slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	**0**	**0**	13	13
	1.5							–25	–17	–25	–17	–12	–4

Note: 1. Shaded cells are not supported.

Table 103: Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ and < $V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 150mV (ps) 1333 Mb/s		^{t}VAC at 150mV (ps) 1600 Mb/s	
	Min	Max	Min	Max
>4.0	58	–	48	–
4.0	58	–	48	–
3.5	56	–	46	–
3.0	53	–	43	–
2.5	50	–	40	–
2.0	45	–	35	–
1.5	37	–	27	–
<1.5	37	–	27	–

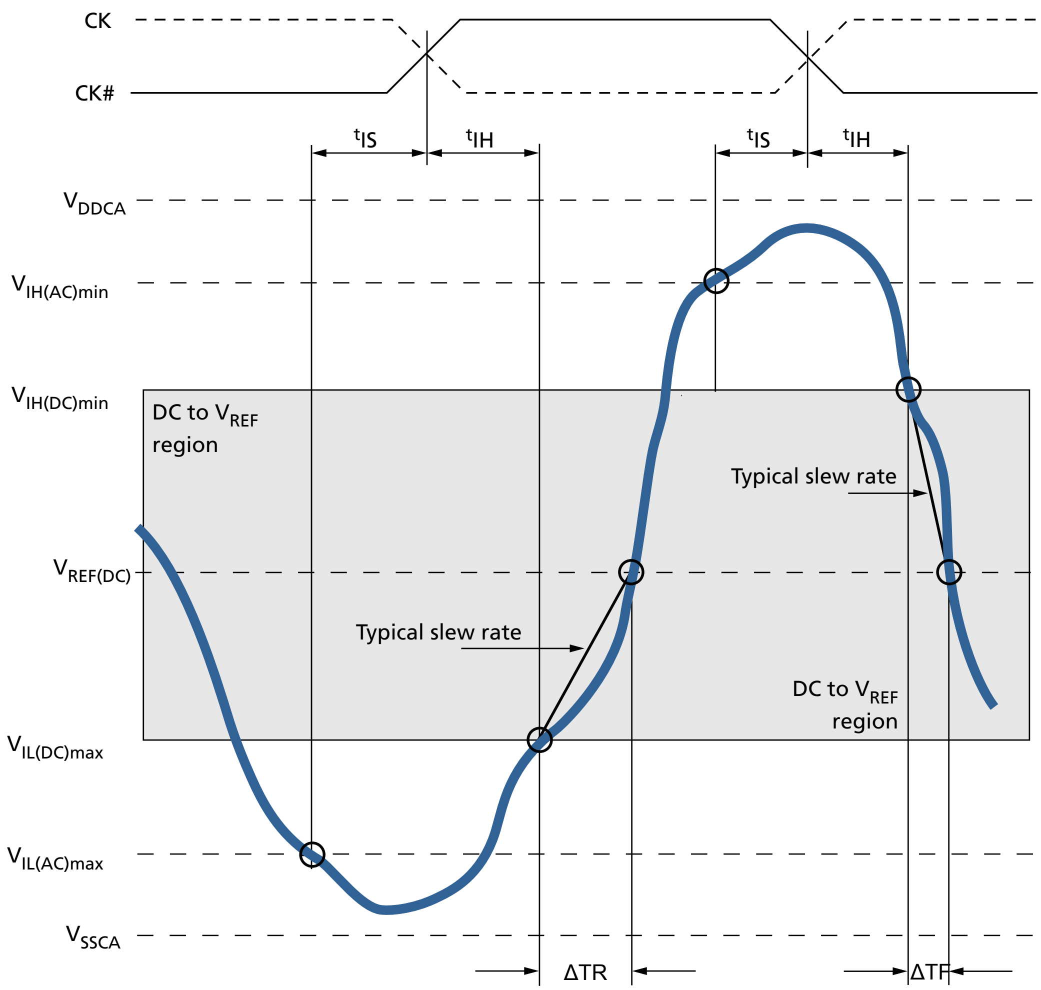
Figure 104: Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

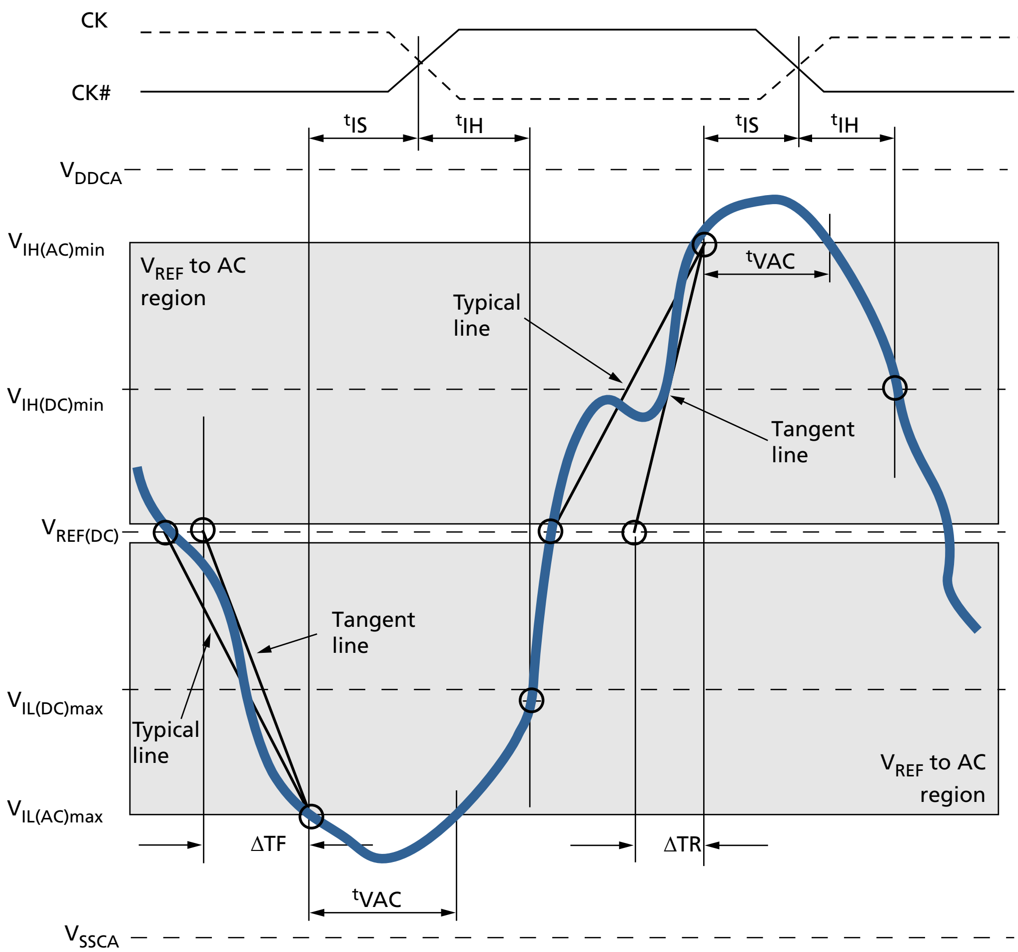
Figure 105: Typical Slew Rate – ^{t}IH for CA and CS# Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

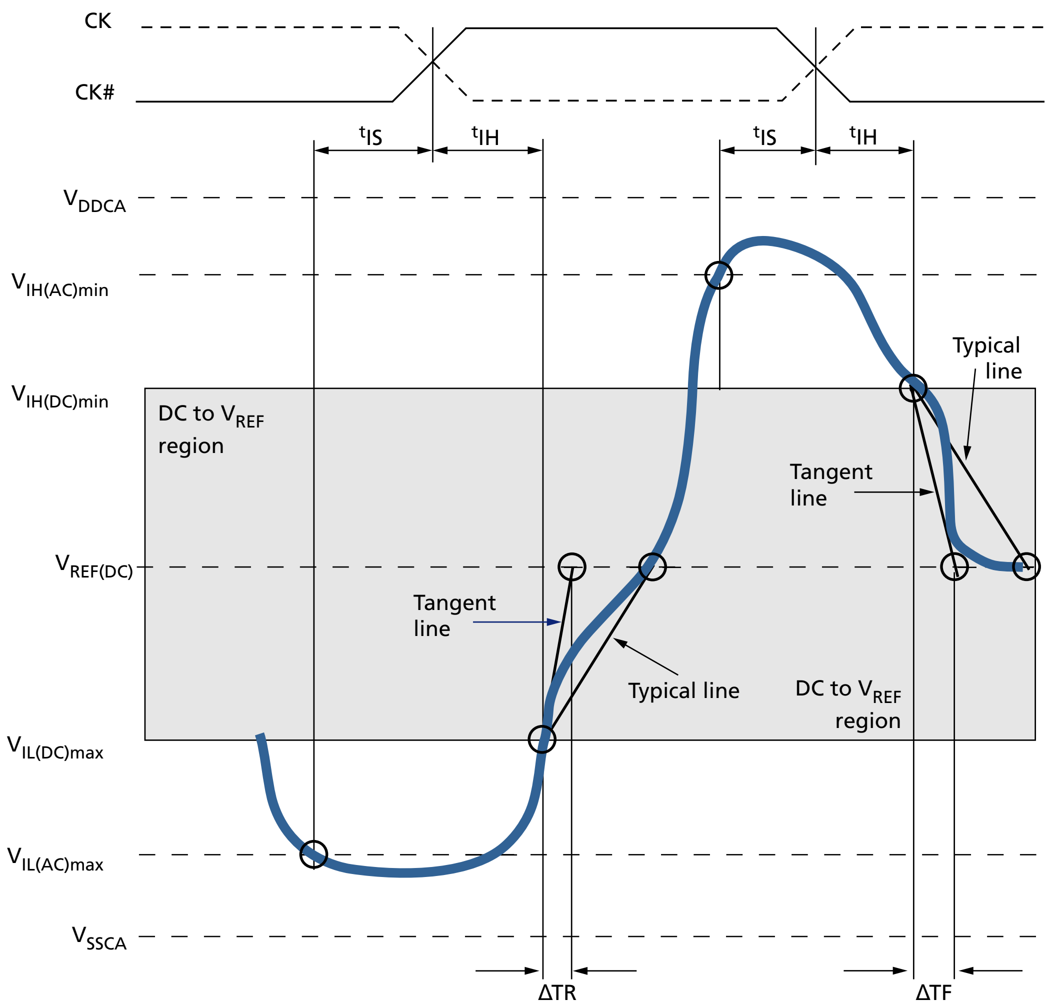
Figure 106: Tangent Line – ^{t}IS for CA and CS# Relative to Clock



$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

Figure 107: Tangent Line – ^{t}IH for CA and CS# Relative to Clock



$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (^{t}DS) and hold time (^{t}DH) by adding the data sheet ^{t}DS(base) and ^{t}DH(base) values (see the Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate) table) to the Δ^{t}DS and Δ^{t}DH derating values, respectively (see the Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC150) table). Example: ^{t}DS = ^{t}DS(base) + Δ^{t}DS.

The typical ^{t}DS slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. The typical ^{t}DS slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$ (see the Typical Slew Rate and ^{t}VAC – ^{t}DS for DQ Relative to Strobe figure).

If the actual signal is consistently earlier than the typical slew rate line in the Typical Slew Rate and ^{t}VAC – ^{t}IS for CA and CS# Relative to Clock figure in the area shaded gray between the $V_{REF(DC)}$ region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded $V_{REF(DC)}$ region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see the Tangent Line – ^{t}IS for CA and CS# Relative to Clock figure).

The typical ^{t}DH slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. The typical ^{t}DH slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$ (see the Typical Slew Rate – ^{t}DH for DQ Relative to Strobe figure).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to-$V_{REF(DC)}$ region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to-$V_{REF(DC)}$ region, the slew rate of a tangent line to the actual signal from the DC level to the $V_{REF(DC)}$ level is used for the derating value (see the Tangent Line – ^{t}DH for DQ with Respect to Strobe figure).

For a valid transition, the input signal must remain above or below $V_{IH}/V_{IL(AC)}$ for the specified time, ^{t}VAC (see the Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$ table).

The total setup time for slow slew rates could be negative (that is, a valid input signal may not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the following table, the derating values can be obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Table 104: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)

Parameter	Data Rate		Reference
	1333	1600	
^{t}DS (base)	100	75	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±150mV
^{t}DH (base)	125	100	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±100mV

Note: 1. AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate.

Table 105: Derating Values for AC/DC-Based ^{t}DS/^{t}DH (AC150)

Δ^{t}DS, Δ^{t}DH derating in ps

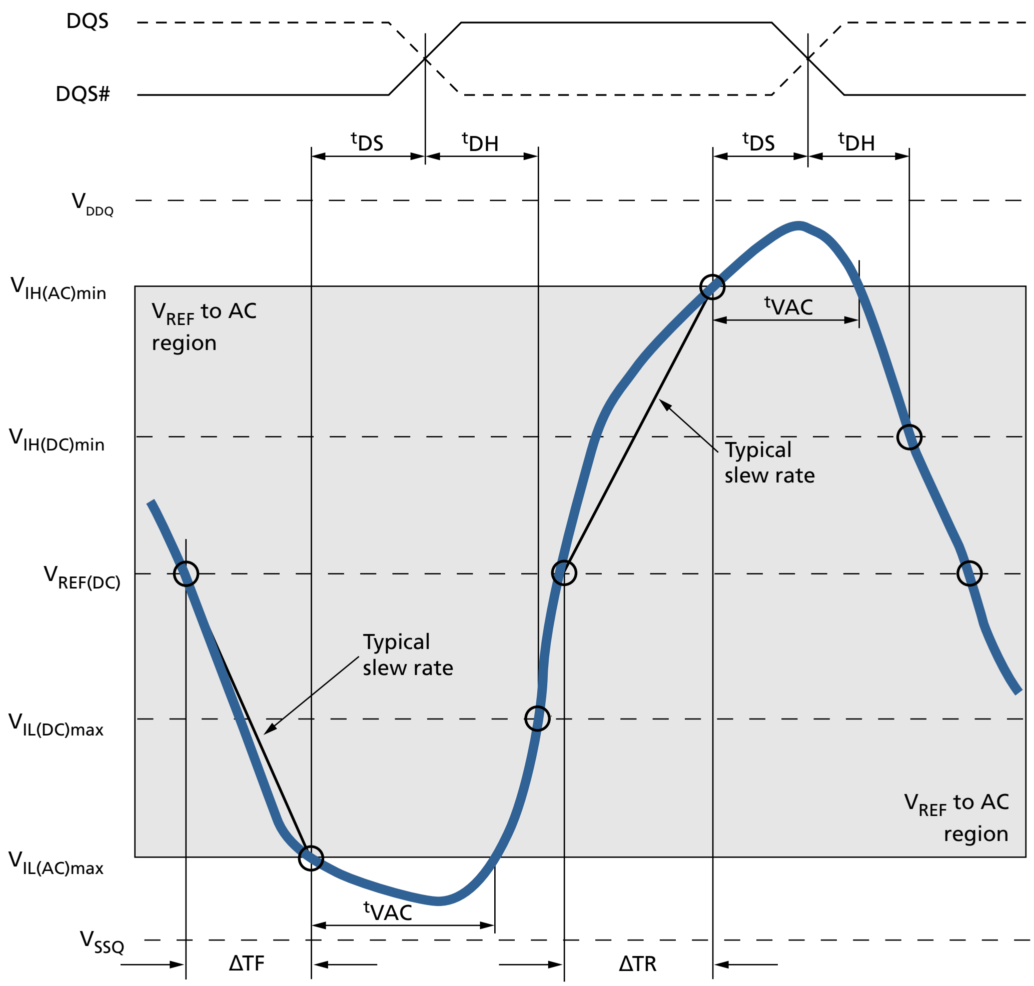
		Δ^{t}IS, Δ^{t}IH Derating in [ps] AC/DC-based AC150 Threshold -> $VIH_{(ac)} = V_{REF(dc)}$+150mV, $V_{IL(ac)} = V_{REF(dc)}$ - 150mV DC100 Threshold -> $V_{IH(dc)}$ = VREF(dc) + 100mV, $V_{IL(dc)} = V_{REF(dc)}$ - 100mV											
		DQS_t, DQS_c Differential Slew Rate											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
DQ, DM slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	**0**	**0**	13	13
	1.5							–25	–17	–25	–17	–12	–4

Note: 1. Shaded cells are not supported.

Table 106: Required Time for Valid Transition – ^{t}VAC > $V_{IH(AC)}$ or < $V_{IL(AC)}$

Slew Rate (V/ns)	^{t}VAC at 150mV (ps) 1333 Mb/s		^{t}VAC at 150mV (ps) 1600 Mb/s	
	Min	Max	Min	Max
>4.0	58	–	48	–
4.0	58	–	48	–
3.5	56	–	46	–
3.0	53	–	43	–
2.5	50	–	40	–
2.0	45	–	35	–
1.5	37	–	27	–
<1.5	37	–	27	–

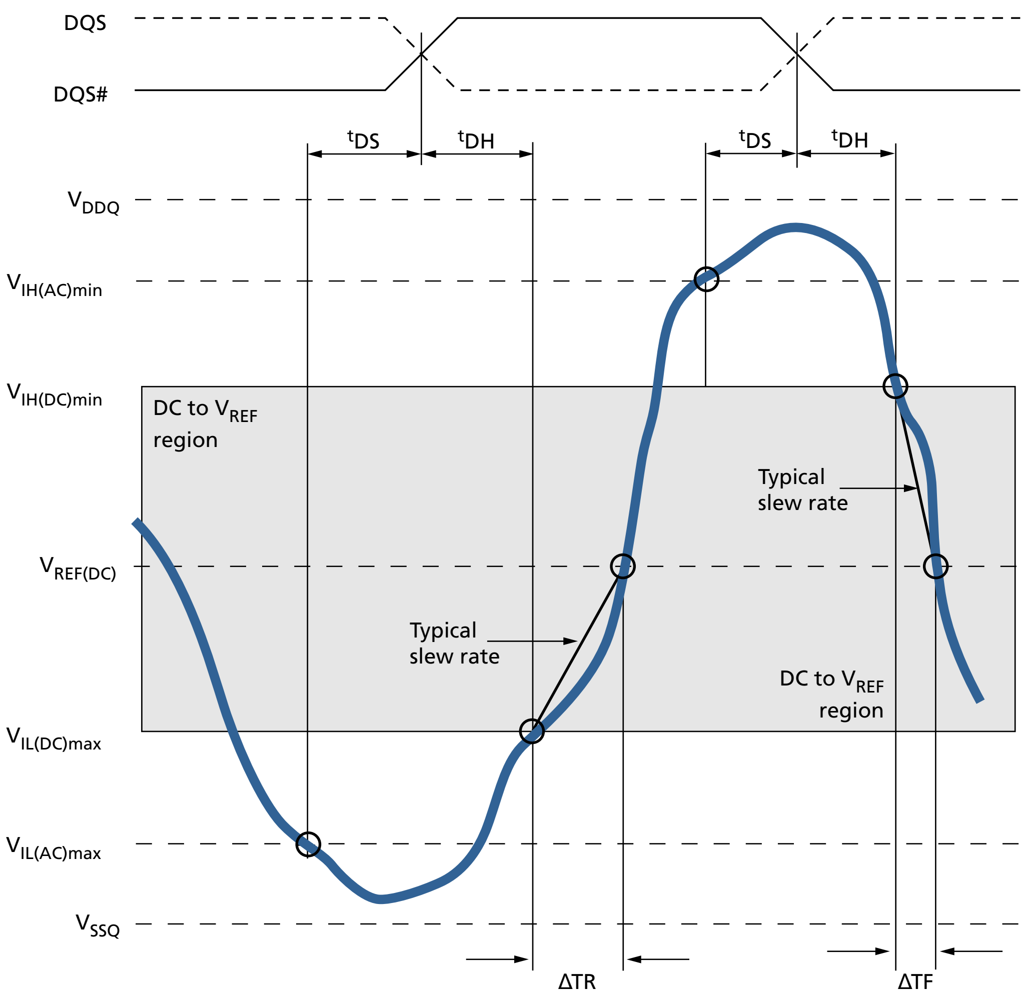
Figure 108: Typical Slew Rate and ^tVAC – ^tDS for DQ Relative to Strobe



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

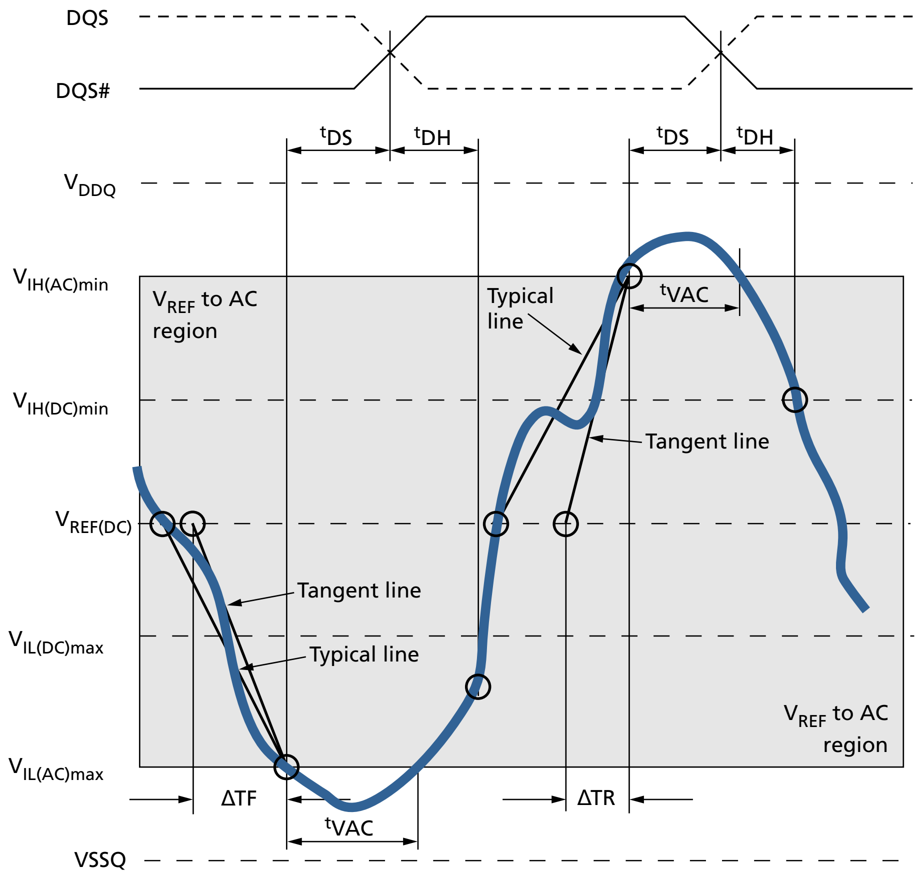
Figure 109: Typical Slew Rate – tDH for DQ Relative to Strobe



$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

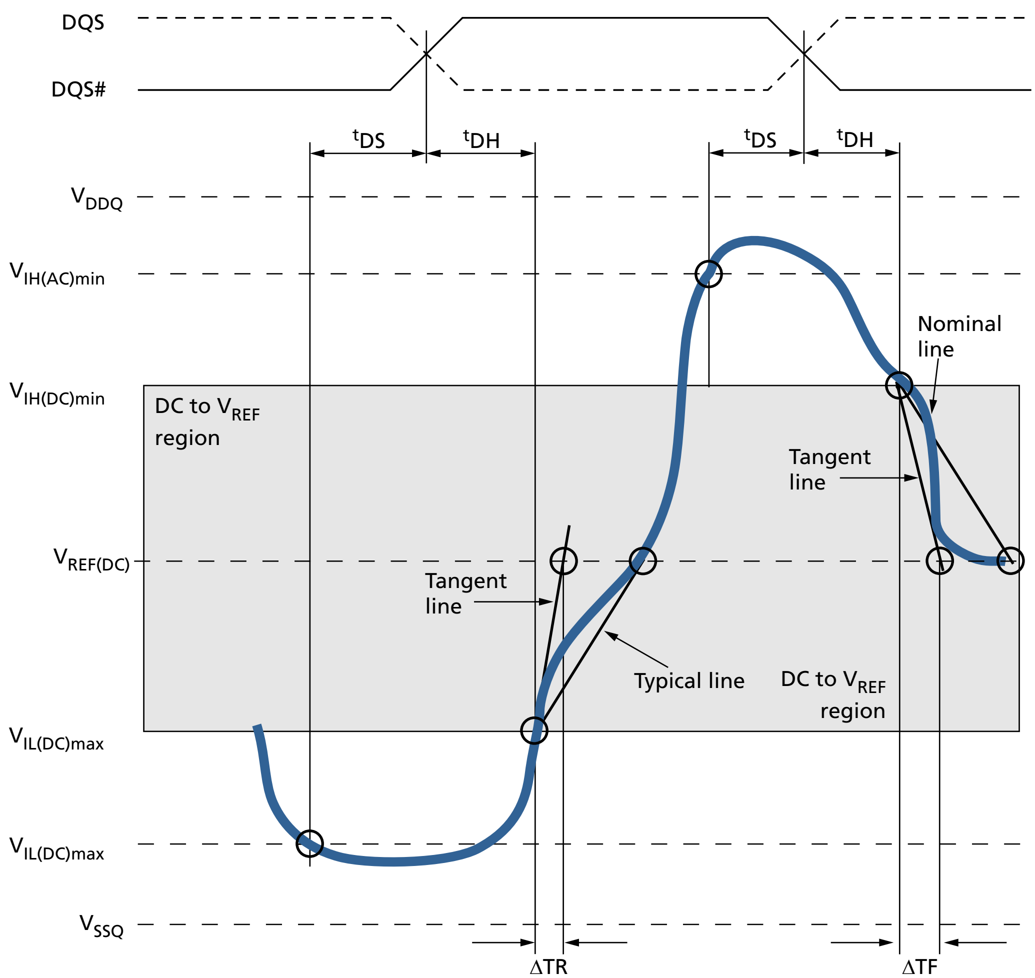
Figure 110: Tangent Line – ^{t}DS for DQ with Respect to Strobe



$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

Figure 111: Tangent Line – ^{t}DH for DQ with Respect to Strobe



$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)min} - V_{REF(DC)}]}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)max}]}{\Delta TR}$$

Revision History

Rev. E – 07/13

- Updated Configuration Addressing – Single-Channel Package table to show 2 ranks per channel for 256 Meg x 32
- Corrected V_{OTDR} equation in note 5 of the Single-Ended AC and DC Input Levels for DQ and DM table.

Rev. F – 05/13

- Production status
- Added 3DP information
- Added 216-ball, package code LP
- Updated CA and CS# Setup, Hold, and Derating figures
- Updated Data Setup, Hold, and Slew Rate Derating figures
- Changed ^{t}DSS and ^{t}DSH descriptions in AC Timing table to match timing diagrams
- Updated WRITE diagrams to reflect ^{t}WPRE timing
- Updated Write-Leveling Timing diagram to reflect ^{t}WLS and ^{t}WLH timing
- Updated Typical Self Refresh Current vs. Temperature I_{DD61} and I_{DD62} figures
- Updated ^{t}MRD in AC Timing table

Rev. E – 02/13

- Added equation ($V_{ODTR} = (2R_{ON} + R_{TT}/R_{ON}+ R_{TT}) \times V_{DDQ}$) to note 5 of the Single-Ended AC and DC Input Levels for DQ and DM table.
- Updated ODT DC Electrical Characteristics (RZQ = 240Ω After Proper ZQ Calibration) table.
- Added ^{t}MRRI to the Mode Register Parmeter table.
- Updated packaging section.
- Updated LPDDR3-1600 to LPDDR3-1333 Input Signal figure.

Rev. D – 12/12

- Removed commercial temp range from Options table.
- Removed commercial temp from Marketing Part Number Chart.

Rev. C – 10/12

- Added 216-ball ET, ER, LH, LV, and LS package drawings
- Corrected WT minimum temperature in the Operating Temperature Range table
- Deleted last sentence of second paragraph under REFRESH Command: Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command (see the Bank Selection for PRECHARGE by Address Bits table).

Rev. B – 08/12

- Corrected logic levels in the following tables: CA Training Mode Enable (MR41 (29H, 0010 1001b), OP = A4H (1010 0100b)) and CA Training Mode Disable (MR42 (2AH, 0010 1010b), OP = A8H(1010 1000b)) in MODE REGISTER WRITE (MRW)
- Clarified CKE function during SELF REFRESH operation
- Typo corrected in Mode Register, MR2 table (Option B, 733 MHz), WL changed from W L= 8 to WL = 9
- Changed CA[10:0] to CA[9:0] in the following figures: ACTIVATE Command, ^{t}FAW Timing, MODE REGISTER WRITE Timing
- Options/Marking: Deleted PoP from FBGA bullet; corrected package descriptions for 216-ball LR and 256-ball LS; changed commercial temperature to 0°C to +85°C
- Marketing Part Number Chart: Added package code LS for 256-ball 14 x 14mm FBGA; added TBD for 216-ball 12 x 12mm FBGA; changed all package code descriptions to FBGA; changed commercial temperature to 0°C to +85°C
- Package Codes and Descriptions: Added table row for 256-ball LS package
- Single Rank, Single Channel Package Block Diagram: Changed ZQ to ZQ0
- Dual Rank, Single Channel Package Block Diagram: Deleted note 1
- Package Dimensions: Added correct FBGA designations in all figure titles; 178-Ball VFBGA – 11 x 11.5mm (Package Code ET): Added placeholder figure and notes; 216-Ball VFBGA – 15 x 15mm (Package Code LT): Changed TBD to LT; 216-Ball VFBGA – 15 x 15mm (Package Code LR): Added placeholder figure and notes; 253-Ball TFBGA – 11.5 x 11.5mm (Package Code ER): Added note 2 for solder ball composition LF35; 256-Ball WFBGA – 14 x 14mm (Package Code LS): Added solder ball composition in note 2
- Ball Assignments: 178-Ball Single-Channel Discrete FBGA – 11 x 11.5mm: Added figure note stating that upper byte DQ pins become NC for x16 devices; 216-Ball Dual-Channel FBGA – 12 x 12mm: Added figure and note; 256-Ball PoP FBGA: Removed Preliminary
- Burst WRITE Command: Updated description
- Single-Ended AC and DC Input Levels for DQ and DM: Updated table note 5
- MODE REGISTER WRITE Timing for MRW RESET: Added figure
- CA Training Timing: Updated figure per JEDEC
- MRW – CA Training Mode: Updated description

Rev. A – 03/12

- Initial release; Advance status

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.