18×12 Auto Breath Matrix LED Driver with 32-bit MCU

Features

- 32-bit Core and up to 72MHz system
- Memory
  - 64KB Flash, 8KB SRAM
  - Embedded Bootloader to support In-System-Programming (ISP)
- Clock, reset and power management
  - Power supply ranges from 2.7 to 5.5V
  - Power-on and Power-down reset (POR/ PDR), Programmable voltage detector (PVD)
  - Multiple low power modes
- One 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers and three 16-bit basic timers
- Up to 23 fast I/O ports
- Up to 7 communication interfaces: UARTx3, I^2C, SPIx2 (support I^2S mode), FlexCAN module supports CAN 2.0B interface
- One 12-bit Analog-to-Digital converter (ADC)
- One high speed analog comparator
- 32-bit hardware divider
- Embedded CRC engine
- Debug mode: Serial Wire Debug (SWD).
- 18 current sinks, 12 current switches, up to drive 216 LEDs or 72 RGBs.
- Programmable matrix size
- Global 256-level DC current configuration
- Individual 256-level PWM for dimming
- Individual 256-level scaling current for color-mixing
- High-precision current sinks
  - Device-to-device error: ±5%
  - Channel-to-channel error: ±5%
- Individual 216 LEDs open/short detection
- Multiple-device clock synchronization by SYNC pin
- WBQFP 10mmX10mm-64L package

General Description

AW22216 is a 32-bit MCU that integrated an up to 18x12 programmable auto breath matrix LED driver. This device has a maximum clocked frequency of 72MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one analog comparator, one 16-bit advanced timer, one 16-bit and one 32-bit general purpose timers and three 16-bit basic timers, as well as communication interfaces including one I2C, one SPI or I2S, three UART and one FlexCAN interface.

Each LED channel has individual 8-bit DC current setting for color-mixing and 8-bit PWM current setting for brightness control. The global current of each channel is configured via register GCCR and external resistor REXT.

Three integrated pattern controllers provide auto breathing or group dimming control. Each pattern controller can work in auto breathing or manual control mode. All breathing parameters are configurable, including rising/falling slope, on/off time, repeat times, and minimum/maximum brightness, etc. Each LED's PWM parameter can be sourced from any one of the 3 pattern controllers optionally.

Phase-delay, phase-inverting, selectable three phase, spread spectrum and slew rate control technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW22216 can be turned off with minimum current consumption by the software configuration.

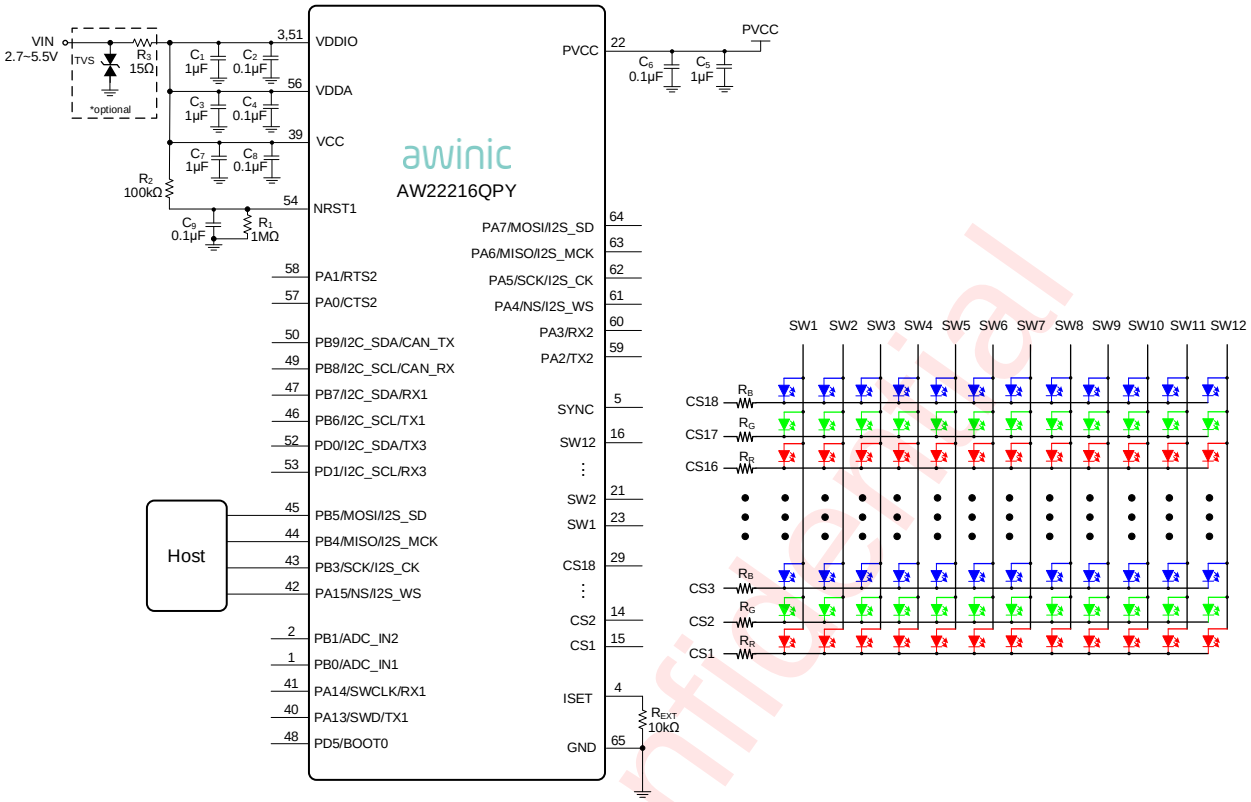
AW22216 is available in QFP 10mmx10mmx 0.75mm-64L package. It operates with 2.7V to 5.5V over the temperature range of -40°C to 85°C.

Applications

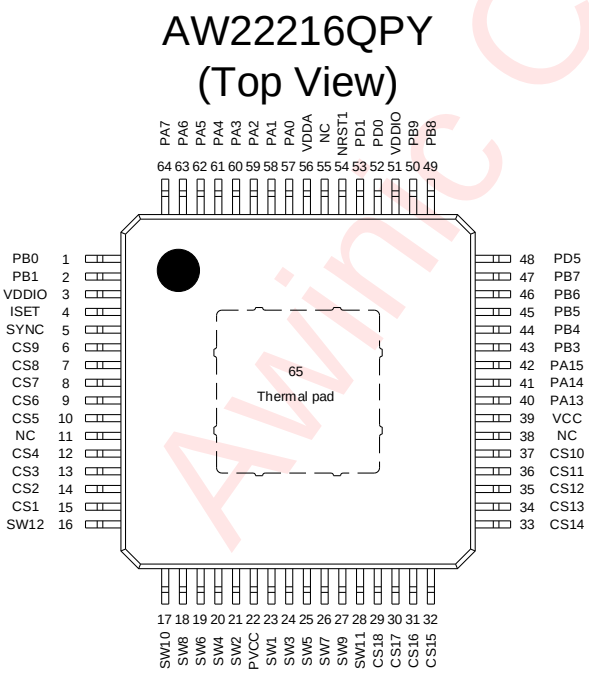
Intelligent audio system

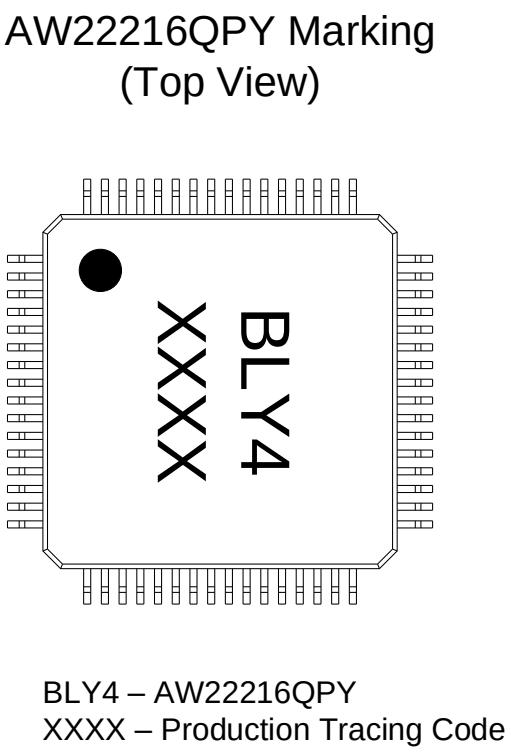
E-cigarette

Typical Application Circuit



Pin Configuration And Top Mark





BLY4 – AW22216QPY
XXXX – Production Tracing Code

Figure 1 AW22216 Pin Configuration and Marking

Pin Definition

No.	NAME	DESCRIPTION
1	PB0	TIM3_CH3/ TIM1_CH2N/ TIM1_CH1N/ TIM1_CH3/ ADC1_VIN[8]
2	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ TIM1_CH4/ TIM1_CH2N/ MCO/ TIM1_CH2/ TIM1_CH1N/ ADC1_VIN[9]
3	VDDIO	Power supply, 2.7V~5.5V
4	ISET	When REXT=10kΩ, global current of LED is 40mA
5	SYNC	Synchronize pin, used to synchronize clock in multiple devices application, internally pulled down to GND with a resistor of 1MΩ
6	CS9	Current sink
7	CS8	Current sink
8	CS7	Current sink
9	CS6	Current sink
10	CS5	Current sink
11	NC	No connect
12	CS4	Current sink
13	CS3	Current sink
14	CS2	Current sink
15	CS1	Current sink
16	SW12	Current switches
17	SW10	Current switches
18	SW8	Current switches
19	SW6	Current switches
20	SW4	Current switches
21	SW2	Current switches
22	PVCC	Current source power supply, 2.7V~5.5V
23	SW1	Current switches
24	SW3	Current switches
25	SW5	Current switches
26	SW7	Current switches
27	SW9	Current switches
28	SW11	Current switches
29	CS18	Current sink
30	CS17	Current sink
31	CS16	Current sink

32	CS15	Current sink
33	CS14	Current sink
34	CS13	Current sink
35	CS12	Current sink
36	CS11	Current sink
37	CS10	Current sink
38	NC	No connect
39	VCC	Power supply, 2.7V~5.5V
40	PA13	SWDIO/ UART1_TX/ SPI2_MISO/ MCO/ TIM1_CH2/ TIM1_BKIN
41	PA14	SWDCLK/ UART2_TX/ UART1_RX/ SPI1_NSS/ I2S1_WS
42	PA15	SPI1_NSS/ I2S1_WS/ UART2_RX/ TIM2_CH1/ TIM2_ETR
43	PB3	SPI1_SCK/ I2S1_CK/ TIM2_CH2/ UART1_TX/ TIM2_CH3/ TIM1_CH1/ TIM2_CH1/ ADC1_VIN[10]
44	PB4	SPI1_MISO/ I2S1_MCK/ TIM3_CH1/ UART1_RX/ TIM17_BKIN TIM1_CH2/ TIM2_CH2/ ADC1_VIN[11]
45	PB5	SPI1_MOSI/ I2S1_SD/ TIM3_CH2/ TIM16_BKIN/ MCO/ TIM1_CH3/ TIM2_CH3
46	PB6	UART1_TX/ I²C_SCL/ TIM16_CH1N/ TIM2_CH1
47	PB7	UART1_RX/ I²C_SDA/ TIM17_CH1N/ UART2_TX/ ADC1_VIN[12]
48	PD5	BOOT0
49	PB8	I²C_SCL/ TIM16_CH1/ CAN_RX/ UART2_RX
50	PB9	I²C_SDA/ TIM17_CH1/ CAN_TX/ TIM1_CH4
51	VDDIO	Power supply, 2.7V~5.5V
52	PD0	UART3_TX I²C_SDA
53	PD1	UART3_RX I²C_SCL
54	NRST1	Reset
55	NC	No connect
56	VDDA	Power supply, 2.7V~5.5V
57	PA0	UART2_CTS/ TIM2_CH1/ TIM2_ETR/ TIM2_CH3/ COMP1_OUT/ ADC1_VIN[0]
58	PA1	UART2_RTS/ TIM2_CH2/ ADC1_VIN[1] / COMP_INP[0]
59	PA2	UART2_TX/ TIM2_CH3/ ADC1_VIN[2] / COMP_INP[1]
60	PA3	UART2_RX/ TIM2_CH4/ ADC1_VIN[3] / COMP_INP[2]
61	PA4	SPI1_NSS/ I2S1_WS/ TIM1_BKIN/ TIM14_CH1/ I²C_SDA/ ADC1_VIN[4]/ COMP_INP[3]
62	PA5	SPI1_SCK/ I2S1_CK/ TIM2_CH1/ TIM2_ETR/ TIM1_ETR/ I²C_SCL/ TIM1_CH3N/ ADC1_VIN[5]/ COMP_INM[0]
63	PA6	SPI1_MISO/ I2S1_MCK/ TIM3_CH1/ TIM1_BKIN UART2_RX/ TIM1_ETR/ TIM16_CH1/ TIM1_CH3/ COMP1_OUT/ ADC1_VIN[6]/ COMP_INM[1]

64	PA7	SPI1_MOSI/ I2S1_SD/ TIM3_CH2/ TIM1_CH1N TIM14_CH1 TIM17_CH1/ TIM1_CH2N/ TIM1_CH3N/ ADC1_VIN[7]/ COMP_INM[2]
65	External Pad	Thermal pad

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PA0	-	UART2_CTS	TIM2_CH1/TIM2_ETR	-	TIM2_CH3	-	-	COMP1_OUT	-
PA1	-	UART2_RTS	TIM2_CH2	-	-	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	-	-	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	-	-	-	-	-	-
PA4	SPI1_NSS/I2S1_WS	-	-	TIM1_BKIN	TIM14_CH1	I2C_SDA	-	-	-
PA5	SPI1_SCK/I2S1_CK	-	TIM2_CH1/TIM2_ETR	TIM1_ETR	-	I2C_SCL	TIM1_CH3N	-	-
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT	-
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N	-
PB3	SPI1_SCK/I2S1_CK	-	TIM2_CH2	UART1_TX	TIM2_CH3	-	TIM1_CH1	TIM2_CH1	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	UART1_RX	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	MCO	-	-	TIM1_CH3	TIM2_CH3	-
PB6	UART1_TX	I2C_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-	-
PB7	UART1_RX	I2C_SDA	TIM17_CH1N	-	UART2_TX	-	-	-	-
PB8	-	I2C_SCL	TIM16_CH1	CAN_RX	UART2_RX	-	-	-	-
PB9	-	I2C_SDA	TIM17_CH1	CAN_TX	TIM1_CH4	-	-	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PD0	UART3_TX	I2C_SDA	-	-	-	-	-	-	-
PD1	UART3_RX	I2C_SCL	-	-	-	-	-	-	-
PD5	-	-	-	-	-	-	-	-	-

Functional Block Diagram

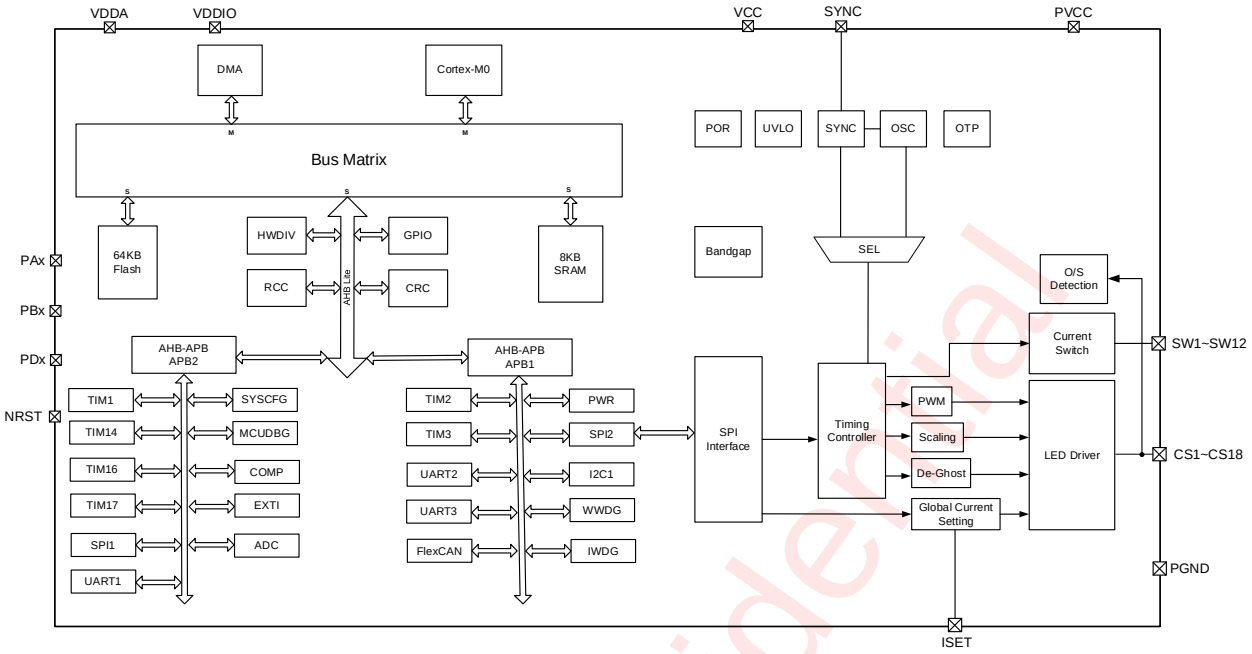


Figure 2 Functional Block

Typical Application Circuits

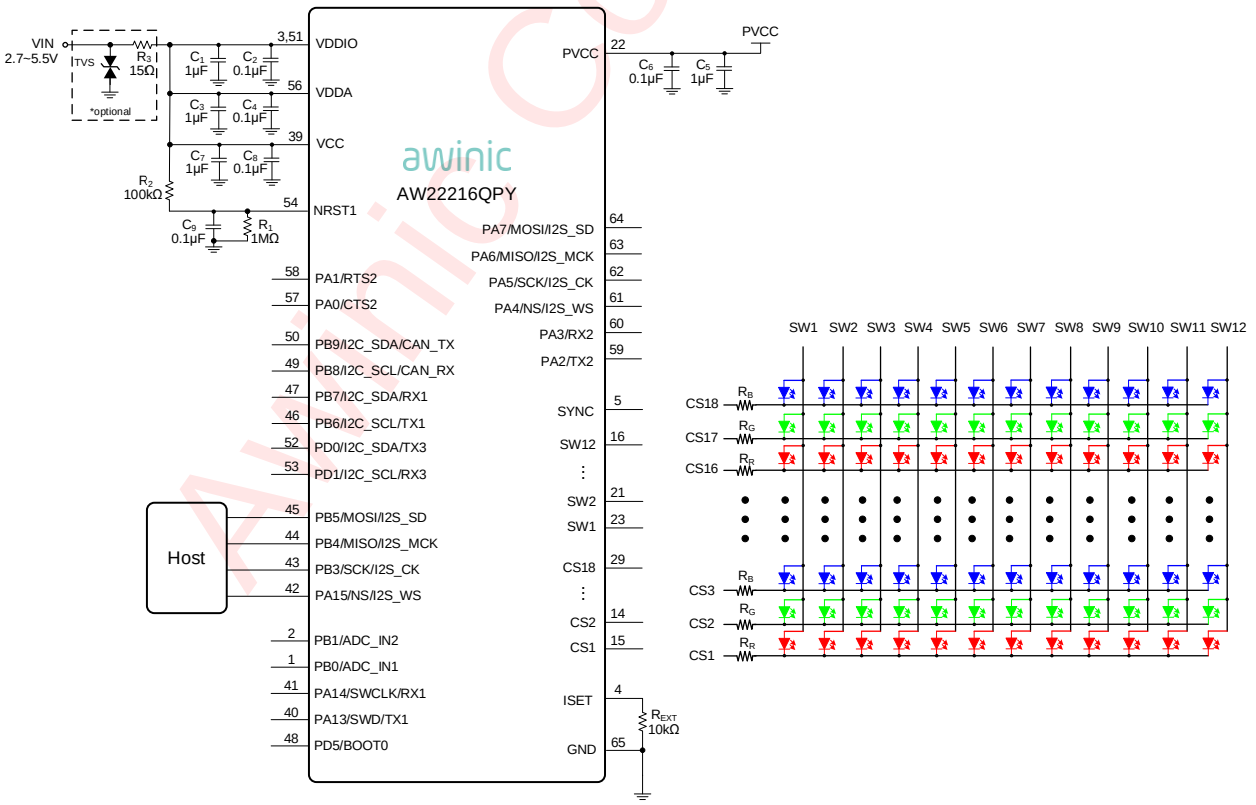


Figure 3 AW22216 Application circuit

Note1: The resistance R_R / R_G /R_B is determined by PVCC, $VF_{(R/G/B)}$ of LED, ILED, VHR of CSx and SWx. R_R / R_G /R_B=(PVCC- $VF_{(R/G/B)}$-VHR_{CS}-VHR_{SW})/I_{MAX}.

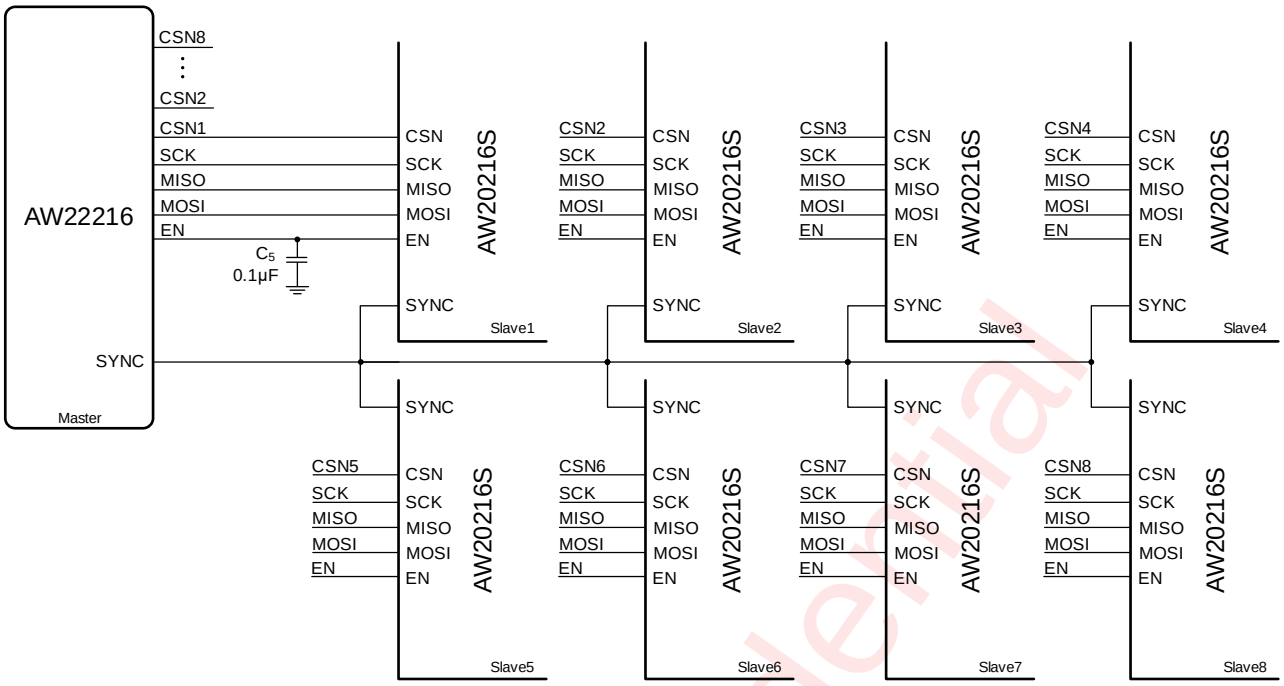


Figure 4 Typical Application Circuit Synchronous with 8 AW20216S

Note2: AW22216 is set as master mode, and all the 8 AW20216S set as slave mode (set master after set all slaves). Master mode or slave mode set by register SSCR (page0, address=0x28). Master part output master clock, and all slaves input the master clock.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW22216QPY	-40℃～85℃	WBQFP 10mmX10mm-64L	BLY4	MSL3	ROHS+HF	1600 units/ 10Tray

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC, PVCC		-0.3V to 6V
Supply voltage range VDD, VDDIO		-0.3V to 5.8V
Output voltage range	SW1~SW12, CS1~CS18	-0.3V to PVCC
Voltage on ISET	ISET	-0.3V to 2V
Input voltage on other pins		-0.3V to V_{DD}+0.3V
Junction-to-ambient thermal resistance θ_{JA}		32.197°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		160°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)(NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78F		+IT：100mA -IT：-100mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM test method: ESDA/JEDEC JS-001-2023. CDM test method: ESDA/JEDEC JS -002-2022.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Input voltage	2.7	3.3	5.5	V
PVCC	Input voltage	2.7	5	5.5	V
VDD	Input voltage	2.7	3.3	5.5	
VDDIO	Input voltage(Must be the same as VDD)	2.7	3.3	5.5	
f_{HCLK}	Internal AHB clock frequency	-	-	72	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	-	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	72	MHz
C_1, C_3 C_5 C_8	Input capacitance	1	1	22	μF
C_2, C_4, C_6 C_7	Input capacitance	0.1	0.1	1	μF
R_{EXT}	External resistor for setting sink current	5	10	20	kΩ
t_{VDD}	V_{DD} rise time t_r	1	-	∞	us
	V_{DD} fall time t_f	400	-	∞	
V_{ft} Note	Power-down threshold voltage	-	0	-	mV
T_A	Operating free-air temperature range	-40°	25	85	°C

Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

Electrical Characteristics

SUPPLY CURRENT CHARACTERISTICS

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle, 48 ~ 72 MHz is 2 waiting cycles).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and V_{DD}=V_{CC}=3.3V, f_{HCLK} = 72MHz，$f_{APB1} = f_{HCLK}$，$f_{APB2} = f_{HCLK}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{STB}	Standby current			1.7	8	μA
I_{ACT}	Quiescent current in active mode	All peripherals disabled		12		mA
		All peripherals enabled		18		

On-chip peripheral current consumption (1)

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load) .
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD}=3.3V..

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	0.95	uA/MHz
	GPIOA		0.55	
	GPIOB		0.56	
	GPIOC		0.52	
	GPIOD		0.54	
	DMA		2.1	
	HWDIV		1.2	
	TIM1	APB2	8.2	

	TIM14		2.0	
	TIM16		2.7	
	TIM17		2.8	
	SPI1		5.7	
	UART1		4.8	
	SYSCFG		0.2	
	MCUDBG		0.2	
	COMP		0.4	
	EXTI		0.1	
	ADC		4.1	
	TIM2	APB1	5.8	
	TIM3		4.4	
	UART2		5.0	
	UART3		5.0	
	IWDG		0.6	
	I^2C1		6.8	
	WWDG		0.2	
	FlexCAN		11.1	

1. f_{HCLK} = 72MHz，f_{APB1} = f_{HCLK}，f_{APB2} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

Stop or Standby mode: the clock source is the oscillator

Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD}=3.3V.

Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSI	3	cycles
t_{WUSTOP}	Wake up from Stop mode (regulator is in Run mode)	System clock is HSI	11	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode (regulator is in low power mode)	System clock is HSI	14	μs
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x1	484	μs
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x2	425	μs
$t_{WUSTDBY}$	Wake up from Standby mode	PWR->CR[15:14] = 0x3	363	μs

MATRIX LED DRIVER BLOCK CHARACTERISTICS

T_A=25°C, PVCC=VCC=3.6V (unless otherwise noted), R_{EXT}=10kΩ

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
LED current						
I_{MAX}	Maximum sink current(CS1~CS18)	V_{LED}=0.5V, GCC= 0xFF,		40		mA

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
		SL= 0xFF				
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}=720mA, GCC=0xFF, SL=0xFF		750		mV
	Current sink headroom voltage CSx	I_{SINK}=40mA, GCC=0xFF, SL=0xFF		300		mV
I_{LIM}	Internal sink current limit	R_{EXT}=0,UVCR.OCPTH=0		75		mA
		R_{EXT}=0,UVCR.OCPTH=1		120		
I_{MATCH}	Device to device current error	All Channels' current set to 20mA	-5		5	%
$\triangle I_{LED}$	Channel to channel current error	All Channels' current set to 20mA	-5		5	%
F_{OSC}	OSC clock frequency		14.88	16	17.12	MHz
T_{SD}	Thermal shutdown threshold			165		°C
	Thermal shutdown hysteresis			25		°C
Timing						
T_{SCAN}	Period of scanning	PCCR.PWMFRQ[2:0] = 000, GCR.SWSEL[3:0] = 1011		216		μs
T_{DG}	Non-overlap time between SW			1		μs
T_{HOLD}	Delay time between the falling edge of CS18 and SWx			125		ns
T_{SETUP}	Delay time between the rising edge of SWx and CS1	PCCR.PWMFRQ[2:0] = 000		250		ns
T_{DLY}	Delay time of each CS group, there are 6 groups of CS	PCCR.PWMFRQ[2:0] = 000		125		ns

EMBEDDED RESET AND POWER CONTROL BLOCK CHARACTERISTICS

The parameters given in the table below are provided under the ambient temperature and V_{DD}=3.3V.

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	1.62	1.8	1.98	V
		PLS[3:0]=0000 (Falling edge)	1.53	1.7	1.87	
		PLS[3:0]=0001 (Rising edge)	1.89	2.1	2.31	
		PLS[3:0]=0001 (Falling edge)	1.80	2.0	2.20	
		PLS[3:0]=0010 (Rising edge)	2.16	2.4	2.64	
		PLS[3:0]=0010 (Falling edge)	2.07	2.3	2.53	
		PLS[3:0]=0011 (Rising edge)	2.43	2.7	2.97	
		PLS[3:0]=0011 (Falling edge)	2.34	2.6	2.86	
		PLS[3:0]=0100 (Rising edge)	2.70	3.0	3.30	

		PLS[3:0]=0100 (Falling edge)	2.61	2.9	3.19	
		PLS[3:0]=0101 (Rising edge)	2.97	3.3	3.63	
		PLS[3:0]=0101 (Falling edge)	2.88	3.2	3.52	
		PLS[3:0]=0110 (Rising edge)	3.24	3.6	3.96	
		PLS[3:0]=0110 (Falling edge)	3.15	3.5	3.85	
		PLS[3:0]=0111 (Rising edge)	3.51	3.9	4.29	
		PLS[3:0]=0111 (Falling edge)	3.42	3.8	4.18	
		PLS[3:0]=1000 (Rising edge)	3.78	4.2	4.62	
		PLS[3:0]=1000 (Falling edge)	3.69	4.1	4.51	
		PLS[3:0]=1001 (Rising edge)	4.05	4.5	4.95	
		PLS[3:0]=1001 (Falling edge)	3.96	4.4	4.84	
		PLS[3:0]=1010 (Rising edge)	4.32	4.8	5.28	
		PLS[3:0]=1010 (Falling edge)	4.23	4.7	5.17	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	30	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	3	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

BUILT-IN VOLTAGE REFERENCE

Build-in voltage reference

The parameters given in the table below are provided under the ambient temperature and V_{DD}=3.3V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VREFINT	Built-in voltage reference	-40°C < TA < 105°C	-	1.2	-	V
Ts_vrefint (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

EXTERNAL CLOCK SOURCE CHARACTERISTICS

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	32	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	15	-	-	ns

1. Guaranteed by design, not tested in production

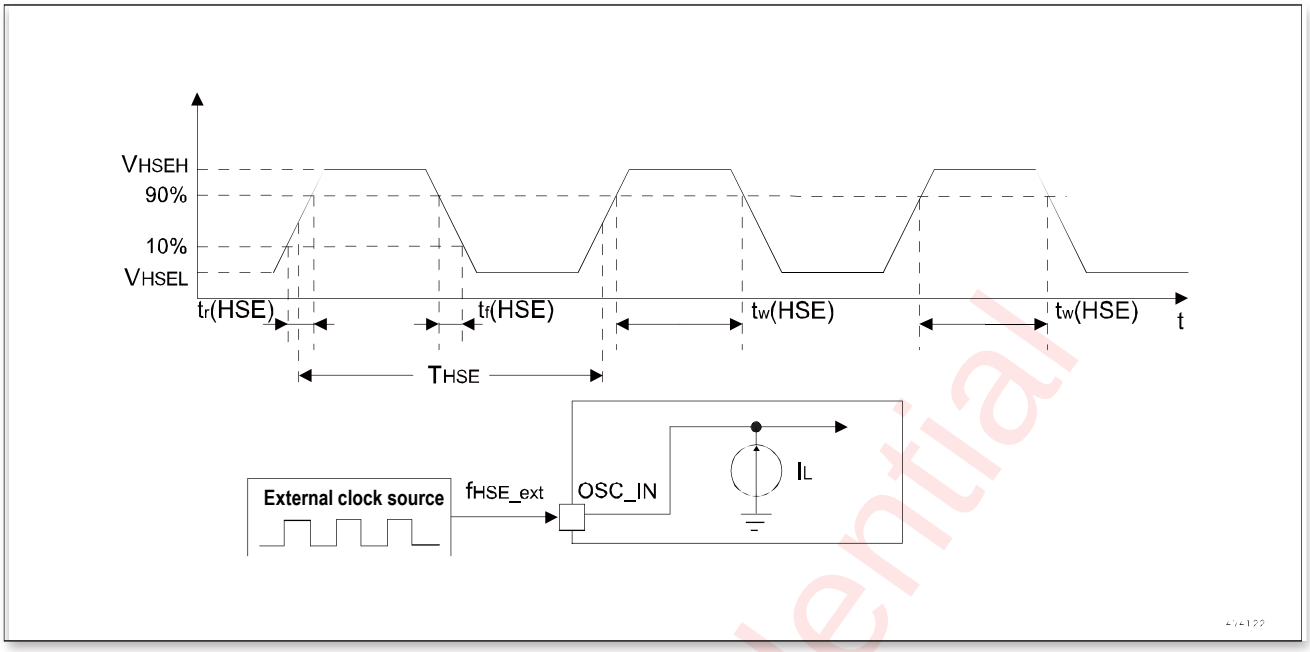


Figure 5 High-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on the design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

HSE oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Oscillator frequency (2)	2V<VDD<3.6V	4	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	MHz
R_F	Feedback resistor (4)	-	-	1000	-	kΩ
ESR	Support crystal serial impedance (C_{L1} C_{L2} (3) is 16pF)	f_{OSC_IN} =24MHz, V_{DD}=3V	-	-	50	Ω
		f_{OSC_IN} =12MHz, V_{DD}=2V	-	-	120	Ω
I_2	HSE current consumption	f_{OSC_IN} =24MHz, ESR=30 V_{DD} = 3.3V, C_{L1} C_{L2} (3) is 20pF	-	1.5	-	mA
g_m	Oscillator transconductance	Start up	-	9	-	mA/V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stable	-	3	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer characteristics Parameter.
2. Guaranteed by design, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

4. The relatively low value of the R_F resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment results in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

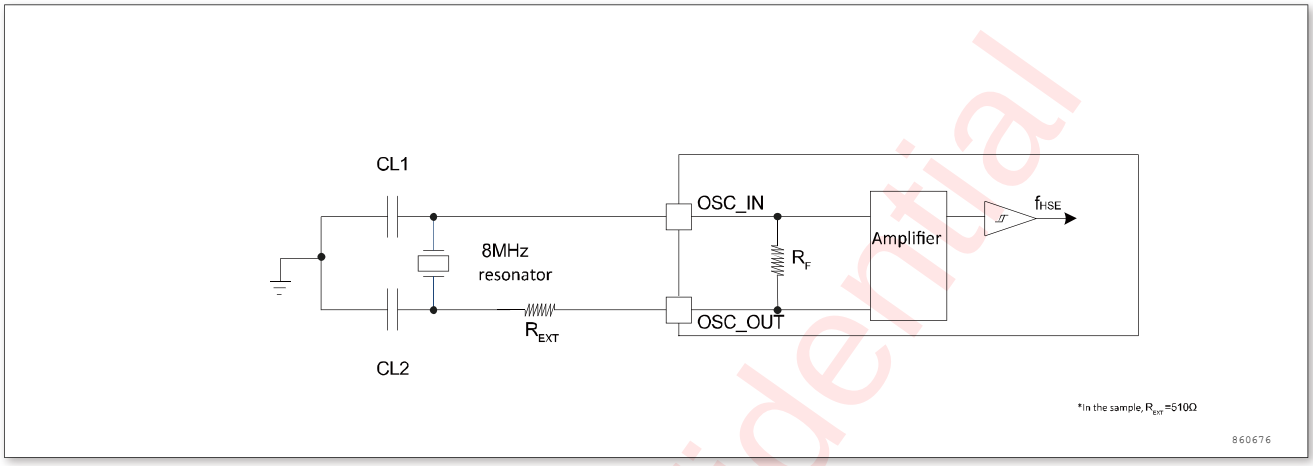


Figure 6 Typical application with an 8 MHz crystal

INTERNAL CLOCK SOURCE CHARACTERISTICS

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
ACC_{HSI}	HSI oscillator deviation	T_A = -40°C~ 105°C	-2.5	-	+2.5	%
		T_A = -20°C~ 85°C	-2	-	+2	%
		T_A = 25°C	-1	-	+1	%
$T_{stab(HSI)}$	HSI oscillator startup time	-	-	-	20	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	-	μA

1. V_{DD} = 3.3V, TA = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI} (2)	Frequency	T_A = -40°C~ 105°C	20	40	70	KHz
$t_{SU(LSI)}$ (3)	LSI oscillator startup time	-	-	-	100	μs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	-	0.26	-	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated.
2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

PLL CHARACTERISTICS

The relationship between the input clock frequency f_{PLL_IN} and output clock f_{PLL_OUT} frequency is:

$$\frac{f_{PLL\_IN}}{\text{PLLDIV}[2:0]+1} = \frac{f_{PLL\_OUT}}{\text{PLLMUL}[6:0]+1}$$

PLLMUL[6:0] and PLLDIV[2:0] are the frequency division ratio settings of the PLL frequency divider and output frequency divider.

The parameters listed in the following table are provided under ambient temperature and power supply voltage in accordance with general working conditions.

PLL characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL input clock (2)	-	4	8	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	20	-	80	%
f_{vco}	VCO output clock	-	80	-	200	MHz
f_{PLL_OUT}	PLL output clock	-	40	-	100	MHz
$I_{DD(PLL)}$	PLL current consumption	-	-	1550	-	uA

1. Guaranteed by design, not tested in production.
2. Use the correct multiplication factor to ensure the f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

MEMORY CHARACTERISTICS

Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	131.5	-	154.5	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms
I_{DD}	Supply current	Read mode 40MHz	-	-	2	mA
		Write mode	-	-	1.2	mA
		Erase mode	-	-	0.6	mA

Flash memory endurance and data retention (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	-	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 105℃	10	-	-	Years
		T_A = 85℃	20	-	-	
		T_A = 25℃	100	-	-	

I/O PORT CHARACTERISTICS

General input/output characteristics

Unless otherwise specified, the ambient temperature and power supply voltage meet General operating conditions. All I/O ports are CMOS compatible.

I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	V_{DD} = 3.3V	-	-	0.8	V
V_{IL}	Low level input voltage	V_{DD} = 5V	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	V_{DD} = 3.3V	2.0	-	-	V
V_{IH}	High level input voltage	V_{DD} = 5V	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 3.3V	0.1 * V_{DD}	0.50	-	V
V_{hy}	Schmitt trigger hysteresis (1)	V_{DD} = 5V	0.1 * V_{DD}	0.60	-	V
I_{lkg}	Input leakage current (2)	V_{DD} = 3.3V	-1	-	1	μA
I_{lkg}	Input leakage current (2)	V_{DD} = 5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PU}	Weak pull-up equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{SS}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 3.3V, V_{IN} = V_{DD}	50	60	75	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{DD} = 5V, V_{IN} = V_{DD}	50	60	75	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Absolute Maximum Ratings:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the General conditions. All I/O ports are CMOS compatible.

Output voltage static characteristics

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，VDD=3.3V	-	0.16	-	V
	V_{OH} (2)	Output high voltage		-	3.11	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA，VDD=3.3V	-	0.2	0.4	
	V_{OH} (2)(3)	Output high voltage		2.4	3.05	-	
	V_{OL} (2)(3)	Output low voltage	$\|I_{IO}\|$=20mA，VDD=3.3V	-	0.57	-	
	V_{OH} (2)(3)	Output high voltage		-	2.62	-	

10	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，VDD=3.3V	-	0.31	-	
	V_{OH} (2)	Output high voltage		-	2.93	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA，VDD=3.3V	-	0.42	-	
	V_{OH} (2)(3)	Output high voltage		-	2.79	-	
01	V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，VDD=3.3V	-	0.31	-	
	V_{OH} (2)	Output high voltage		-	2.93	-	
	V_{OL} (1)(3)	Output low voltage	$\|I_{IO}\|$= 8mA，VDD=3.3V	-	0.42	-	
	V_{OH} (2)(3)	Output high voltage		-	2.79	-	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the general condition.

I/O AC characteristics (1)(2)(3)

MODE[1:0]	Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
11	$t_{f(IO)out}$	Output fall time	C_L = 50pF VDD=3.3V	3.34	4.4	9.27	ns
	$t_{r(IO)out}$	Output rise time		3.34	4.4	9.27	ns
10	$t_{f(IO)out}$	Output fall time		5.91	10.9	17.0	ns
	$t_{r(IO)out}$	Output rise time		5.91	10.6	17.0	ns
01	$t_{f(IO)out}$	Output fall time		6.06	10.9	17.4	ns
	$t_{r(IO)out}$	Output rise time		6.06	10.8	17.4	ns

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this chip user manual.
2. The maximum frequency is defined in Recommended Operating Conditions.
3. Guaranteed by design, not tested in production.

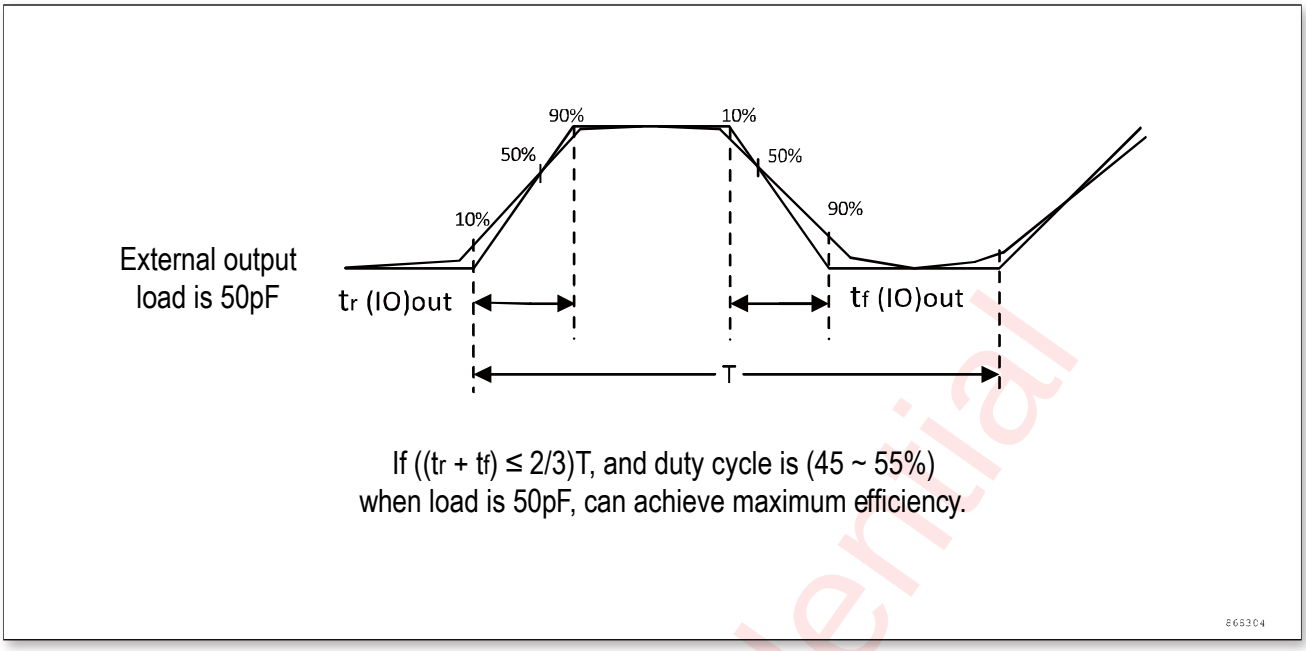


Figure 7 I/O AC characteristics

NRST PIN CHARACTERISTICS

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}. Unless otherwise stated, the parameters listed in the table below are measured under the ambient temperature and V_{DD} supply voltage in accordance with the general conditions.

NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$ (1)	NRST input low voltage	VDD=3.3V	-	-	1.4	V
$V_{IH(NRST)}$ (1)	NRST input high voltage	VDD=3.3V	2.0	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	VDD=3.3V		0.6		V
R_{PU}	Weak pull-up equivalent resistor (1)	$V_{IN} = V_{SS}$	50	60	75	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	-	-	-	1.0	uS
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse	-	4.0	-	-	uS

1. Guaranteed by design, not tested in production.

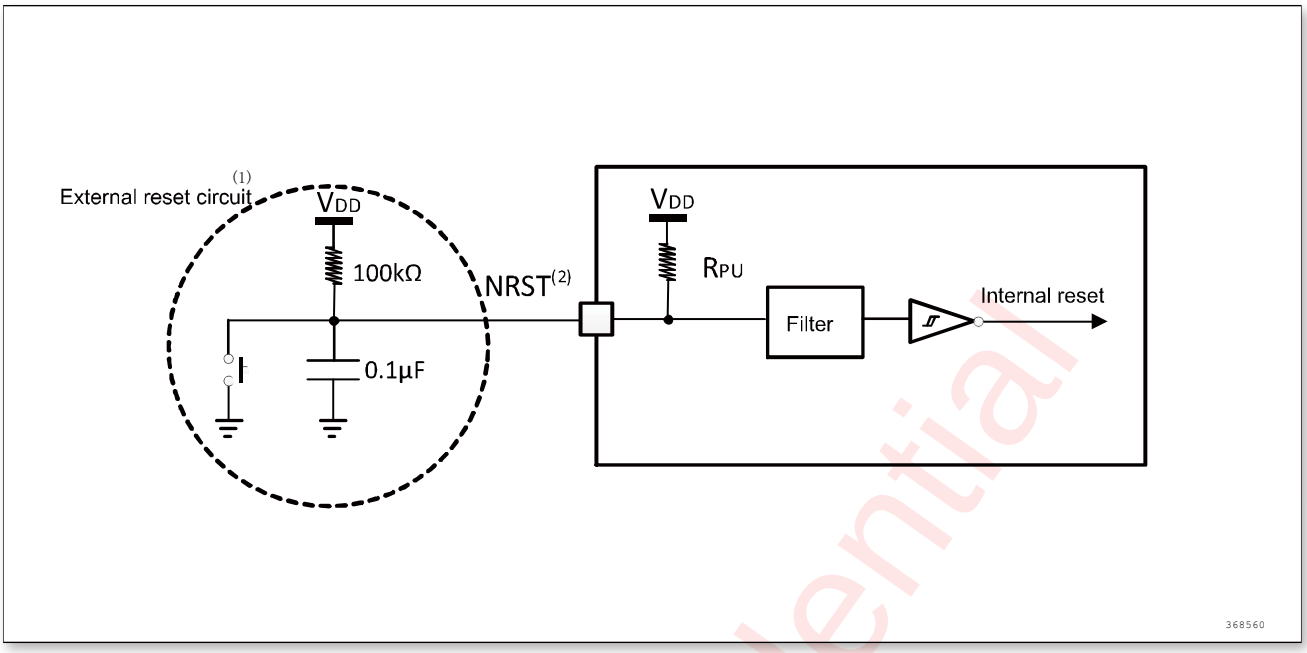


Figure 8 Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in NRST pin characteristics, otherwise the MCU cannot be reset.

TIMER CHARACTERISTICS

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see I/O port characteristics.

TIMx(1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.89	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 72MHz	0	72	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.01389	910.2	µs
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	-	59.7	S
t_{MAX_IN}	TIM maximum input frequency	-	-	144	MHz

1. Guaranteed by design, not tested in production.

COMMUNICATION INTERFACES

I²C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and general supply voltage conditions.

The I²C interface conforms to the standard I²C communication protocol but has the following limitations: SDA

and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I²C characteristics are listed in the following table. Refer to I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

I²C characteristics

Symbol	Parameter	Standard I²C (1)		Fast mode I²C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	μs
$t_{w(SCLH)}$	SCL clock high time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{su(SDA)}$	SDA setup time	$2*t_{PCLK}$	-	$2*t_{PCLK}$	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	$6*t_{PCLK} – 1$ (4)	-	$6*t_{PCLK}$ - 0.3 (4)	μs
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	$6*t_{PCLK} – 1$ (4)	-	$6*t_{PCLK}$ - 0.3 (4)	μs
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$	-	$8*t_{PCLK}$	-	μs
$t_{su(STA)}$	Start condition setup time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{su(STO)}$	Stop condition setup time	$6*t_{PCLK}$	-	$6*t_{PCLK}$	-	μs
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	$5*t_{PCLK}$	-	$5*t_{PCLK}$	-	μs
C_b	Capacitive load of each bus	4.7	-	1.2	-	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I²C frequencies. It must be at least 12MHz to achieve fast mode I²C frequencies.
3. Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.
   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.
4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

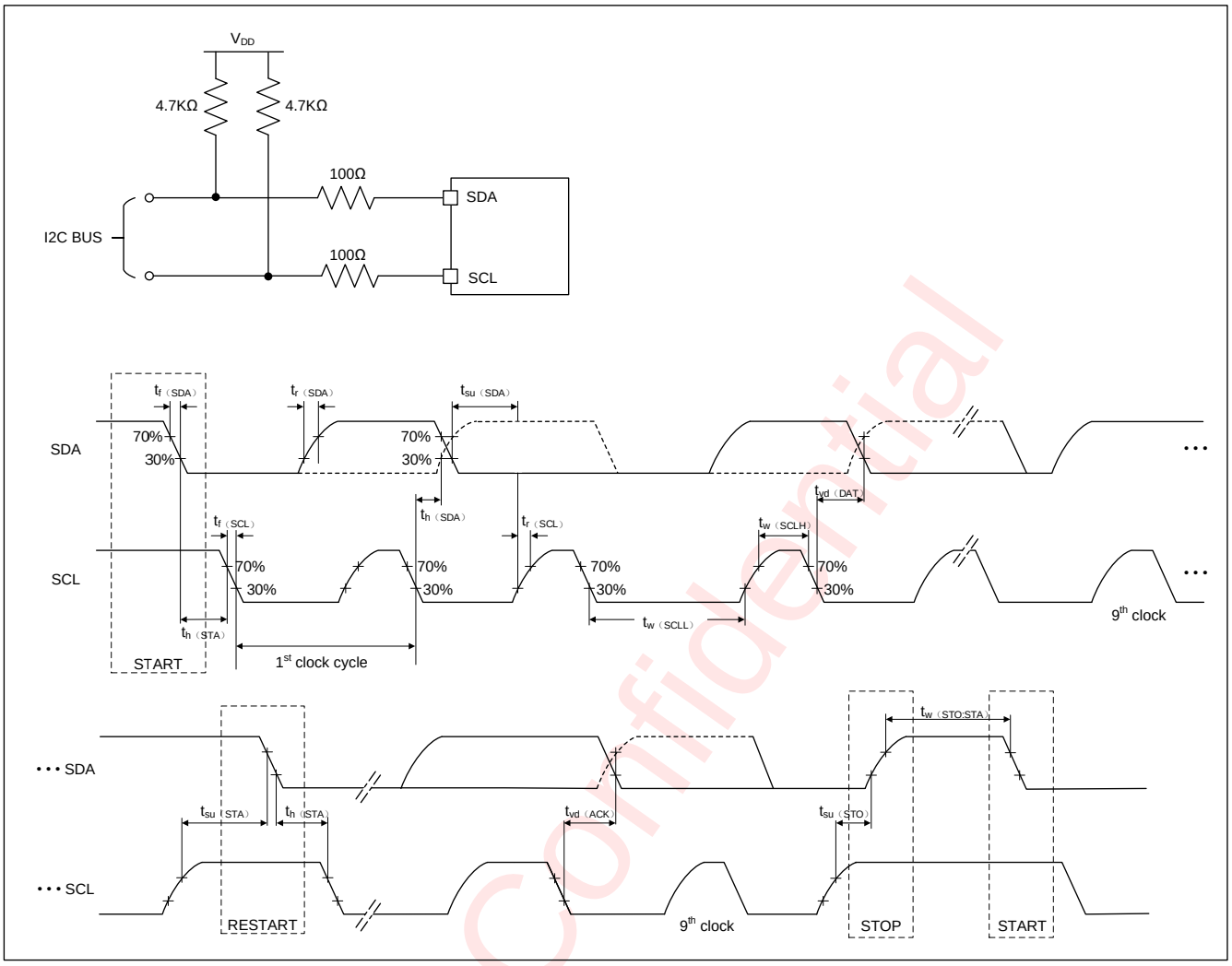


Figure 9 I²C bus AC waveform and measurement circuit (1)

1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage general conditions.

Refer to section I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, T_A = 25°C	-	36 (4)	MHz
		Slave mode, T_A = 25°C	-	18	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	10	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	10	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$+ 6	ns

$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	15	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	15	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	15	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.
4. When the SPI works at its limit speed, it is recommended to connect a serial matching resistor to the SCK wire to ensure the stability of transmission; and ensure that the SCK wire of the SPI Master and SPI Slave are as short as possible.

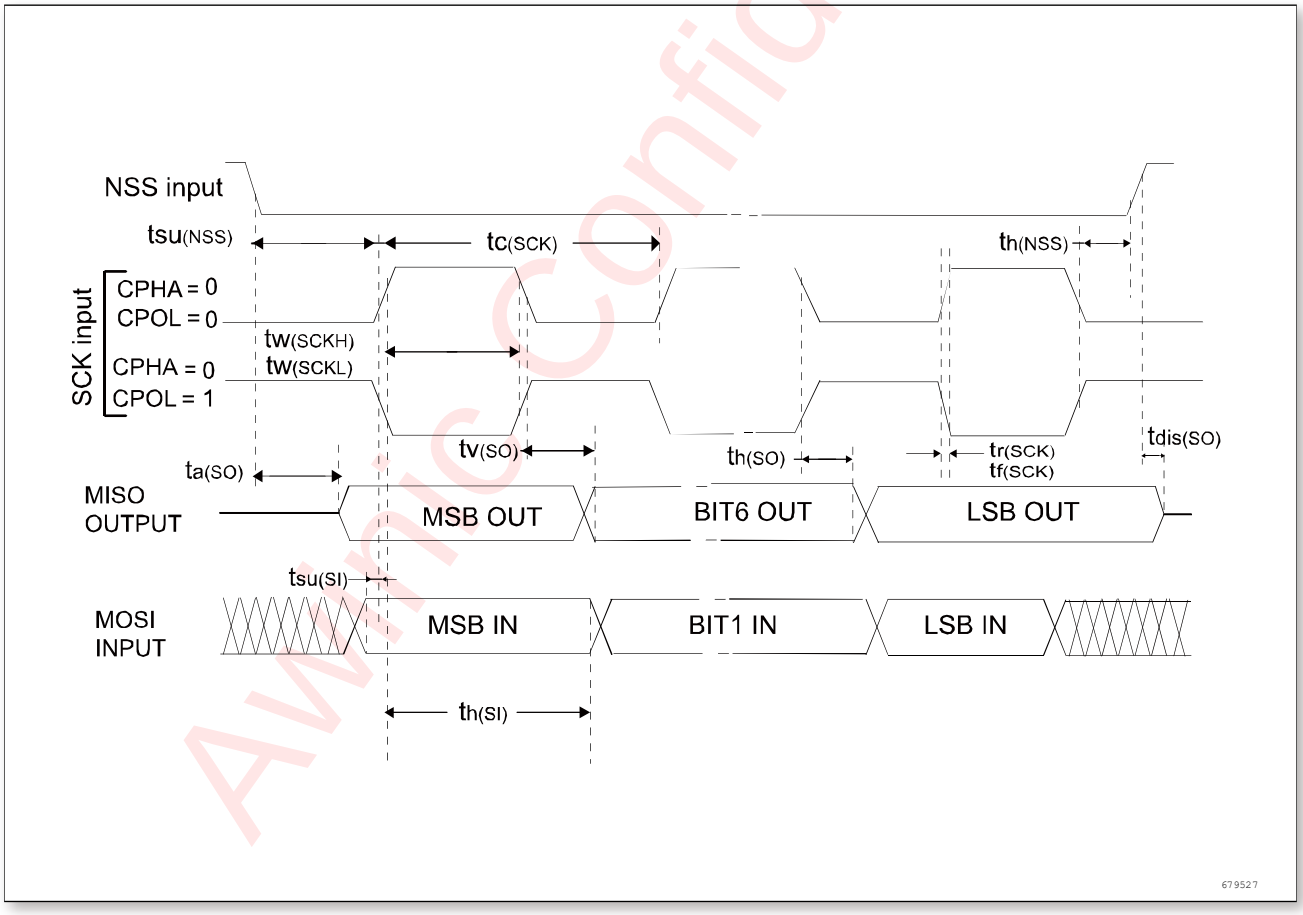


Figure 10 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

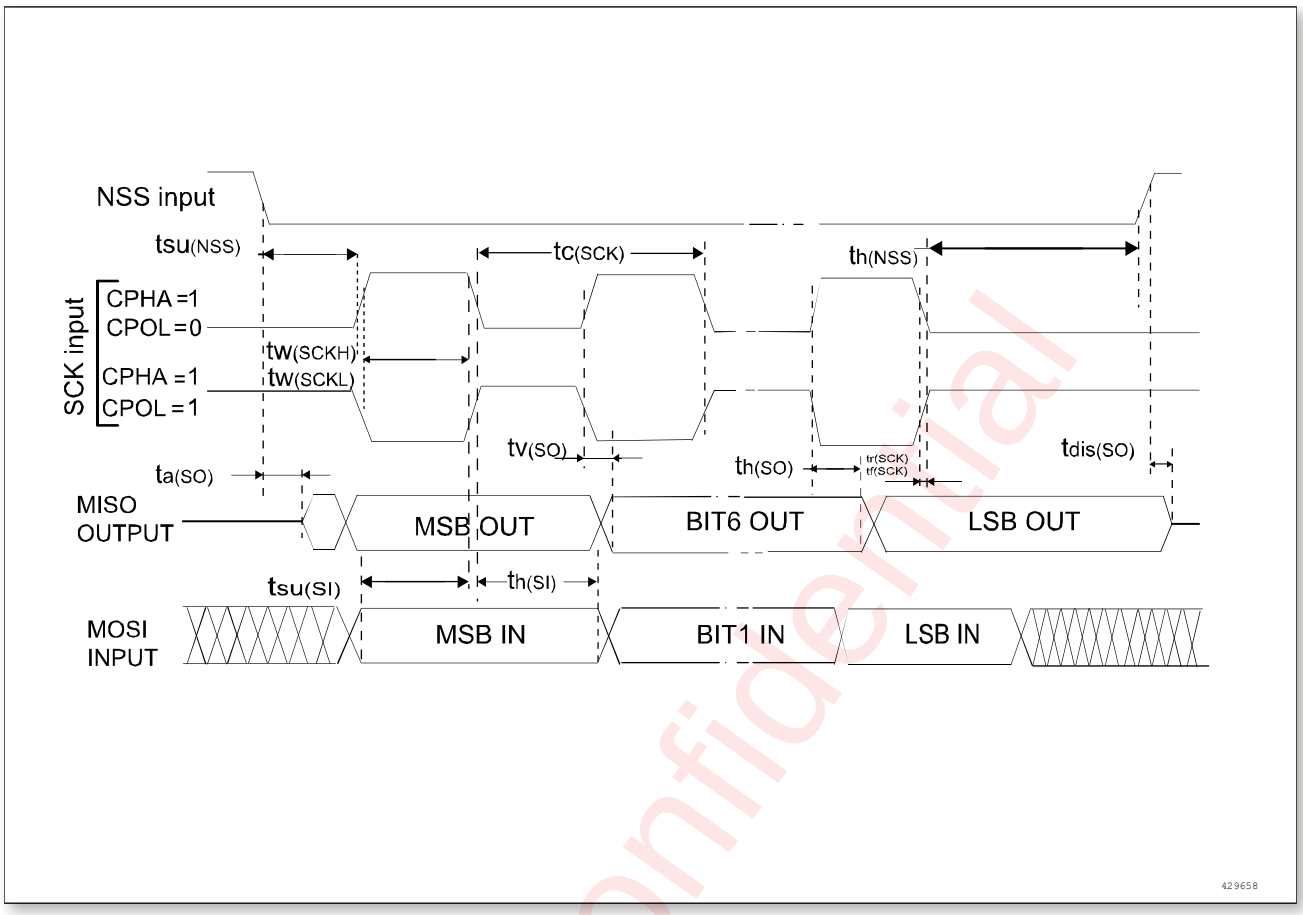


Figure 11 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

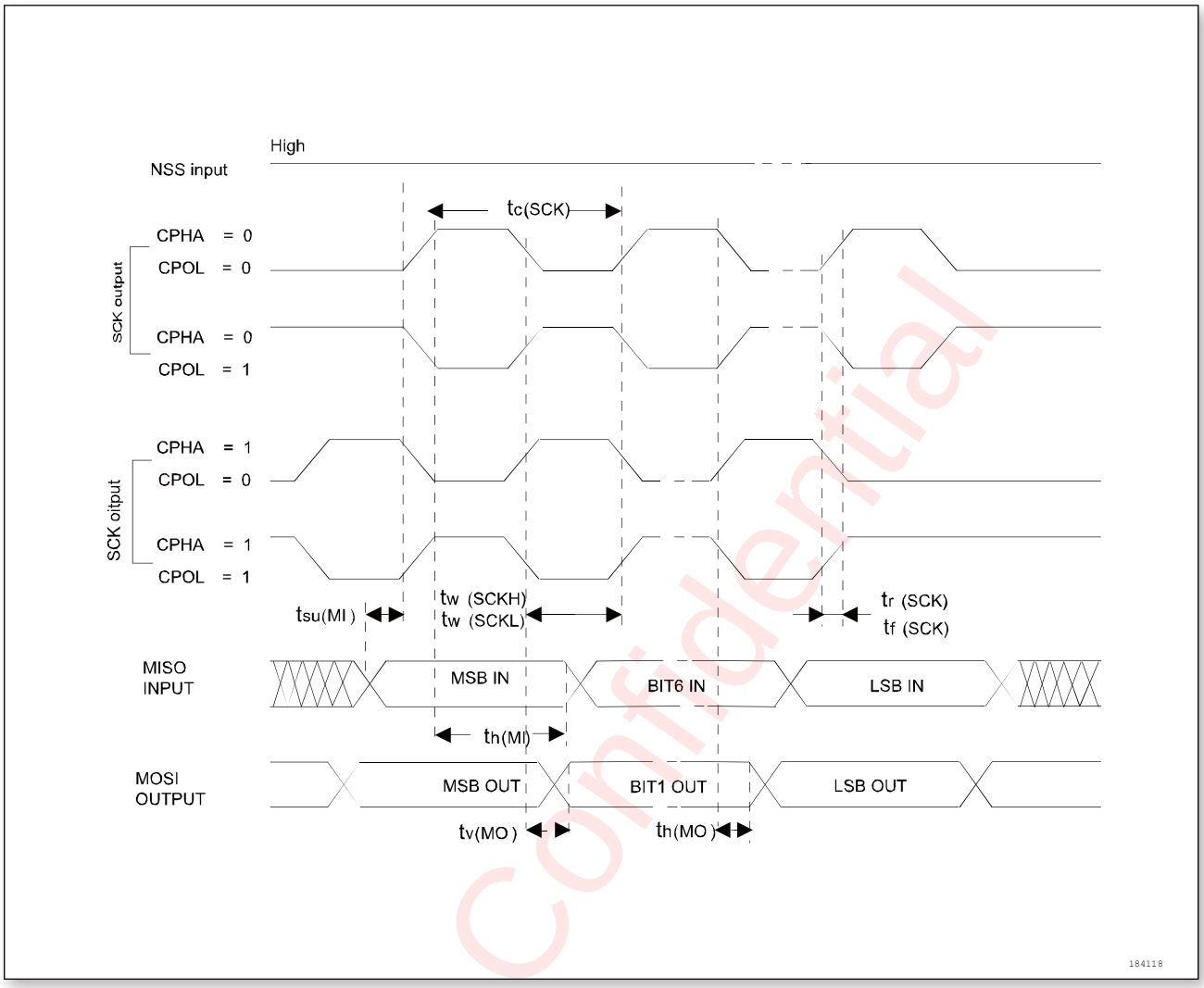


Figure 12 SPI timing diagram-master mode, CPHASEL = 1 (1)

1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

FLEXCAN INTERFACE

For details on the characteristics of the input and output alternate function pins (CAN_TX and CAN_RX), see I/O port characteristics.

ADC CHARACTERISTICS

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the general conditions.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	-	-	-	1	MHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V

R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
			2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	10.7	-	bit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Maximum R_{AIN} at f_{ADC} = 15MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design. Not tested in production.

ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-6/+3	LSB
EO	Offset error		-2/+3	
EG	Gain error		+3	
ED	Differential linearity error		-1/+2	
EL	Integral linearity error		-3/+3	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section Recommended Operating Conditions does not affect the ADC accuracy.
2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 12.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

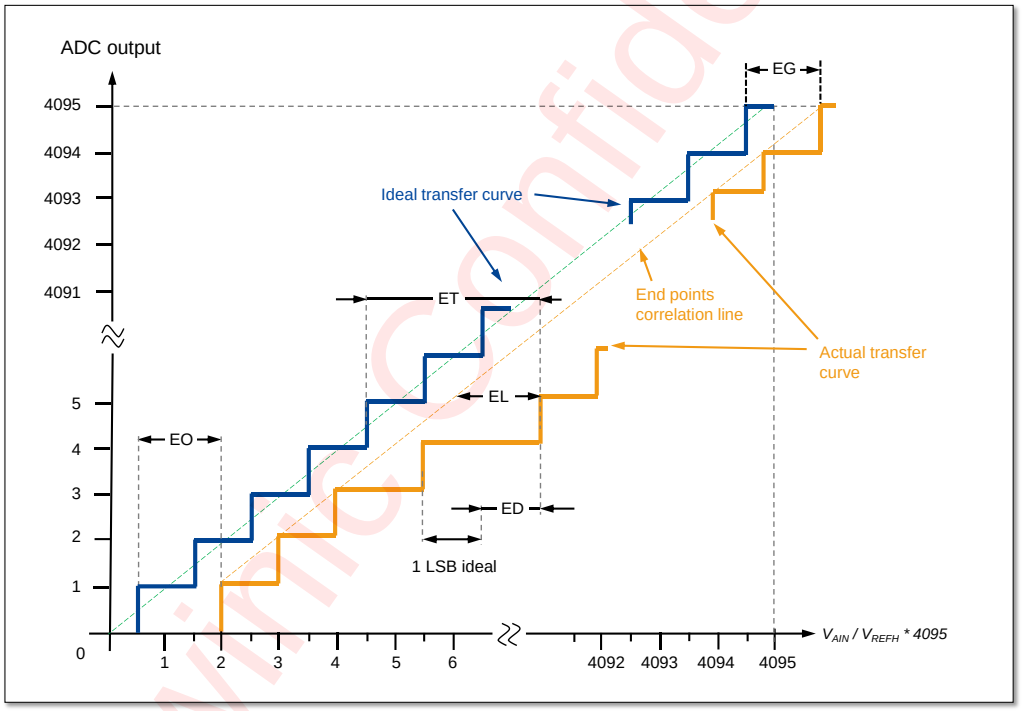


Figure 13 Schematic diagram of ADC static parameters

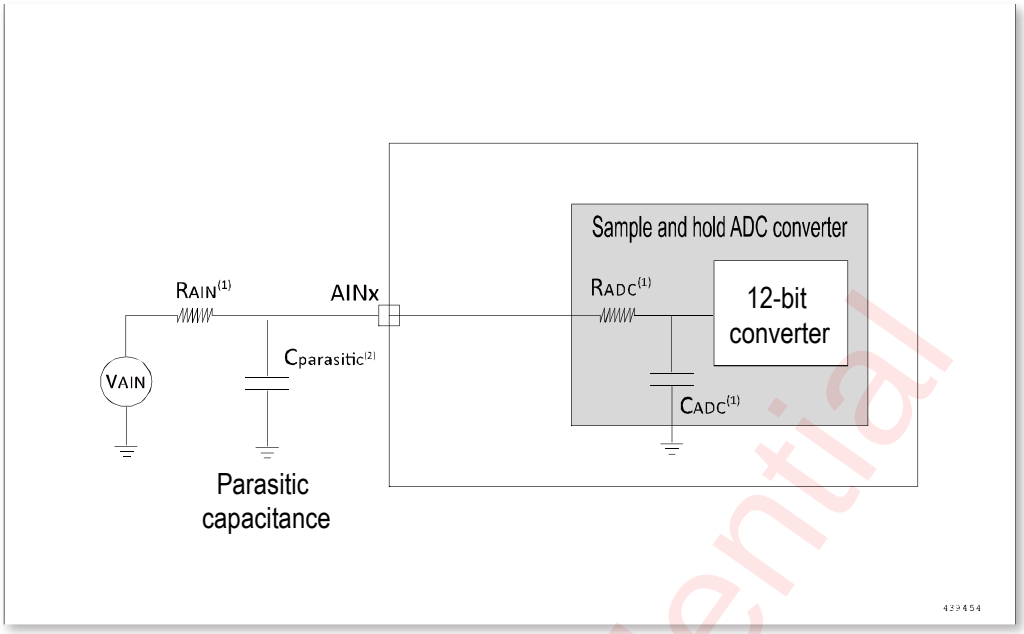


Figure 14 Typical connection diagram using the ADC

1. See ADC CHARACTERISTICS for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality), and they should be as close as possible to the MCU chip.

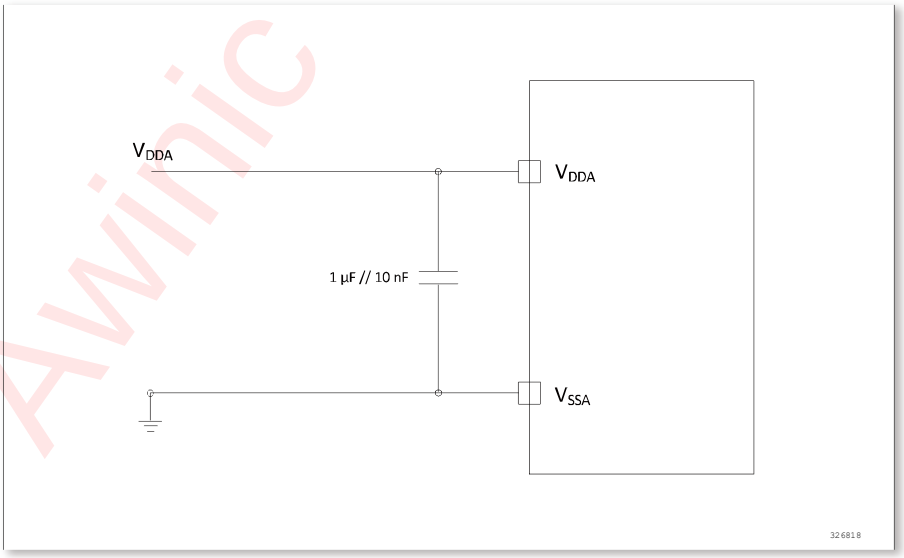


Figure 15 Power supply and reference power supply decoupling circuit

TEMPERATURE SENSOR CHARACTERISTICS

The temperature sensor is calculated using the formula below:

Temperature formula

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

Where offset is recorded in the lower 12bits of 0x1FFFF7F6

Temperature sensor characteristics (3)(4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature	-10	-	+10	°C
Avg_Slope (2)	Average slope	4.4	4.955	5.313	mV/°C
V_{25} (1)	Voltage at 25℃	1.086	1.465	1.744	V
t_{START} (2)	Setup time	-	-	10	μS
t_{S_temp} (2)	ADC sampling time when reading temperature	-	11.8	-	μS

1. Guaranteed based on characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. The shortest sampling time can be determined by application through multiple iterations.
4. VDD = 3.3V

COMPARATOR CHARACTERISTICS

Comparator characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{HYST}	Hysteresis	HYST = 00, MODE = 00	-	0	-	mV
		HYST = 01, MODE = 00	15	22	43	mV
		HYST = 10, MODE = 00	32	45	92	mV
		HYST = 11, MODE = 00	55	85	182	mV
		HYST = 00, MODE != 00	-	0	-	mV
		HYST = 01, MODE != 00	13	15	23	mV
		HYST = 10, MODE != 00	25.2	32	46.7	mV
		HYST = 11, MODE != 00	25.5	60	83.9	mV
V_{OFFSET}	Offset voltage	HYST = 00	-	±6	±10.4	mV
		HYST = 01	-	±5.5	±10	mV
		HYST = 10	-	±5	±9	mV
		HYST = 11	-	±4	±7	mV
t_{DELAY}	Propagation delay	MODE = 00	3.7	10.7	43	ns
		MODE = 01	10.5	34.9	83	ns
		MODE = 10	13.8	49	114	ns
		MODE = 11	22.2	86	194.5	ns
I_q	Average working current	MODE = 00	6.5	45	89.2	uA
		MODE = 01	3.3	8.6	24.7	uA
		MODE = 10	2.6	6	25.4	uA
		MODE = 11	1.7	4.6	16	uA

1. Guaranteed by design, not tested in production.

Detailed Functional Description

CORE INTRODUCTION

The processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The core is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

BUS INTRODUCTION

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, HWDIV, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

MEMORY MAP

Table 1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 FFFF	64 KB	Map to main Flash, system memory or SRAM according to boot configuration
	0x0800 0000 - 0x0800 FFFF	64 KB	Main Flash
	0x1FFE 1000 - 0x1FFE 11FF	0.5 KB	Encrypted area
	0x1FFE 1200 - 0x1FFE 1BFF	2.5 KB	Encrypted area
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option bytes
SRAM	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM
APB1	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 4800 - 0x4000 4BFF	1 KB	UART3
	0x4000 5400 - 0x4000 57FF	1 KB	I^2C1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 C000 - 0x4000 FFFF	16 KB	FlexCAN
APB2	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1

Bus	Address range	Size	Peripheral
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3C00 - 0x4001 3FFF	1 KB	COMP
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
AHB	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 2000 - 0x4002 23FF	1 KB	Flash Interface
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4003 0000 - 0x4003 03FF	1 KB	HWDIV
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD

FLASH

This product provides up to 64KB embedded Flash memory available for storing code and data.

SRAM

This product provides up to 8KB embedded SRAM.

NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect a pulse width shorter than the internal APB2 clock period.

CLOCK AND BOOT

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB (APB1 and APB2) bus. The maximum frequency of the AHB and APB bus clock can reach up to 72MHz.

BOOT MODES

During boot, BOOT0 pin and nBOOT1 bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

POWER SUPPLY SCHEMES

- V_{DD} = 2.7V ~ 5.5V: I/O ports and internal voltage regulator are powered by the VDD Pins.
- V_{DDA} = 2.7V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the VDDA pin. VDDA and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and GND.
- The GPIO input or pull-up should be later than VDD and VDDA is established.

POWER SUPPLY SUPERVISORS

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled.

VOLTAGE REGULATOR

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that used by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

LOW POWER MODE

This product supports multiple low power modes, user can select the low power modes according to their application to achieve a balance between power consumption, wakeup time and wakeup source.

Sleep mode

In Sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In Stop mode, low power consumption can be achieved with all RAM and registers content in retention. In Stop mode, HSI is powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep Stop mode

Similar as Stop mode, but with lower power consumption.

Standby mode

In Standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL and HSI are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin, IWDG reset. SRAM and registers content are lost in this mode. Only standby circuit are powered.

The peripheral status in each low-power mode is shown in **Table** , please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.
- High-z represents a high-impedance state.

Table 2 Peripheral status in different power modes

Module/Mode	Run	Sleep	Stop	Deep Stop	Standby
Max. Freq.	72MHz	72MHz	40KHz	40KHz	40KHz
PVD	Optional	Optional	Optional	Optional	OFF
POR/BOR	ON	ON	ON	ON	ON
CPU	ON	OFF	OFF	OFF	Power Down
SRAM	ON	ON	Retention	Retention	Power Down
Flash	ON	Standby	Standby	Deep Standby	Power Down
HSI	Optional	Optional	OFF	Power Down	Power Down
PLL	Optional	Optional	Power Down	Power Down	Power Down
LSI	Optional	Optional	Optional	Optional	Optional
ADC	Optional	Optional	OFF	OFF	OFF
COMP	Optional	Optional	Optional	Optional	OFF
IWDG	Optional	Optional	Optional	Optional	Optional
Other Peripherals	Optional	Optional	OFF	OFF	Power Down
I/O	Optional	Retention	Retention	Retention	High-z (1)

1. NRST maintains the reset function, wakeup I/O (WKUP) can wake up, other I/Os are high impedance.

HARDWARE DIVIDER

This product has a hardware divider unit (HWDIV). It can automatically run the 32-bit signed or unsigned integer division operation. The HWDIV is especially useful in some high-performance applications.

DMA

This product has a 5-channel direct memory access (DMA) controller. The DMA controller can be used to move data from memory to memory, peripherals to memory or memory to peripherals without CPU intervention. The DMA controller support ring buffer mode, when data reaches end of the buffer, the ring buffer mode can avoid generating an interrupt.

Each DMA channel has independent DMA request handling logic. All channels can be triggered by software. For each channel, the data length, source address and destination address can be independently configured by software.

DMA can be used for peripherals include UART, I^2C, SPI, ADC, and general purpose, advanced, or basic timers.

TIMERS AND WATCHDOGS

This product has one advanced timer, two general purpose timers, three basic timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	up, down, up/down	1 to 65536	Yes	4	No
	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM14	16-bit	up	1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	up	1 to 65536	Yes	1	1

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide

synchronization and event trigger function.

In debug mode, the counter can be frozen.

General-purpose timer (TIMx)

This product has two general-purpose timers (TIM2, TIM3). The timer has a 16- or 32-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

32-bit general-purpose timer

This timer has a 32-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used as input capture, output compare, PWM or single pulse output.

16-bit general-purpose timer

This timer has a 16-bit up and down counter, a 16-bit prescaler and four independent channels, each channel can be used for input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer. Each timer has independent DMA request.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter can be frozen.

Basic timer (TIM14 / TIM16 / TIM17)

This product has three basic timers (TIM14 / TIM16 / TIM17), each timer has a 16-bit counter, supports automatic reload, and only supports up-counting. The timer has a 16-bit prescaler and one independent channel, each channel can be used as input capture, output compare, PWM or single pulse output. When used in PWM mode, TIM14 has no complementary output port, TIM16 and TIM17 are equipped with complementary output port, which can generate complementary PWM pairs and support hardware dead-timer insertion.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in Stop and Standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

UART

This product has up to three UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode. All UART interfaces support DMA operation.

I²C

This product has up to one I²C interface. The I²C bus interface can work in multi-master mode or slave mode and supports standard and fast mode. The I²C interface supports 7-bit or 10-bit addressing.

SPI

This product has up to two SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 36 Mbps in master mode and 18 Mbps in slave mode. All SPI interfaces support DMA operation.

I2S

This product has up to two I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

FLEXCAN

This product has up to one FlexCAN interface. The FlexCAN interface is compatible with CAN 2.0A and 2.0B (active) standard, with bit rate up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

ADC

This product has one 12-bit analog/digital converter (ADC), with up to 13 external channels available, supports single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed. The ADC supports DMA operation.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

Temperature sensor

The temperature sensor can generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC to covert the output of the sensor to a digital value.

COMP

This product has one build-in analog comparators (COMP), which can be used independently (applicable to all I/O ports that have comparator function) or combined with timers. The COMP module can be used for a variety of functions including low-power mode wake-up event triggered by analog input, fast PWM output break when over-current detected, events capture and OCref-clr events used for cycle-by-cycle current control. The COMP module supports programmable hysteresis voltage, programmable rate and power consumption, rail-to-rail comparator. Each comparator can select the voltage reference from the I/O ports or the internal voltage reference (CRV) which is a divided voltage value of the V_{DDA} or internal bandgap voltage.

CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

SWD

This product equips standard Serial Wire Debug (SWD)

MATRIX LED DRIVER BLOCK OPERATION MODE AND RESET

POWER UP TIMING

It is recommended that VCC, VDD and VDDIO should be connected to the same power supply. During initial power-up, VCC should power up no later than VDD. After LED driver module initialization, pull LED_Driver_EN (PB14) up to enable matrix LED driver module. The LED_Clock need 100μs to enter stable operation mode, then matrix LED driver module can be configured.

Below is the recommended operation timing:

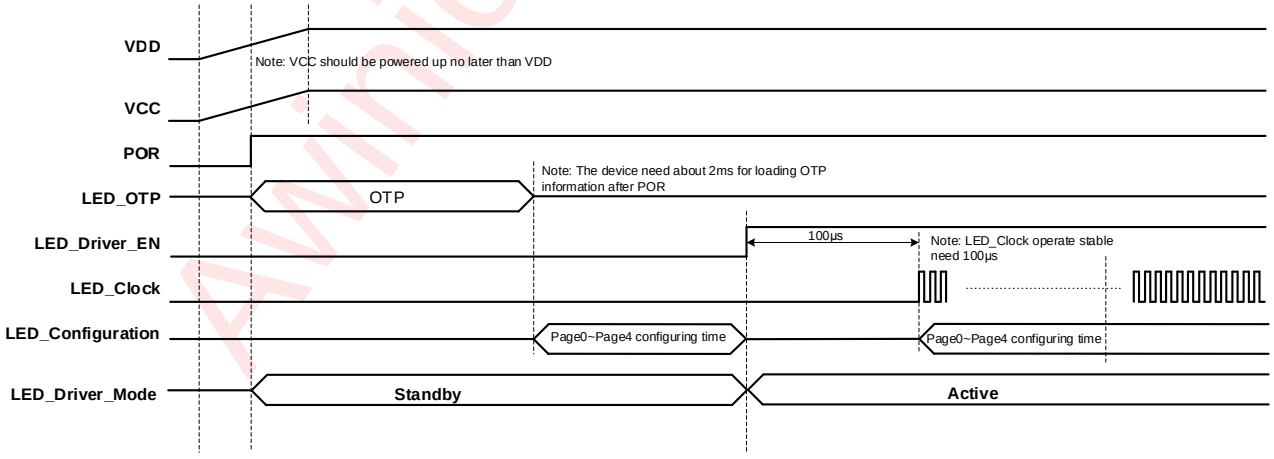


Figure 16 Power up Timing

STANDBY MODE

When the EN pin (PB14) of the matrix LED Driver module is pulled low or the CHIPEN [Bit0] configuration of the GCR (Page0:00H) register is set to 0, the LED Driver module will automatically enter Standby mode. When the LED Driver is in Standby mode, all analog LED Driver modules are powered off, but the SPI interface can be accessed and all registers can be configured. When the LED Driver module POR is triggered, the LED

Driver module enters Standby mode and all registers will be reset.

ACTIVE MODE

When the EN pin (PB14) of the AW22216 LED Driver module is pulled high and the CHIPEN [Bit0] configuration of the GCR (Page0:00H) register is set to 1, the LED Driver module enters Active mode.

LOW POWER MODE

When the LPEN [Bit1] of the MIXCR (Page 0:46H) register of the LED Driver module is set to 1, the low-power mode of the LED Driver module is enabled. When all PWM registers of the LED Driver have a value of 0x00, the LED Driver automatically enters low-power mode. Once a non-zero value is written to any PWM register, the LED Driver will immediately exit low-power mode.

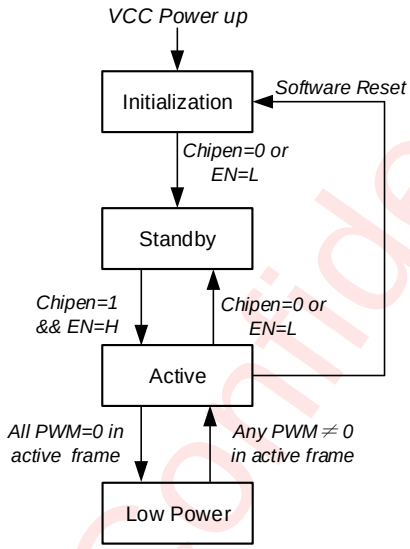


Figure 17 Matrix LED Driver Module Operating Mode Transition

MATRIX LED DRIVER OVER TEMPERATURE PROTECTION (OTP)

OVER TEMPERATURE ROLL OFF

The bits TRTH[1:0] and bits TROF[1:0] of register OTCR (page0, address=0x27) are thermal roll off threshold temperature and thermal roll off percentage of I_{OUT} respectively. The threshold temperature can be configured as 140°C, 120°C, 100°C or 90°C. Thermal roll off percentage can be configured as 100%, 75%, 50% or 30%. When set the bits TRTH[1:0] to be “00” and set bits TROF[1:0] to be “10”, the thermal roll off threshold temperature is “140°C”. Once the temperature is over 140°C, the flag bit TRFLG of register OTCR (page0, address=0x27) is set to “1”, and I_{OUT} will be decreased to its 55%.

OVER TEMPERATURE ALL LED IS OFF

When bit OTDIS of the register OTCR (page0, address=0x27) is set to “0”, the over-temperature detection is enabled. Once the temperature of this device reaches 165°C, the over-temperature condition is detected, and the bit OTFLG of the register OTCR (page0, address=0x27) will be set to “1”. The OTFLG will be cleared to “0” after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (page0, address=0x27) are set to “0”, the Over-Temperature Protection (OTP) function is enabled. Once the temperature is over 165°C, the bit CHIPEN of the register GCR (page0, address=0x00) will be cleared to “0”, and then the device will enter into standby mode. When the temperature returns below 140°C, the device will enter into active mode again after writing “1” to bit CHIPEN.

By default, control bits OTDIS and OTPD are all “0”, both OT monitor and OT protection are enable.

LED OPEN/SHORT DETECTION

AW22216 supports LED open/short detection. When bits OSDE[1:0] of the register GCR (page0, address=0x00) are set to “11”, open detection is enabled, and the detection results can be read out via the registers OSR0~OSR35 (page0, address=0x03~0x26) when CHIPEN is “1”. Similarly, when set bits OSDE[1:0] of the register GCR (page0, address=0x00) to “10”, short detection is enabled, and the results also can be read out via the registers OSR0~OSR35 when CHIPEN is “1”. Each bit of OSR0~OSR35 store a LED’s open/short status. Each OSR register stores 6 LEDs open/short status in bit5~bit0. For example, OSR0 stores the status of LED0~LED5, in which MSB is status of LED5, and LSB is status of LED0.

	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	CS16	CS17	CS18
SW1	OSR0						OSR1						OSR2					
SW2	OSR3						OSR4						OSR5					
SW3	OSR6						OSR7						OSR8					
SW4	OSR9						OSR10						OSR11					
SW5	OSR12						OSR13						OSR14					
SW6	OSR15						OSR16						OSR17					
SW7	OSR18						OSR19						OSR20					
SW8	OSR21						OSR22						OSR23					
SW9	OSR24						OSR25						OSR26					
SW10	OSR27						OSR28						OSR29					
SW11	OSR30						OSR31						OSR32					
SW12	OSR33						OSR34						OSR35					

Figure 18 Open/Short Register

The valid detect result is determined by:

Short detection: V_{cs} > PVCC-VTH_{SHORT}

Open detection: V_{cs} < VTH_{OPEN}

VTH_{SHORT}: Threshold of short detection (VTH_{SHORT} = 1.5V, typical).

VTH_{OPEN}: Threshold of open detection (VTH_{OPEN} = 0.1V, typical).

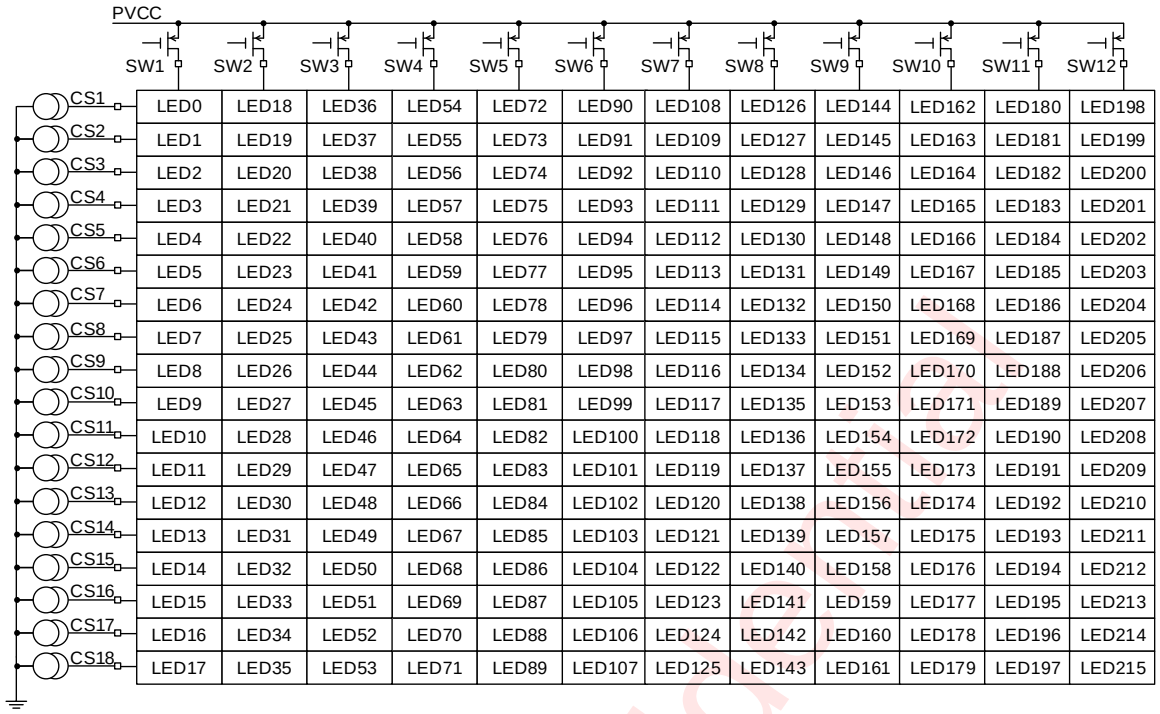
The recommend configuration in PVCC=4.2V is:

- PSEL[1:0] = 2’b00, (page0.PCCR[1:0]);
- 0x05 ≤ GCC[7:0] ≤ 0x80, (page0.GCCR);
- 0x20 ≤ PWM[7:0] ≤ 0xFF, (page1.PWMn, n=0~215);
- SL=0xFF, (page2.SLn, n=0~215);

LED DISPLAY AND CONTROL

LED DISPLAY CONTROL DESCRIPTION

The device supports up to 216 LEDs. The location of each LED is shown by the following figure. The parameter location in page1~page3 is the same as the LED.



LED0	LED18	LED36	LED54	LED72	LED90	LED108	LED126	LED144	LED162	LED180	LED198
LED1	LED19	LED37	LED55	LED73	LED91	LED109	LED127	LED145	LED163	LED181	LED199
LED2	LED20	LED38	LED56	LED74	LED92	LED110	LED128	LED146	LED164	LED182	LED200
LED3	LED21	LED39	LED57	LED75	LED93	LED111	LED129	LED147	LED165	LED183	LED201
LED4	LED22	LED40	LED58	LED76	LED94	LED112	LED130	LED148	LED166	LED184	LED202
LED5	LED23	LED41	LED59	LED77	LED95	LED113	LED131	LED149	LED167	LED185	LED203
LED6	LED24	LED42	LED60	LED78	LED96	LED114	LED132	LED150	LED168	LED186	LED204
LED7	LED25	LED43	LED61	LED79	LED97	LED115	LED133	LED151	LED169	LED187	LED205
LED8	LED26	LED44	LED62	LED80	LED98	LED116	LED134	LED152	LED170	LED188	LED206
LED9	LED27	LED45	LED63	LED81	LED99	LED117	LED135	LED153	LED171	LED189	LED207
LED10	LED28	LED46	LED64	LED82	LED100	LED118	LED136	LED154	LED172	LED190	LED208
LED11	LED29	LED47	LED65	LED83	LED101	LED119	LED137	LED155	LED173	LED191	LED209
LED12	LED30	LED48	LED66	LED84	LED102	LED120	LED138	LED156	LED174	LED192	LED210
LED13	LED31	LED49	LED67	LED85	LED103	LED121	LED139	LED157	LED175	LED193	LED211
LED14	LED32	LED50	LED68	LED86	LED104	LED122	LED140	LED158	LED176	LED194	LED212
LED15	LED33	LED51	LED69	LED87	LED105	LED123	LED141	LED159	LED177	LED195	LED213
LED16	LED34	LED52	LED70	LED88	LED106	LED124	LED142	LED160	LED178	LED196	LED214
LED17	LED35	LED53	LED71	LED89	LED107	LED125	LED143	LED161	LED179	LED197	LED215

Figure 19 LED Location

In the LED driver module, each LED is controlled by 4 independent parameters:

- GCC[7:0] control, Global Current Controal, register GCCR (page0, address=0x01);
- PWM[7:0] control, register PWMn (page1, address=0x00~0xD7, n=0~215)
- SL[7:0] control, register SLn (page2, address=0x00~0xD7, n=0~215)
- PAT[1:0] selection, PAT choice, register PATn (page3, address= 0x00~0x47, n=0~215)

User can program above parameters to control each LED. Register PWM can control the brightness of LEDs, register SL can control the constant current and register GCCR can adjust the global current. Via configuring registers PATn (n=0~215), Each LED can be controlled by an internal pattern controller (PAT0, PAT1, PAT2) to dimming synchronously or output the same breathing lighting effect. A group PAT of LEDs controlled by register PATGn (n=0~71) which contains 3 adjacent LEDs. The figure below shows the LED current control model of AW22216.

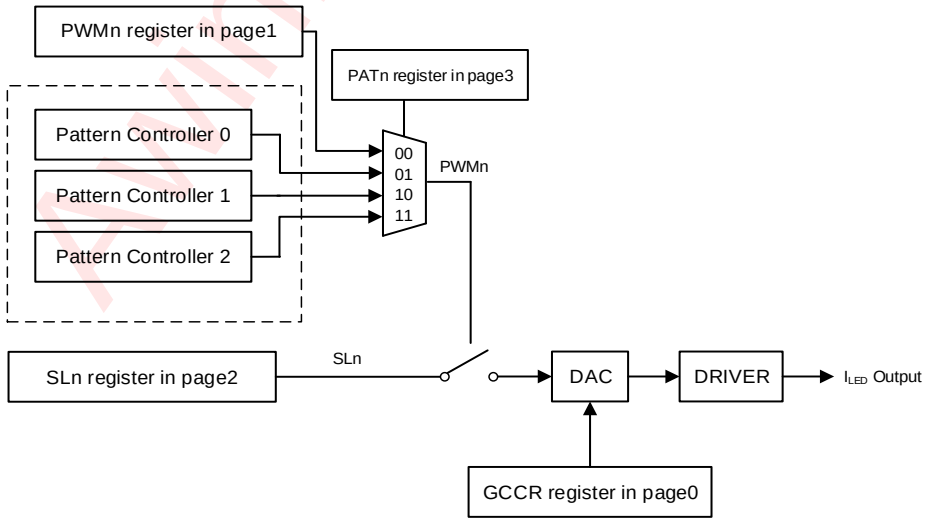


Figure 20 LED Current Control Model

The device supports multiple parameters fast updating. The PWM, SL and PAT parameters of each LED are distributed in page1, page2 and page3 respectively. The page4 is virtual page. In page4, PWM and SL

parameter of each LED are put together, so it is easy to update both PWM and SL in the order of LED in very short time via one continuous write operation of SPI. The following figure shows the distribution of display parameter in different page.

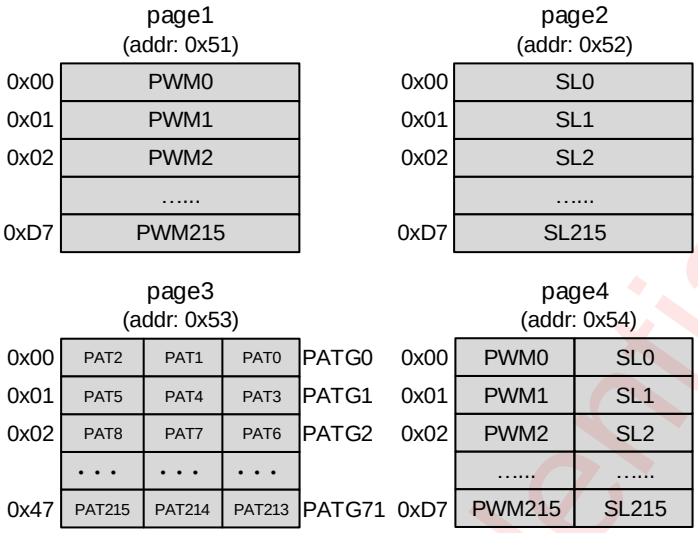


Figure 21 Display Parameter Distribution in Page1~Page4

SCANNING TIMING

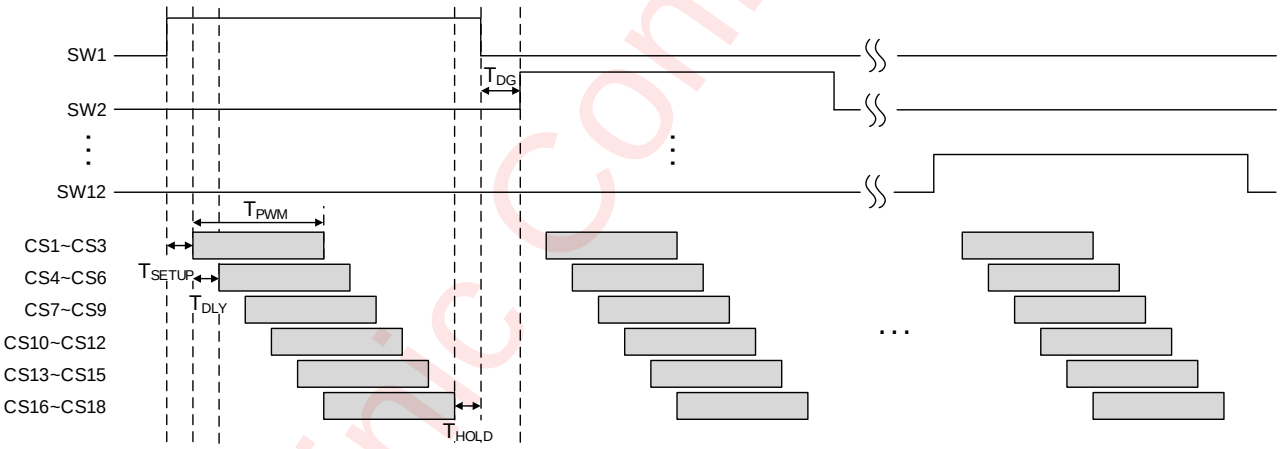


Figure 22 Scanning Timing

As shown in scanning timing figure, the SW1~SW11 is turned on by serial, LED is driven by CS1~CS18 within the SWx (x=1~12) active time. T_{DG} is the non-overlap between SW is De-Ghost time. T_{SETUP} is the delay time between the rising edge of SWx and CS1. SW Control 18 channels current sink (CS1~CS18). CS are divided into 6 groups, and each group has a delay time, which is T_{DLY}. T_{PWM} is PWM active time when the register PWMn=0xFF (n=0~215), and T_{HOLD} is the time between the falling edge of CS18 and SWx. In addition, SW scanning number N (N=1~12) can be controlled by bits SWSEL[3:0] in register GCR. N is the sum of 1 and the value of SWSEL[3:0],when the value of SWSEL[3:0] is below 2'b1100. Otherwise N is 12.

When PCCR.PWMFRQ[2:0] = 000 (page0, address=0x29), the DUTY is:

$$DUTY = \frac{15.9375us}{0.25us + 5 \times 0.125us + 16us + 0.125us + 1us} \times \frac{1}{N}$$

Where T_{PWM} = 15.9375us, T_{SETUP}=0.25us, T_{DLY}=0.125us, T_{HOLD}=0.125us, and T_{DG}=1us. The period of PWM is 16us. N is the SW scanning number.

The average output current of LED_n (n=0~215) can be expressed by the following formula,

$$I_{LED} = \frac{K}{R_{EXT}} \times \frac{GCC}{255} \times \frac{SL_n}{255} \times \frac{PWM_n}{256} \times DUTY$$

Where K = 400V, and R_{EXT} is the value of external resistor.

PWM MODULATION

PWM FREQUENCY

The PWM frequency is decided by bits PWMFRQ[2:0] of register PCCR (page0, address=0x29). Following table shows the relationship of PWM frequency and the PWMFRQ[2:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency higher than 20 kHz.

PWMFRQ[2:0]	000	001	010	011	100	101	110	111
PWM Freq.	62.5kHz	31.25kHz	15.6kHz	7.8kHz	3.9kHz	1.95kHz	975Hz	488Hz

PWM PHASE CONTROL

To reduce the peak load current and ceramic-capacitor audible ringing, AW22216 supports 6 groups phase delay, phase inverting and three-phase mode. When the bits PSEL[1:0] in register PCCR (page0, address=0x29) is "00", the 6 group PWM phase-delay scheme is enabled, which means only 3 of 18 LEDs could switch on in the same time. The following figure shows the timing of phase delay mode.

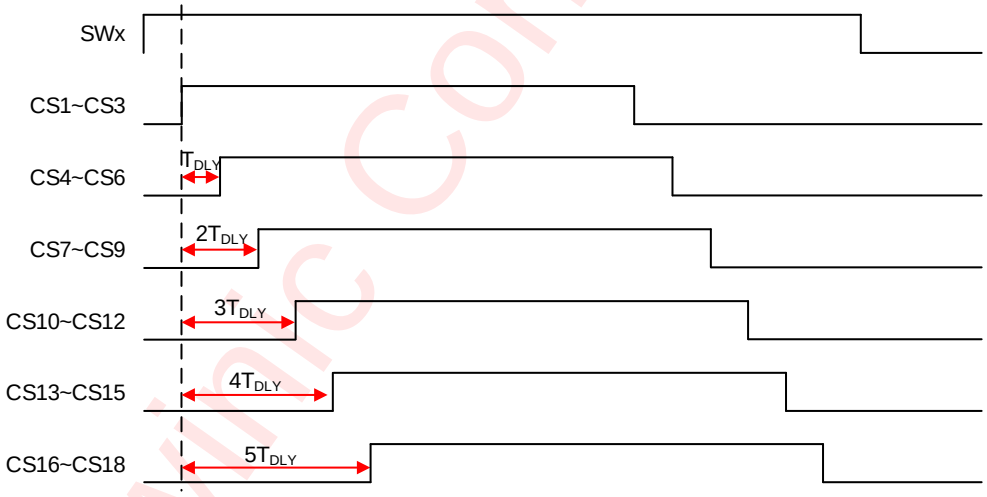


Figure 23 Phase Delay Mode

When setting the PSEL[1:0] to "01", the PWM phase of the even-numbered channels is inverted on the basis of phase-delay, as shown figure phase inverting mode. When setting the PSEL[1:0] to "10/11", three-phase mode is enabled, as shown figure three-phase mode. Phase delay, phase inverting and three-phase mode reduce the number of switch-on LEDs at the same time, which is good for reducing the input-current ripple.

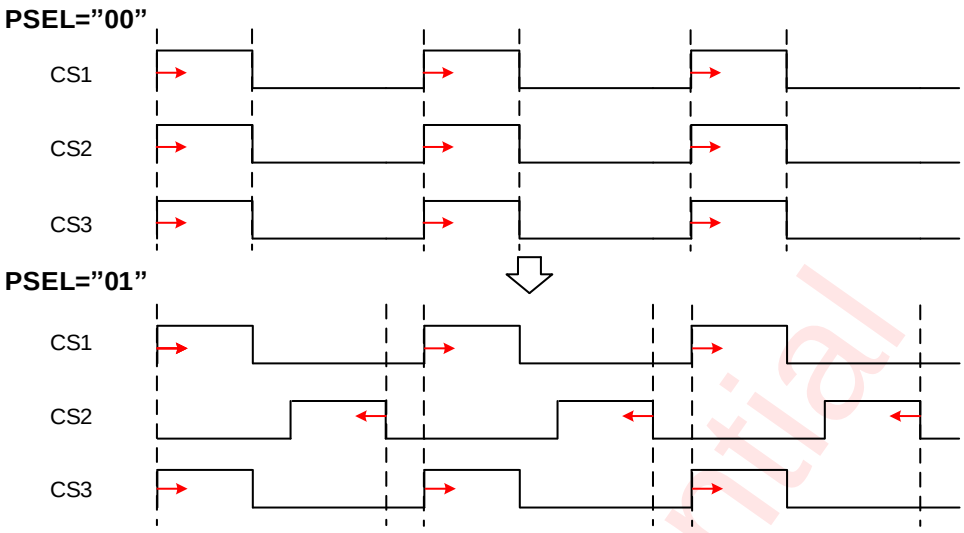


Figure 24 Phase Inverting Mode

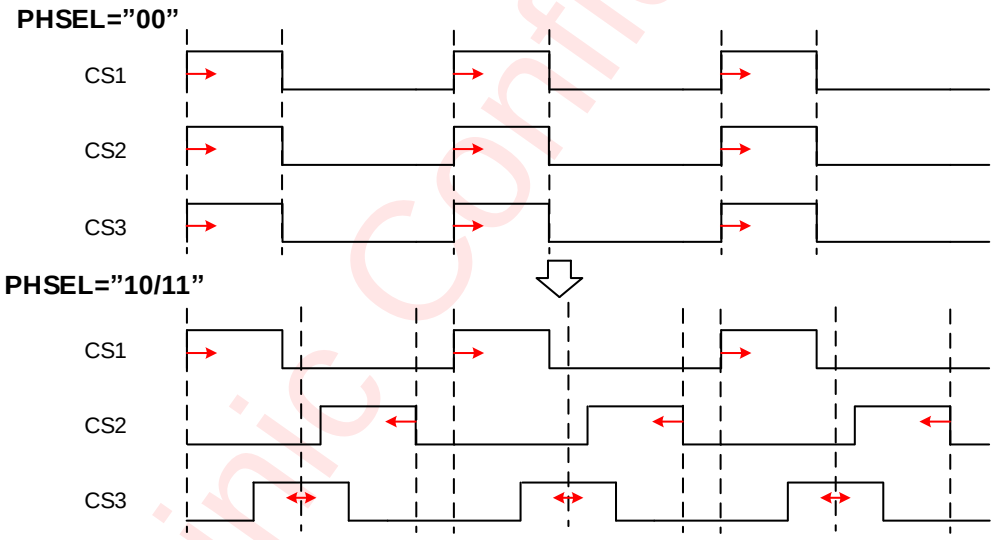


Figure 25 Three-Phase Mode

EMI REDUCTION

SLEW RATE

AW22216 supports programmed slew rate control, which can change the transition time of the LED current sink (CS1~CS18) on or off, so as to achieve the effect of reducing EMI. The slew rate control is configured by the bits SRR and SRF[1:0] of register SRCR(page0, address=0x2B).

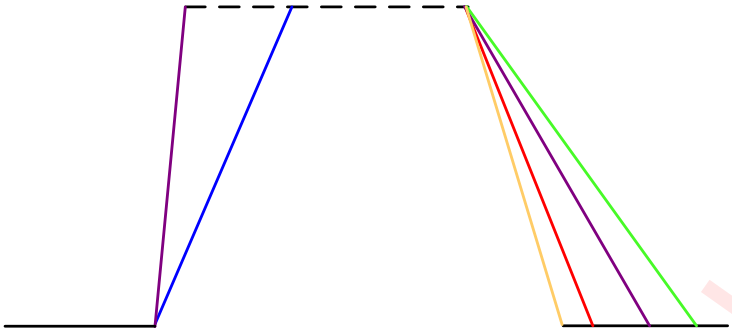


Figure 26 Slew Rate Control

SPREAD SPECTRUM

AW22216 has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (page0, address=0x28) is set to “1”, spread spectrum function is enabled. By setting the bit SSR in register SSCR (page0, address=0x28), four spread spectrum range 5%, 15%, 25% and 35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

DE-GHOST FUNCTION

To prevent the LED ghost effect, AW22216 has integrated pull down resistors for each SWx (x=1~12) and pull up resistor for each CSx (x=1~18). The pull up 8kΩ resistor is disabled when bit PUDIS of register DGCR (page0, address=0x02) is set to “1”, and the PUDIS is “0” in default. In addition, SWPDR[2:0] of register DGCR (page0, address=0x02) can select the SWx pull down resistor. The PDMD of register DGCR (page0, address=0x02) can select the operating mode of de-ghost resistors. When the bit PDMD is “0”, the SWx pull down resistor only work at CSx turning-off time. When the bit PDMD is “1”, the SWx pull down resistor work all the time.

PATTERN CONTROLLERS

There is a breathing pattern controller (BPC) in the device, it has three patterns (PAT0~PAT2). Each LED can be configured different patterns by Page3 (PAT choice register), each register can control three LEDs, and each LED have three patterns (00: PWM, 01: PAT0, 10: PAT1, 11: PAT2). Page3 has 72 registers (72x3). PAT0CFG~PAT2CFG (page0, address=0x42~0x44) are PAT0~PAT2 configure registers. When bit PATEN in register PATxCFG (x=0~2) is set to “1”, breathing pattern controller is enabled. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode.

AUTONOMOUS BREATHING MODE

When PATEN is set to “1”, the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off-time respectively. Register PWMxH (x=0~2, page0, address=0x30~0x32) and PWMxL (x=0~2, page0, address=0x33~0x35) control the maximum and minimum brightness of the breathing, respectively. When bit LOGEN in register PATxCFG (x=0~2) is set to “1”, the lighting effects switch to logarithmic mode. In the logarithmic mode, the lighting effect is smoother than the linear mode during T0 and T2, and causes the change in intensity to appear more linear to the human eye.

The actual time of 4 key periods is as follows:

$$Tx_{real} = \frac{\mathrm{PWMxH} - \mathrm{PWMxL}}{256} \times Tx \qquad (x = 0\ or\ 2)$$

$$Tx_{real} = Tx \qquad (x = 1\ or\ 3)$$

The parameter Tx_{real} is the actual time of 4 key periods, The parameter Tx is the register configuration time.

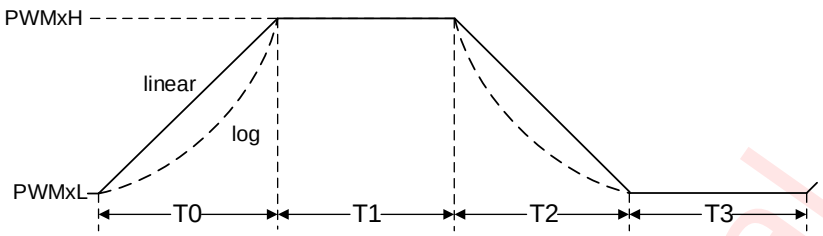


Figure 27 LED Breath Timing in Pattern Mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3, which is set by bits LB[1:0] in register PATxT2 (x=0~2, page0, address=0x38, 0x3C, 0x40). The end point of the loop can only be selected between the end of T0 and the end of T2, which is determined by bits LE[1:0] in register PATxT2 (x=0~2). The repeat times are determined by the end point defined. If bits LE[1:0] are not “00”, the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If bits LE[1:0] are “00”, the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times are decided by bits LT[11:8] in register PATxT2x (x=0~2) and register PATxT3.LT[7:0] (x=0~2, page0, address=0x39, 0x3D, 0x41). When setting LT[11:0] to “0”, the breathing pattern will run unlimited times.

After the breathing pattern is over, the status bit PATFLG in register PATxCFG (x=0~2) will be set to “1”, and PATFLG will be cleared to “0” after reading out through SPI bus. Once breathing loop start again or pattern controller switches to manual mode by setting PATMD bit to “0”, the PATFLG will also be cleared.

When bit RUNx in register PATGO (x=0~2, page0, address=0x45) is set to “1”, breathing pattern x is started. The full process of the autonomous breathing is as follows:

a) Set GCC, SL and PWMxH/L parameter.
b) Set Page 3 (PAT choice registers) to select the pattern of LEDs.
c) Configure PATxT0, PATxT1, PATxT2, PATxT3 (x=0~2) to control the breath time, start/stop point, and repeat times.
d) Set PATEN=1 to enable breathing pattern mode.
e) Set PATMD=1 and RAMPE=1 to select auto breathing mode and enable breathing ramp (x=0~2).
f) Set LOGEN to select the breathing in log curve mode or linear mode (x=0~2).
g) Set RUNx=1 to start the breath pattern x (x=0~2).

MANUAL CONTROL MODE

If bit PATMD is set to “0”, manual control mode is selected. In manual control mode, user could set the bit SWITCH of register PATxCFG (x=0~2) to control the output of pattern controller. When SWITCH is “1”, the output of pattern controller is decided by register PWMxH (x=0~2). When bit SWITCH is set to “0”, the output is the decided by register PWMxL (x=0~2).

If bit RAMPE in register PATxCFG (x=0~2) is set to “1”, the smooth ramp up/down will be enabled. At the same time, if SWITCH changes from “0” to “1”, the output will be ramp up to PWMxH (x=0~2) smoothly. Similarly, if SWITCH changes from “1” to “0”, the output of the pattern controller will ramp down to PWMxL (x=0~2) smoothly. It’s also support the logarithmic mode ramp.

However, if RAMPE is set to “0”, the output of the pattern controller will change to PWMxH or PWMxL(x=0~2) directly with no ramp as the SWITCH changes.

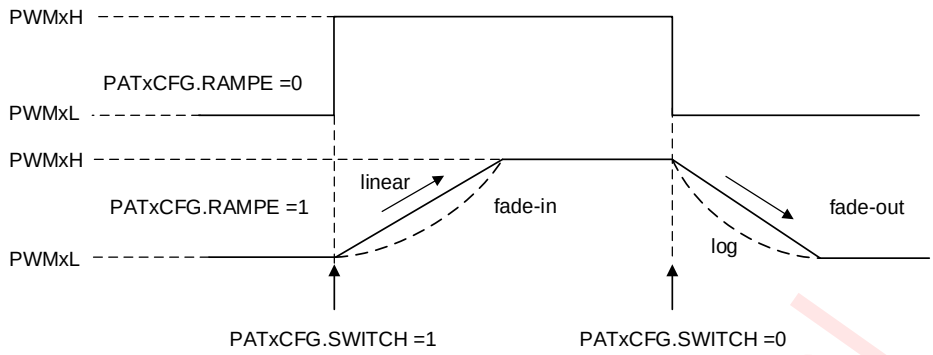


Figure 28 Manual Control Mode

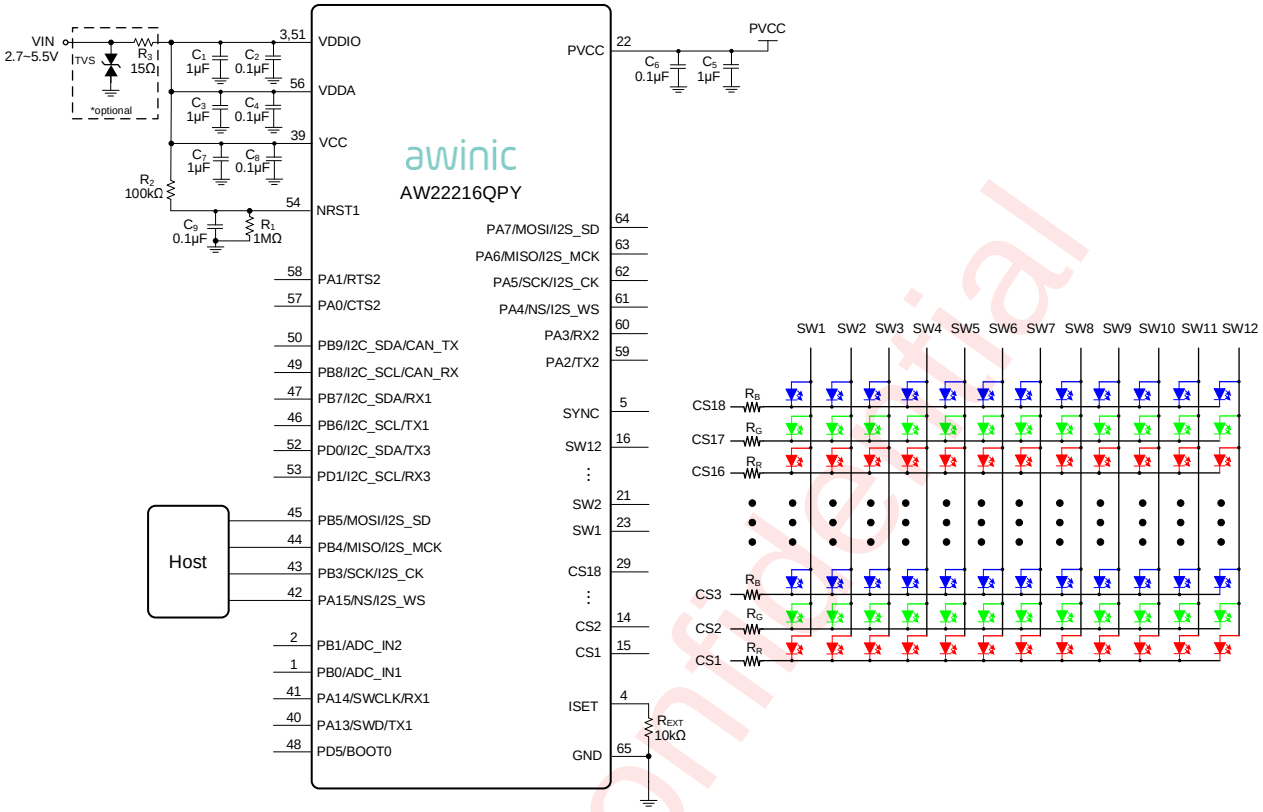
MULTIPLE DEVICE SYNCHRONIZATION

AW22216 supports multiple device synchronization to drive more than 216 LEDs by cascade of multiple devices. In this application, all devices share a common clock, one device works as a master to output common clock on pin SYNC, and other devices work as slave to use external input clock from pin SYNC. Bit CLKOE and CLKSEL in Register SSCR (page0, address=0x28) select the clock input or output on pin SYNC.

CLKOE	CLKSEL	Device Clock Selection
0	0	Use Internal clock and pin SYNC is high-Z
1	0	Master, use internal clock and output it on pin SYNC
0	1	Slave, use external clock from pin SYNC
1	1	Forbidden

Application Information

If the equipment has antenna, the IC should be far away from the antenna in order to avoid the EMI.



REXT

The selection of R_{EXT} determined the maximum LED0~LED215 current I_{max} as described in below formula (1).

$$I_{max} = \frac{K}{R_{EXT}} \quad (1)$$

When R_{EXT} = 10KΩ, I_{max} = 40mA, I_{switch} = 720mA, SDCR[2:0] = 000 (page0, address = 0x4D)

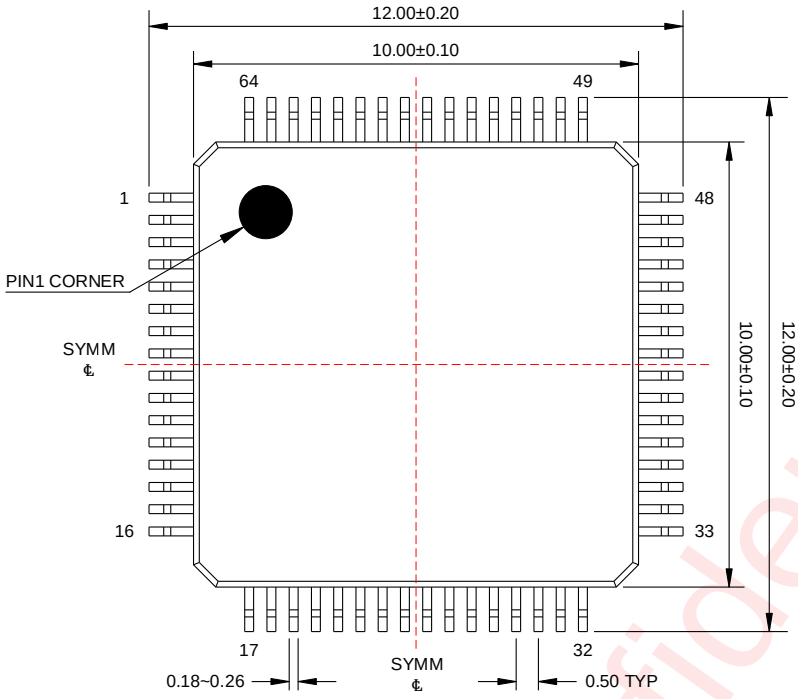
When R_{EXT} = 5KΩ, I_{max} = 80mA, I_{switch} = 1.44A, SDCR[2:0] = 111 (page0, address = 0x4D).

PCB Layout Consideration

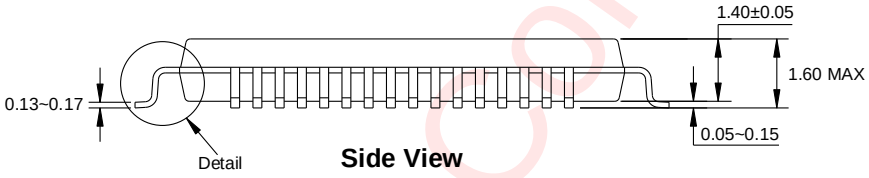
AW22216 is a matrix LED driver with 32-bit MCU, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C_{1-8} should be close to VDDIO, VDD, VCC and PVCC pins respectively. Avoid to connect device and chip pins with two different layers of copper, use the same layer of copper instead.
2. All the LEDs are powered by PVCC, please route according to the LED current setting be R_{EXT}. The maximum current with 5kΩ R_{EXT} is 1.44A, and the advised width is 60mil. Similarly, the route of SWx also needs enough width to support LED current.
3. R_{EXT} should be placed as close to the ISET pin to ensure LED current accuracy.
4. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal via as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

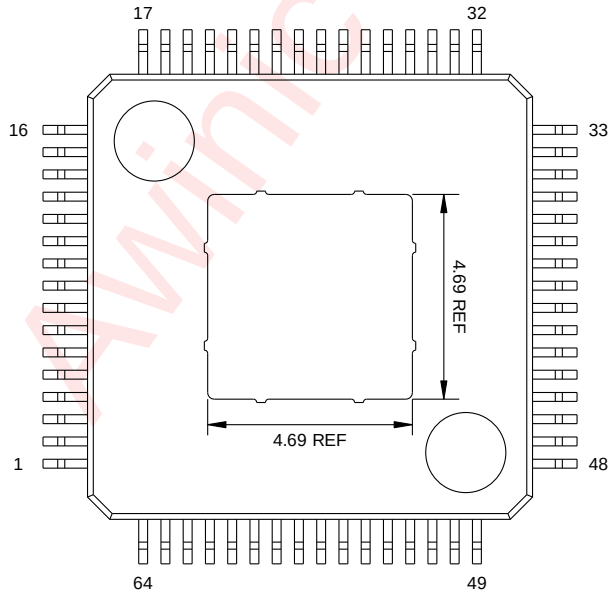
Package Description



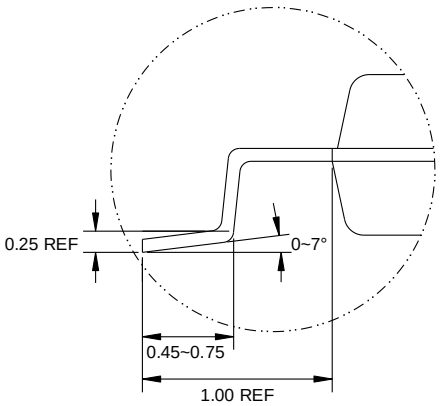
Top View



Side View



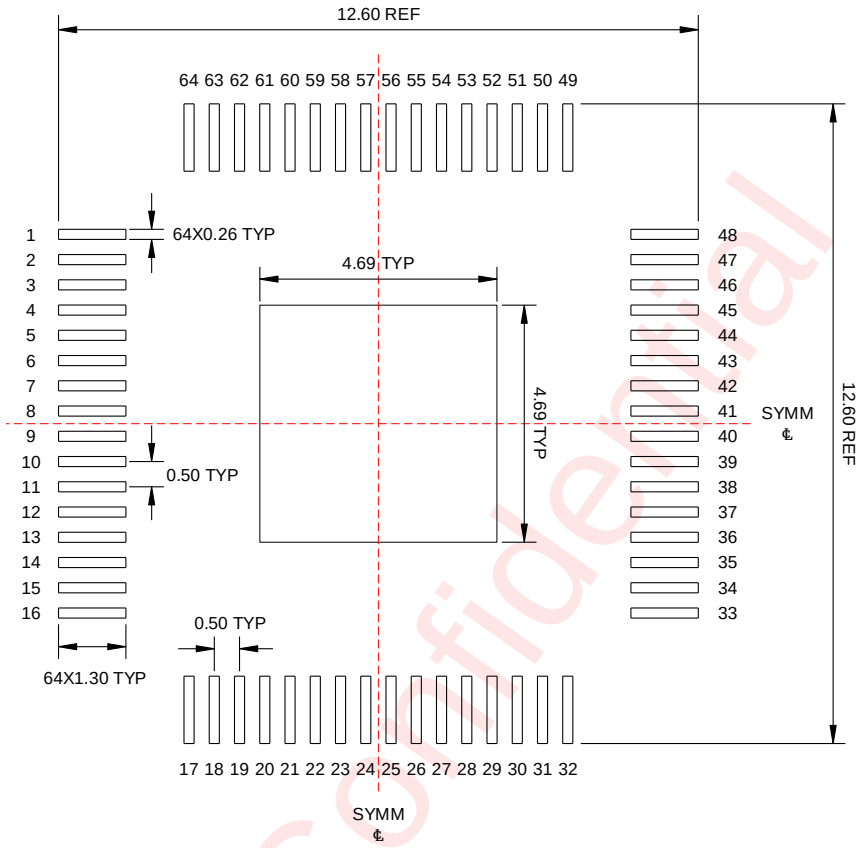
Bottom View

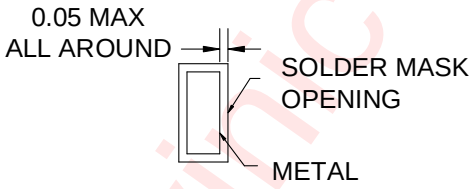


Detail

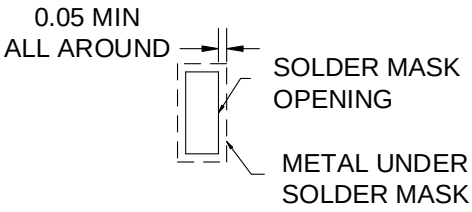
Unit:mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	Feb. 2025	Officially released
V1.1	Mar. 2025	Update Package Description and Land Pattern Data (P49-50)
V1.2	Jun. 2025	Update Typical Application Circuit (P2, P6, P47)

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