

0.1-5.925GHz DPDT Antenna Cross Switch

Features

- Qualified to AEC-Q100 Grade 2
- Broadband frequency range: 0.1 to 5.925GHz
- Wide VDD range: 1.65V to 3.3V
- GPIO interface for 1.0V to VDD positive control voltage
- Low insertion loss: 0.35dB typical @ 2.7GHz
- Max input RF power of 38.5dBm
- Excellent linearity and harmonic performance
- No DC blocking capacitors in typical application
- Small QFN 1.5X1.1-10L package

Applications

- Automotive application
- Cellular 2G/3G/4G/5G TRX
- Antenna switching
- Other RF front-end modules

Typical Application Circuit

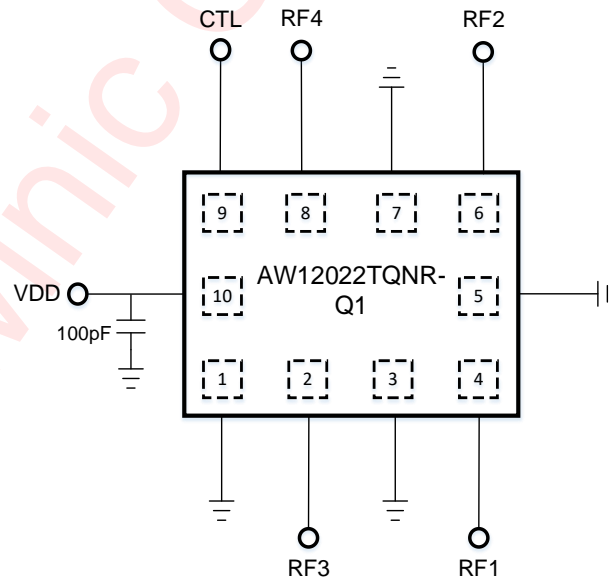


Figure 1 Typical Application Circuit of AW12022TQNR-Q1

General Description

The AW12022TQNR-Q1 is a Silicon-On-Insulator(SOI) DPDT switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 4G/5G, data cards and tablets.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pin as referenced in the chip block diagram and the control logic. The chip allows power-supply voltages from 1.65V to 3.3V and the positive control voltages from 1.0V to VDD.

The AW12022TQNR-Q1 is provided in a compact QFN 1.5X1.1-10L package.

Pin Configuration And Top Mark

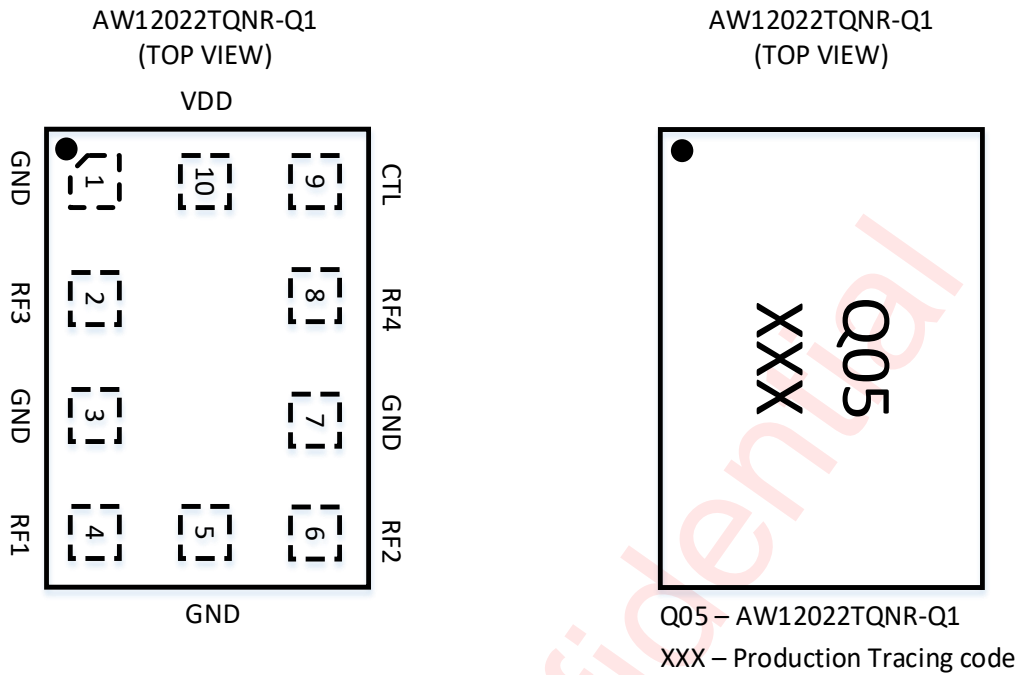


Figure 2 Pin Configuration And Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground
2	RF3	RF I/O path 3
3	GND	Ground
4	RF1	RF I/O path 1
5	GND	Ground
6	RF2	RF I/O path 2
7	GND	Ground
8	RF4	RF I/O path 4
9	CTL	DC control voltage
10	VDD	DC power supply

Functional Block Diagram

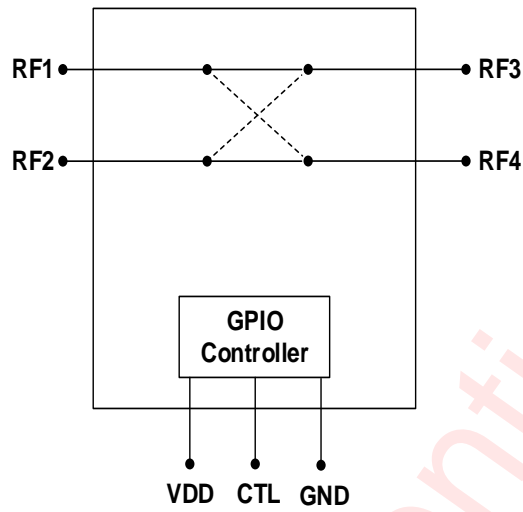


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW12022TQNR-Q1	-40°C~105°C	QFN 1.5X1.1-10L	Q05	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		-0.3V to 3.6V
Control Voltage Range	VCTL	-0.3V to 3.3V
RF input power	900MHz, 25% Duty Cycle, VSWR=1:1, 25°C	38.5dBm
	900MHz, 25% Duty Cycle, VSWR=1:1, 105°C	38dBm
	1900MHz, 25% Duty Cycle, VSWR=1:1, 25°C	39dBm
	1900MHz, 25% Duty Cycle, VSWR=1:1, 105°C	38.5dBm
Operating Free-air Temperature Range		-40°C to 105°C
Storage Temperature T _{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
HBM ^{NOTE2}		±1000V
CDM ^{NOTE3}		±1000V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Reference AEC-Q100-002-RevE.

NOTE3: Reference AEC-Q100-011-RevD.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	VDD	1.65	1.8	3.3	V
Control Voltage High	VCTL_H	1	1.8	VDD	V
Control Voltage Low	VCTL_L	0		0.3	V
Operating Temperature	Top	-40	25	105	°C

Electrical Characteristics

VDD=1.8/2.8V, CTL=0/1.8V, PIN=0dBm, T_A =+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
IDD	Supply Current	VDD=2.8V		55	80	μA
ICTL	Control Current	VCTL_H=3.3V		4.5	8	μA
Tsw	Switching Time	50% CTRL to 90% or 10% RF		1.5	3	μs
IL	Insertion Loss	100-960MHz		0.25	0.4	dB
		960-2200MHz		0.3	0.45	dB
		2200-2690MHz		0.35	0.5	dB
		3300-4200MHz		0.42	0.6	dB
		4400-5000MHz		0.46	0.7	dB
		5150-5925MHz		0.57	0.8	dB
ISO	Isolation	100-960MHz	29	33		dB
		960-2200MHz	22	26		dB
		2200-2690MHz	20	24		dB
		3300-4200MHz	17	21		dB
		4400-5000MHz	15	19		dB
		5150-5925MHz	14	18		dB
RL ^[1]	Return Loss	100-960MHz	25	33		dB
		960-2200MHz	21	29		dB
		2200-2690MHz	20	27		dB
		3300-4200MHz	18	26		dB
		4400-5000MHz	18	25		dB
		5150-5925MHz	16	23		dB
H2 ^[1]	Second Harmonics	PIN=35dBm, 850/900MHz, 25% Duty Cycle, VSWR=1:1		-58	-50	dBm
H2 ^[1]	Second Harmonics	PIN=33dBm, 1800/1900MHz, 25% Duty Cycle, VSWR=1:1		-64	-55	dBm
H3 ^[1]	Third Harmonics	PIN=35dBm, 850/900MHz, 25% Duty Cycle, VSWR=1:1		-54	-45	dBm
H3 ^[1]	Third Harmonics	PIN=33dBm, 1800/1900MHz, 25% Duty Cycle, VSWR=1:1		-63	-55	dBm

[1] Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Timing Diagram (Power ON And OFF Sequence)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal CTL should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

- 1) Apply voltage supply --- VDD
- 2) Set Controls---CTL
- 3) Apply RF input

Change switch position from one RF port to another:

- 1) Remove RF input
- 2) Change control voltages CTL to set the switch to desired RF port
- 3) Apply RF input

Power OFF:

- 1) Remove RF input
- 2) Remove control voltages-CTL
- 3) Remove VDD input

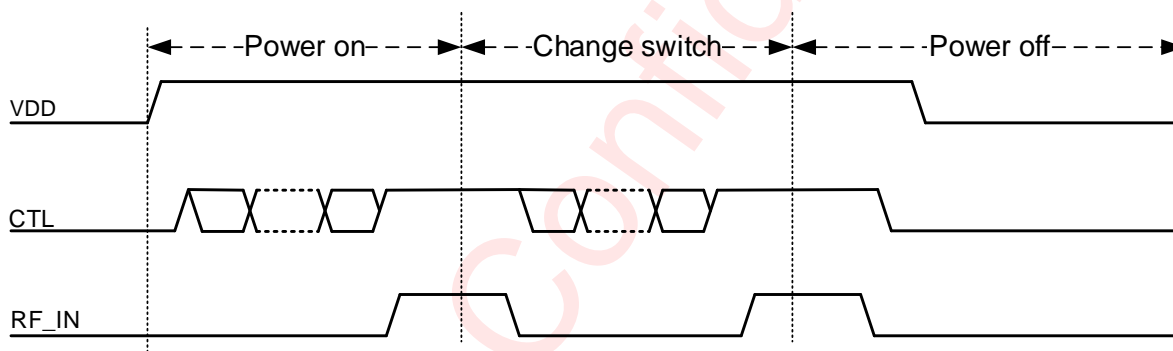
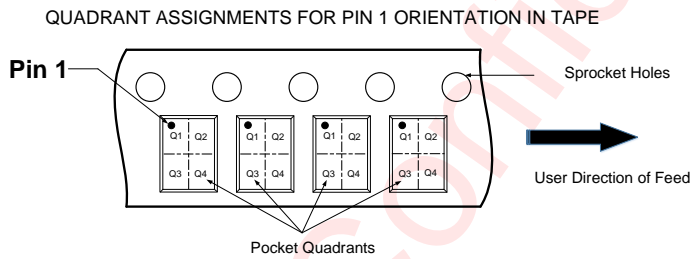
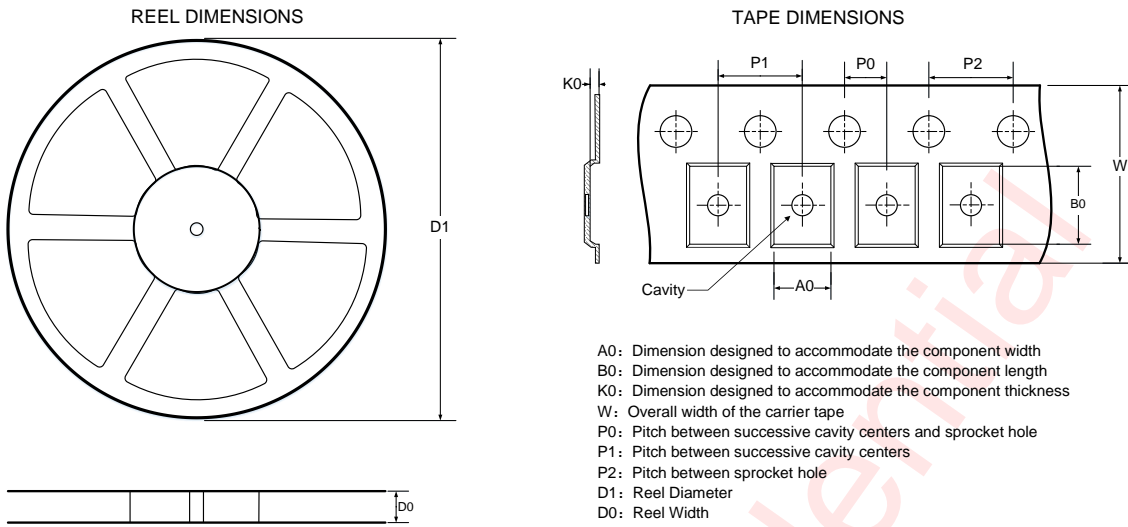


Figure 4 Power On/Change Switch/Power Off Sequence

AW12022TQNR Control Logic

State	Active Path	CTL
1	RF1 to RF4; RF2 to RF3	1
0	RF2 to RF4; RF1 to RF3	0

Tape And Reel Information



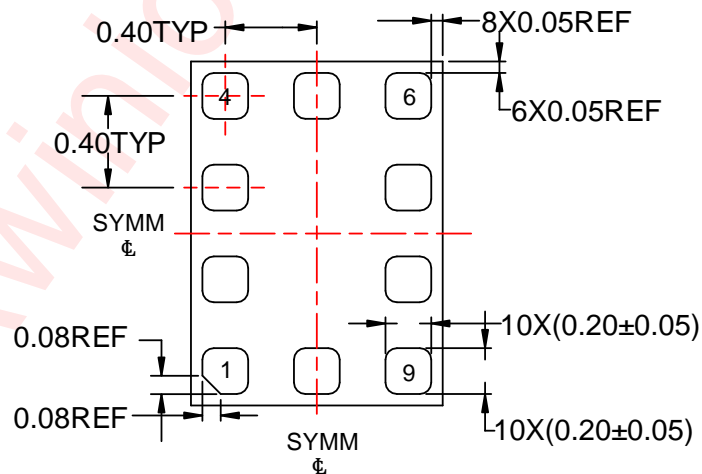
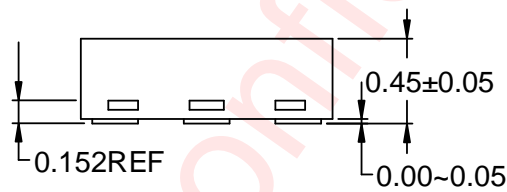
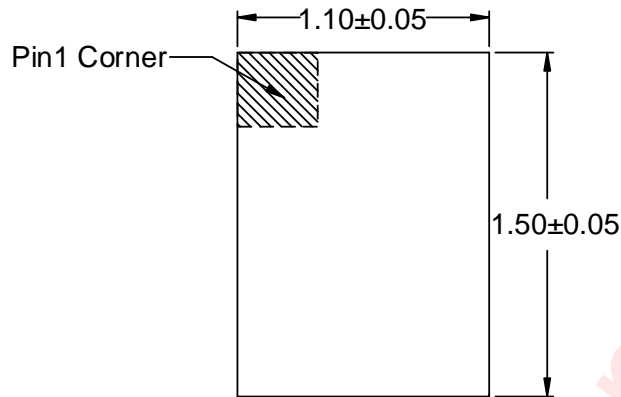
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.3	1.7	0.6	2	4	4	8	Q1

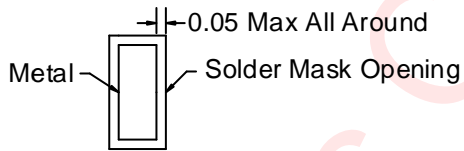
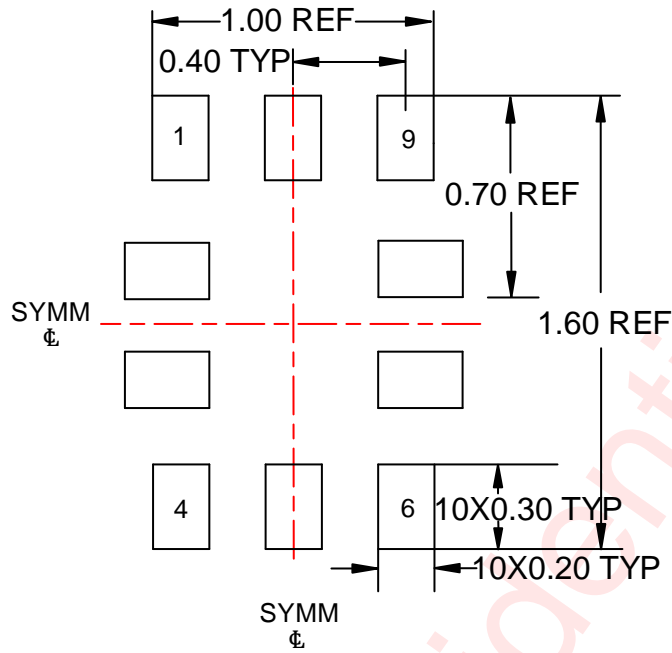
All dimensions are nominal

Package Outline Dimensions

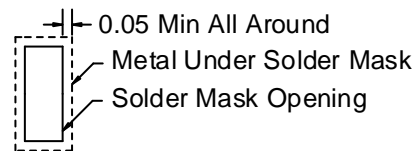


Unit:mm

Land Pattern Data



Non-solder Mask Defined



Solder Mask Defined

Unit:mm

Revision History

Version	Date	Change Record
V1.0	Sept 2025	Officially Released

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