20-V 200-mA Ultra-Low Noise Ultra-High PSRR Low Dropout Linear Regulator

1 Features

- Ultra-low RMS noise: 1uV RMS
- Ultra-low noise density: 3 nV/√Hz @10 kHz
- Ultra-low noise density: 78dB @1MHz
- Output current: 200mA
- Wide input voltage range: 2.7V to 20V
- Single Capacitor Pin Improves Noise and PSRR
- Programmable current limit
- Single-resistor pin configuration for output voltage
- Low voltage: 350mV@200mA
- Output voltage range: 0.5V to 16V
- Quick startup capability
- High-precision enable/under-voltage lockout
- Internal return current protection
- Minimum output capacitance: 4.7uF (ceramic)
- 3mm x 3mm DFN package

2 Typical Applications

- RF power supply: PLL, VCO, mixer, low-noise amplifier
- Ultra-low noise instruments, medical imaging, diagnostics
- Infrared sensor
- High-speed/high-precision data converter
- Used as a rear-stage regulator for switching power supplies

3 Description

The LKP4153 is a linear power regulator featuring ultra-low noise and exceptional PSRR performance. Utilizing a high-performance current as a reference benchmark, it drives the power transistor through a high-performance voltage buffer. Additionally, parallel configuration can further reduce noise, enhance output current capacity, and optimize board-level thermal management.

The device supplies 200mA at a typical 350mV dropout voltage, Operating quiescent current is nominally 1.9mA and drops to <<1μA in shutdown. The LKP4153's wide output voltage range (0V to 16V) while maintaining unitygain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation

The LKP4153 is stable with a minimum 4.7μF ceramic output capacitor. Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis. , enabling normal operation within a temperature range of-55°C to +125°C.

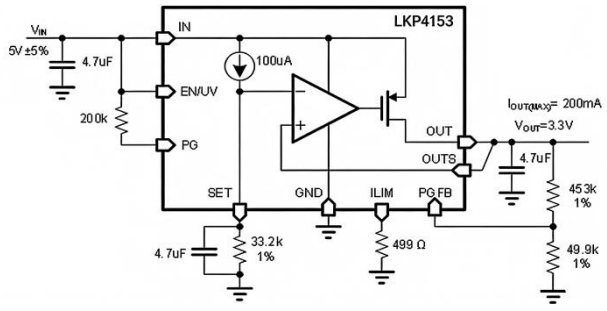


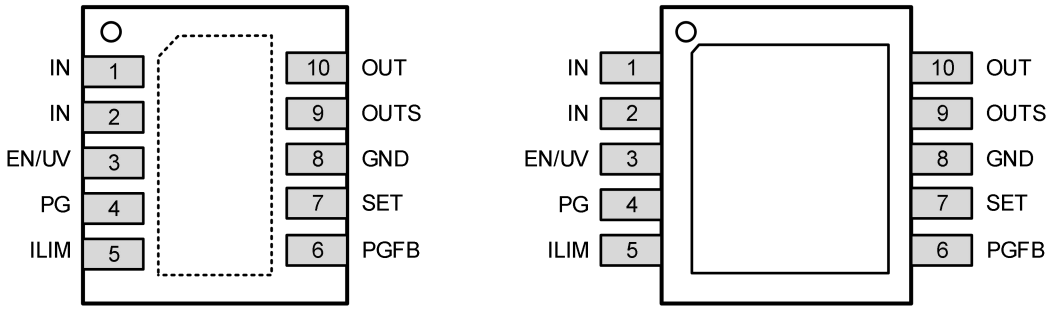
Figure 1. Typical applications

Head Record

4 Pin and Function Description

Table 1. Version History

date	edition	description
09/16/2023	Version Rev. Pre-0.1	Initial version
01/15/2024	Version Rev. Pre-0.2	Several test data and charts need updating
04/13/2026	Version Rev.1.0	Several test data and charts need updating



DFN-10 package (top view) MSOP-10 package (top view)

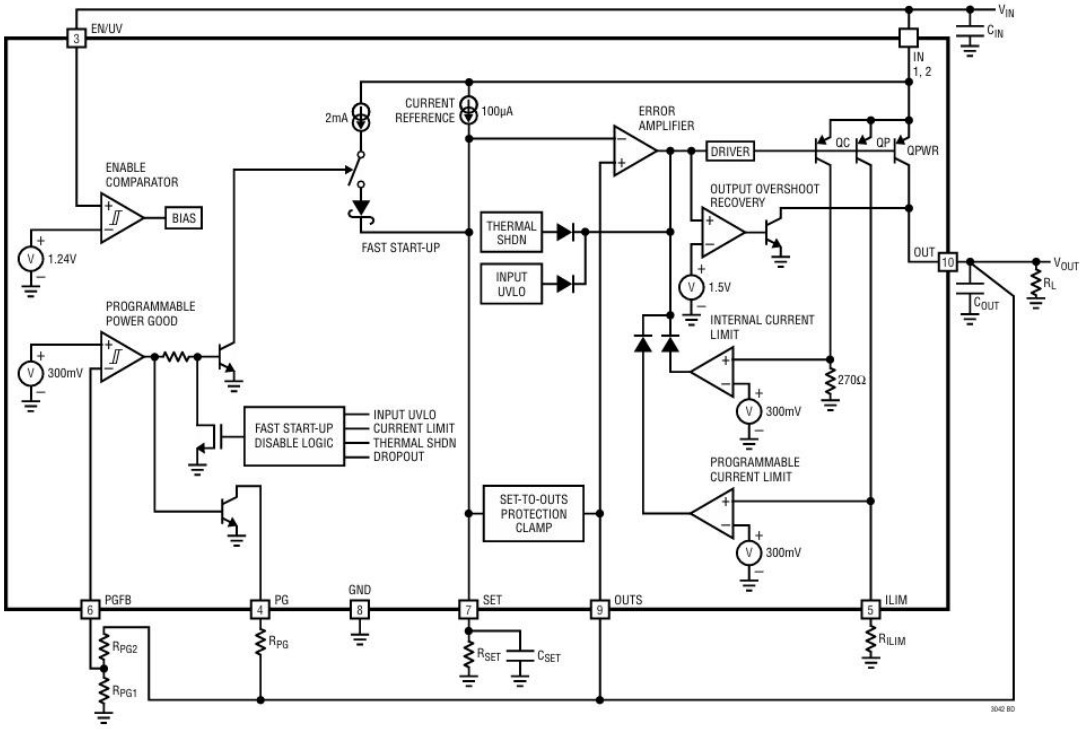
Figure 2. Pin Configuration

Table 2. Pin function description

Pin numbering	Pin name	IO type	description
1,2	IN	PWR	Input pin. These pins supply power to the regulator. requires a bypass capacitor at the IN pin. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 4.7μF input bypass capacitor gener ally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop.
3	EN/UV	IP	EN/UVLO pins. Pulling the pins to a low level puts the device into shutdown mode,Quiescent current in shutdown drops to less than 1μA and the output voltage turns off. Connecting the pins to a high level (above 1.2V) activates the device. If unused, tie EN/UV to IN. Do not float the EN/UV pin.
4	PG	OP	Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low if PGFB is below 300mV. If the power good functionality is not needed, float the PG pin
5	ILIM	IP	Current limit programming pin. A resistor connected between ILIM and GND can configure current limits. For optimal accuracy, it is recommended to use Kelvin connections to directly link the resistor to the GND pin. The ILIM pin's programmable current limiting ratio maintains a 1:400 output

			current ratio. Additionally, the ILIM pin serves as a current monitoring pin with a 0V to 300mV range. If unused, the ILIM pin may be connected to GND.
6	PGFB	IP	Power good feedback pin. The PG pin pulls high if PGFB increases beyond 300mV on its rising edge, with 10mV hysteresis on its falling edge. connecting an external resistor divider between the OUT pin, PGFB pin, and GND pin, the programmable power threshold can be set using the following formula: 0.3V*（1+R_{PGFB2}/R_{PGFB1}）. The PGFB pin also activates the fast-start circuit, If unused this function, connect the PGFB pin to the IN pin.
7	SET	IP	Voltage setting pin. The SET pin serves as the reference input voltage reference point for the error amplifier. It delivers a precise 100μA current that flows through an external resistor between the SET pin and GND. The device's output voltage is determined by VSET = ISET × RSET, with a range of 0.5V to 16V. Inserting a capacitor between the SET pin and GND improves noise rejection, PSRR (Post-Signal Response Ratio), and transient response, though it may increase startup response time.
8,11	GND	G	Ground pin. The exposed backside should be soldered to the PCB ground and directly connected to the GND pin.
9	OUTS	IP	Output Sense. This pin is the non-inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. Moreover, place the input and output capacitors (and their GND connections) very close together.
10	OUT	OP	Output pin. This pin supplies power to the load. For stability, use a minimum 4.7μF output capacitor with an ESR below 50mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients.

5 Functional block diagram



6 Absolute Maximum Rated Value

Power Supply, Reference Voltage, and Device Temperature Characteristics

TA =25℃

Table 3

parameter	MIN	TYP	MAX
IN, EN/UV, PG, PGFB to GND voltage	-0.3	+22	V
ILIM to GND voltage	-0.3	+1	V
SET to GND voltage	-0.3	+16	V
Out-to-GND voltage	-0.3	+16	V
OUTS to GND voltage	-0.3	+16	V
SET pin current	-10	+10	mA
Storage Temperature Range (TSTG)	-65	150	℃
Device junction temperature (TJ)		150	℃
Lead-tin soldering temperature (TL, reflow soldering for 10 seconds)		260	℃

Note: Exceeding the specified absolute maximum rated values may cause permanent device damage, and prolonged operation under these conditions will compromise device reliability.

ESD characteristic

Table 4

project	description	standard	max value
HBM	Simulate pin input only	JEDEC JS-001	±2000 V
HBM	Unlike analog input pins	JEDEC JS-001	±2000 V
CDM	All pins	JEDEC JS-002	±750 V

encapsulated thermal resistance

Table 5

Encapsulation type	θJA	θJC	unit
DFN-10	34	5.5	°C/W
MSOP-10	33	8	°C/W

Note: θJA is calculated for the worst-case scenario where the chip is soldered onto the circuit board to achieve surface-mount packaging.

7 Electrical character

Test conditions: VIN=MAX (VOUT+1V,2.7V), IOUT=10mA, CIN=COUT=4.7μF

Unless otherwise specified, TA = 25°C

Table 6. Electrical characteristics

parameter	Test conditions	MIN	TYP	MAX	UNIT
Minimum input voltage	ILOAD=200mA, VIN UVLO rise time		2.7		V
	VIN UVLO hysteresis		100		mV
SET pin current (ISET)	VIN=4V，ILOAD=1mA,VOUT=3V		100		uA
	2.7V < VIN < 20V,1.5V < VOUT < 15V, 1mA < ILOAD<200mA		100		uA
Fast start SET pin current	VPGFB=289mV, VIN=4V, VSET=3V		2		mA
Output offset voltage (VOS)	VIN=4V, ILOAD=1mA, VOUT=3V	-2.5		3.5	mV
Vout - Vset	2.7V < VIN < 20V,1.5V < VOUT < 15V, 1mA < ILOAD<200mA	-3.5		5.0	mV
Voltage regulation: ΔISET	VIN: 2.7V to 20V, ILOAD: 1mA, VOUT: 1.8V		0.7		nA/V
Voltage regulation: ΔVOS	VIN: 2.7V to 20V, ILOAD: 1mA, VOUT: 1.8V		6		uV/V
Load regulation: ΔISET	VIN=4V, ILOAD=1mA to 200mA, VOUT=3V		35		nA
Load regulation: ΔVOS	VIN=4V, ILOAD=1mA to 200mA, VOUT=3V		0.3		mV
Change in ISET with VSET	VSET ranges from 1.5V to 15V, VIN is 16V, and ILOAD is 1mA		100		nA
Change in VOS with VSET	VSET ranges from 1.5V to 15V, VIN is 16V, and ILOAD is 1mA		0.8		mV
Dropout voltage	ILOAD=1mA		300		mV
	ILOAD=10mA		300		mV
	ILOAD=50mA		330		mV
	ILOAD=200mA		350		mV
GND pin current（VIN=VOUT）	ILOAD=10uA		2.3		mA
	ILOAD=10mA		2.7	4	mA
	ILOAD=50mA		3.7	6	mA

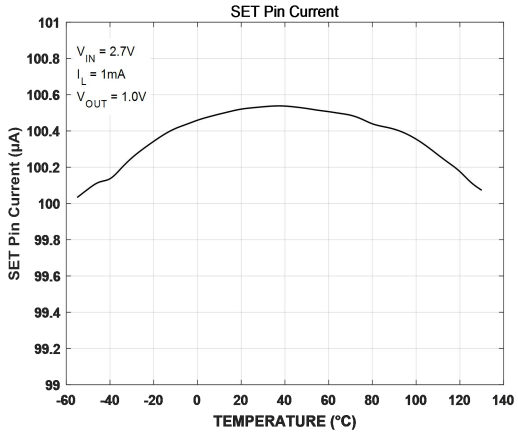
	ILOAD=200mA		7.9	18	mA
output noise spectral density (ILOAD=10mA, VOUT=3V COUT=CSET=4.7uF)	Frequency=100Hz		24		nV/√Hz
	Frequency=10kHz		3		nV/√Hz
	Frequency=100kHz		3		nV/√Hz
Output RMS noise (BW = 10 Hz to 100 kHz)	ILOAD=10mA, COUT=4.7uF, CSET=4.7uF		1.0		uVRMS
	ILOAD=200mA, COUT=4.7uF, CSET=4.7uF		1.0		uVRMS
Power Supply Voltage Ripple Rejection (1.5V≤VOUT≤15V VRipple=200mVPP, ILOAD=200mA CIN=4.7nF,COUT=CSET=4.7uF)	fRipple=100Hz,		114		dB
	fRipple=10kHz		112		dB
	fRipple=100kHz		100		dB
	fRipple=1MHz		78		dB
	fRipple=10MHz		50		dB
EN/UV pin threshold	EN/UV transition point rise (on)		1.2		V
EN/UV pin hysteresis	EN/UV transition point hysteresis		9		mV
EN/UV pin current	VEN/UV=0V, VIN=20V		2.3		mA
	VEN/UV=1.24V, VIN=20V		1.3		mA
	VEN/UV=20V, VIN=0V		2.6		mA
Quiescent Current in Shutdown (VEN/UV = 0V)	EN/UV=0V, VIN=4V		0.8	1	uA
Internal current limit	VIN=2V, VOUT=0V		700		mA
	VIN=12V, VOUT=0V		250		mA
	VIN=20V, VOUT=0V		160		mA
Programmable current limit (2V < VIN < 20V)	VIN=2V, VOUT=0V, RILIM=625Ω		200		mA
	VIN=2V, VOUT=0V, RILIM=2.55kΩ		50		mA
PGFB pin threshold	PGFB jump point rising		300	330	mV
PGFB pin hysteresis	PGFB transition point hysteresis		2		mV
PG outputs low voltage	IPG=100uA		20	60	mV
PG leakage current	VPG=20V			1	uA
thermal shutdown	TJ increase		150		℃
	slow-moving		12		℃
Start-up time (VOUT=7V, VIN=9V, ILOAD=200mA)	CSET=4.7uF, VPGFB=9V, RSET=169kΩ		600		ms
	CSET=4.7uF, RPGFB1=22kΩ, RPGFB2=1kΩ, RSET=169kΩ		12		ms

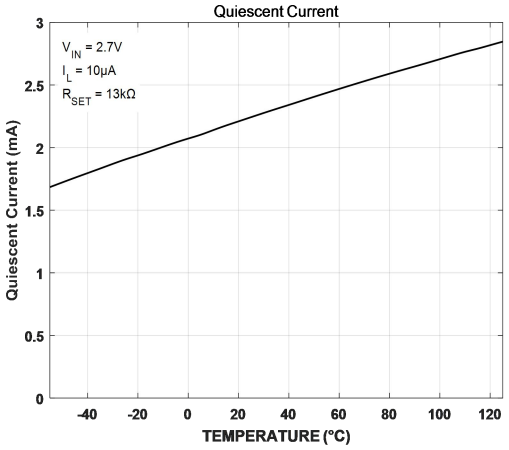
explanatory notes ：

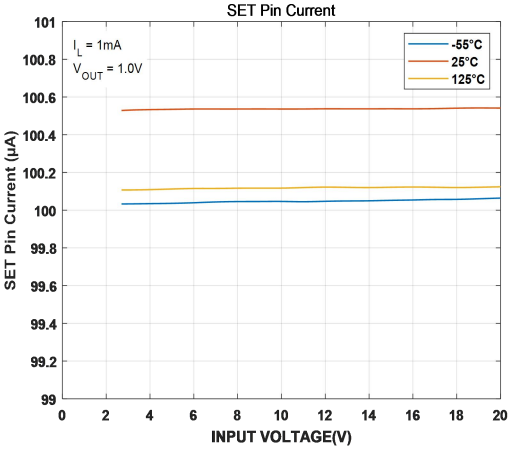
1） All chips undergo testing during the release period to ensure compliance with standard requirements.

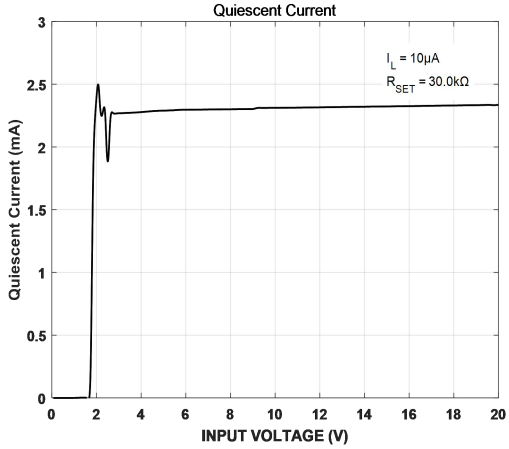
8 Typical performance characteristics

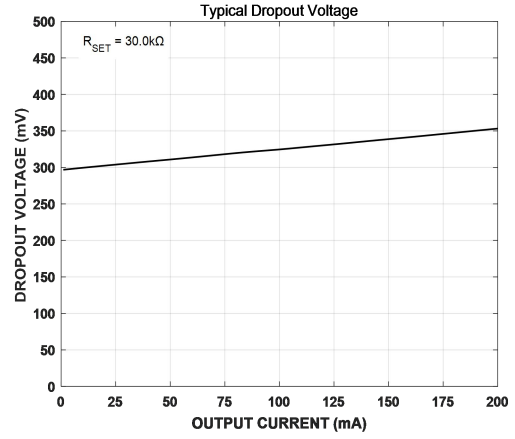
Test conditions (unless otherwise specified): CIN=COUT=CSET=4.7μF, TA=25°C.

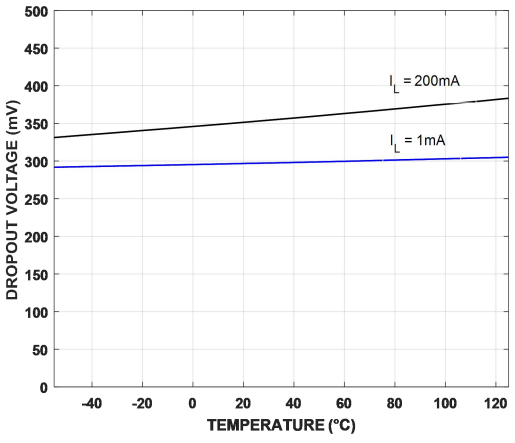


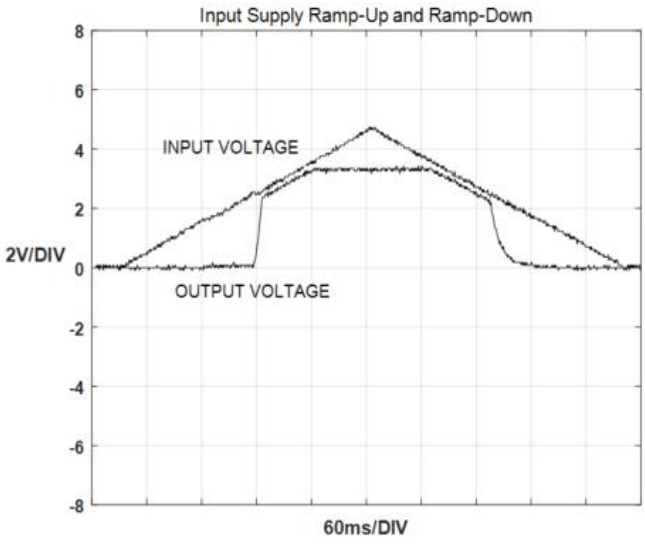


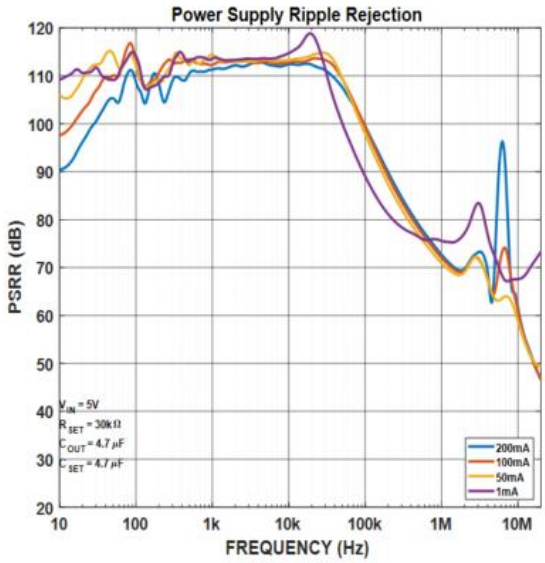


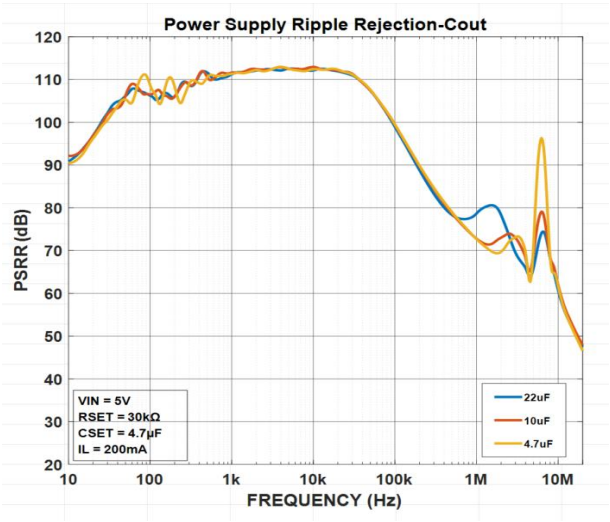


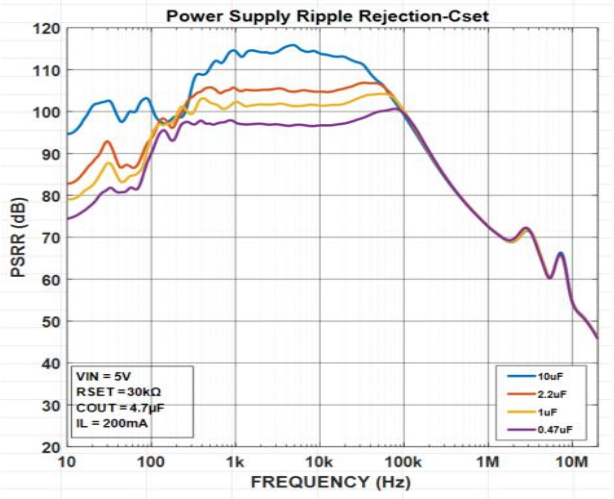


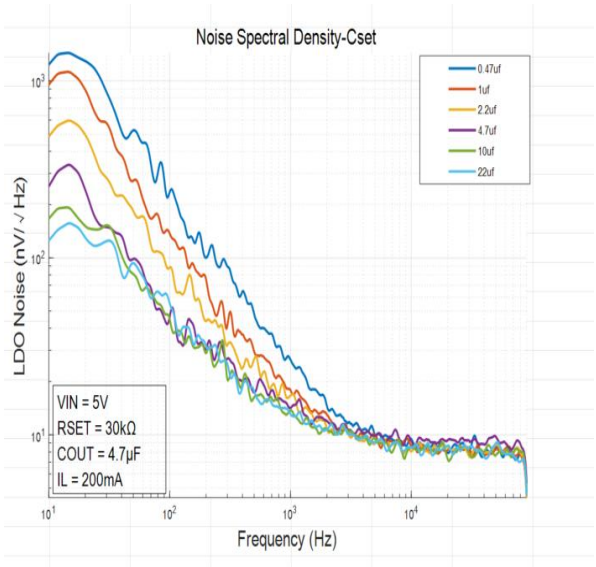


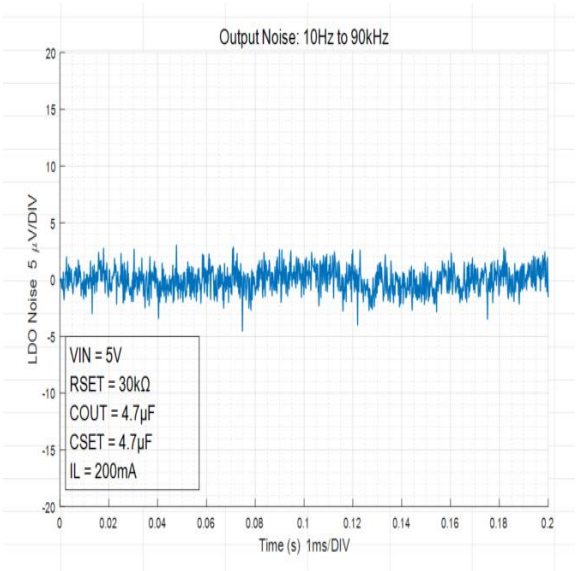

Input Supply Ramp-Up and Ramp-Down
INPUT VOLTAGE
OUTPUT VOLTAGE
2V/DIV
60ms/DIV


Power Supply Ripple Rejection
PSRR (dB)
FREQUENCY (Hz)
200mA
100mA
50mA
1mA


Power Supply Ripple Rejection-Cout
PSRR (dB)
FREQUENCY (Hz)
VIN = 5V
RSET = 30kΩ
CSET = 4.7μF
IL = 200mA
22uF
10uF
4.7uF


Power Supply Ripple Rejection-Cset
PSRR (dB)
FREQUENCY (Hz)
VIN = 5V
RSET = 30kΩ
COUT = 4.7μF
IL = 200mA
10uF
2.2uF
1uF
0.47uF


Noise Spectral Density-Cset
LDO Noise (nV/√Hz)
Frequency (Hz)
VIN = 5V
RSET = 30kΩ
COUT = 4.7μF
IL = 200mA
0.47uf
1uf
2.2uf
4.7uf
10uf
22uf


Output Noise: 10Hz to 90kHz
LDO Noise 5 μV/DIV
Time (s) 1ms/DIV
VIN = 5V
RSET = 30kΩ
COUT = 4.7μF
CSET = 4.7μF
IL = 200mA

9 Application information

The LKP4153 is a high performance low dropout linear regulator featuring ultralow noise (3nV/√Hz at 10kHz) and ultrahigh PSRR (78dB at 1MHz) architecture for powering noise sensitive applications. Designed as a precision current source followed by a high performance rail-to-rail voltage buffer, the LKP4153 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability and programmable power good. The LKP4153 is easy to use and incorporates all of the protection features expected in high performance regulators. Included are short-circuit protection, safe operating area protection, reverse battery protection, reverse current protection, and thermal shutdown with hysteresis.

9.1 Output Voltage

The LKP4153 generates a high-precision 100μA current source through its SET pin, which is externally connected to a high-precision resistor grounded to form a reference power supply. Simultaneously, the SET pin internally connects to the inverting input terminal of an error amplifier. This unit-gain error amplifier produces a low-impedance mirror image at its inverting input (i.e., the OUTS pin, externally connected to the OUT pin) through its in-phase input terminal.

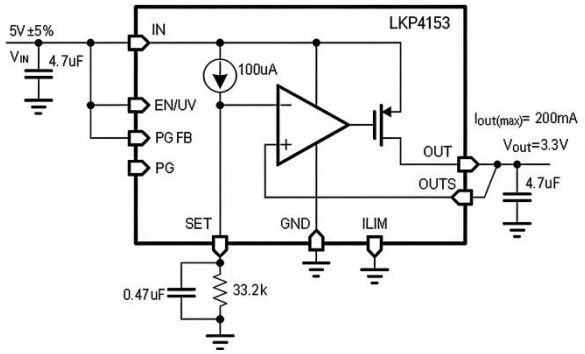


Figure 3. Typical adjustable voltage regulator

VOUT (V)	RSET(kΩ)
2.5	24.9
3.3	33.2
5.0	49.9
7.0	69.8
12.0	121

Table 7. Resistor values corresponding to common output voltages

The rail-to-rail error amplifier and current reference of the LKP4153 provide an output voltage range from 0.5V (using a

5kΩ resistor) to VIN voltage differential (up to 16V). Refer to the electrical characteristic table for parameters including input offset voltage, SET pin current, output noise, and PSRR variation of the error amplifier. The table lists common output voltages along with corresponding RSET resistors.

Compared to traditional voltage regulators that use voltage references, current references offer the advantage of operating the regulator in a potential-gain configuration. This allows devices to maintain loop gain, frequency response, and bandwidth unaffected by output voltage variations. Consequently, noise levels, PSRR (Power Supply Regulator Response), and transient performance remain stable regardless of output voltage fluctuations. Additionally, since SET pin voltage amplification to higher output levels requires no error amplifier gain, output voltage regulation can be precisely controlled within a narrow range of several hundred microvolts rather than being limited to fixed percentage values.

Due to the high accuracy of the zero-temperature drift current source integrated in the chip, an improperly selected resistor on the SET pin may compromise precision. Therefore, it is recommended to use high-precision resistors with premium insulating materials. Additionally, all insulating surfaces must be thoroughly cleaned to remove solder flux and other residues. In high-humidity environments, a moisture barrier layer should be applied to the SET pin.

Minimize board leakage by encircling the SET pin with a guard ring operated at a potential close to itself — ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. Leakages of 100nA into or out of he SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over wide operating temperature range. Figure 4 illustrates a typical guard ring layout technique.

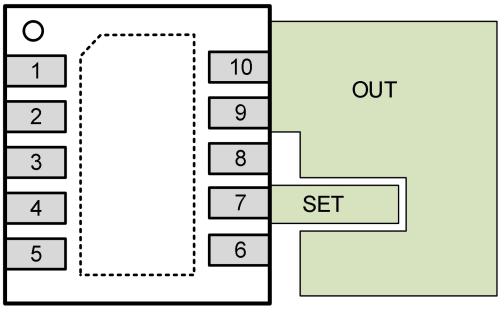


Figure 4. Protection ring layout

Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. By passing the SET pin with a small capacitance to ground resolves this issue — 10nF is sufficient. For applications requiring higher accuracy or an adjust able output voltage, the SET pin may be actively driven by an external voltage source capable of sinking 100μA. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

9.2 Output detection and Stability

The OUTS pin of LKP4153 provides a Kelvin detection connection to the output. The GND terminal of the SET pin resistor establishes a Kelvin connection to the load's GND terminal. Additionally, the OUTS pin should be directly connected to the output capacitor, and the GND terminal of the SET pin capacitor C_{SET} should be directly connected to the GND terminal of C_{SET}. This ensures that the GND terminals of both input and output capacitors are in close proximity, which is critical for device stability.

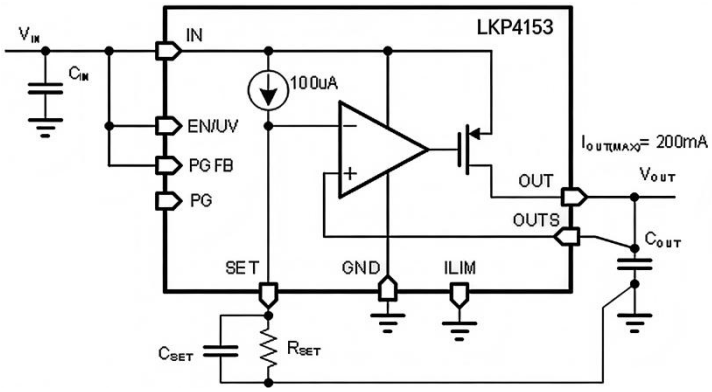


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Figure 5. C_{OUT} and C_{SET} connections enhance stability

9.3 Stability and Output capacitance

The LKP4153 requires an output capacitor to ensure stability. Given the device's high bandwidth, ceramic capacitors with ESR below 50mΩ and ESL below 2nH (minimum capacitance 4.7μF) are recommended. To minimize the impact of PCB inductance on dynamic performance, connect the OUTS pin directly to the output capacitor using Kelvin junction, and similarly link the GND terminal of the SET pin capacitor to the output capacitor's GND terminal. Additionally, position the GND connection of the input capacitor as close as possible to the GND connection of the output capacitor.

To achieve high PSRR and low noise levels, 4.7μF ceramic capacitors are typically employed. However, further increasing the output capacitor capacitance yields limited performance gains, primarily because the regulator's loop bandwidth decreases with higher capacitance values. Nevertheless, larger output capacitors can effectively reduce peak output deviations during load transient events. It should be noted that the regulator capacitor supplying power to the regulator also increases its output capacitance value.

The type of ceramic capacitors also requires careful consideration. These capacitors are manufactured using various dielectrics that exhibit different operational characteristics under varying temperatures and voltage conditions. The most commonly used dielectrics utilize EIA temperature characteristics, such as models Z5U, Y5V, X5R, and X7R. While Z5U and Y5V dielectrics are suitable for providing high capacitance in compact packages, they typically demonstrate significant voltage and temperature coefficients.

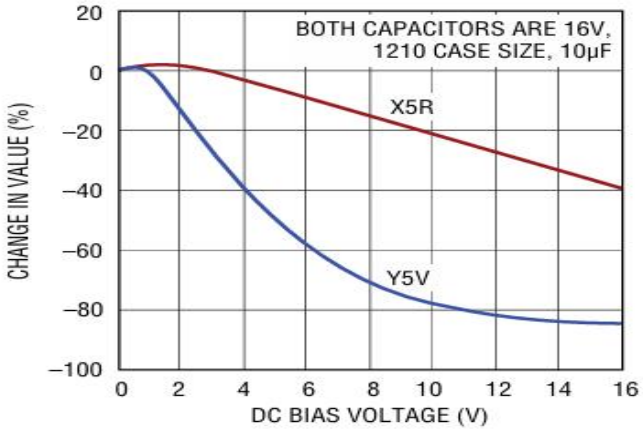


Figure 6. DC characteristics of ceramic capacitors

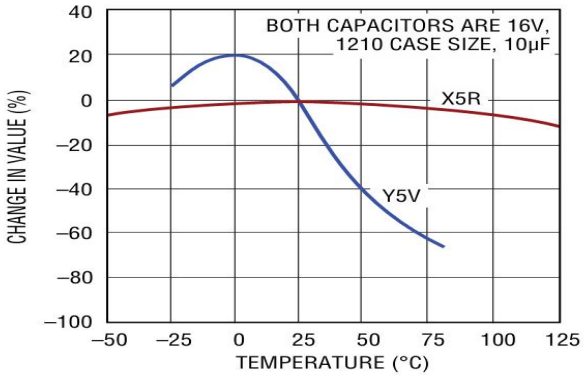


Figure 7. Temperature characteristics of ceramic capacitors

The capacitors for the X5R and X7R models exhibit more stable performance characteristics, making them more suitable for the LKP4153. While the dielectric material of the X7R capacitor demonstrates superior stability across a wide temperature range, the X5R offers better cost-performance ratio.

9.4 Stability and input capacitance

The LKP4153 can be stabilized using a capacitor with a minimum capacitance of 4.7uF, and ceramic capacitors with low ESR are recommended. When long wires connect the power supply to the regulator's input and ground terminals, combining low-value input capacitors with high load currents may cause instability. This occurs because the parasitic inductance of the wires and input capacitance form an LC resonant cavity.

When powered by a nearby battery for the LKP4153, a 4.7µF input capacitor suffices to ensure stability. For power supply from a remote battery, a larger input capacitor is required. A practical guideline suggests adding 1µF of extra capacitance for every 20cm increase in wire length beyond the minimum 4.7µF value. In practical applications, the minimum input capacitance needed may vary depending on output capacitance and load current requirements.

9.5 Filter high-frequency spikes

For applications where the LKP4153 is used to post-regulate a switching converter, its high PSRR effectively sup presses any “noise” present at the switcher’s switching frequency — typically 100kHz to 4MHz. However, the very high frequency (100s of MHz) “spikes” — beyond the LKP4153’s bandwidth — associated with the switcher’s power switch transition times will almost directly pass through the LKP4153. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (e.g. 0.5”) PCB trace between the switcher’s output and the LKP4153’s input can serve as an LC-filter to suppress these very high frequency spikes.

9.6 Output noise

The LKP4153 delivers significant advantages in noise performance. Traditional linear regulators contain multiple noise sources, including voltage reference noise, error amplifier noise, and noise from the resistor network used to set output voltage. Unlike most low-noise regulators that typically achieve noise reduction through bypass capacitor filtering at the voltage reference output pin, the LKP4153 employs a 100μA low-noise current reference with approximately 60pA/√Hz current noise (integral current noise ranging from 10Hz to 100kHz, 12nA RMS). The equivalent output voltage noise is calculated by multiplying the current noise by the resistor value (RSET), then summing this with error amplifier noise and the resistor's thermal noise (4KTR, where k is Boltzmann constant 1.38×10^{-23} J/K and T is absolute temperature).

Traditional linear regulators face a fundamental issue: the resistor divider network used to set output voltage introduces gain, which amplifies noise from the reference voltage. However, the LKP4153's unit gain follower architecture eliminates this problem. By incorporating a bypass capacitor on the SET pin resistor, the regulator's output noise becomes independent of the set output voltage value. The output noise then primarily depends on the error amplifier's noise characteristics, with approximately 4nV/√Hz in the 10kHz-1MHz frequency range and 1.5uVRMS in the 10Hz-100kHz bandwidth. When employing parallel devices, output noise can be further reduced to 1/√N (where N represents the number of parallel regulators).

9.7 SET Pin Capacitance: Noise, PSRR, Transient Response, and Soft Start

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass capacitor leakage deteriorates the LKP4153’s DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, LTC recommends the use of a good quality low leakage ceramic capacitor. Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Ramp-up rate from 0 to 90% of nominal VOUT is:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET}$$

9.8 Quick start

In ultra-low noise applications requiring 1/f noise rejection (e.g., frequencies below 100Hz), engineers typically employ a large SET pin bypass capacitor (e.g., 22μF). However, this approach significantly increases the regulator's startup time. To

address this, the LKP4153 incorporates an integrated fast-start circuit that boosts the SET pin current to 2mA during initialization.

As illustrated in the functional block diagram, the 2mA fast-start current source activates only when the PGFB voltage drops below 300mV. Additionally, the fast-start current source remains inactive if the voltage regulator is in current-limiting mode, voltage differential mode, thermal shutdown mode, or if the input voltage falls below the minimum power supply threshold.

If the fast start function is not used, connect the PGFB pin to either the IN or OUT pin. Note that this will also disable the power status indicator function.

9.9 Enable /UVLO

The EN/UV pins are used to configure the voltage regulator into a low-power shutdown state. The LKP4153 features a precise 1.2V turn-on threshold and 100mV hysteresis at the EN/UV pins. This threshold, combined with the input power divider resistor, determines the accurate undervoltage lockout (UVLO) threshold. When calculating the input resistor divider network, the EN/UV pin current (IEN) specified in the electrical characteristic table must be considered:

$$V_{IN(UVLO)} = 1.2V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN} \times R_{EN2}$$

If REN1 is less than 100kΩ, the EN/UV pin current (IEN) can be ignored. When this function is not required, the EN/UV pin can be connected to the IN pin.

9.10 Programmable Power Good

As shown in the functional block diagram, the power supply threshold can be configured by the user using two external resistors (RPG2 and RPG1).

$$V_{OUT(PG\_THRESHOLD)} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) - I_{PGFB} \times R_{PG2}$$

If the PGFB pin voltage exceeds 300mV, the drain open-circuit PG pin becomes invalid and enters a high-impedance state. The power good comparator features a 2mV hysteresis and 5μs de-boost time. When determining the resistor divider network, the PGFB pin current (I_{PGFB}) specified in the electrical characteristic table must be considered. If RPG1 is less than 30kΩ, the PGFB pin current (I_{PGFB}) can be disregarded. It should be noted that if the output voltage falls below 300mV or the regulator enters shutdown mode, both the power good indication function and fast start function will remain inactive.
If the power supply status indicator function is not used, the PG pin can be left floating.

9.11 External programmable current limit

The current limit threshold for the ILIM pin is set at 300mV. Connecting a resistor between the ILIM and GND pins allows you to determine the maximum current flowing through the ILIM pin, effectively setting the current limit for the LKP4153. The programming factor is 128mA·kΩ. For instance, a 1kΩ resistor sets the current limit at 128mA, while a 2kΩ resistor reduces it to 64mA. To ensure optimal accuracy, connect the ILIM pin resistor to GND using a Kelvin junction configuration.
As shown in the functional block diagram, the ILIM pin provides a current limiting value proportional to the output current

while also serving as a current monitoring pin with a range of 0V to 300mV. If this functionality is not required, the ILIM can be connected to GND.

9.12 Output overload recovery

During the transition from full load to no load (or light load) in a voltage regulator, output voltage overload may occur before the power transistor is turned off. If the output terminal is unloaded (or lightly loaded), it takes a considerable amount of time to complete the discharge of the output capacitor.

As shown in the functional block diagram, the LKP4153 incorporates an overdrive recovery circuit internally. This circuit can discharge charges from the output capacitor by activating the overdrive recovery function, typically generating a discharge current of approximately 4mA. When the potential at the OUTS pin is pulled up by external components beyond the SET pin level, the discharge current actively restores the OUTS pin potential to the programmed setting until the external components release the pin voltage.

9.13 Provide higher current in parallel

The LKP4153 can achieve higher current by paralleling multiple devices. Connect all SET pins together and all IN pins together, while using short PCB traces (functioning as ballast resistors) to connect the OUT pins, thereby balancing the current between voltage regulators.

Each voltage regulator in the parallel circuit exhibits minimal worst-case offset (5mV), thereby significantly reducing the required ballast resistor value. The two LKP4153 regulators each utilize a 50mΩ PCB printed wire as ballast resistor, delivering output current distribution superior to 20% under full load conditions. At maximum output current of 400mA, the two 50mΩ external resistors only increase the output regulation voltage drop by 10mV. For a 3.3V output voltage, this configuration demonstrates merely 0.3% improvement in voltage regulation accuracy.

Connecting two or more LKP4153 regulators in parallel enhances output current capacity while reducing noise levels. Additionally, parallel configuration improves heat dissipation on printed circuit boards (PCBs). For applications requiring high input-to-output voltage differentials, heat dissipation can be achieved through series resistors or parallel resistors connected to the LKP4153.

9.14 Thermal consideration

The LKP4153 supports internal power and thermal limits under overload conditions. The thermal shutdown temperature is rated at 155°C with a 10°C hysteresis. For continuous normal load operation, it is recommended to avoid exceeding the maximum junction temperature of 125°C. According to application specifications, this temperature must account for thermal transfer between the junction and package housing, between the package housing and heat sink interface, as well as between the heat sink circuit board and external environment. Additionally, all heat sources surrounding the voltage regulator must be considered.

The bottom surfaces of DFN and MSOP packages feature exposed metal from the lead frame to the chip mounting structure. Both packaging types facilitate direct heat transfer from chip nodes to PCB metal layers to limit maximum operating junction temperature. Additionally, the dual-row direct-insertion pin configuration enables metal extension beyond the package end faces.

For surface-mount packaging, heat dissipation is achieved through the thermal conductivity of the PCB and its copper printed wiring. Additionally, copper plate stiffeners and electroplated vias can also be utilized to dissipate heat generated by the voltage regulator.

Example: The input voltage is 5V ±5%, the output voltage is 2.5V, and the output current ranges from 1mA to 200mA. The maximum ambient temperature is 85°C. Calculate the maximum junction temperature.
The power dissipation calculation formula is as follows:

$$I_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right) + I_{GND} \times V_{IN(MAX)}$$

Where IOUT (MAX) = 200mA, VIN (MAX) = 5.25V, and IGND = 7.2mA, therefore:

$$P_{DISS} = 0.2A \times (5.25V - 2.5V) + 7.2mA \times 5.25V = 0.59W$$

When using DFN packaging, the thermal resistance coefficient ranges from approximately 34°C/W to 36°C/W (depending on the copper-clad PCB area). Consequently, the estimated increase in junction temperature can be calculated as follows:

$$0.59W \times 35℃/W = 20.7℃$$

Therefore, the maximum junction temperature equals the ambient temperature plus the increase in junction temperature, i.e.:

$$T_{JMAX} = 85℃ + 20.7℃ = 105.7℃$$

9.15 Protection function

In battery-powered applications, the LKP4153 offers multiple protection features. The voltage regulator incorporates high-precision current limits and overheat protection to prevent excessive output load or thermal failure. Under normal operating conditions, ensure the junction temperature of the voltage regulator does not exceed 125°C.
To protect the error amplifier of LKP4153, the clamping voltage between the SET pin and OUTS pin is limited to 15V, meaning the maximum current through the clamping circuit between these pins is capped at 20mA. For applications requiring active drive of the SET pin via a voltage source, the current draw from this source must be kept below 20mA. Additionally, to address transient faults, transient current clamping must be implemented—for instance, by setting the maximum value of the SET pin capacitor (CSET) to 22μF.

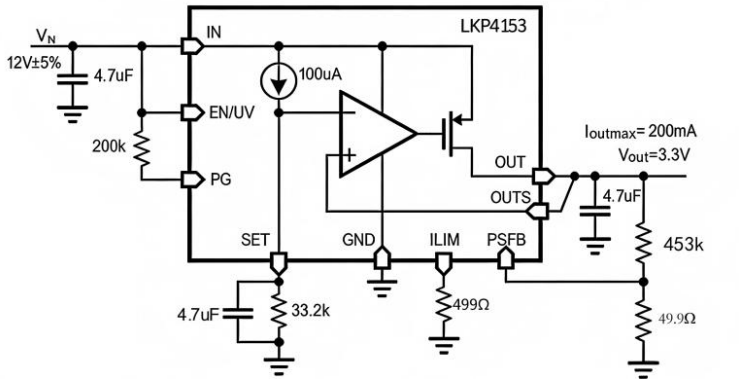
The LKP4153 incorporates built-in reverse current protection. When the input voltage drops to-20V, it prevents reverse current flow and negative output voltage, thereby safeguarding batteries inserted in reverse polarity.

In applications requiring backup batteries, varying input/output conditions frequently occur. For instance, when the power input is pulled to GND, intermediate potentials, or floating states, the output voltage may still be elevated. In such scenarios, the LKP4153 provides reverse current protection to prevent output current from backflowing into the input. The clamping

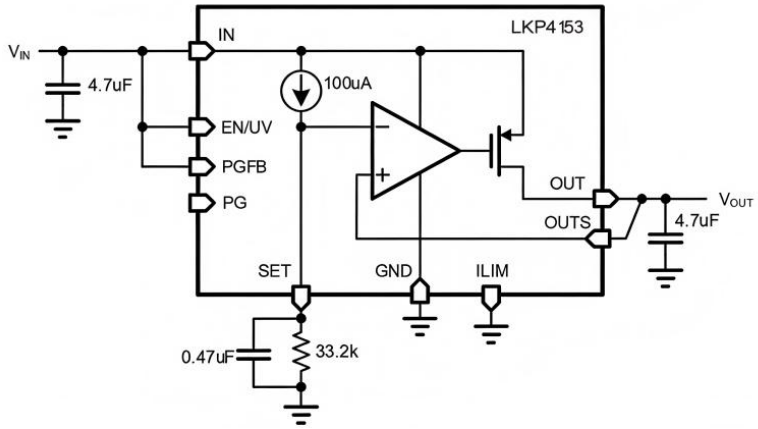
circuit between OUTS and SET pins (unless SET is floating) allows current to flow through the SET pin's resistor to GND, while also enabling current to return via the surge recovery circuit. The presence of a Schottky diode between OUTS and SET pins significantly reduces current during surge recovery circuit activation protection.

10 Typical Applications

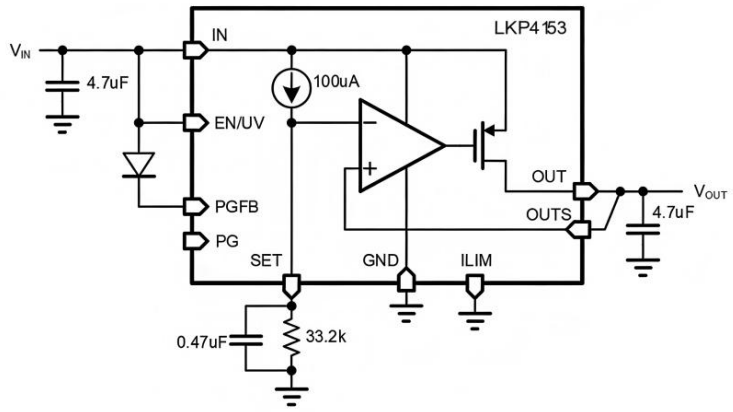
12V in to 3.3Vout with 1.5V_{RMS} Integrated Noise



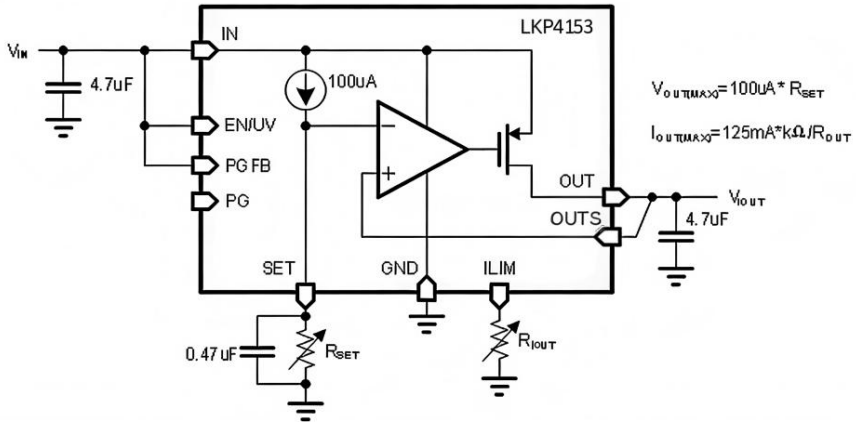
PGFB Disable without Reverse Input Protection



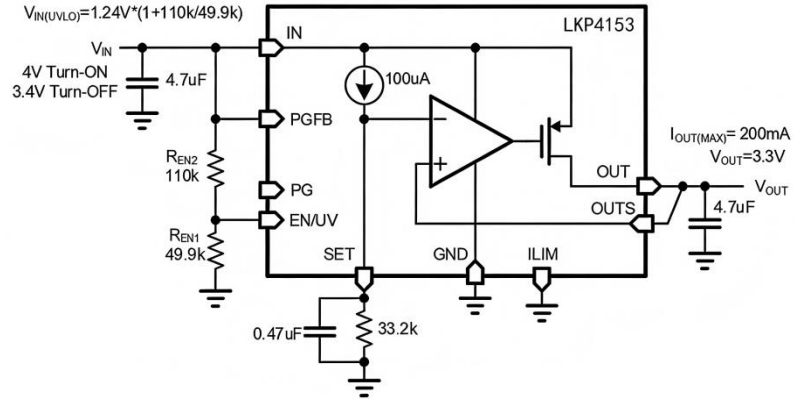
PGFB Disable with Reverse Input Protection



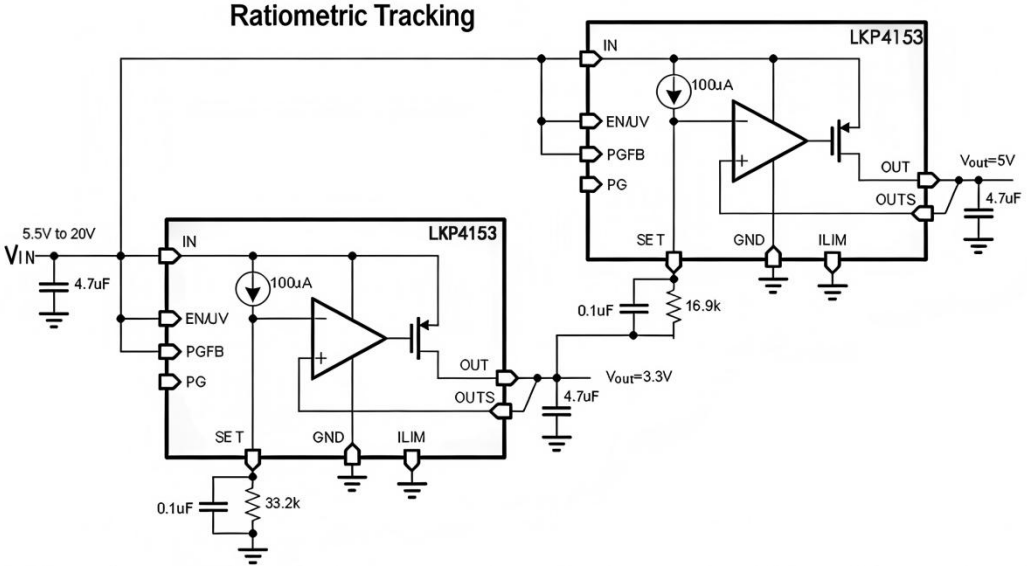
Low Noise CC/CV Lab Power Supply



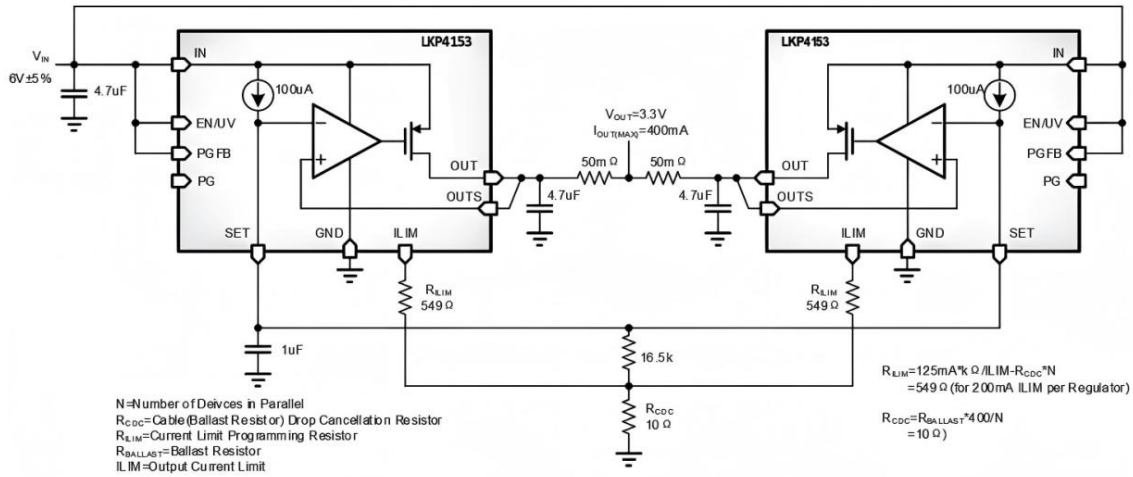
Programming Undervoltage Lockout



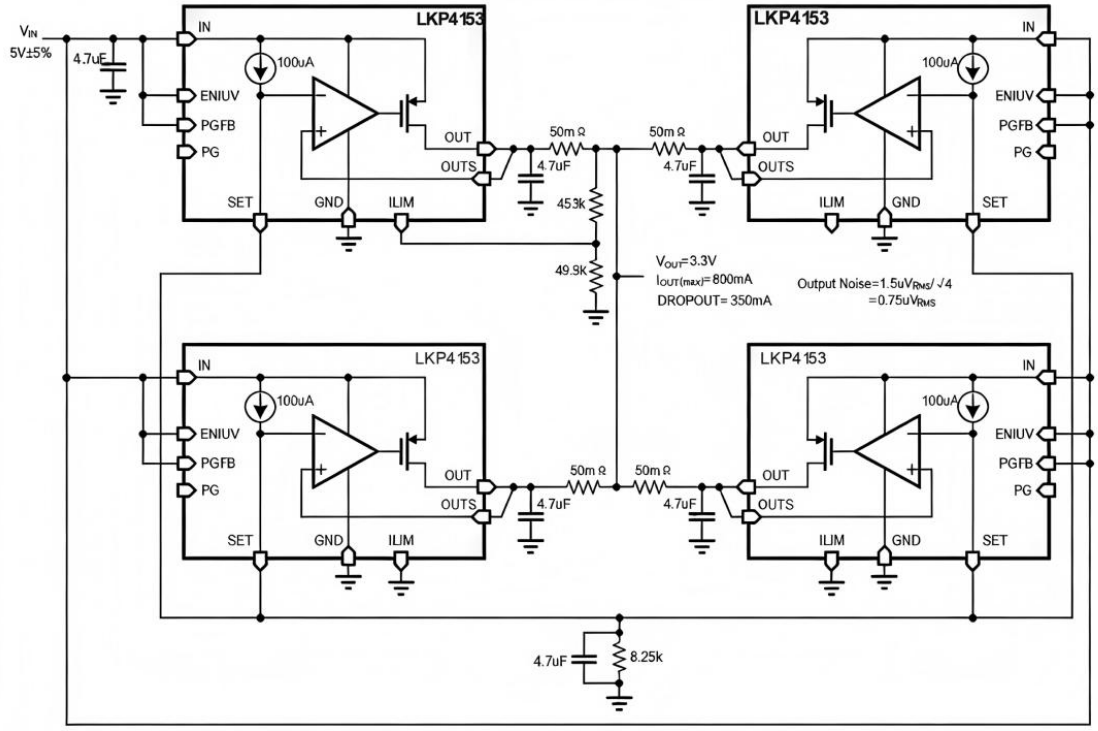
Ratiometric Tracking



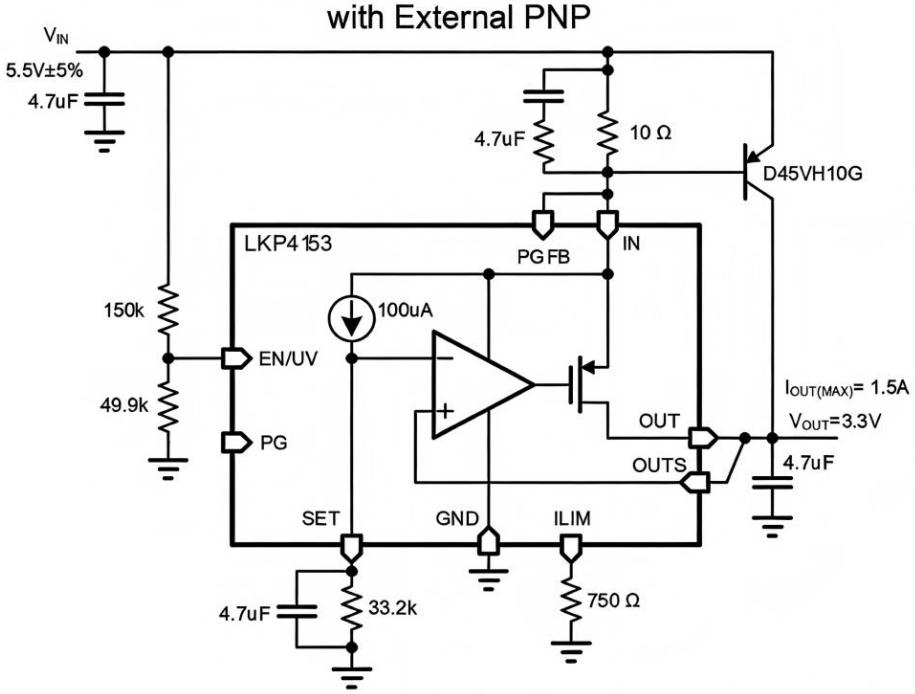
Paralleling Multiple Devices Using ILIM to Cancel Ballast Resistor Drop

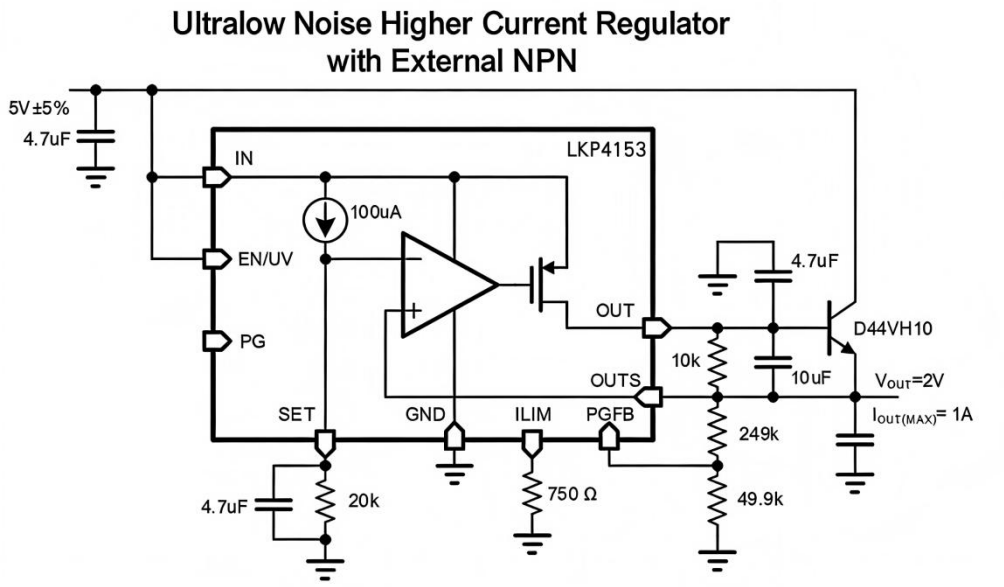


Paralleling Multiple LKP4153 for Higher Output Current



Ultralow Noise Higher Current Regulator
with External PNP





11 Encapsulation Description

The LKP4153 is available in two package configurations: DFN10 and MSOP10.

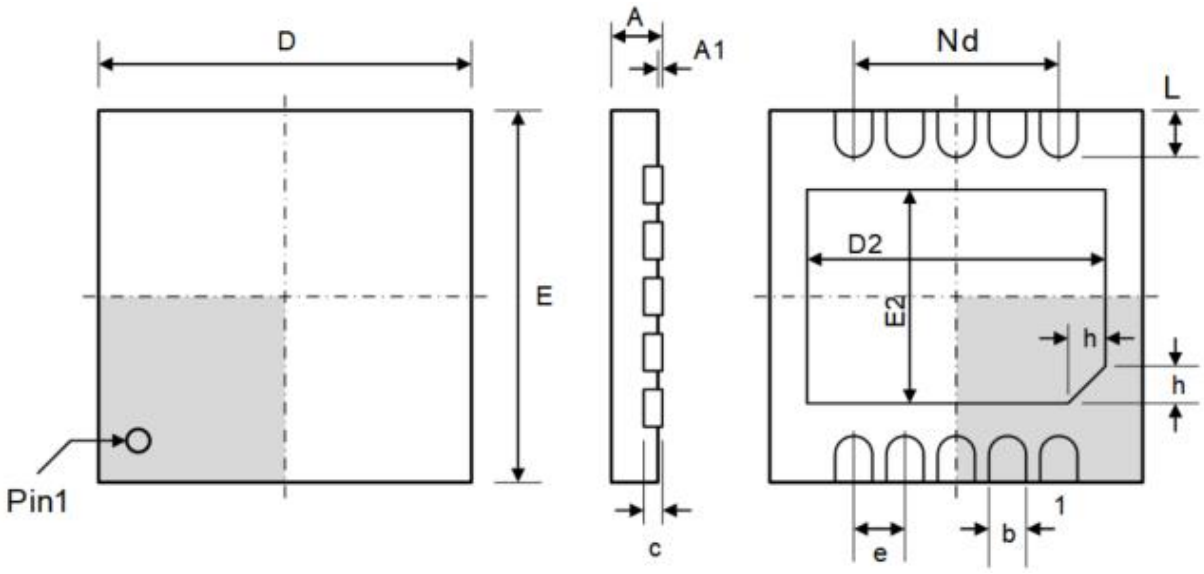


Figure 8. DFN10 package

explain ：

1） The drawing is not drawn to actual scale
2） All package standard size units are in millimeters (mm)
3） The shaded areas in the top and bottom views are shown only as pin 1.

4） Exposed solder pads should be plated with solder.

Table 8. DFN10 dimensions (unit: mm)

labeled	least value	standard value	crest value	labeled	least value	standard value	crest value
A	0.70	0.75	0.80	e	0.50 BSC		
A1	-	0.02	0.05	Nd	2.00 BSC		
b	0.18	0.25	0.30	E	2.90	3.00	3.10
c	0.18	0.20	0.25	E2	0.30	0.40	0.50
D	2.90	3.00	3.10	L	0.30	0.40	0.50
D2	2.40	2.50	2.60	h	0.20	0.25	0.30

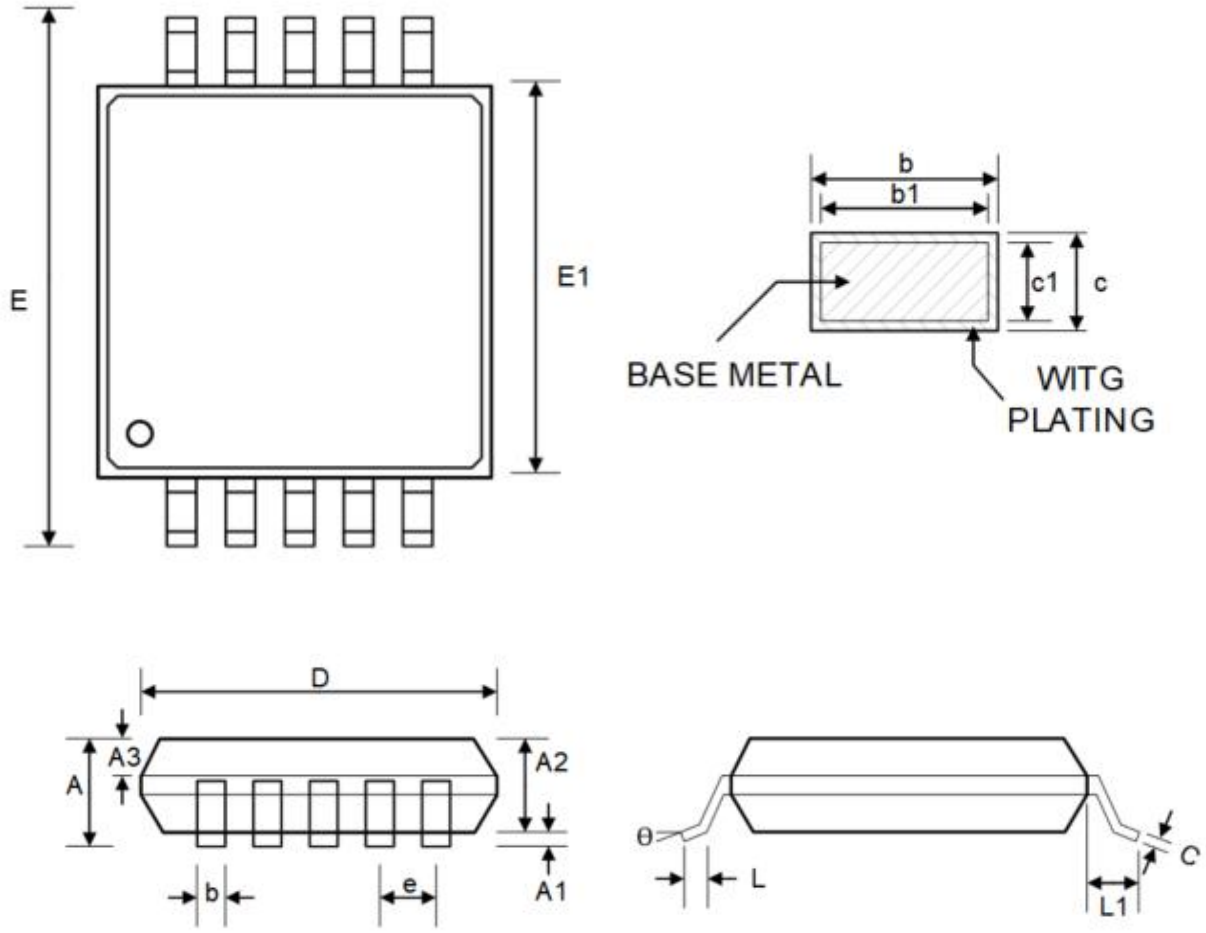


Figure 9. MSOP10 package

explain ：

1） The drawing is not drawn to actual scale

2） All package standard size units are in millimeters (mm)

3） Exposed solder pads should be plated with solder.

Table 9. MSOP10 dimensions (unit: mm)

labeled	least value	standard value	crest value	labeled	least value	standard value	crest value
A			1.10	D	2.90	3.00	3.10
A1	0.05	0.10	0.15	E	4.70	4.90	5.10
A2	0.75	0.85	0.95	E1	2.90	3.00	3.10
A3	0.30	0.35	0.40	b	0.18	0.22	0.26
L	0.40	0.55	0.70	b1	0.17	0.20	0.23
L1	0.95 REF			e	0.50 BSC		
c	0.15	0.17	0.19	Θ	0°		8°
c1	0.14	0.15	0.16				

12 Purchase Guide

Table 10. Product Order Information

Model	Temperature range	On-product information	Encapsulation description	Silk-screen
LKP4153DN10A	-40°C to +125°C	Adjustable voltage output ranging from 0.5V to 16V, with a maximum output current of 200mA	DFN-10	LKP4153
LKP4153DN10B	-55°C to +125°C	Adjustable voltage output ranging from 0.5V to 16V, with a maximum output current of 200mA	DFN-10	LKP4153
LKP4153MS10A	-40°C to +125°C	Adjustable voltage output ranging from 0.5V to 16V, with a maximum output current of 200mA	MSOP-10	LKP4153